



Audio Click-Pop Suppressor

General Description

The MAX9890 provides click-and-pop suppression for devices such as CODECs with integrated headphone amplifiers that lack a clickless/popless startup/power-up or shutdown/power-down. The device controls the ramping of the DC bias voltage on the output-coupling capacitors and the application of the audio signal to ensure that no audible transients are present at the headphones. The MAX9890A features a 200ms startup time for use with up to 100 μ F coupling capacitors. The MAX9890B features a 330ms startup time for use with greater than 100 μ F coupling capacitors.

The MAX9890 consumes 14 μ A of supply current and 0.001 μ A in shutdown, while contributing less than 0.003% THD+N into a 32 Ω load. ESD (Human Body Model) protection circuitry on the outputs protect the MAX9890 and devices further up the signal chain from ESD strikes up to \pm 8kV.

The MAX9890 is available in a miniature (1.5mm x 1.5mm x 0.6mm) 9-bump chip-scale package (UCSP™), as well as an 8-pin TDFN package (3mm x 3mm x 0.8mm), and is specified for operation over the -40°C to +85°C extended temperature range.

Applications

High-End Notebook Audio

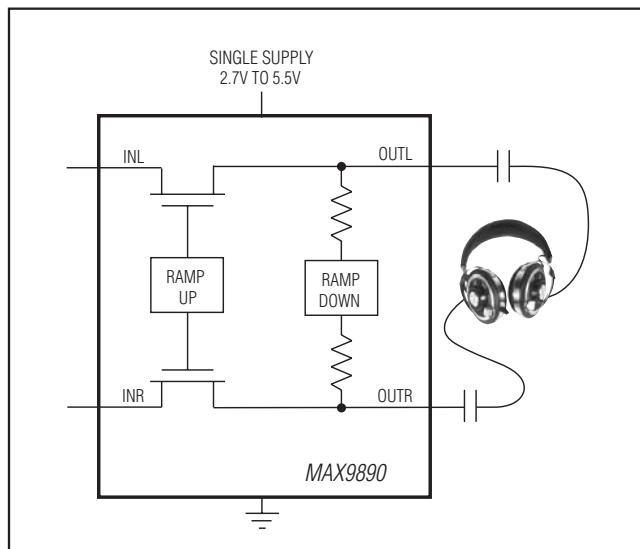
PDAs

Portable DVD Players

Cell Phones

Portable MP3 Players

Simplified Block Diagram



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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Features

- ◆ 36dB Click-Pop Suppression
- ◆ 2.7V to 5.5V Single-Supply Operation
- ◆ Clickless/Popless Startup/Power-Up and Shutdown/Power-Down
- ◆ 0.001 μ A Low-Power Shutdown Mode
- ◆ THD+N < 0.003% Into 32 Ω
- ◆ \pm 8kV ESD Protected Outputs (Human Body Model)
- ◆ Requires Only One 0.1 μ F Capacitor to Complete the Circuit
- ◆ Low 14 μ A Supply Current
- ◆ Tiny Packaging
9-Bump UCSP (1.5mm x 1.5mm x 0.6mm)
8-Pin TDFN (3mm x 3mm x 0.8mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9890AEBL-T	-40°C to +85°C	9 UCSP-9	ADV
MAX9890AETA	-40°C to +85°C	8 TDFN-EP**	AHA
MAX9890BEBL-T	-40°C to +85°C	9 UCSP-9	ADW
MAX9890BETA	-40°C to +85°C	8 TDFN-EP**	AHB
MAX9890BETA/V+	-40°C to +85°C	8 TDFN-EP**	BRQ

**EP = Exposed pad.

T = Tape and reel.

/V denotes an automotive qualified part that conforms to AEC-Q100.

Selector Guide

PART	PIN-PACKAGE	SWITCH TURN-ON TIME (ms)
MAX9890AEBL-T	9 UCSP-9	200
MAX9890AETA	8 TDFN-EP	200
MAX9890BEBL-T	9 UCSP-9	330
MAX9890BETA	8 TDFN-EP	330
MAX9890BETA/V+	8 TDFN-EP	330

Typical Application Circuit and Pin Configurations appear at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

(All Voltages are Referenced to GND)

V _{CC}	+6V
C _{EXT} , $\overline{\text{SHDN}}$, OUT _—	-0.3V to +6V
IN _—	-0.3V to (V _{CC} + 0.3V)
Continuous Current (IN _— , OUT _—)	±150mA
Continuous Current (All Other Pins)	±20mA
Continuous Power Dissipation (T _A = +70°C)	
8-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
9-Bump UCSP (derate 4.7mW/°C above +70°C)	379mW

Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Reflow	+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, $\overline{\text{SHDN}} = \text{V}_{\text{CC}}$, GND = 0, C_{EXT} = 0.1μF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)
(Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{CC}	Inferred from R _{ON} test		2.7	5.5	5.5	V
Supply Current	I _{CC}	(Note 2)			14	22	μA
Shutdown Supply Current	I _{SHDN}	$\overline{\text{SHDN}} = \text{GND}$			0.001	1	μA
Input Voltage Range		Inferred from R _{ON} test		0	V _{CC}	V _{CC}	V
On-Resistance	R _{ON}	Over input voltage range	V _{CC} = 5.5V	0.4	1	1	Ω
			V _{CC} = 2.7V	0.7	1.5	1.5	
On Resistance Flatness	R _{FLAT(ON)}	Over input voltage range		2		2	mΩ
Output Discharge Resistance	R _{OUT(DIS)}			220		220	kΩ
Input Off-Leakage Current		$\overline{\text{SHDN}} = \text{GND}$		0.001	1	1	μA
V _{CC} Power-Down Threshold (Note 3)	V _{UVLO}	V _{CC} falling		2.5		2.5	V
Click-Pop Reduction				36		36	dB
FSD Protection		OUT _— , Human Body Model		±8		±8	kV

DYNAMIC

Turn-On Time (Note 4)	t _{ON}	MAX9890A	200	ms
		MAX9890B	330	
Turn-Off Time	t _{OFF}	(Note 5)	120	ns
Bandwidth			>100	kHz
Total Harmonic Distortion Plus Noise	THD+N	R _L = 32Ω, 30mW, f = 1kHz	0.003	%
Off-Isolation, IN _— to OUT _—		f = 20kHz, $\overline{\text{SHDN}} = \text{GND}$, R _L = 32Ω	-108	dB
Crosstalk (Switches ON)		f = 20kHz	-100	dB
Power-Supply Rejection Ratio (Note 6)	PSRR	V _{RIPPLE} = 0.5V _{P-P} at 20Hz, f _{IN} = 3kHz at 1V _{P-P} , R _L = 32Ω	-100	dB
		V _{RIPPLE} = 0.5V _{P-P} at 1kHz, f _{IN} = 3kHz at 1V _{P-P} , R _L = 32Ω	-100	
		V _{RIPPLE} = 0.5V _{P-P} at 20kHz, f _{IN} = 3kHz at 1V _{P-P} , R _L = 32Ω	-84	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3V$, $SHDN = V_{CC}$, $GND = 0$, $C_{CEXT} = 0.1\mu F$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)
(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT (SHDN)						
Logic-Input High Voltage	V_{IH}	$V_{CC} = 2.7V$ to $5.5V$	2.0			V
		$V_{CC} = 2.7V$ to $5.5V$, MAX9890BETA/V+ only, $T_A = -40^\circ C$	2.2			
Logic-Input Low Voltage	V_{IL}	$V_{CC} = 2.7V$ to $5.5V$		0.8		V
Logic-Input Current	I_{IN}			± 1		μA

Note 1: All devices are 100% tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

Note 2: Supply current is measured when switch is on (i.e., $SHDN = V_{CC}$, $t > t_{ON}$).

Note 3: Supply voltage level where the device enters its power-down cycle.

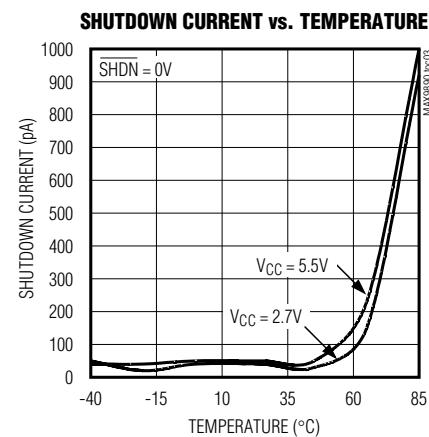
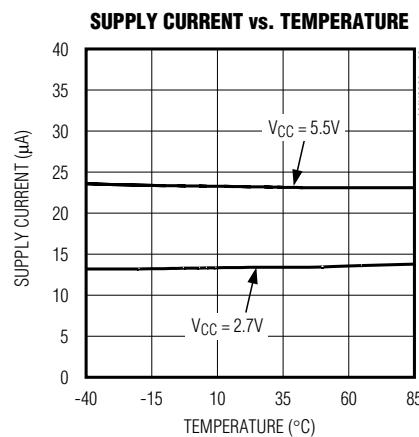
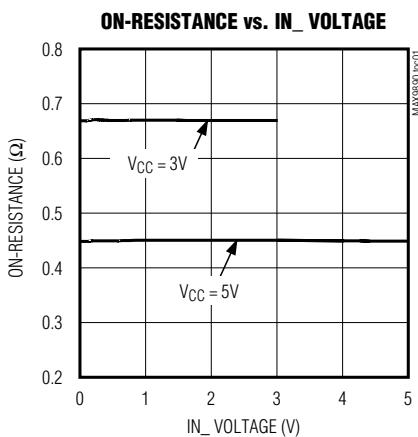
Note 4: Turn-on time is measured from the time $V_{CC} = 3V$ and $SHDN > V_{IH}$ until the R_{ON} specification is met.

Note 5: Switch turn-off time is measured from the time $SHDN < V_{IL}$ or $V_{CC} < V_{UVLO}$ until the off-isolation specification is met.

Note 6: See the *Power-Rejection Ratio* section for test method.

Typical Operating Characteristics

($V_{CC} = 3V$, $C_{CEXT} = 0.1\mu F$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

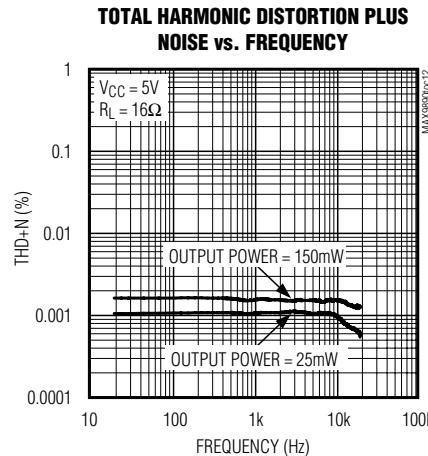
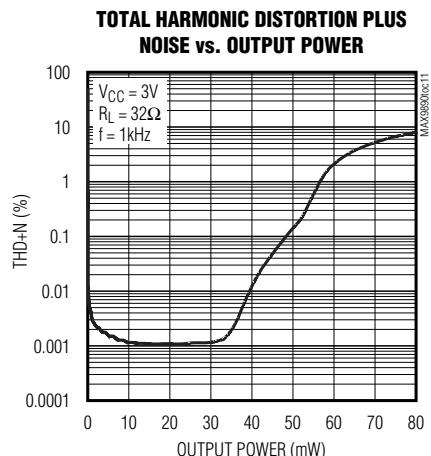
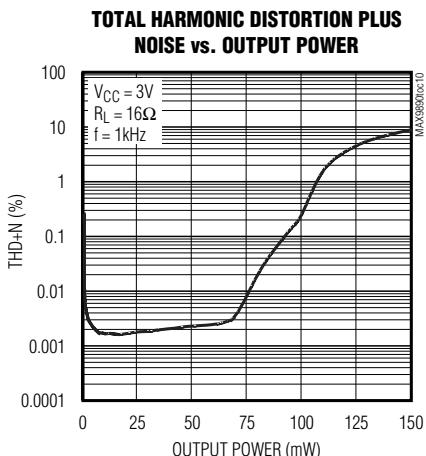
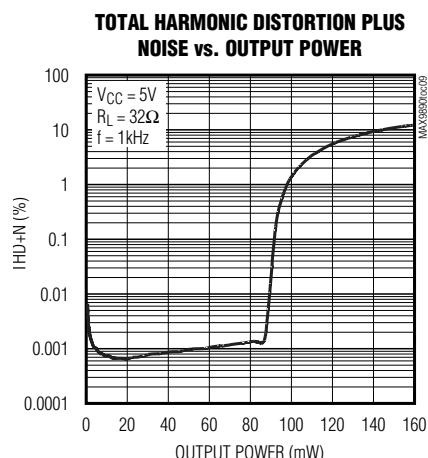
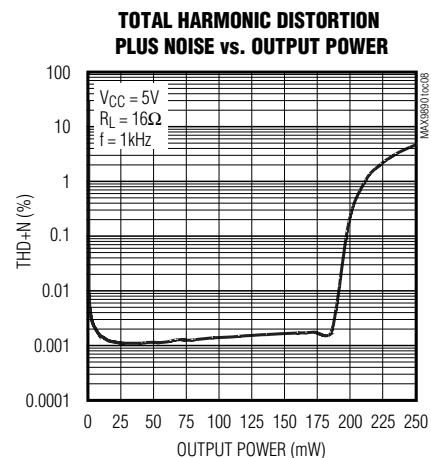
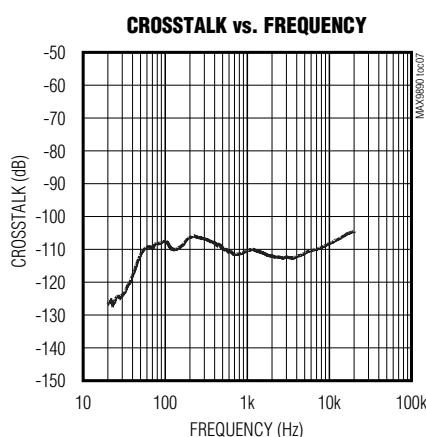
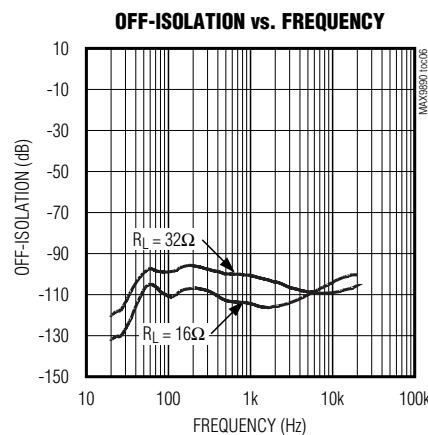
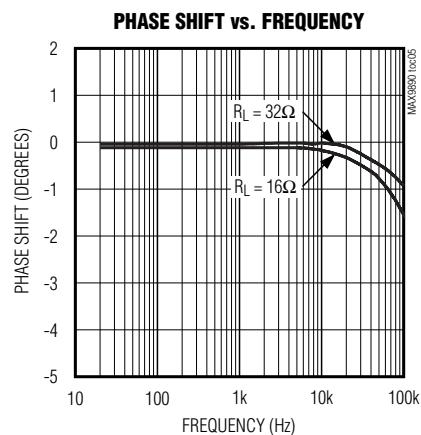
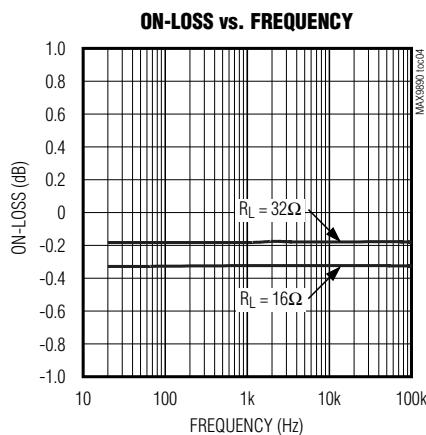


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Typical Operating Characteristics (continued)

($V_{CC} = 3V$, $C_{CEXT} = 0.1\mu F$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

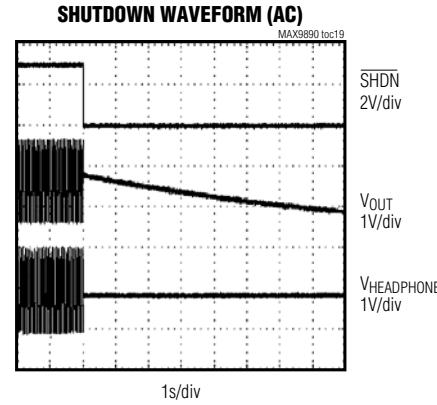
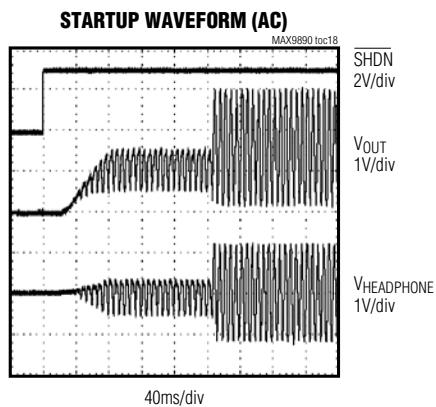
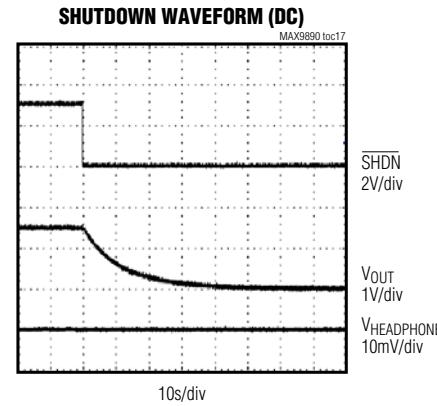
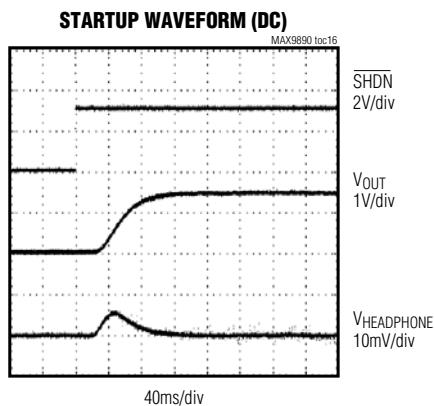
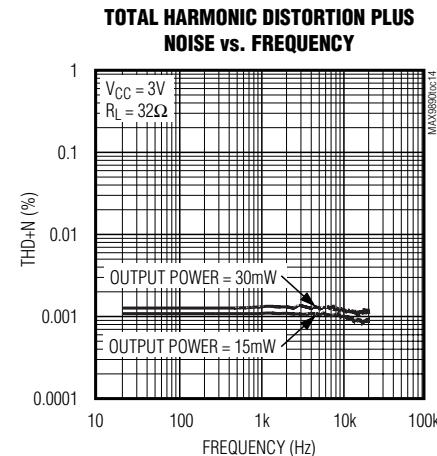
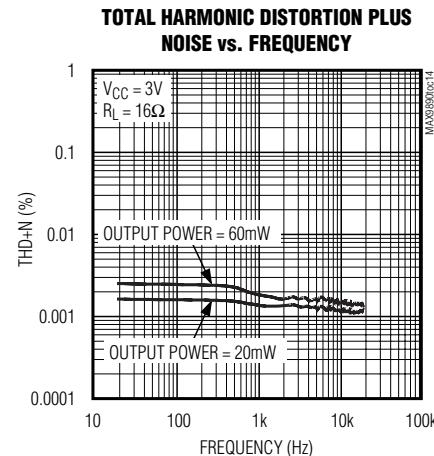
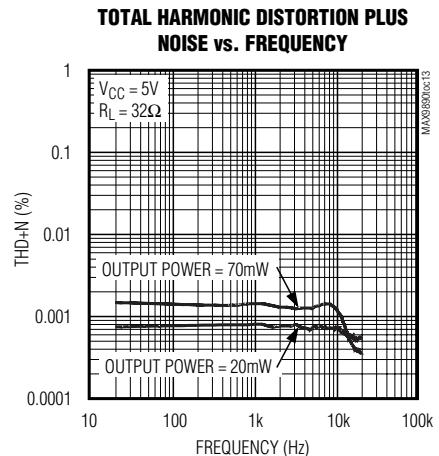


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Typical Operating Characteristics (continued)

($V_{CC} = 3V$, $C_{CEXT} = 0.1\mu F$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN/BUMP		NAME	FUNCTION
TDFN	UCSP		
1	C2	V _{CC}	Power Supply. V _{CC} accepts 2.7V to 5.5V input supply. Bypass V _{CC} to GND with a 1 μ F capacitor.
2	C1	SHDN	Active-Low Shutdown. Connect SHDN to GND to enter a 0.1 μ A shutdown mode. Connect SHDN to V _{CC} for normal operation.
3	B1	INL	Left-Channel Audio Input. Connect to output of headphone amplifier.
4	A1	OUTL	Left-Channel Audio Output. AC couple to headphone.
5	A2	GND	Ground
6	A3	OUTR	Right-Channel Audio Output. AC couple to headphone.
7	B3	INR	Right-Channel Audio Input. Connect to output of headphone amplifier.
8	C3	CEXT	External Capacitor. Connect a 0.1 μ F capacitor from CEXT to GND.

Detailed Description

The MAX9890 provides click-and-pop suppression for single-supply devices such as CODECs and other headphone amplifiers that do not have click-and-pop suppression. Single-supply audio amplifier outputs have a DC bias voltage, V_{CC} / 2, and require large output-coupling capacitors to block the DC voltage from the speaker. During startup or shutdown, the DC bias voltage is quickly raised or lowered (Figure 1), resulting in an audible transient through the headphone load. The MAX9890 prevents the audible transient by slowly ramping the DC bias in an S-shaped waveform (Figure 2), suppressing the large transient at the output of the coupling capacitor. The S-shaped waveform shapes the frequency spectrum, minimizing the amount of audible components present at the output.

Internal switches couple the inputs to the outputs after the coupling capacitors have fully charged to the input common-mode bias voltage. When power is removed or the device is put into shutdown, the internal switches in the MAX9890 immediately disconnect the output and slowly discharge the coupling capacitors through 220 $k\Omega$ resistors.

The MAX9890 has an undervoltage lockout (UVLO) that prevents device operation when V_{CC} is below the power-down threshold (2.5V, typ). The MAX9890 features $\pm 8\text{kV}$ ESD (Human Body Model) protection on the audio outputs.

Startup

The MAX9890 monitors V_{CC} and SHDN. The UVLO holds the device off when V_{CC} is below the power-down threshold (V_{UVLO}) or SHDN is held low. The device needs both V_{CC} above the power-down thresh-

old and SHDN = high for the part to start up. Once the supply voltage is above the power-down threshold and SHDN is high, the device charges the coupling capacitors to the input DC bias voltage using CEXT to control the ramp. After the DC bias ramp, the internal switches close, coupling the audio input to the output. The MAX9890 provides click-pop suppression even if the output blocking capacitors are already partially or fully charged.

The MAX9890A features a 200ms switch turn-on time, enabling the use of up to 100 μ F coupling capacitors at the output for applications requiring only a limited low-frequency response and a rapid turn-on time. The MAX9890B features a 330ms switch turn-on time, enabling the use of >100 μ F coupling capacitors at the output for extended low-frequency response applications. For optional click-pop suppression, mute the audio signal until after the turn-on time has elapsed.

The internal switches stay closed as long as V_{CC} is above the power-down threshold voltage and SHDN is high. Figures 1 and 2 show typical startup/power-up sequences with and without click-pop suppression.

Shutdown

If the supply voltage falls below the UVLO threshold or if SHDN is driven low, the device enters low-power shutdown mode. In low-power shutdown mode, quiescent current reduces to 0.001 μ A. The switches are immediately turned off and 220 $k\Omega$ resistors slowly bleed the charge off the coupling capacitors. Figures 3 and 4 show typical shutdown/power-down sequences with and without click-pop suppression. For optimal click-pop performance, mute the audio signal before shutting down the MAX9890.

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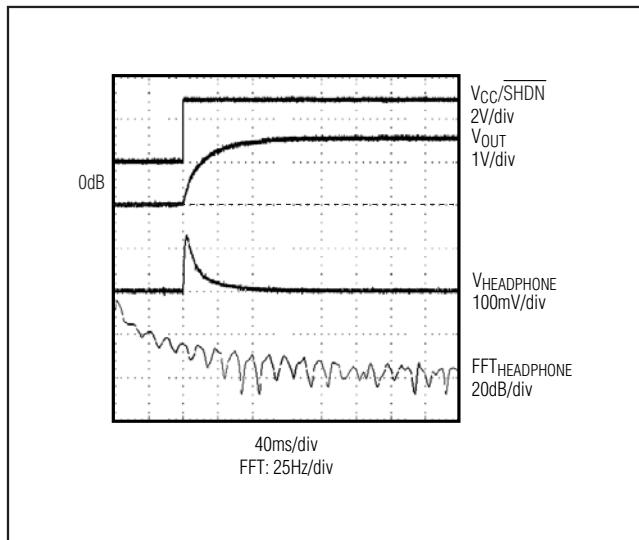


Figure 1. Startup/Power-Up Sequence Without Click-Pop Suppression

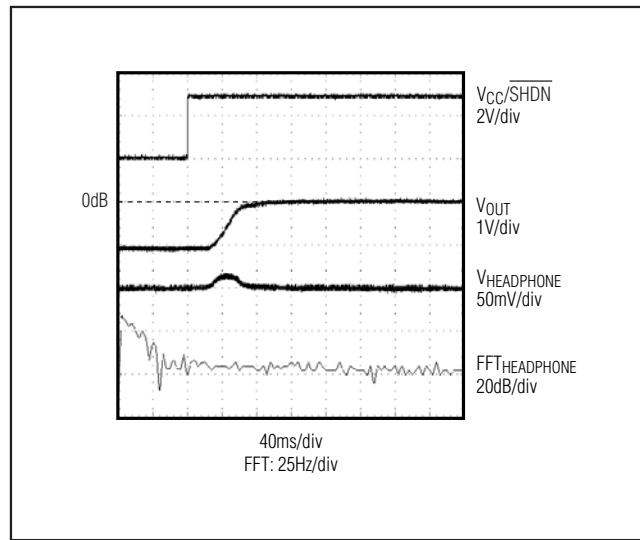


Figure 2. Startup/Power-Up Sequence With Click-Pop Suppression

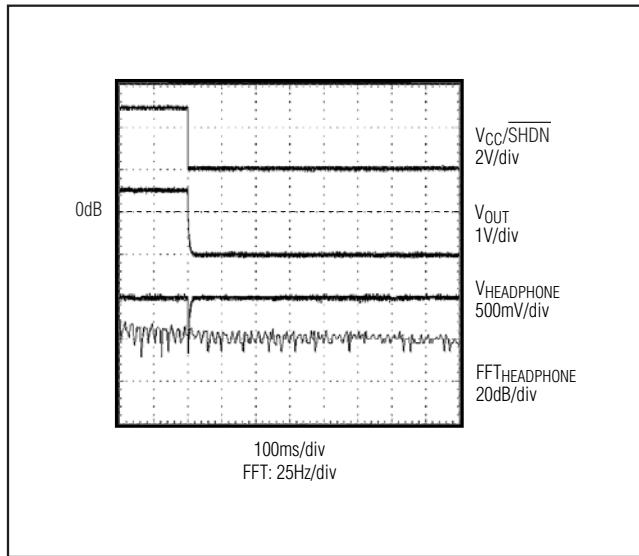


Figure 3. Shutdown/Power-Down Sequence Without Click-Pop Suppression

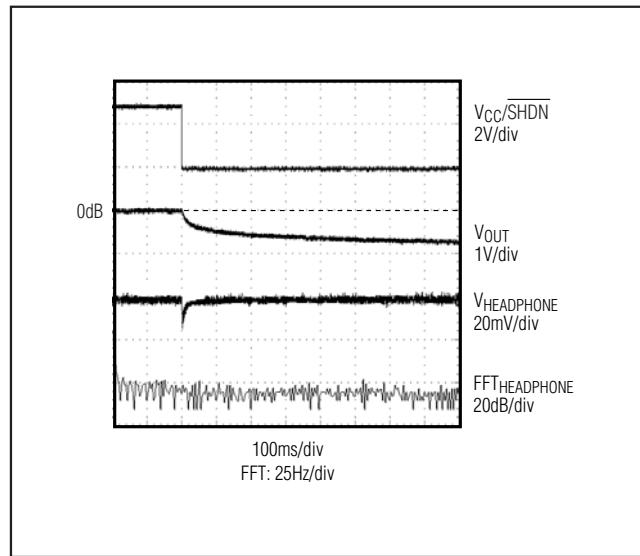


Figure 4. Shutdown/Power-Down Sequence With Click-Pop Suppression

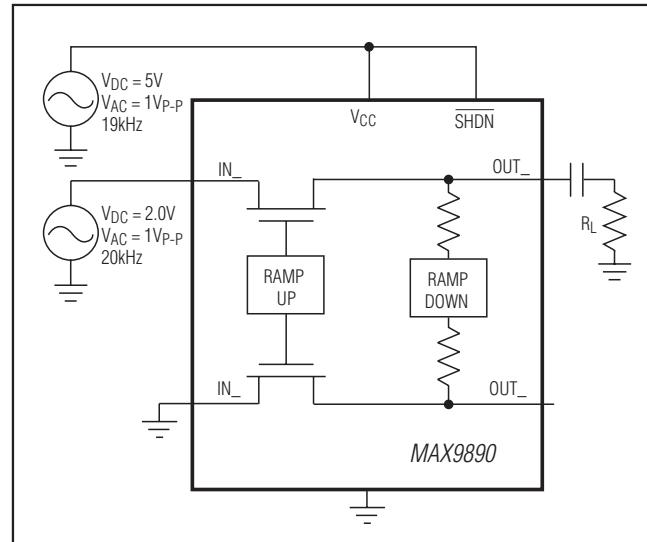
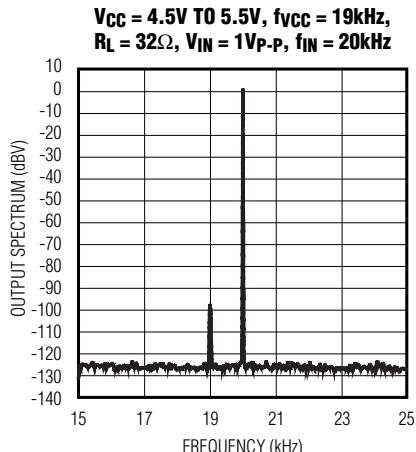
Switches

The MAX9890's internal switches connect the input to the output after the coupling capacitors are fully charged. The MAX9890A holds the switches open for 200ms and is ideal for coupling capacitors less than 100 μ F. The MAX9890B has a longer turn-on time of 330ms and is

ideal with larger coupling capacitors less than 220 μ F. The internal switches have a low on-resistance ($R_{ON} = 0.5\Omega$) and on-resistance flatness ($R_{FLAT(ON)} = 2m\Omega$) minimizing total harmonic distortion plus noise (THD+N). The relationship below shows the contribution to THD+N through the switch, due to on-resistance and on-resistance flat-

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ness (on-resistance flatness is defined as the difference between the maximum and minimum values of on-resistance measured over the specific analog-signal range).

$$THD_{MAXIMUM} = \frac{R_{FLAT(ON)}}{4R_{LOAD}} \times 100\%$$

Power-Supply Rejection Ratio (PSRR)

PSRR is the measurement of AC power-supply ripple or noise that couples to the output. Variations in supply voltage corrupt the audio signal, due to changes in the R_{ON} value by supply modulation. The FFT shown in Figure 5 was taken with a 19kHz 1Vp-P sine wave onto the 5V DC supply voltage, and a 20kHz 1Vp-P sine wave applied at IN_- with a 32Ω load is shown in Figure 6. The MAX9890 maintains a -100dB (typ) PSRR across the supply voltage range eliminating any corruption of the audio signal from supply variations. Therefore, with a zero audio signal, the R_{ON} variation due to supply voltage ripple does not contribute to any output signal modulation.

Low-Frequency Response

In addition to the cost and size disadvantages of the output-coupling capacitors, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

The impedance of a headphone or speaker load and the output-coupling capacitor form a highpass filter with the -3dB point set by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where R_L is the headphone impedance and C_{OUT} is the output-coupling capacitor value. The highpass filter is required by conventional single-ended, single power-supply headphone drivers to block the midrail DC bias component of the audio signal from the headphones. The drawback to the filter is that it can attenuate low-frequency signals. Larger values of C_{OUT} reduce this effect but result in physically larger, more expensive capacitors. Figure 7 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16Ω headphone with a $100\mu F$ blocking capacitor is 100Hz, well within the normal audio band, resulting in low-frequency attenuation of the reproduced signal.

The MAX9890A and MAX9890B have different turn-on times to accommodate different size output-coupling capacitors (see Table 1). Using a capacitor smaller than the specified maximum allowed does not degrade click-pop suppression. Therefore, capacitors less than $100\mu F$ can be used with the A or B version devices.

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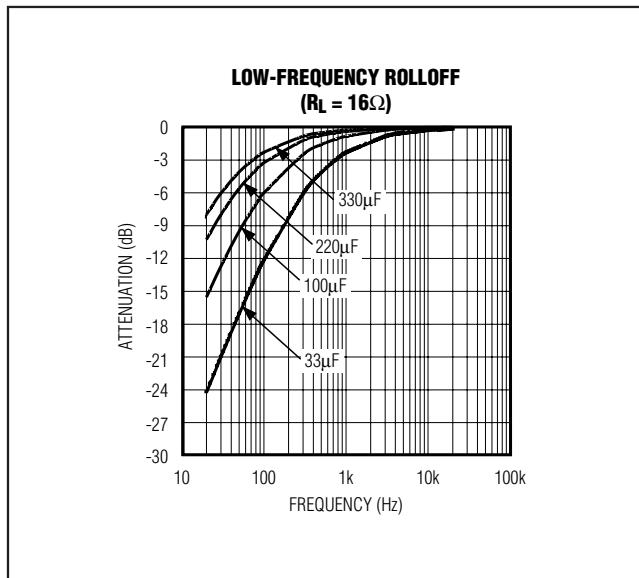


Figure 7. Low-Frequency Attenuation for Common DC-Blocking Capacitor Values

Table 1. Coupling Capacitor

CAPACITOR SIZE (μF)	MAX9890A TURN-ON TIME (200ms)	MAX9890B TURN-ON TIME (300ms)
33	✓	✓
47	✓	✓
100	✓	✓
150	*	✓
220	*	✓
330	—	*
470	—	*

*May experience some degradation of click-pop suppression.

External Capacitor (C_{CEXT})

The external click-pop suppression capacitor at C_{CEXT} serves a dual purpose. On power-up, C_{CEXT} is charged by an internal current source and is used to slowly ramp up the external coupling capacitors. When the device is powered down, C_{CEXT} powers the internal circuitry used to drain the external coupling capacitors. A 0.1 μF capacitor between C_{CEXT} and GND provides clickless/popless operation with coupling capacitors for both the MAX9890A and MAX9890B, even with the rapid removal of supply voltage.

Applications Information

Layout

Good layout improves performance by decreasing the amount of stray capacitance and noise. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components as close to the device as possible.

Power Supply and Bypassing

The excellent PSRR of the MAX9890 allows it to operate from noisy power supplies. In most applications, a 0.1 μF capacitor from V_{CC} to GND is sufficient. This bypass capacitor should be placed close to V_{CC}.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape-carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to *Application Note 1891: Wafer-Level Packaging (WLP) and its Applications* at www.maximintegrated.com/UCSP.

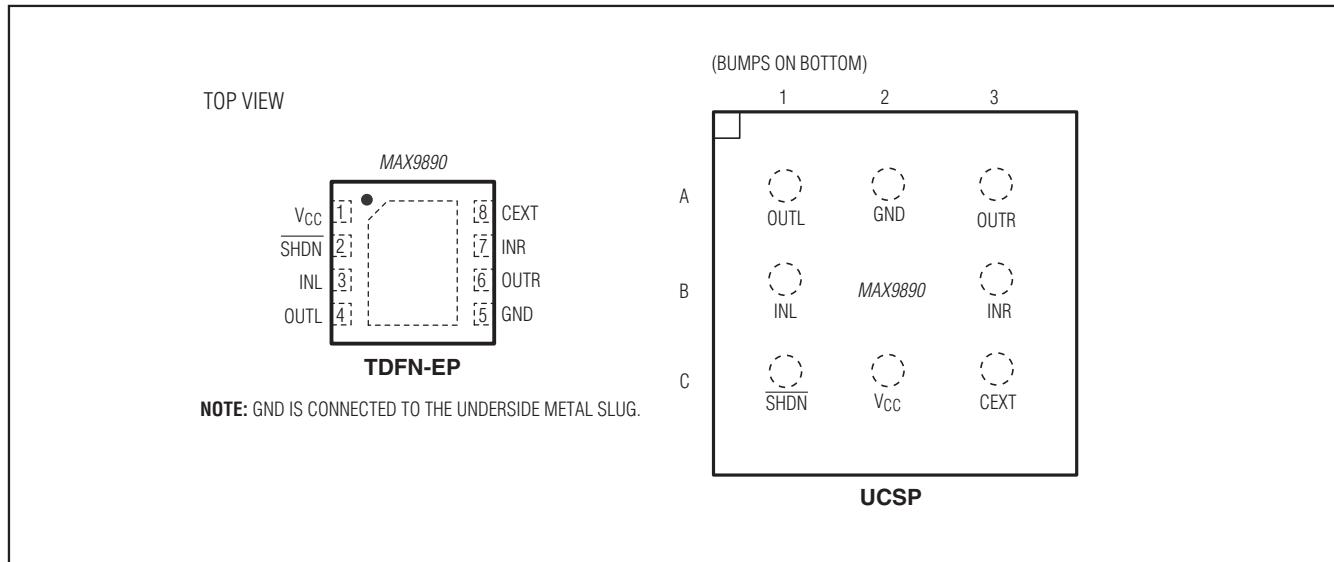
Chip Information

PROCESS: BiCMOS

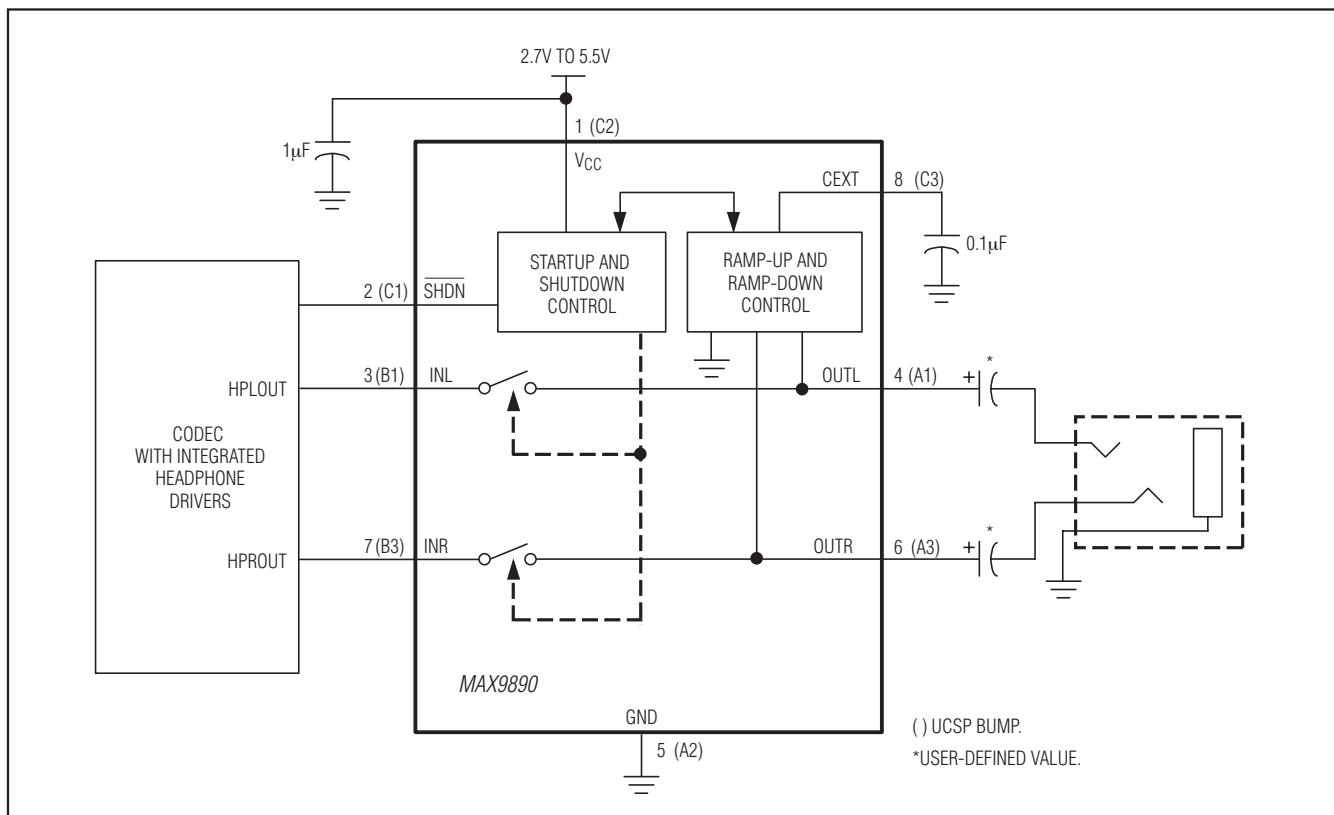
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Pin Configurations



Typical Application Circuit



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Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
UCSP	B9+2	21-0093	Refer to Application Note 1891
TDFN-EP	T833+2	21-0137	90-0059

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	3/14	Added the MAX9890BETAN+ to the <i>Ordering Information</i> , <i>Selector Guide</i> , and <i>Electrical Characteristics</i> tables	1, 3



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