54/7448
54LS/74LS48
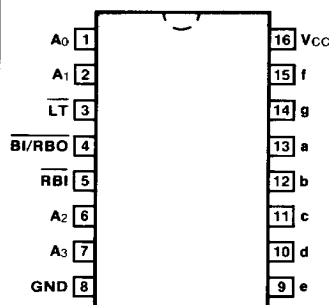## BCD TO 7-SEGMENT DECODER

CONNECTION DIAGRAM
PINOUT A

DESCRIPTION — The '48 translates four lines of BCD (8421) input data into the 7-segment numeral code and provides seven corresponding outputs having pull-up resistors, as opposed to totem pole pull-ups. These outputs can serve as logic signals, with a HIGH output corresponding to a lighted lamp segment, or can provide a 1.3 mA base current to npn lamp driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.

The '48 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. For a detailed description of the blanking, lamp test and zero-suppression functions refer to the '46A data sheet, but note that the segment output states of the '48 are the logical inverse of those of the '46A. Also see the 'LS248 data sheet.
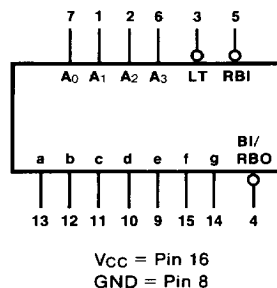
LOGIC SYMBOL

V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7448PC, 74LS48PC		9B
Ceramic DIP (D)	A	7448DC, 74LS48DC	5448DM, 54LS48DM	7B
Flatpak (F)	A	7448FC, 74LS48FC	5448FM, 54LS48FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0 — A_3	BCD Inputs	1.0/1.0	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	-/2.5	-/0.75
	Ripple Blanking Output (Active LOW)	5.0/5.0	1.25/2.0 (1.0)
a — g	Segment Outputs (Active HIGH)	10/4.0	2.5/3.75 (1.25)

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	LT	RBI	A₃	A₂	A₁	A₀	BI/RBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

(1) BI/RBO is wired-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input (RBI) and inputs A₀, A₁, A₂, and A₃ are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

LOGIC DIAGRAM
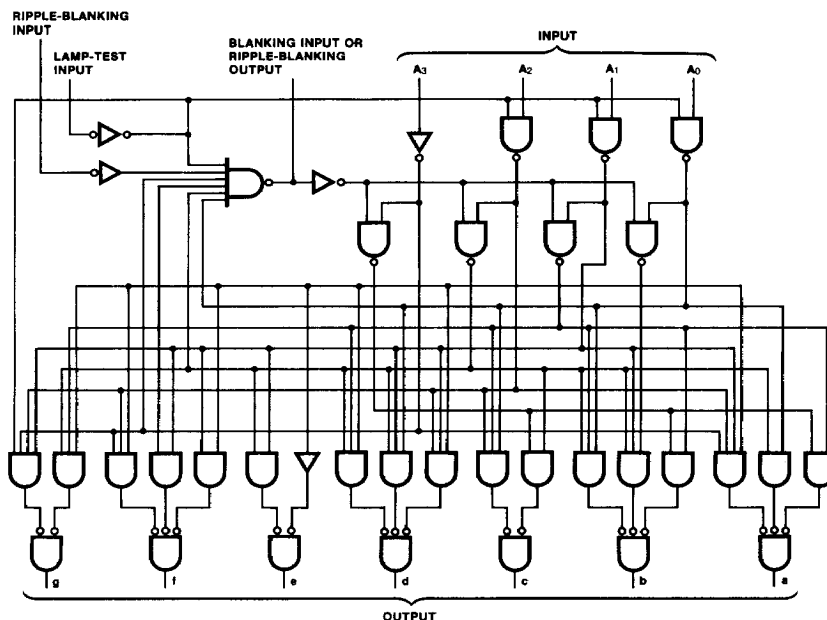
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
IoH	Output HIGH Current at a — g		-1.3		-1.3		mA	V_{CC} = Min, V_{OUT} = 0.85 V
Ios	Output Short Circuit Current at $\overline{BI/RBO}$			-4.0	-0.3	-2.0	mA	V_{CC} = Max, V_{OUT} = 0 V
Icc	Power Supply Current	XM		76		38	mA	V_{CC} = Max
		XC		90		38		All Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 1 kΩ Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
tPLH tPHL	Propagation Delay A_n to a — g		100 100		100 100	ns	Figs. 3-1, 3-20
tPLH tPHL	Propagation Delay $\overline{RBI}$ to a — f		100 100		100 100	ns	Figs. 3-1, 3-5 $\overline{LT}$=HIGH, A_0 — A_3=HIGH