PSMN011-30YLC

N-channel 30 V 11.6 mΩ logic level MOSFET in LFPAK using NextPower technology

Rev. 3 — 24 October 2011 Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

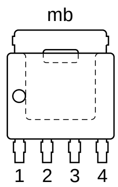
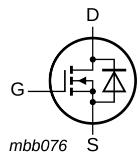
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1	-	-	37	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	29	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; see Figure 12	-	12.3	14.5	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see Figure 12	-	9.9	11.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 10 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	1.4	-	nC
$Q_{G(tot)}$	total gate charge	V_{GS} = 4.5 V; I_D = 10 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	4.9	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			SOT669 (LFPAK; Power-SO8)	

3. Ordering information

Table 3. Ordering information

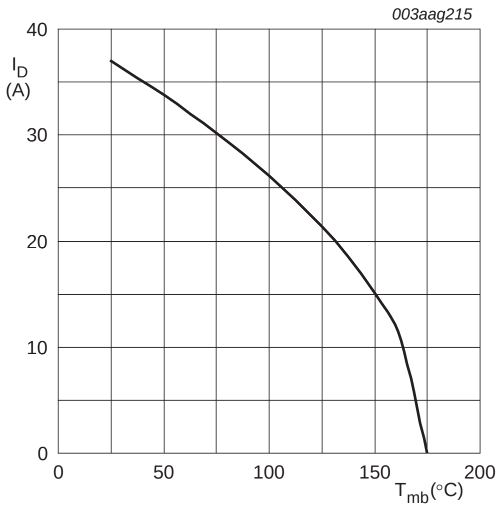
Type number	Package		
	Name	Description	Version
PSMN011-30YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

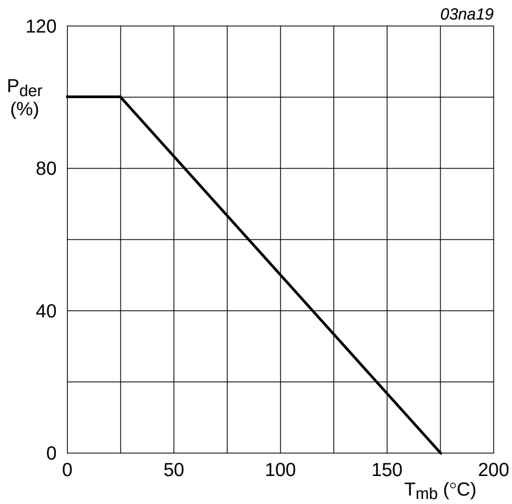
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	37	A
		V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	26	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; see Figure 4	-	150	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	29	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	140	-	V
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	26	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 37 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped; see Figure 3	-	9	mJ



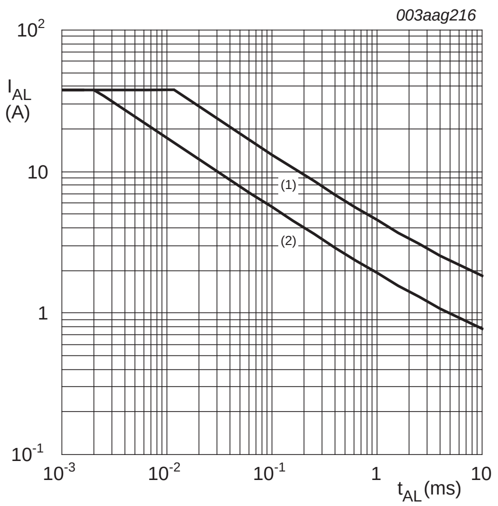
$$V_{GS} \geq 10V$$

Fig 1. Continuous drain current as a function of mounting base temperature



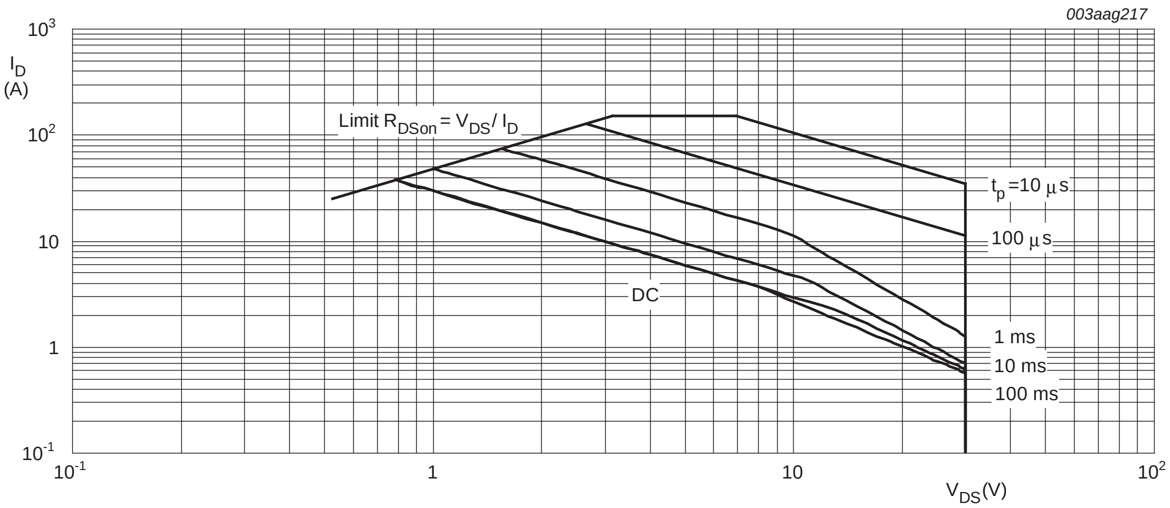
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$(1)\ T_{j\,(init)} = 25^\circ C;\ (2)\ T_{j\,(init)} = 100^\circ C$$

Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



$T_{mb} = 25°C;\ I_{DM}$ *is a single pulse*

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	4.87	5.06	K/W

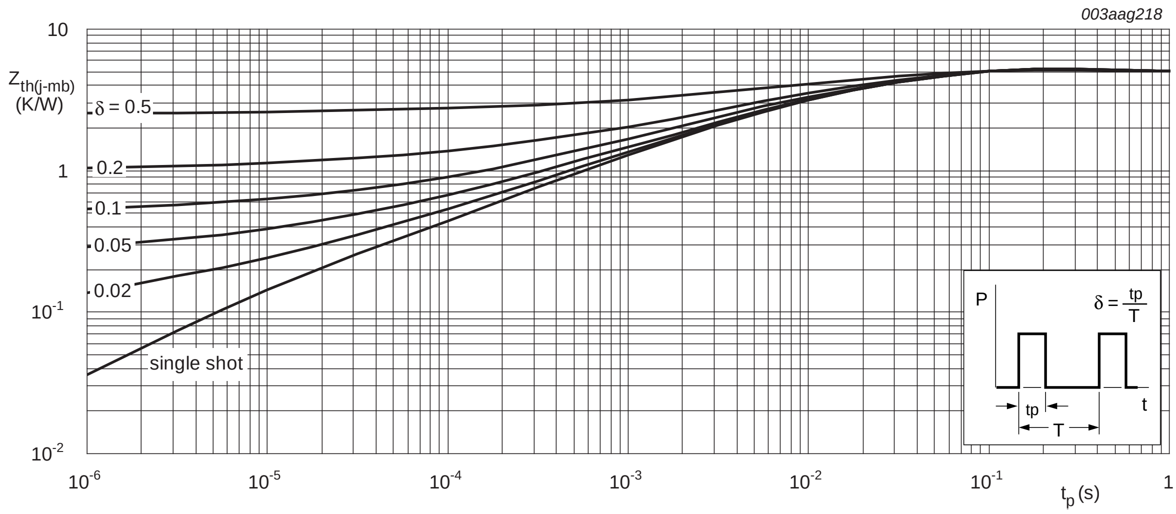


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

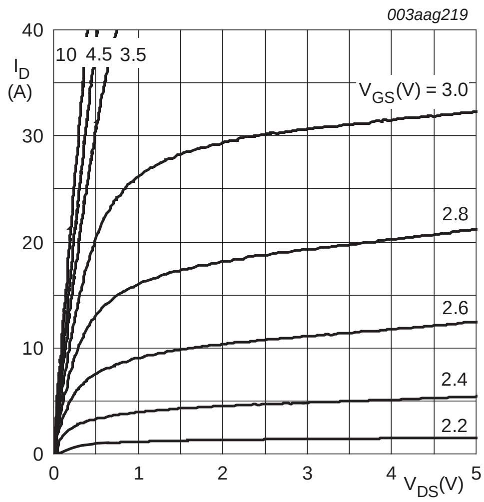
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	1.05	1.57	1.95	V
		I_D = 10 mA; V_{DS} = V_{GS}; T_j = 150 °C	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C	-	-	2.25	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; see Figure 12	-	12.3	14.5	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 150 °C; see Figure 12; see Figure 13	-	-	23.4	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see Figure 12	-	9.9	11.6	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 150 °C; see Figure 12; see Figure 13	-	-	18.8	mΩ
R_G	gate resistance	f = 1 MHz	-	2	4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	10.3	-	nC
		I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see Figure 14; see Figure 15	-	4.9	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	9	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see Figure 14; see Figure 15	-	1.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.4	-	nC
Q_{GD}	gate-drain charge		-	1.4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	2.5	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	641	-	pF
C_{oss}	output capacitance		-	146	-	pF
C_{rss}	reverse transfer capacitance		-	46	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω	-	13.4	-	ns
t_r	rise time		-	12.7	-	ns
$t_{d(off)}$	turn-off delay time		-	16.8	-	ns
t_f	fall time		-	6.6	-	ns

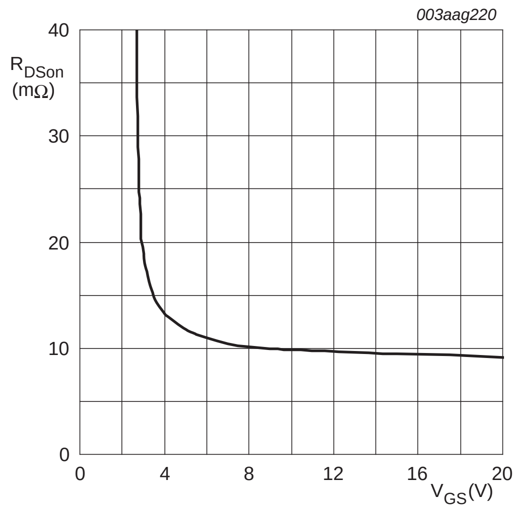
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C	-	3.8	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 17	-	0.85	1.1	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V	-	17	-	ns
Q_r	recovered charge		-	7	-	nC
t_a	reverse recovery rise time	V_{GS} = 0 V; I_S = 10 A; dI_S/dt = -100 A/µs; V_{DS} = 15 V; see Figure 18	-	10	-	ns
t_b	reverse recovery fall time		-	7	-	ns



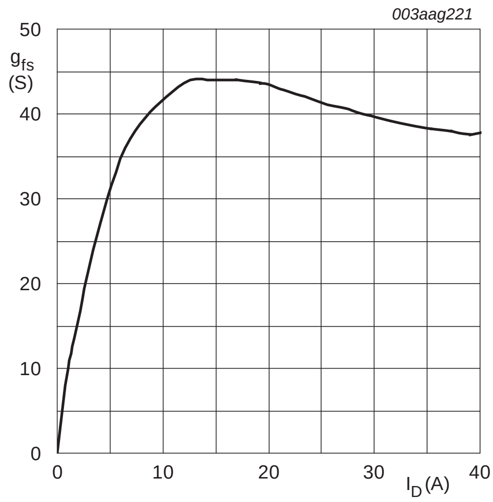
$T_j = 25°C$

Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



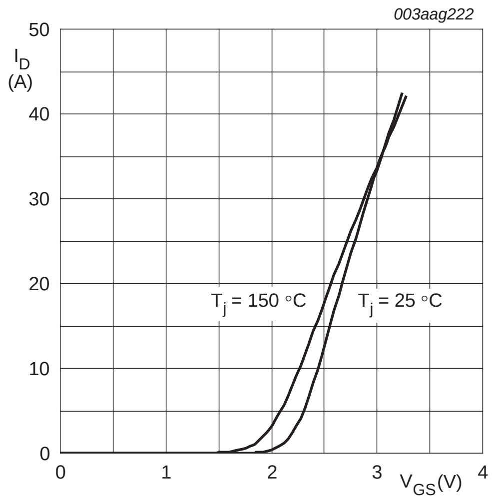
$T_j = 25°C;\ I_D = 10A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



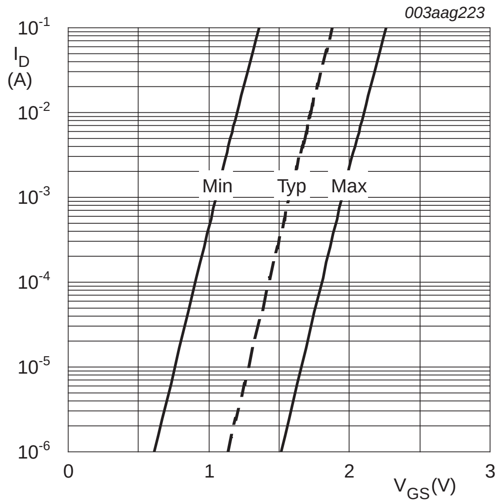
$T_j = 25°C$; $V_{DS} = 10V$

Fig 8. Forward transconductance as a function of drain current; typical values



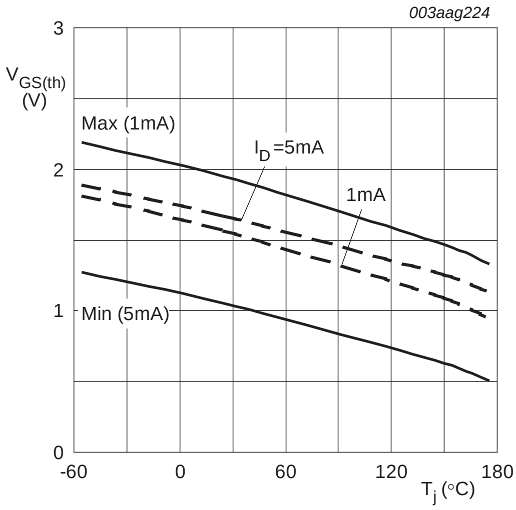
$V_{DS} = 10V$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



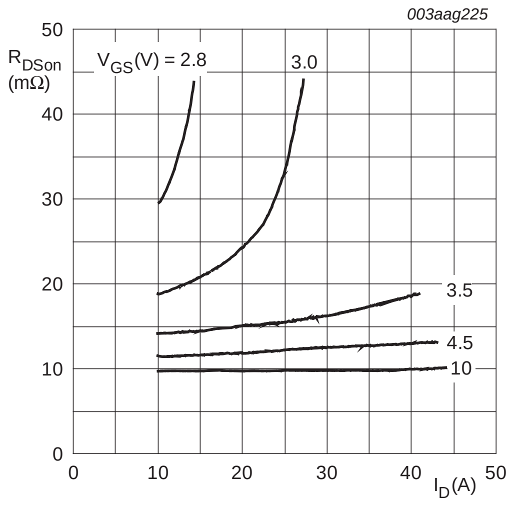
$T_j = 25°C$; $V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



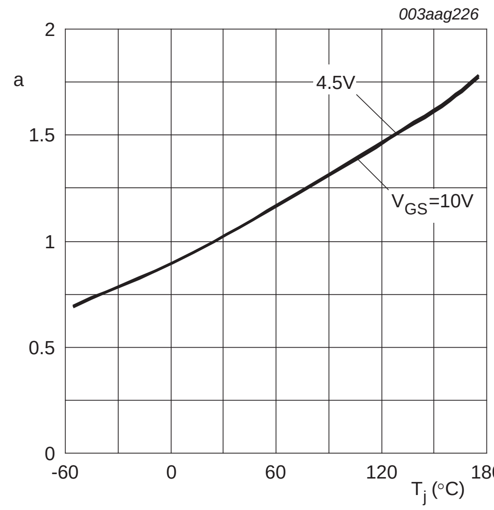
$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

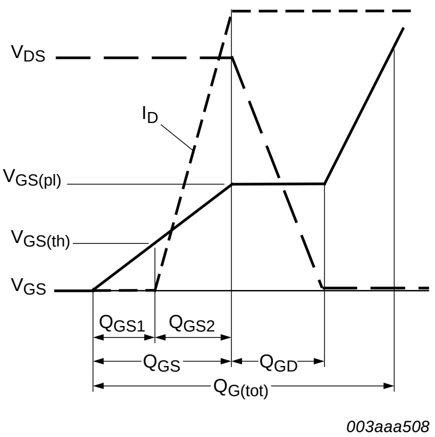
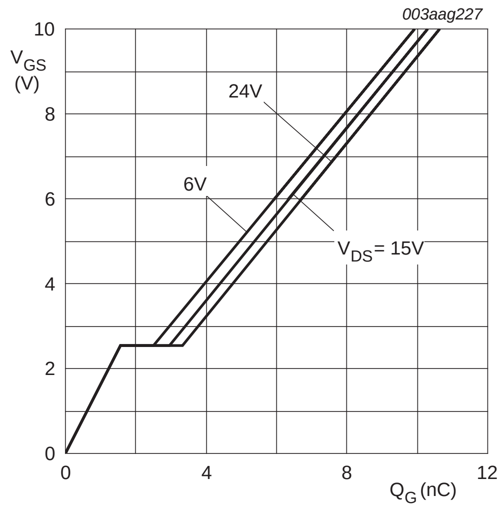
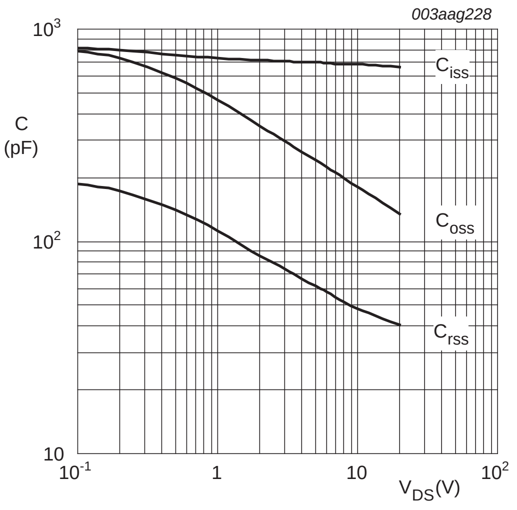


Fig 14. Gate charge waveform definitions



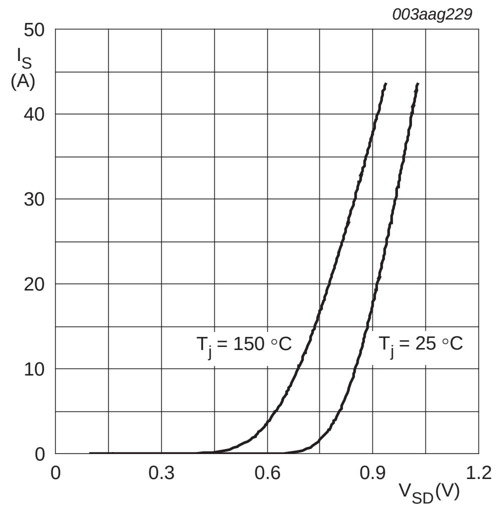
$T_j = 25°C;\ I_D = 10A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V;\ f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 17. Source current as a function of source-drain voltage; typical values

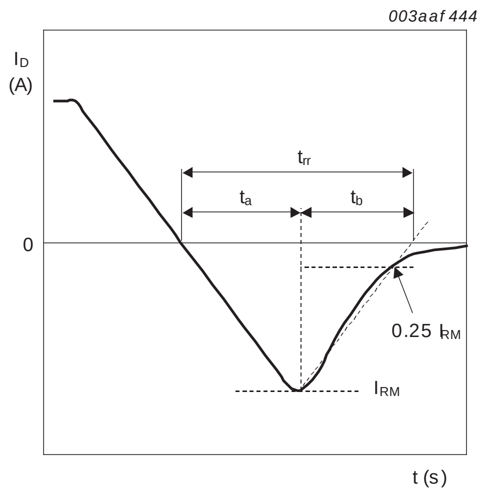
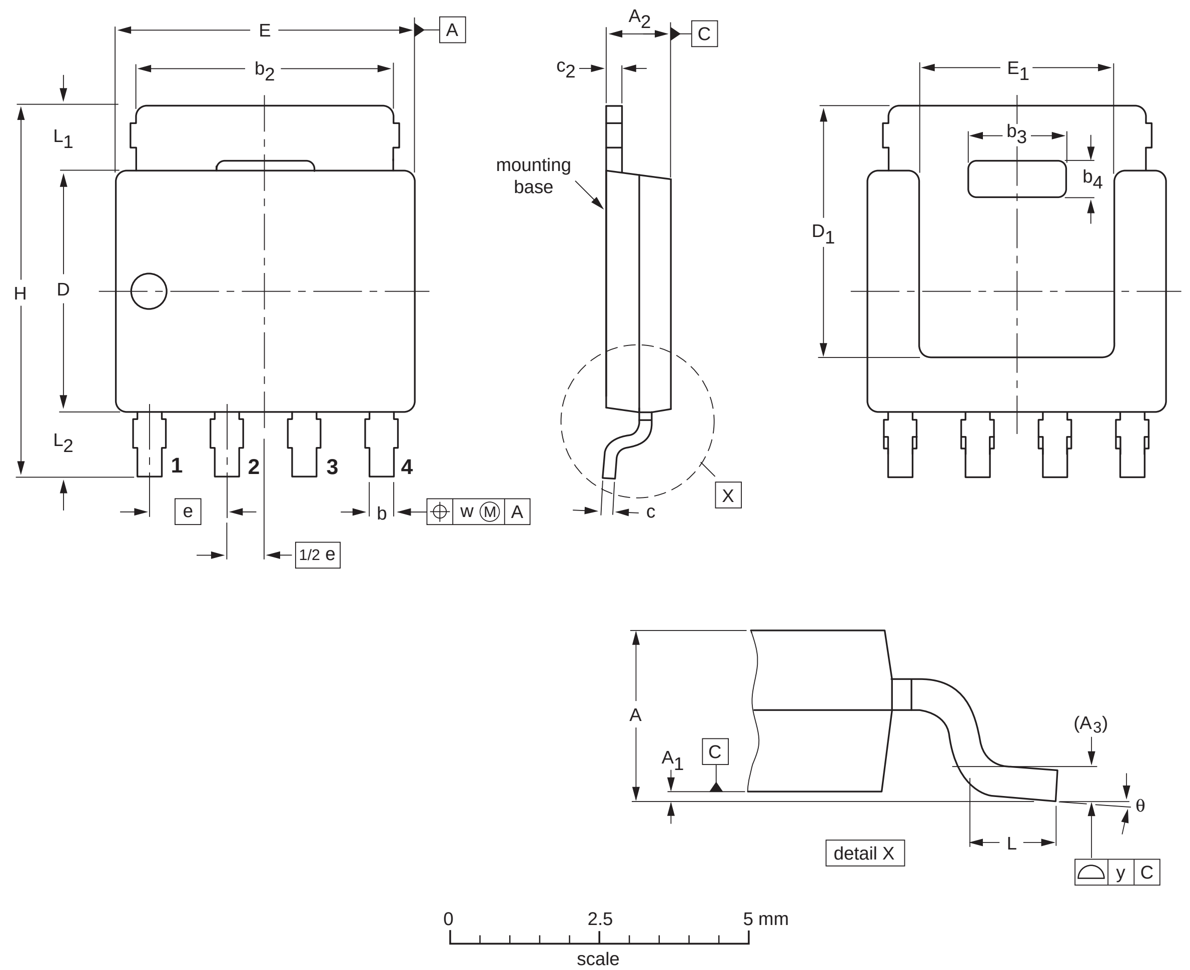


Fig 18. Reverse recovery timing definition

7. Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~06-03-16~~ 11-03-25

Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN011-30YLC v.3	20111024	Product data sheet	-	PSMN011-30YLC v.2
Modifications:	• Data sheet status changed from preliminary to product. • Various changes to content.			
PSMN011-30YLC v.2	20110930	Preliminary data sheet	-	PSMN011-30YLC v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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