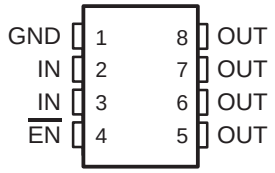
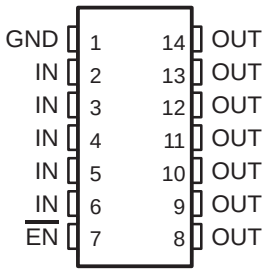
- **95-mΩ Max (5.5-V Input) High-Side MOSFET Switch With Logic Compatible Enable Input**
- **Short-Circuit and Thermal Protection**
- **Typical Short-Circuit Current Limits:**
  0.4 A, TPS2010; 1.2 A, TPS2011;
  2 A, TPS2012; 2.6 A, TPS2013
- **Electrostatic-Discharge Protection, 12-kV Output, 6-kV All Other Terminals**
- **Controlled Rise and Fall Times to Limit Current Surges and Minimize EMI**
- **SOIC-8 Package Pin Compatible With the Popular Littlefoot™ Series When GND Is Connected**
- **2.7-V to 5.5-V Operating Range**
- **10-μA Maximum Standby Current**
- **Surface-Mount SOIC-8 and TSSOP-14 Packages**
- **–40°C to 125°C Operating Junction Temperature Range**

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TPS201x family of power-distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ N-channel MOSFET. Gate drive is provided by an internal driver and charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump operates at 100 kHz, requires no external components, and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short circuit is present, the TPS201x limits the output current to a safe level by switching into a constant-current mode. Continuous heavy overloads and short circuits increase power dissipation in the switch and cause the junction temperature to rise. If the junction temperature reaches approximately 180°C, a thermal protection circuit shuts the switch off to prevent damage. Recovery from thermal shutdown is automatic once the device has cooled sufficiently.

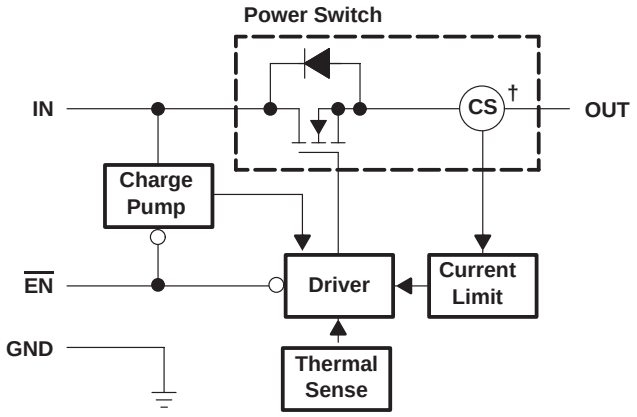
The members of the TPS201x family differ only in short-circuit current threshold. The TPS2010 is designed to limit at 0.4-A load; the other members of the family limit at 1.2 A, 2 A, and 2.6 A (see the available options table). The TPS201x family is available in 8-pin small-outline integrated circuit (SOIC) and 14-pin thin shink small-outline (TSSOP) packages and operates over a junction temperature range of –40°C to 125°C. Versions in the 8-pin SOIC package are drop-in replacements for Siliconix's Littlefoot™ power PMOS switches, except that GND must be connected.

AVAILABLE OPTIONS

T_J	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT OUTPUT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES		CHIP FORM (Y)
			SOIC (D)†	TSSOP (PW)‡	
–40°C to 125°C	0.2	0.4	TPS2010D	TPS2010PWLE	TPS2010Y
	0.6	1.2	TPS2011D	TPS2011PWLE	TPS2011Y
	1	2	TPS2012D	TPS2012PWLE	TPS2012Y
	1.5	2.6	TPS2013D	TPS2013PWLE	TPS2013Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2010PWLE).

functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D	PW		
$\overline{EN}$	4	7	I	Enable input. Logic low turns power switch on.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5–8	8–14	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5.5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

detailed description (continued)

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{EN}$)

A logic high on the $\overline{EN}$ input turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET monitors the current supplied to the load. The sense FET is a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

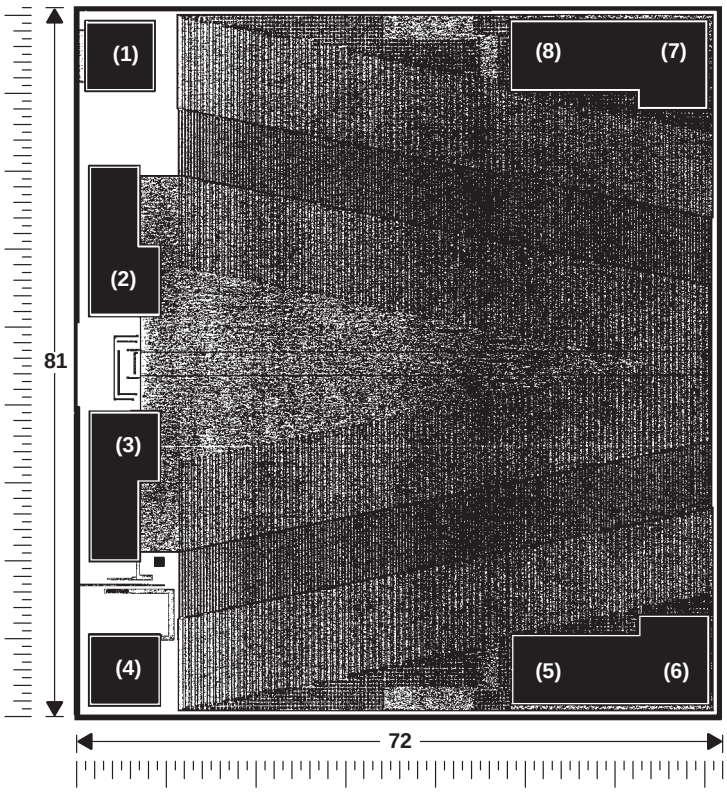
thermal sense

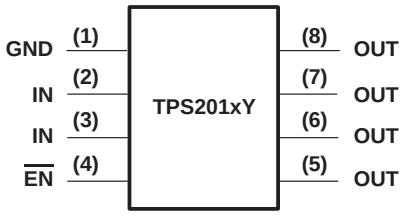
An internal thermal-sense circuit shuts the power switch off when the junction temperature rises to approximately 180°C. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

TPS201xY chip information

This chip, when properly assembled, displays characteristics similar to the TPS201xC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.3 V to $V_{I(IN)}$ +0.3 V
Input voltage range, V_I at $\overline{EN}$ . . . . . –0.3 V to 7 V
Continuous output current, I_O . . . . . internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$		2.7	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2010	0	0.2	A
	TPS2011	0	0.6	
	TPS2012	0	1	
	TPS2013	0	1.5	
Operating virtual junction temperature, T_J		–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†		TPS2010, TPS2011 TPS2012, TPS2013 MIN	TYP	MAX	UNIT
On-state resistance		$V_{I(IN)}$ = 5.5 V,	T_J = 25°C		75	95	mΩ
		$V_{I(IN)}$ = 4.5 V,	T_J = 25°C		80	110	
		$V_{I(IN)}$ = 3 V,	T_J = 25°C		120	175	
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C		140	215	
Output leakage current		$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.001	1	µA
			–40°C ≤ T_J ≤ 125°C			10	
t_r	Output rise time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 µF		4		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 µF		3.8		
t_f	Output fall time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 µF		3.9		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013 MIN	TYP	MAX	UNIT
	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ < 4.5 V			0.4	
	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$	–0.5		0.5	µA
t_{PLH}	Propagation (delay) time, low-to-high-level output	C_L = 1 µF			20	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	C_L = 1 µF			40	

current limit

PARAMETER	TEST CONDITIONS†		TPS2010, TPS2011 TPS2012, TPS2013 MIN	TYP	MAX	UNIT
Short-circuit current	T_J = 25°C, $V_{I(IN)}$ = 5.5 V, OUT connected to GND, device enabled into short circuit	TPS2010	0.22	0.4	0.6	A
		TPS2011	0.66	1.2	1.8	
		TPS2012	1.1	2	3	
		TPS2013	1.65	2.6	4.5	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS		TPS2010, TPS2011 TPS2012, TPS2013			UNIT
			MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.015	1	µA
		–40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73	100	µA
		–40°C ≤ T_J ≤ 125°C			100	

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V, T_J = 25°C (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†		TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
			MIN	TYP	MAX	
On-state resistance	$V_{I(IN)}$ = 5.5 V,			75		mΩ
	$V_{I(IN)}$ = 4.5 V,			80		
	$V_{I(IN)}$ = 3 V,			120		
	$V_{I(IN)}$ = 2.7 V,			140		
Output leakage current	$\overline{EN}$ = $V_{I(IN)}$			0.001		µA
Output rise time	$V_{I(IN)}$ = 5.5 V,	C_L = 1 µF		4		ms
	$V_{I(IN)}$ = 2.7 V,	C_L = 1 µF		3.8		
Output fall time	$V_{I(IN)}$ = 5.5 V,	C_L = 1 µF		3.9		ms
	$V_{I(IN)}$ = 2.7 V,	C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

current limit

PARAMETER	TEST CONDITIONS†	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Short-circuit current	$V_{I(IN)}$ = 5.5 V, OUT connected to GND, Device enabled into short circuit		0.4		A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN}$ = $V_{I(IN)}$		0.015		µA
Supply current, high-level output	$\overline{EN}$ = 0 V		73		µA

PARAMETER MEASUREMENT INFORMATION

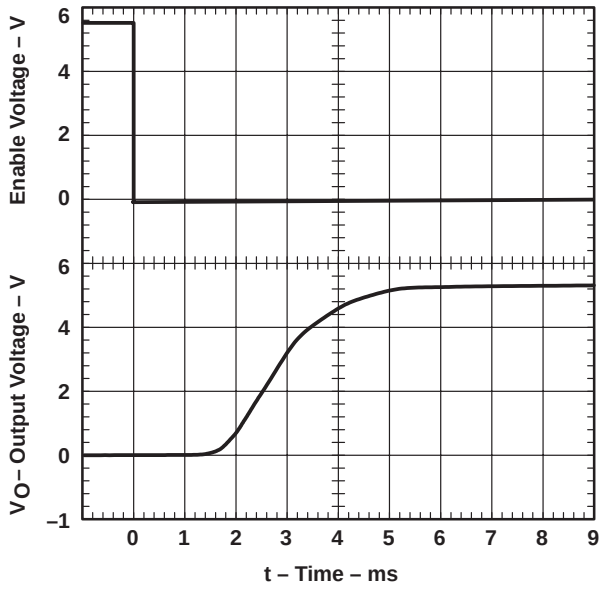


Figure 1. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

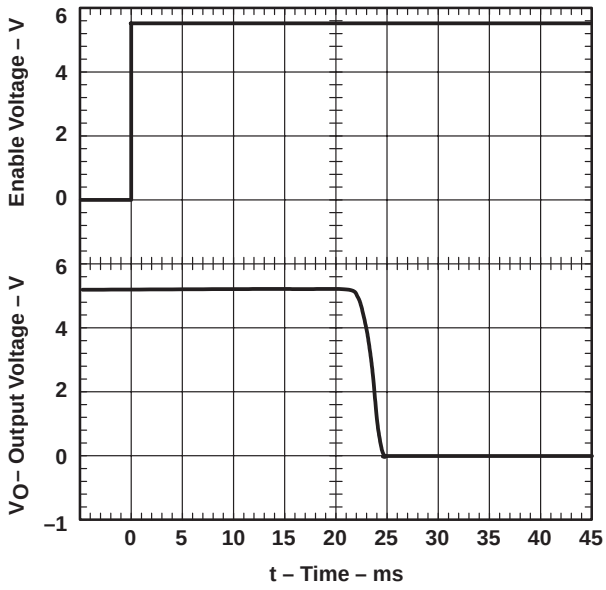


Figure 2. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

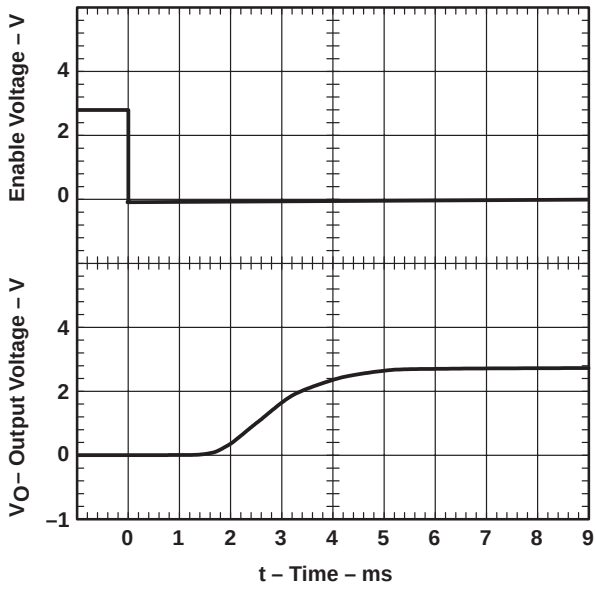


Figure 3. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

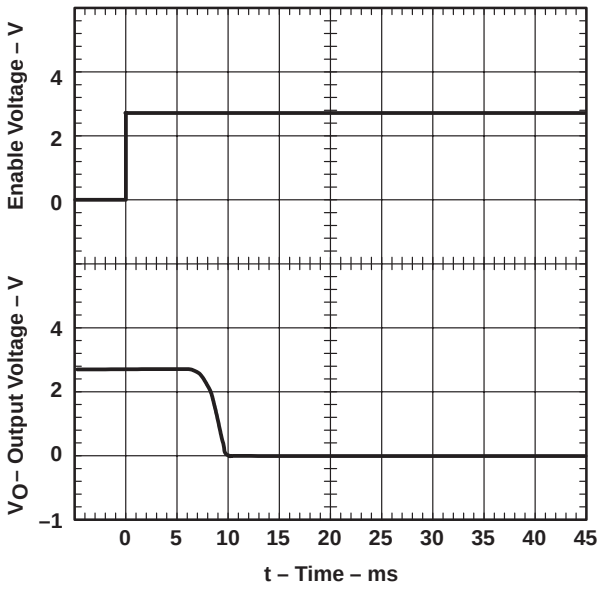


Figure 4. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

PARAMETER MEASUREMENT INFORMATION

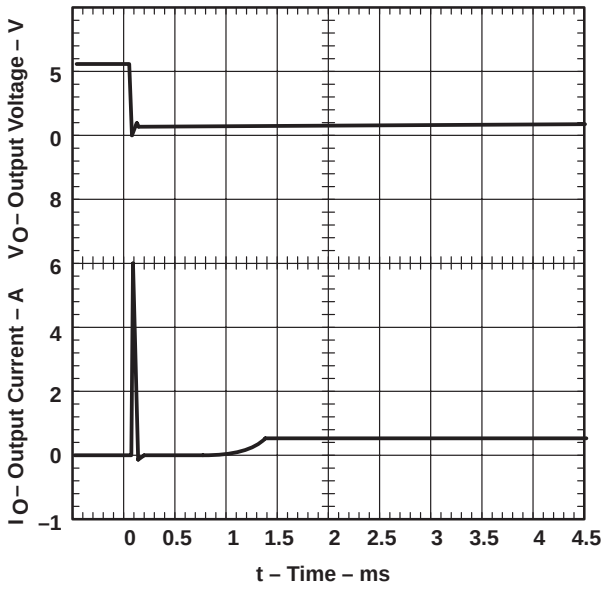


Figure 5. TPS2010, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

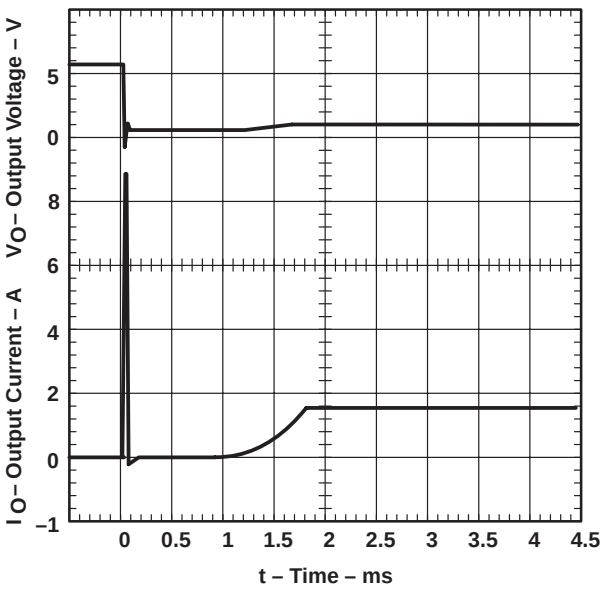


Figure 6. TPS2011, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

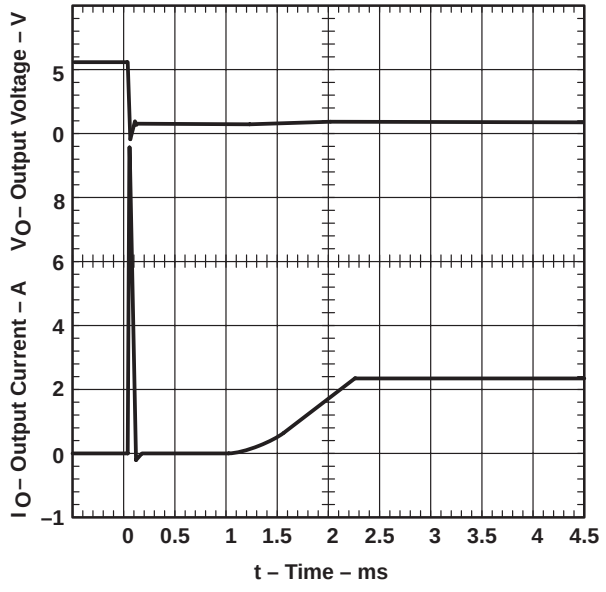


Figure 7. TPS2012, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

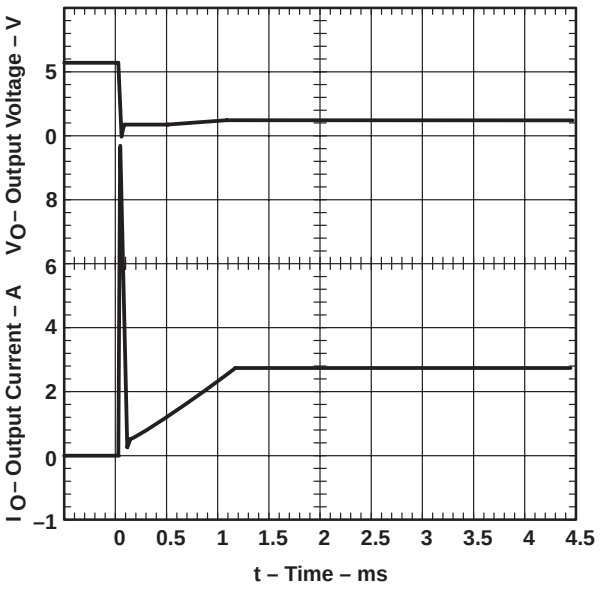


Figure 8. TPS2013 – Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

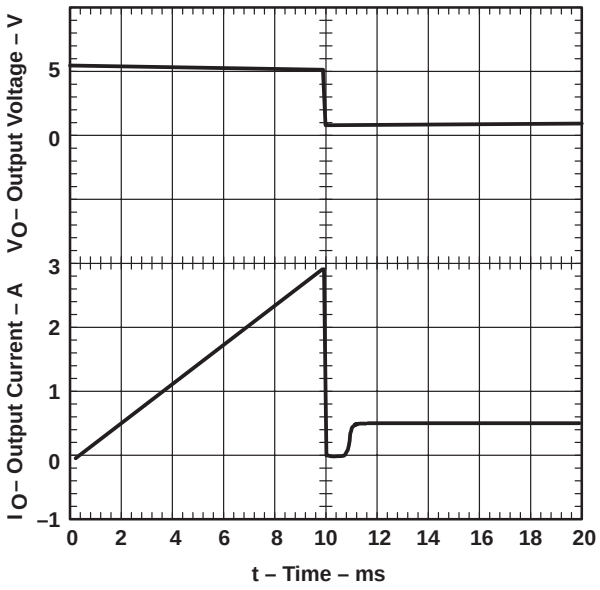


Figure 9. TPS2010 – Threshold Current, $V_{I(IN)}$ = 5.5 V

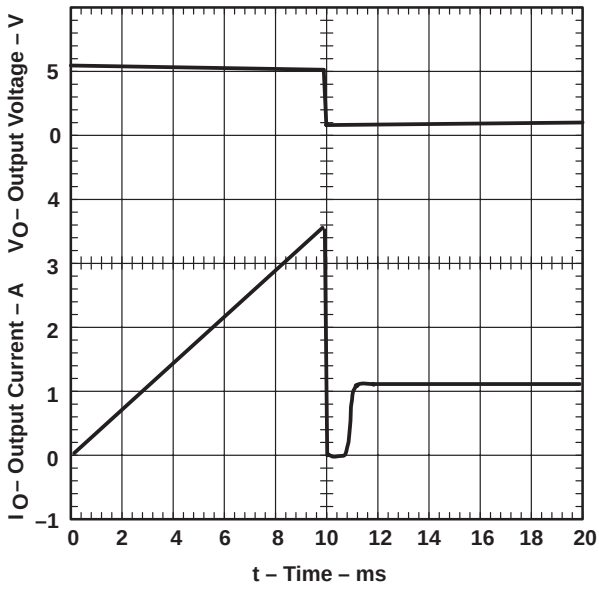


Figure 10. TPS2011 – Threshold Current, $V_{I(IN)}$ = 5.5 V

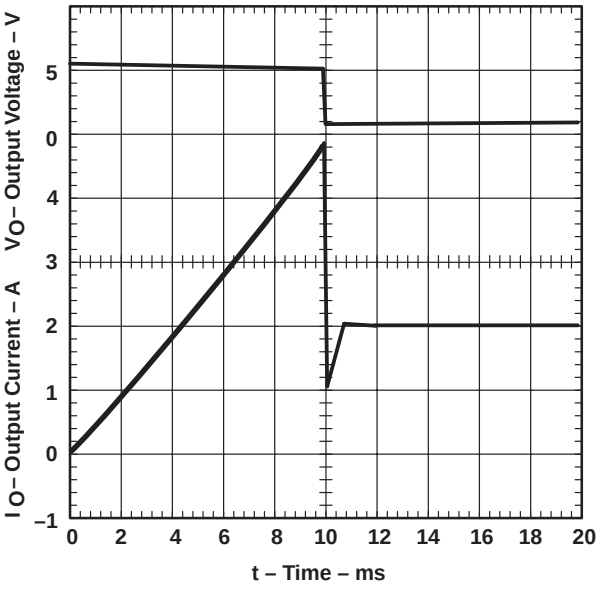


Figure 11. TPS2012 – Threshold Current, $V_{I(IN)}$ = 5.5 V

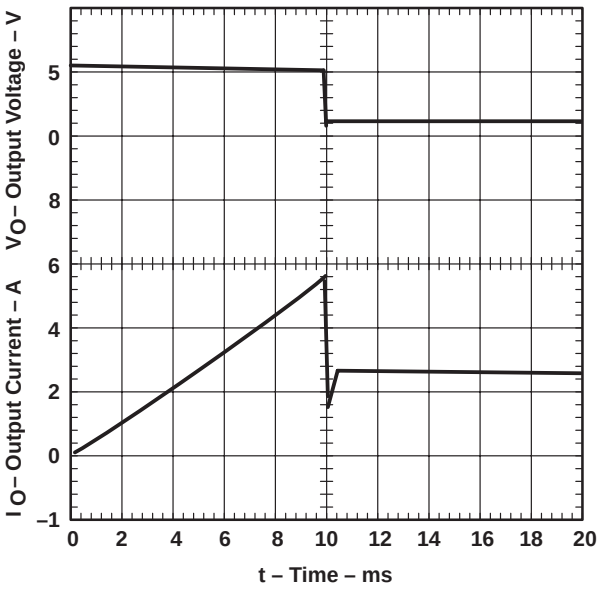


Figure 12. TPS2013 – Threshold Current, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

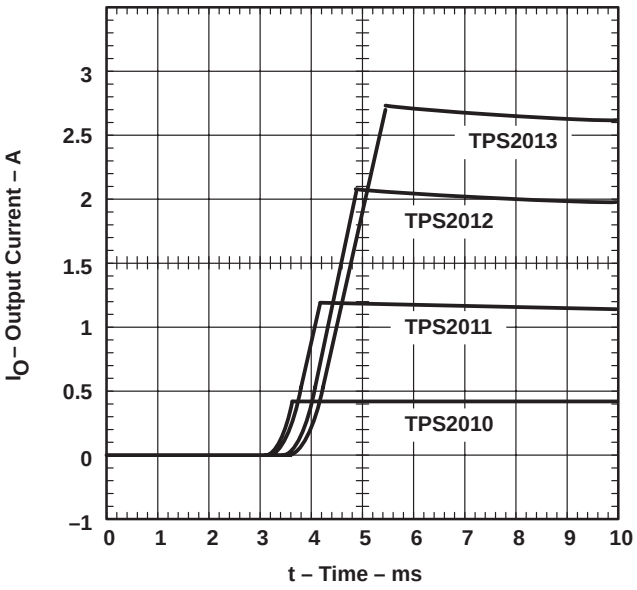


Figure 13. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V

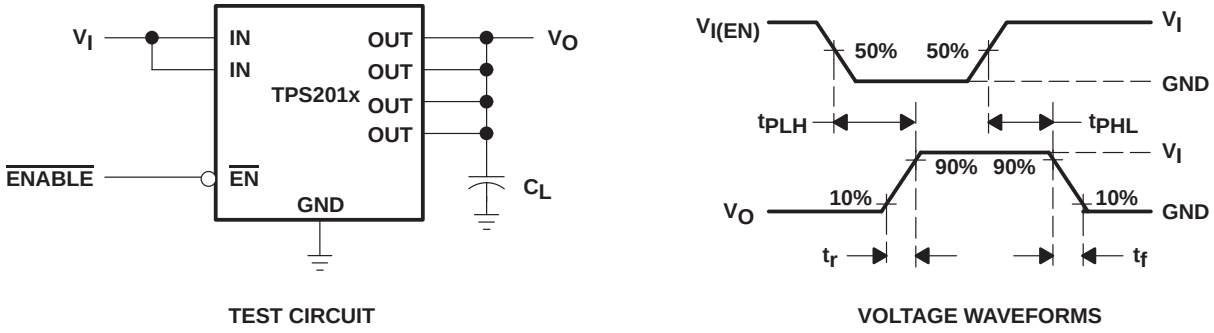


Figure 14. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME vs INPUT VOLTAGE

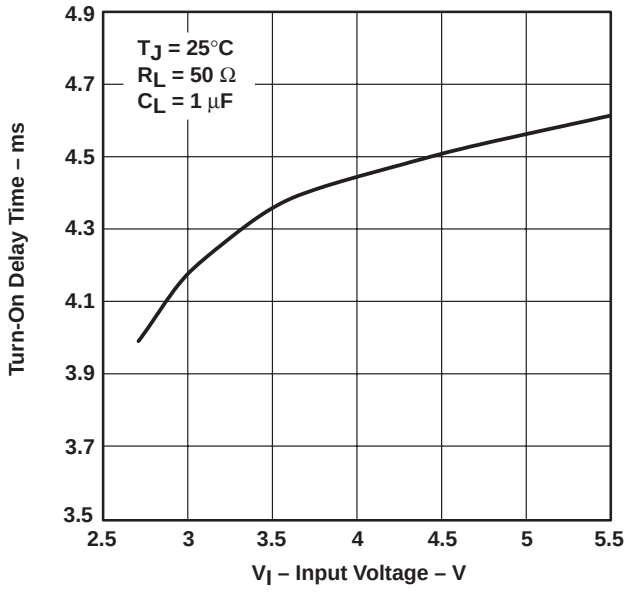


Figure 15

TURN-OFF DELAY TIME vs INPUT VOLTAGE

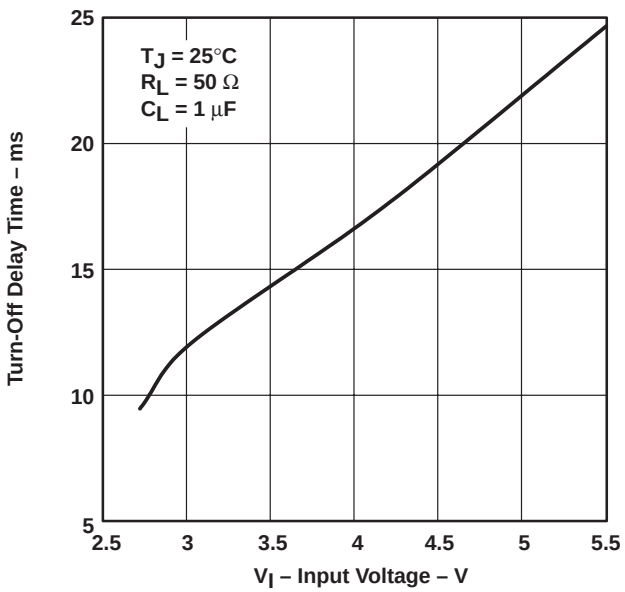


Figure 16

RISE TIME vs OUTPUT CURRENT

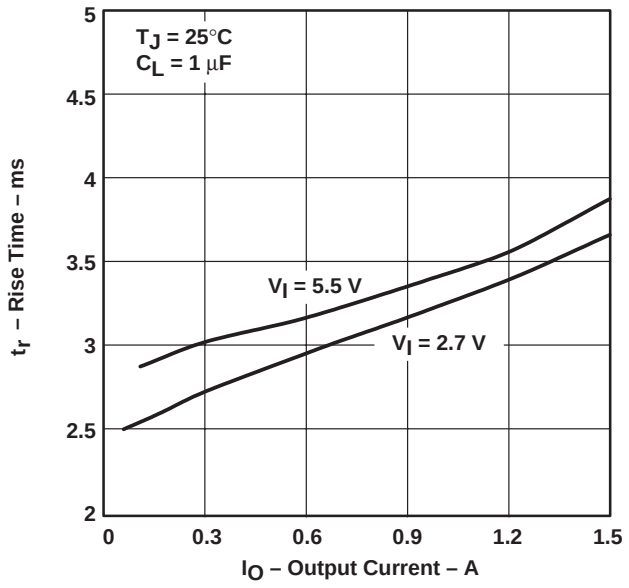


Figure 17

FALL TIME vs OUTPUT CURRENT

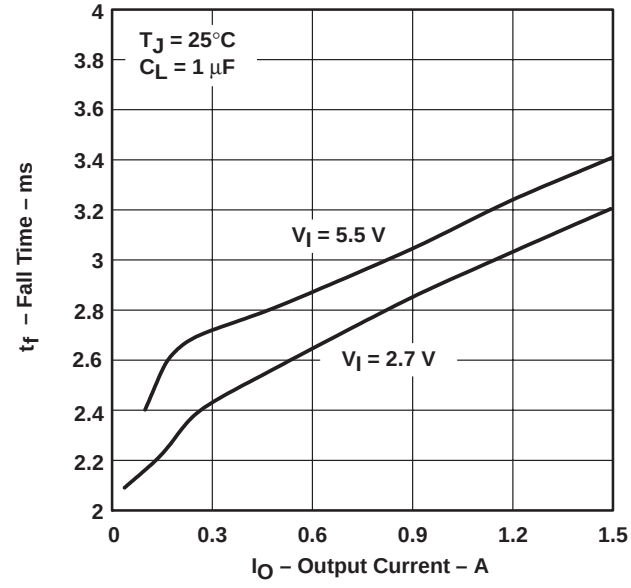


Figure 18

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT (OUTPUT ENABLED)
vs
JUNCTION TEMPERATURE**

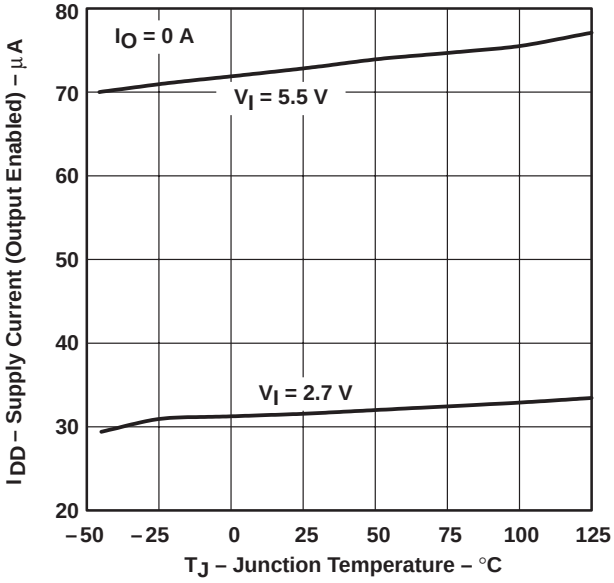


Figure 19

**SUPPLY CURRENT (OUTPUT DISABLED)
vs
JUNCTION TEMPERATURE**

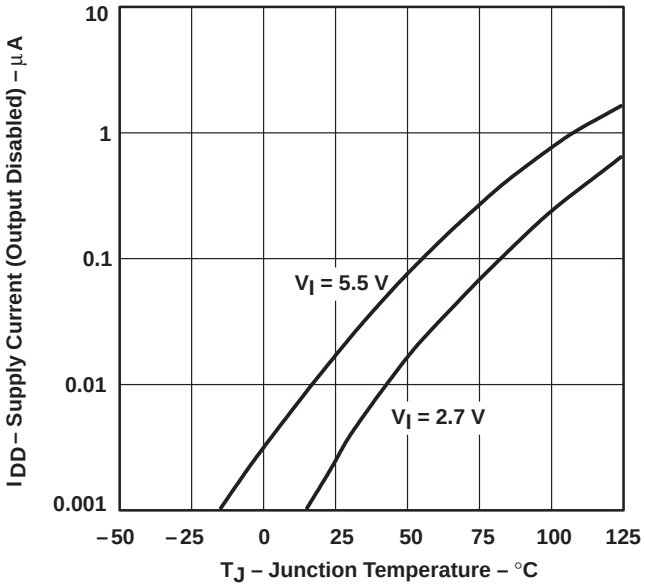


Figure 20

**SUPPLY CURRENT (OUTPUT ENABLED)
vs
INPUT VOLTAGE**

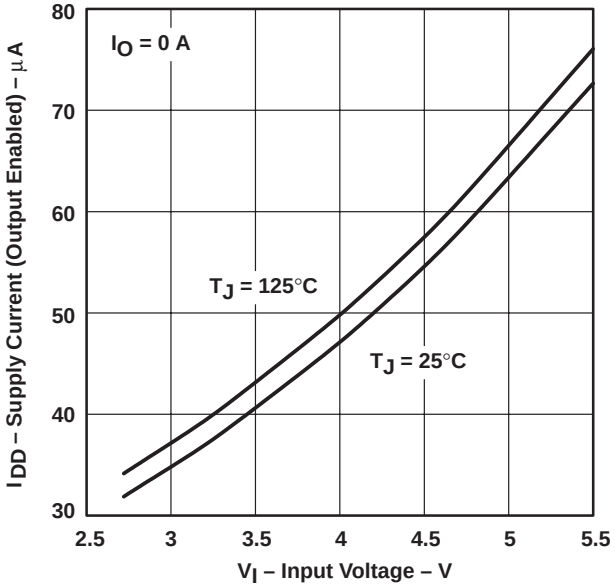


Figure 21

**SUPPLY CURRENT (OUTPUT DISABLED)
vs
INPUT VOLTAGE**

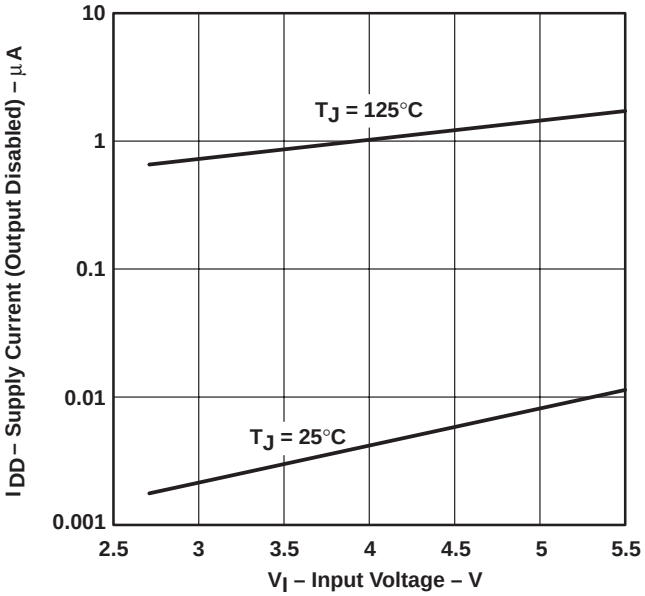


Figure 22

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

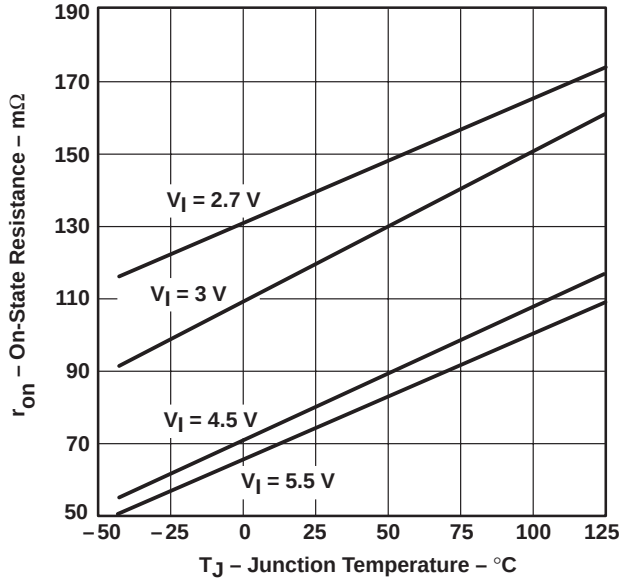


Figure 23

ON-STATE RESISTANCE vs INPUT VOLTAGE

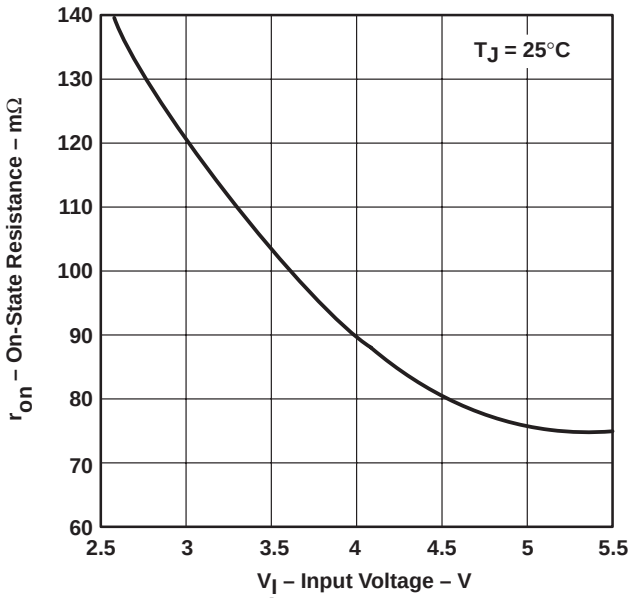


Figure 24

INPUT VOLTAGE TO OUTPUT VOLTAGE vs INPUT VOLTAGE

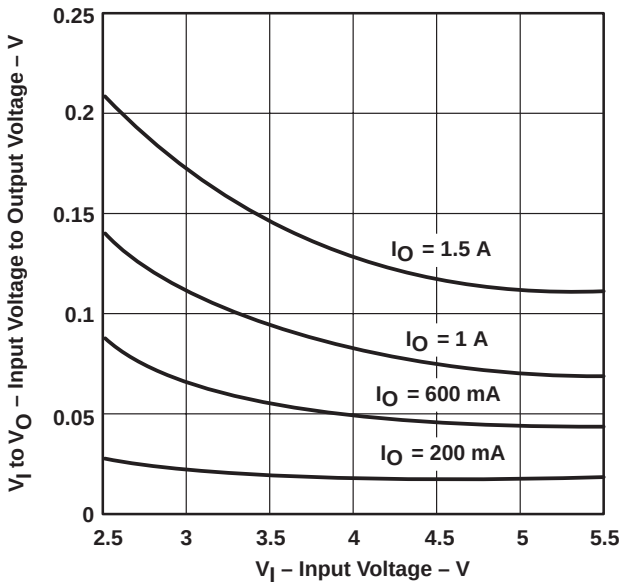


Figure 25

SHORT-CIRCUIT CURRENT vs INPUT VOLTAGE

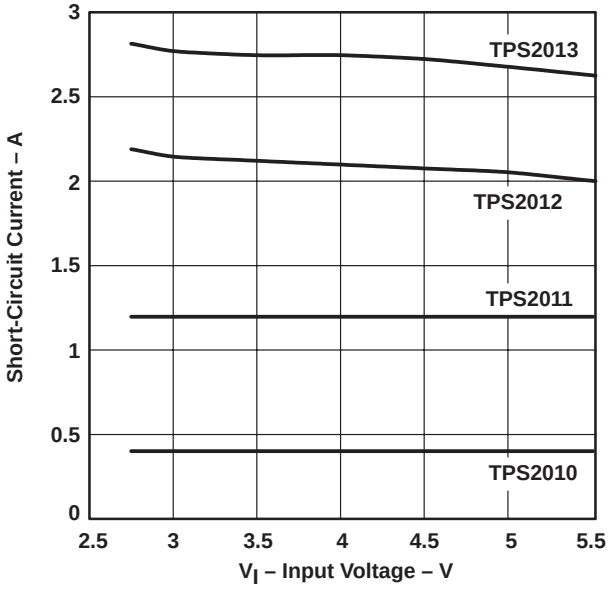


Figure 26

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

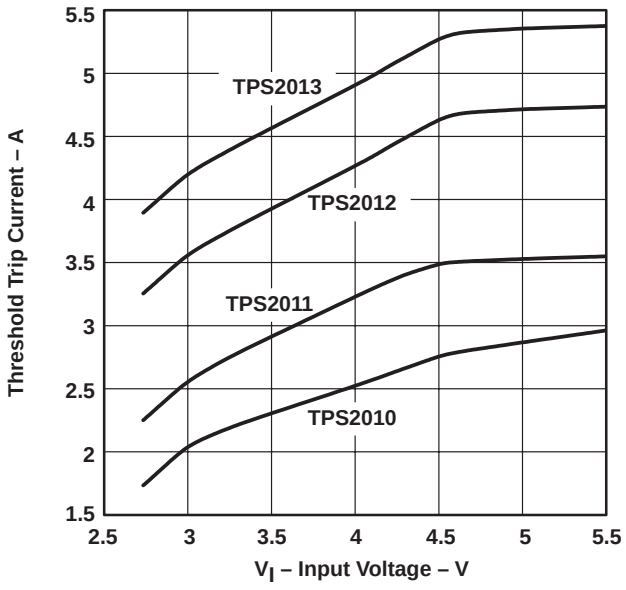


Figure 27

SHORT-CIRCUIT CURRENT vs JUNCTION TEMPERATURE

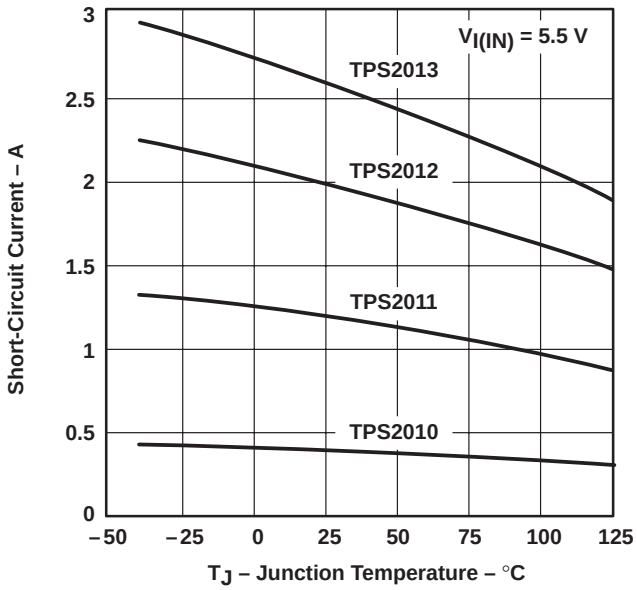


Figure 28

APPLICATION INFORMATION

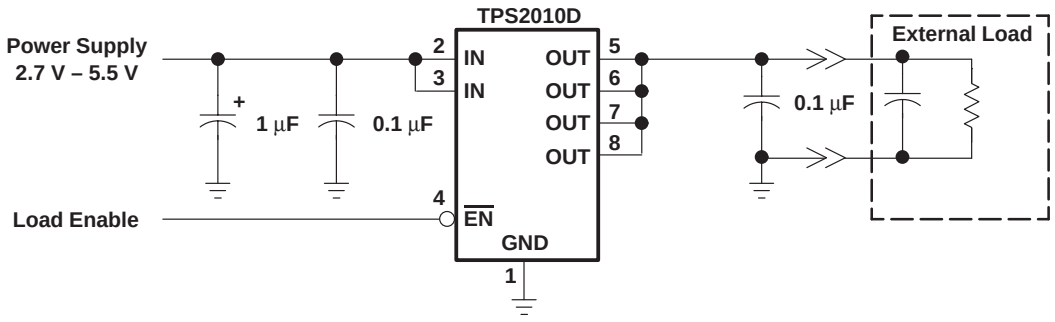


Figure 29. Typical Application

power supply considerations

The TPS201x family has multiple inputs and outputs, which must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.047-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 30). The TPS201x senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 5, 6, 7, and 8). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 9, 10, 11, and 12). The TPS201x family is capable of delivering currents up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

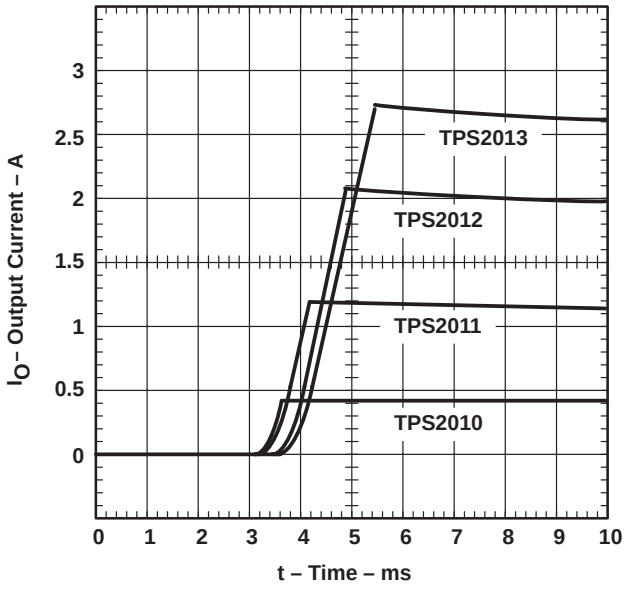


Figure 30. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V

APPLICATION INFORMATION

power dissipation and junction temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages, such as SOIC or TSSOP to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, TSSOP = 179°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection is provided to prevent damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201x into its constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or input power is removed.

ESD protection

All TPS201x terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2010D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010
TPS2010D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010
TPS2010DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010
TPS2010DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010
TPS2010DRG4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010
TPS2011D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011
TPS2011D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011
TPS2011DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011
TPS2011DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011
TPS2012D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012
TPS2012D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012
TPS2012DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012
TPS2012DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012
TPS2013D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013
TPS2013D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013
TPS2013DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013
TPS2013DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013
TPS2013DRG4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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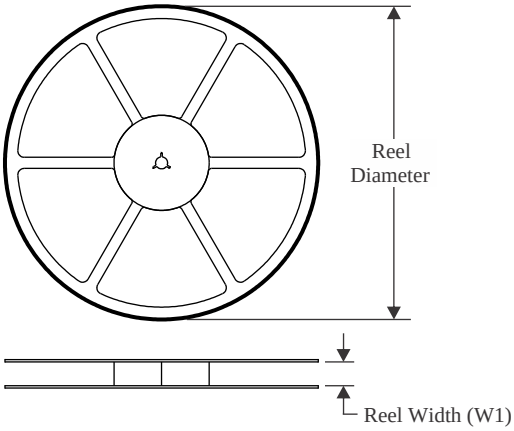
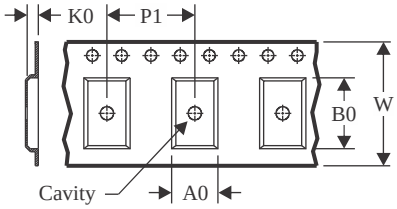
TAPE AND REEL INFORMATION

REEL DIMENSIONS

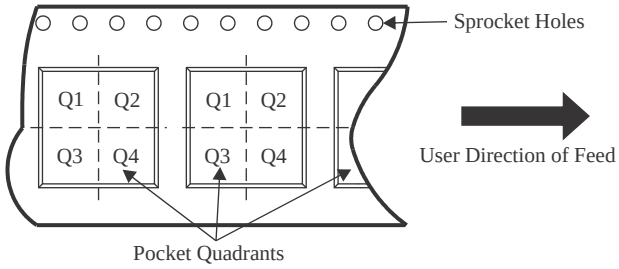


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

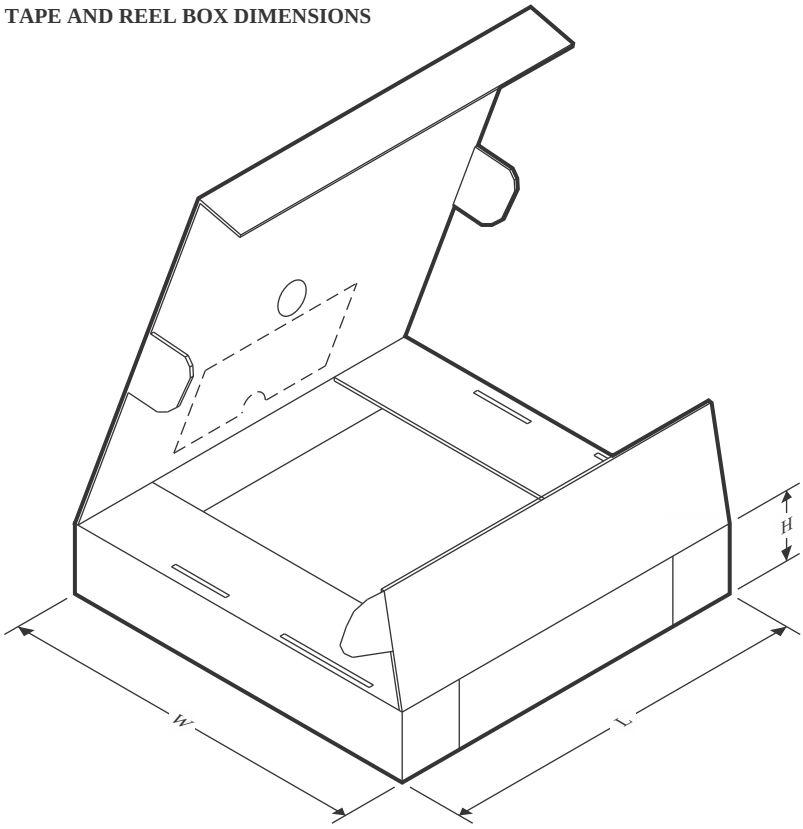
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2010DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2011DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2012DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2013DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

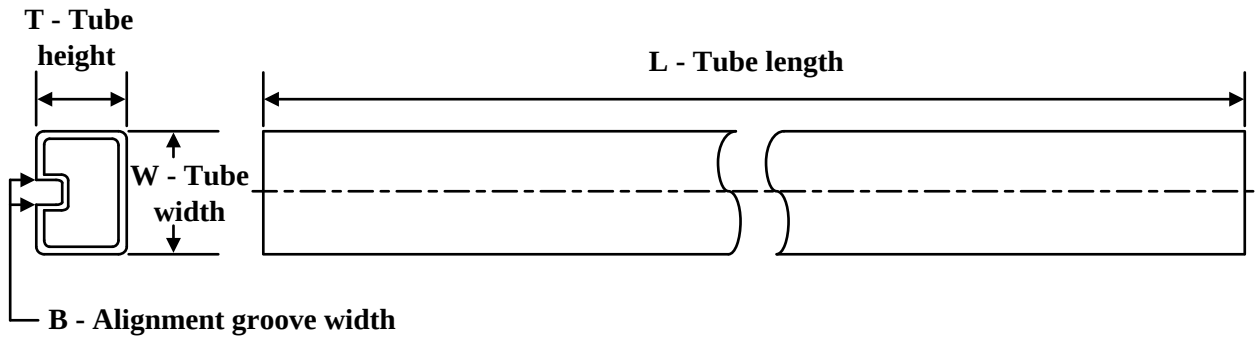
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2010DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2011DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2012DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2013DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2010D	D	SOIC	8	75	507	8	3940	4.32
TPS2010D.A	D	SOIC	8	75	507	8	3940	4.32
TPS2011D	D	SOIC	8	75	507	8	3940	4.32
TPS2011D.A	D	SOIC	8	75	507	8	3940	4.32
TPS2012D	D	SOIC	8	75	507	8	3940	4.32
TPS2012D.A	D	SOIC	8	75	507	8	3940	4.32
TPS2013D	D	SOIC	8	75	507	8	3940	4.32
TPS2013D.A	D	SOIC	8	75	507	8	3940	4.32

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