# V55C2256164VB
# 256Mbit MOBILE SDRAM
# 2.5 VOLT FBGA PACKAGE 16M X 16

| | 7 | 8PC | 10 |
|---|---|---|---|
| System Frequency ($f_{CK}$) | 143 MHz | 125 MHz | 100MHz |
| Clock Cycle Time ($t_{CK3}$) | 7 ns | 8 ns | 10 ns |
| Clock Access Time ($t_{AC3}$) $\overline{CAS}$ Latency = 3 | 5.4 ns | 6 ns | 7 ns |
| Clock Access Time ($t_{AC2}$) CAS Latency = 2 | 6 ns | 6 ns | 8 ns |
| Clock Access Time ($t_{AC1}$) CAS Latency = 1 | 19 ns | 19 ns | 22 ns |

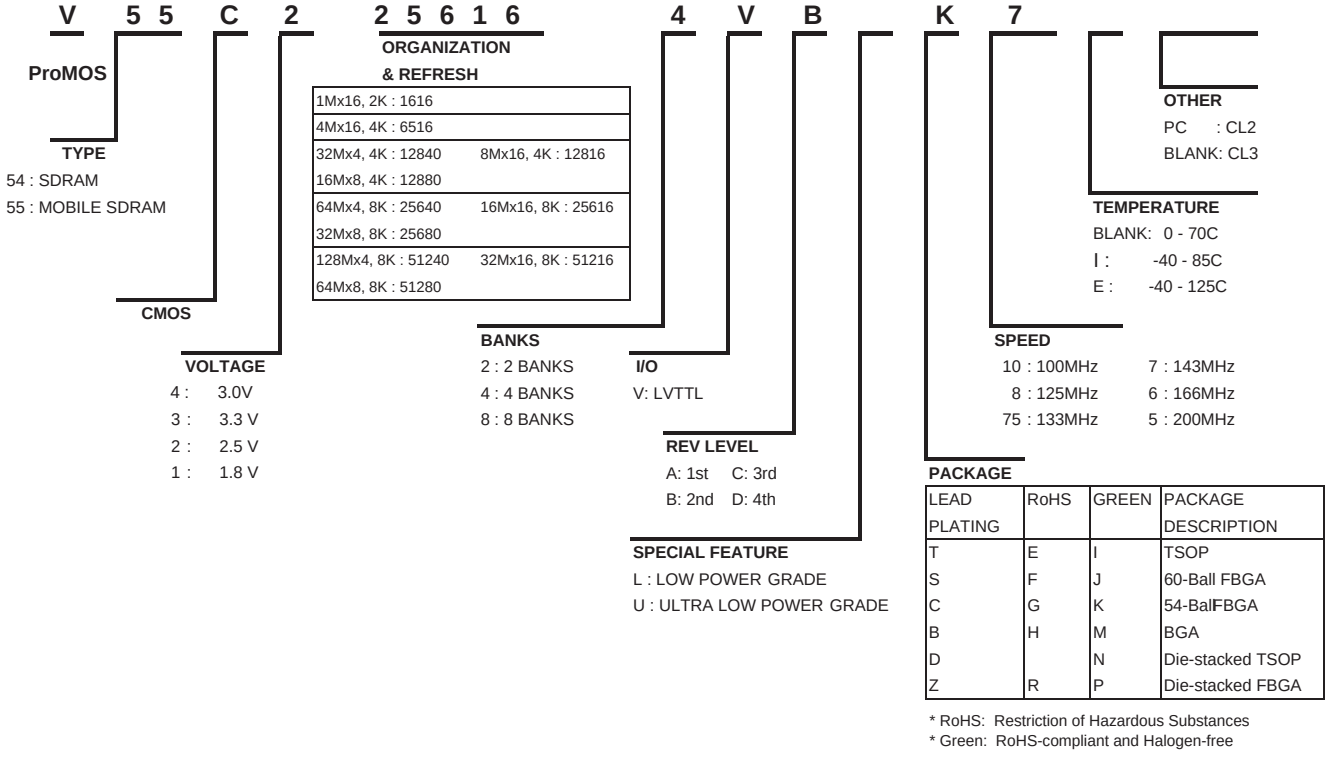
## *Features*

- 4 banks x 4Mbit x 16 organization
- High speed data transfer rates up to 143 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed $\overline{RAS}$ Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency:1, 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8, Full page for Sequential Type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode and Clock Suspend Mode
- Deep Power Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64 ms
- Available in 54-ball FBGA, with 9x6 ball array with 3 depupulated rows, 13x8 mm and 54 pin TSOP II
- VDD=2.5V, VDDQ=1.8V
- Programmable Power Reduction Feature by partial array activation during Self-Refresh
- Operating Temperature Range
  Commercial (0°C to 70°C)
  Industrial (-40°C to +85°C)

## *Device Usage Chart*

| Operating Temperature Range | Package Outline | Access Time (ns) | | | Temperature Mark |
|---|---|---|---|---|---|
| | C/T | 7 | 8PC | 10 | |
| 0°C to 70°C | • | • | • | • | Commercial |
| -40°C to 85°C | • | • | • | • | Industrial |

## *Part Number Information*




| LEAD PLATING | RoHS | GREEN | PACKAGE DESCRIPTION |
|---|---|---|---|
| T | E | I | TSOP |
| S | F | J | 60-Ball FBGA |
| C | G | K | 54-Ball FBGA |
| B | H | M | BGA |
| D | | N | Die-stacked TSOP |
| Z | R | P | Die-stacked FBGA |

* RoHS: Restriction of Hazardous Substances
* Green: RoHS-compliant and Halogen-free

| Description | Pkg. | Pin Count |
|---|---|---|
| FBGA | C | 54 |

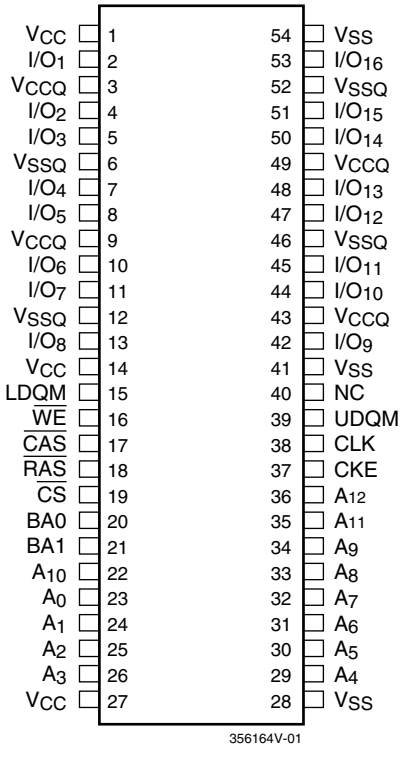
Pin Configuration for x16 devices:

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VSS | DQ15 | VSSQ | A | VDDQ | DQ0 | VDD |
| DQ14 | DQ13 | VDDQ | B | VSSQ | DQ2 | DQ1 |
| DQ12 | DQ11 | VSSQ | C | VDDQ | DQ4 | DQ3 |
| DQ10 | DQ9 | VDDQ | D | VSSQ | DQ6 | DQ5 |
| DQ8 | NC | VSS | E | VDD | LDQM | DQ7 |
| UDQM | CLK | CKE | F | $\overline{CAS}$ | $\overline{RAS}$ | $\overline{WE}$ |
| A12 | A11 | A9 | G | BA0 | BA1 | $\overline{CS}$ |
| A8 | A7 | A6 | H | A0 | A1 | A10 |
| VSS | A5 | A4 | J | A3 | A2 | VDD |

< Top-view >

| Description | Pkg. | Pin Count |
|---|---|---|
| TSOP-II | T | 54 |

### *54 Pin Plastic TSOP-II PIN CONFIGURATION Top View*



356164V-01

### *Pin Names*

| | |
|---|---|
| CLK | Clock Input |
| CKE | Clock Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $A_0$–$A_{12}$ | Address Inputs |
| BA0, BA1 | Bank Select |
| $I/O_1$–$I/O_{16}$ | Data Input/Output |
| LDQM, UDQM | Data Mask |
| $V_{CC}$ | Power (+2.5V) |
| $V_{SS}$ | Ground |
| $V_{CCQ}$ | Power for I/O's (+1.8V) |
| $V_{SSQ}$ | Ground for I/O's |
| NC | Not connected |

### Description

The V55C2256164VB is a four bank Synchronous DRAM organized as 4 banks x 4Mbit x 16. The V55C2256164VB achieves high speed data transfer rates up to 143 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 143 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

### Signal Pin Description

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CLK | Input | Pulse | Positive Edge | The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock. |
| CKE | Input | Level | Active High | Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode. |
| $\overline{CS}$ | Input | Pulse | Active Low | $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM. |
| A0 - A12 | Input | Level | — | During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization:<br>• 8M x 16 SDRAM CA0–CA8.<br><br>In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled.<br>During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge. |
| BA0, BA1 | Input | Level | — | Selects which bank is to be active. |
| DQx | Input Output | Level | — | Data Input/Output pins operate in the same manner as on conventional DRAMs. |
| LDQM UDQM | Input | Pulse | Active High | The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. |
| VCC, VSS | Supply | | | Power and ground for the input buffers and the core logic. |
| VCCQ VSSQ | Supply | — | — | Isolated power supply and ground for the output buffers to provide improved noise immunity. |

### *Operation Definition*

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the thruth table for the operation commands.

| Operation | Device State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | A0-9, A11 | A10 | BS0 BS1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Row Activate | Idle[3] | H | X | L | L | H | H | X | V | V | V |
| Read | Active[3] | H | X | L | H | L | H | X | V | L | V |
| Read w/Autoprecharge | Active[3] | H | X | L | H | L | H | X | V | H | V |
| Write | Active[3] | H | X | L | H | L | L | X | V | L | V |
| Write with Autoprecharge | Active[3] | H | X | L | H | L | L | X | V | H | V |
| Row Precharge | Any | H | X | L | L | H | L | X | X | L | V |
| Precharge All | Any | H | X | L | L | H | L | X | X | H | X |
| Mode Register Set | Idle | H | X | L | L | L | L | X | V | V | V |
| No Operation | Any | H | X | L | H | H | H | X | X | X | X |
| Device Deselect | Any | H | X | H | X | X | X | X | X | X | X |
| Auto Refresh | Idle | H | H | L | L | L | H | X | X | X | X |
| Self Refresh Entry | Idle | H | L | L | L | L | H | X | X | X | X |
| Self Refresh Exit | Idle (Self Refr.) | L | H | H | X | X | X | X | X | X | X |
| | | | | L | H | H | X | | | | |
| Power Down Entry | Idle Active[4] | H | L | H | X | X | X | X | X | X | X |
| | | | | L | H | H | X | | | | |
| Power Down Exit | Any (Power Down) | L | H | H | X | X | X | X | X | X | X |
| | | | | L | H | H | L | | | | |
| Data Write/Output Enable | Active | H | X | X | X | X | X | L | X | X | X |
| Data Write/Output Disable | Active | H | X | X | X | X | X | H | X | X | X |
| Deep Pwoer Down Entry | Idle | H | L | L | H | H | L | H | X | X | X |
| Deep Pwoer Down Exit | Deep power-Down | L | H | X | X | X | X | H | X | X | X |

**Notes:**
1. V = Valid , x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. These are state of bank designated by BS0, BS1 signals.
4. Power Down Mode can not entry in the burst cycle.
5. After Deep Power Down mode exit a full new initialization of memory device is mandatory

### *Power On and Initialization*

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VCC+0.3V on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 μs is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register and Low Power Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

### *Programming the Mode Register*

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

### *Low Power Mode Register*

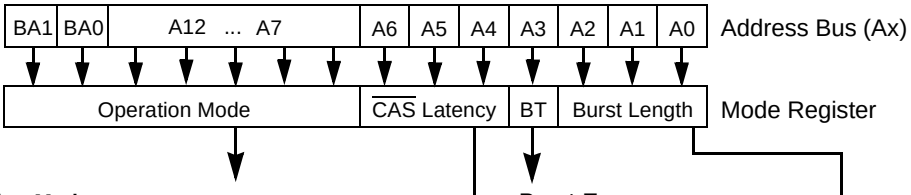
The Low Power Mode Register controls functions beyond those controlled by the Mode Register. These additional functions are unique to the Low-Power DRM and includes a Refresh Period field (TCR) for temperature compensated self-refresh and a Partial-Array Self-Refresh field (PAS). The PASR field is used to specify whether only one quarter (bank 0), one half (bank 0+1) or all banks of the SDRAM array are enabled. Disabled banks will not be refreshed in Self-Refresh mode and written data will be lost. When only bank 0 is selected, it’s possible to partially select only half or mone quarter of bank 0. The TCR field has four entries to set Refresh Period during self-refresh depending on the case temperature of the Low power RAM. It’s required during the initialization seuqence and can be modified when the part id idle.

### *Read and Write Operation*

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, $t_{RCD}$, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 125 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

### *Address Input for Mode Set (Mode Register Operation)*




**Operation Mode**

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | Mode |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Burst Read/Burst Write |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Burst Read/Single Write |

**Burst Type**

| A3 | Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

**CAS Latency**

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserve |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserve |
| 1 | 0 | 1 | Reserve |
| 1 | 1 | 0 | Reserve |
| 1 | 1 | 1 | Reserve |

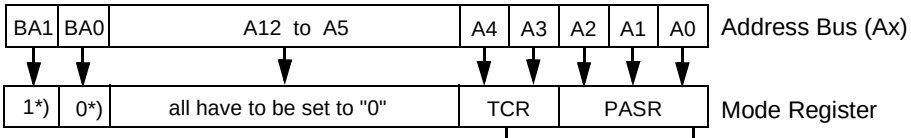
**Burst Length**

| A2 | A1 | A0 | Length | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserve | Reserve |
| 1 | 0 | 1 | Reserve | Reserve |
| 1 | 1 | 0 | Reserve | Reserve |
| 1 | 1 | 1 | Full page | Reserve |

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum $t_{RAS}$ or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

### *Low Power Mode Register Table*




**Self-Refresh: Temperature-Compensated**

| A4 | A3 | Max case temp |
|---|---|---|
| 0 | 0 | 70°C |
| 0 | 1 | 45°C |
| 1 | 0 | 15°C |
| 1 | 1 | 85°C |

**Partial-Array Self Refresh:**

| A2 | A1 | A0 | banks to be self-refreshed |
|---|---|---|---|
| 0 | 0 | 0 | all banks |
| 0 | 0 | 1 | 1/2 array (BA1=0) |
| 0 | 1 | 0 | 1/4 array (BA1=0, BA0=0) |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 1/8 array (BA1=BA0=0, A11=0) |
| 1 | 1 | 0 | 1/16 array (BA1=BA0=0, A11=A10=0) |
| 1 | 1 | 1 | Reserved |

*)BA1 and BA0 must be 1, 0 to select the Extended Mode Register (Vs. the Mode Register)

The Low Power Mode Register must be set during the initialization sequence. Once the device is operational, the Low Power Mode Register set can be issued anytime when the part is idle.

### *Burst Length and Sequence:*

| Burst Length | Starting Address (A2 A1 A0) | Sequential Burst Addressing (decimal) | Interleave Burst Addressing (decimal) |
|---|---|---|---|
| 2 | xx0 | 0, 1 | 0, 1 |
| | xx1 | 1, 0 | 1, 0 |
| 4 | x00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 |
| | 001 | 1 2 3 4 5 6 7 0 | 1 0 3 2 5 4 7 6 |
| | 010 | 2 3 4 5 6 7 0 1 | 2 3 0 1 6 7 4 5 |
| | 011 | 3 4 5 6 7 0 1 2 | 3 2 1 0 7 6 5 4 |
| | 100 | 4 5 6 7 0 1 2 3 | 4 5 6 7 0 1 2 3 |
| | 101 | 5 6 7 0 1 2 3 4 | 5 4 7 6 1 0 3 2 |
| | 110 | 6 7 0 1 2 3 4 5 | 6 7 4 5 2 3 0 1 |
| | 111 | 7 0 1 2 3 4 5 6 | 7 6 5 4 3 2 1 0 |
| Full Page | nnn | Cn, Cn+1, Cn+2 | Not supported |

### *Refresh Mode*

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the CAS -before-RAS refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when RAS and CAS are held low and CKE and WE are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when RAS, CAS, and CKE are low and WE is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one $t_{RC}$ delay is required prior to any access command.

### *DQM Function*

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency $t_{DQZ}$ ). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency $t_{DQW}$ = zero clocks).

### *Power Down*

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for mode entry and exit.

### *Auto Precharge*

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for CAS latencies 2, two clocks for CAS latencies 3 and three clocks for CAS latencies 4. If CA10 is high when a Write Command is issued, the **Write**

**with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to $t_{WR}$ (Write recovery time) after the last data in.

### *Precharge Command*

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3. Writes require a time delay twr from the last data out to apply the precharge command.

Bank Selection by Address Bits:

| A10 | BA0 | BA1 | |
|---|---|---|---|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| 0 | 1 | 0 | Bank 2 |
| 0 | 1 | 1 | Bank 3 |
| 1 | X | X | all Banks |

### *Burst Termination*

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory.

### *Deep Power Down Mode*

TheDeep Power Down mode is an unique functi on with very low standby currents. All internal volat ge generators inside the RAM are stopped and all memory data is lost in this mode. To enter the Deep Power Down mode all banks must be precharged.

### *Recommended Operation and Characteristics*

$T_A$ = 0 to 70 °C(Commercial)/-40 to 85 °C(Industrial); $V_{SS}$ = 0 V; $V_{CC}$= 2.5 V,$V_{CCQ}$ = 1.8V

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply voltage | $V_{CC}$ | 2.3 | 2.9 | V | |
| I/O Supply Voltage | $V_{CCQ}$ | 1.65 | 2.9 | V | 1, 2 |
| Input high voltage | $V_{IH}$ | 0.8x$V_{CCQ}$ | Vcc+0.3 | V | 1, 2 |
| Input low voltage | $V_{IL}$ | – 0.3 | 0.3 | V | 1, 2 |
| Output high voltage ($I_{OUT}$ = – 4.0 mA) | $V_{OH}$ | $V_{CCQ}$-0.2 | – | V | |
| Output low voltage ($I_{OUT}$ = 4.0 mA) | $V_{OL}$ | – | 0.4 | V | |
| Input leakage current, any input (0 V < $V_{IN}$ < 3.6 V, all other inputs = 0 V) | $I_{I(L)}$ | – 5 | 5 | µA | |
| Output leakage current (DQ is disabled, 0 V < $V_{OUT}$ < $V_{CC}$) | $I_{O(L)}$ | – 5 | 5 | µA | |

**Note:**
1. All voltages are referenced to $V_{SS}$.
2. $V_{IH}$ may overshoot to $V_{CC}$ + 0.8 V for pulse width of < 4ns with 2.5V. $V_{IL}$ may undershoot to -0.8 V for pulse width < 4.0 ns with 2.5V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

### *Absolute Maximum Ratings**

Operating temperature range (commercial)0 to 70 °C
Operating temperature range (industrial) -40 to 85 °C
Storage temperature range ..... -55 to 150 °C
Input/output voltage ..... -0.3 to ($V_{CC}$+0.3) V
Power supply voltage ..... -0.3 to 3.6 V
Power dissipation ..... 0.7 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### *Operating Currents* $T_A$ = 0 to 70 °C(Commercial)/-40 to 85 °C(Industrial);

$V_{SS}$ = 0 V; $V_{CC}$= 2.5 V,$V_{CCQ}$ = 1.8V(Recommended Operating Conditions unless otherwise noted)

| Symbol | Parameter & Test Condition | | Max. -7 | Max. -8PC | Max. 10 | Unit | Note |
|---|---|---|---|---|---|---|---|
| ICC1 | Operating Current<br>$t_{RC}$ = $t_{RCMIN.}$, $t_{RC}$ = $t_{CKMIN}$.<br>Active-precharge command cycling, without Burst Operation | 1 bank operation | 110 | 100 | 90 | mA | 7 |
| ICC2P | Precharge Standby Current in Power Down Mode<br>$\overline{CS}$ =$V_{IH}$, CKE≤ $V_{IL(max)}$ | $t_{CK}$ = min. | 0.5 | 0.5 | 0.5 | mA | 7 |
| ICC2PS | | $t_{CK}$ = Infinity | 0.5 | 0.5 | 0.5 | mA | 7 |
| ICC2N | Precharge Standby Current in Non-Power Down Mode<br>$\overline{CS}$ =$V_{IH}$, CKE≥ $V_{IL(max)}$ | $t_{CK}$ = min. | 20 | 20 | 20 | mA | |
| ICC2NS | | $t_{CK}$ = Infinity | 5 | 5 | 5 | mA | |
| ICC3N | No Operating Current<br>$t_{CK}$ = min, $\overline{CS}$ = $V_{IH(min)}$<br>bank ; active state ( 4 banks) | CKE ≥ $V_{IH(MIN.)}$ | 25 | 25 | 25 | mA | |
| ICC3P | | CKE ≤ $V_{IL(MAX.)}$<br>(Power down mode) | 5 | 5 | 5 | mA | |
| ICC4 | Burst Operating Current<br>$t_{CK}$ = min<br>Read/Write command cycling | | 110 | 90 | 70 | mA | 7,8 |
| ICC5 | Auto Refresh Current<br>$t_{CK}$ = min<br>Auto Refresh command cycling | | 165 | 155 | 150 | mA | 7 |
| ICC7 | Deep Power down Current | | 10 | 10 | 10 | uA | |

**Notes:**

7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of $t_{CK}$ and $t_{RC}$. Input signals are changed one time during $t_{CK}$.
8. These parameter depend on output loading. Specified values are obtained with output open.

### *Temperature Compensated/Partial Array Self-Refresh Currents*

| Parameter & Test Condition | Extended Mode Register M[4:3] Tcase[$^{O}$C] | Symb. | Max. | Unit |
|---|---|---|---|---|
| Self Refresh Current<br>Self refresh Mode<br>CKE=0.2V, tck=infinity,<br>full array activations, all banks | 85$^{O}$C max | ICC6 | 900 | uA |
| | 70$^{O}$C max | | 600 | uA |
| | 45$^{O}$C max | | 500 | uA |
| | 15$^{O}$C max | | 400 | uA |
| Self Refresh Current<br>Self refresh Mode<br>CKE=0.2V, tck=infinity,<br>1/2 array activations, Bank 0+1 | 85$^{O}$C max | ICC6 | 600 | uA |
| | 70$^{O}$Cmax | | 500 | uA |
| | 45$^{O}$C max | | 400 | uA |
| | 15$^{O}$Cmax | | 350 | uA |
| Self Refresh Current<br>Self refresh Mode<br>CKE=0.2V, tck=infinity,<br>1/4 array activations, Bank 0 | 85$^{O}$C max | ICC6 | 450 | uA |
| | 70$^{O}$C max | | 420 | uA |
| | 45$^{O}$C max | | 350 | uA |
| | 15$^{O}$C max | | 300 | uA |
| Self Refresh Current<br>Self refresh Mode<br>CKE=0.2V, tck=infinity,<br>1/8 array activations, Bank 0 | 85$^{O}$C max | ICC6 | 400 | uA |
| | 70$^{O}$C max | | 350 | uA |
| | 45$^{O}$C max | | 310 | uA |
| | 15$^{O}$C max | | 290 | uA |
| Self Refresh Current<br>Self refresh Mode<br>CKE=0.2V, tck=infinity,<br>1/16 array activations, Bank 0 | 85$^{O}$C max | ICC6 | 350 | uA |
| | 70$^{O}$C max | | 320 | uA |
| | 45$^{O}$C max | | 295 | uA |
| | 15$^{O}$C max | | 280 | uA |

## *AC Characteristics* [1,2,3]

$T_A$ = 0 to 70 °C(Commercial)/-40 to 85 °C(Industrial);$V_{SS}$ = 0 V; $V_{CC}$= 2.5 V,$V_{CCQ}$ = 1.8V, $t_T$=1 ns

| # | Symbol | Parameter | Limit Values | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -8PC | | -10 | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| **Clock and Clock Enable** | | | | | | | | | | |
| 1 | $t_{CK}$ | Clock Cycle Time | | | | | | | | |
| | | $\overline{CAS}$ Latency = 3 | 7 | – | 8 | – | 10 | – | ns | |
| | | $\overline{CAS}$ Latency = 2 | 10 | – | 10 | – | 12 | – | ns | |
| | | $\overline{CAS}$ Latency = 1 | 20 | – | 20 | – | 25 | – | ns | |
| 2 | $t_{CK}$ | Clock Frequency | | | | | | | | |
| | | $\overline{CAS}$ Latency = 3 | – | 143 | – | 125 | – | 100 | MHz | |
| | | $\overline{CAS}$ Latency = 2 | – | 100 | – | 100 | – | 83 | MHz | |
| | | $\overline{CAS}$ Latency = 1 | – | 50 | – | 50 | – | 40 | MHz | |
| 3 | $t_{AC}$ | Access Time from Clock | | | | | | | | 2, 4 |
| | | $\overline{CAS}$ Latency = 3 | – | 5.4 | – | 6 | – | 7 | ns | |
| | | $\overline{CAS}$ Latency = 2 | _ | 6 | _ | 6 | _ | 8 | ns | |
| | | $\overline{CAS}$ Latency = 1 | _ | 19 | _ | 19 | _ | 22 | ns | |
| 4 | $t_{CH}$ | Clock High Pulse Width | 2.5 | – | 3 | – | 3 | – | ns | |
| 5 | $t_{CL}$ | Clock Low Pulse Width | 2.5 | – | 3 | – | 3 | – | ns | |
| 6 | $t_T$ | Transition Tim | 0.3 | 1.2 | 0.5 | 10 | 0.5 | 10 | ns | |
| **Setup and Hold Times** | | | | | | | | | | |
| 7 | $t_{IS}$ | Input Setup Time | 1.5 | – | 2 | – | 2.5 | – | ns | 5 |
| 8 | $t_{IH}$ | Input Hold Time | 0.8 | – | 1 | – | 1 | – | ns | 5 |
| 9 | $t_{CKS}$ | Input Setup Time | 1.5 | – | 2 | – | 2.5 | – | ns | 5 |
| 10 | $t_{CKH}$ | CKE Hold Time | 0.8 | – | 1 | – | 1 | – | ns | 5 |
| 11 | $t_{RSC}$ | Mode Register Set-up Time | 14 | – | 16 | – | 20 | – | ns | |
| 12 | $t_{SB}$ | Power Down Mode Entry Time | 0 | 7 | 0 | 8 | 0 | 8 | ns | |
| **Common Parameters** | | | | | | | | | | |
| 13 | $t_{RCD}$ | Row to Column Delay Time | 15 | – | 20 | – | 20 | – | ns | 6 |
| 14 | $t_{RP}$ | Row Precharge Time | 15 | – | 20 | – | 20 | – | ns | 6 |
| 15 | $t_{RAS}$ | Row Active Time | 42 | 100K | 45 | 100k | 50 | 100k | ns | 6 |
| 16 | $t_{RC}$ | Row Cycle Time | 60 | – | 60 | – | 70 | – | ns | 6 |
| 17 | $t_{RRD}$ | Activate(a) to Activate(b) Command Period | 14 | – | 16 | – | 20 | – | ns | 6 |
| 18 | $t_{CCD}$ | $\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period | 1 | – | 1 | – | 1 | – | CLK | |

## *AC Characteristics* (Cont'd)

| # | Symbol | Parameter | Limit Values | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -8PC | | -10 | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| **Refresh Cycle** | | | | | | | | | | |
| 19 | $t_{REF}$ | Refresh Period (8192 cycles) | — | 64 | — | 64 | — | 64 | ms | |
| 20 | $t_{SREX}$ | Self Refresh Exit Time | 1 | — | 1 | — | 1 | — | CLK | |
| **Read Cycle** | | | | | | | | | | |
| 21 | $t_{OH}$ | Data Out Hold Time | 3 | – | 3 | – | 3 | – | ns | 2 |
| 22 | $t_{LZ}$ | Data Out to Low Impedance Time | 1 | – | 1 | – | 1 | – | ns | |
| 23 | $t_{HZ}$ | Data Out to High Impedance Time | 3 | 7 | 3 | 7 | 3 | 7 | ns | 7 |
| 24 | $t_{DQZ}$ | DQM Data Out Disable Latency | – | 2 | – | 2 | – | 2 | CLK | |
| **Write Cycle** | | | | | | | | | | |
| 25 | $t_{WR}$ | Write Recovery Time | 1 | – | 1 | – | 1 | – | CLK | |
| 26 | $t_{DQW}$ | DQM Write Mask Latency | 0 | – | 0 | – | 0 | – | CLK | |

## *Notes for AC Parameters:*

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests are referenced to the 0.9V crossover point for VCCQ=1.8V components. The transition time is measured between $V_{IH}$ and $V_{IL}$. All AC measurements assume $t_T$ = 1ns with the AC output load circuit shown in

Figure 1.

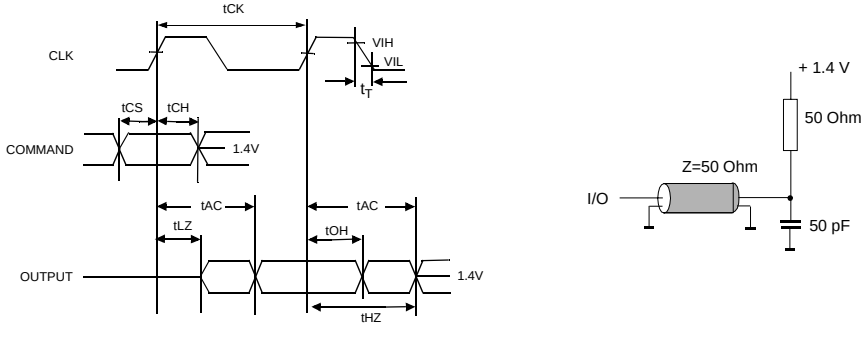



**Figure 1.**

4. If clock rising time is longer than 1 ns, a time ($t_T$/2 – 0.5) ns has to be added to this parameter.
5. If $t_T$ is longer than 1 ns, a time ($t_T$ – 1) ns has to be added to this parameter.
6. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

   *the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*

   Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

### *Timing Diagrams*

1. Bank Activate Command Cycle

2. Burst Read Operation

3. Read Interrupted by a Read

4. Read to Write Interval

    4.1 Read to Write Interval

    4.2 Minimum Read to Write Interval

    4.3 Non-Minimum Read to Write Interval

5. Burst Write Operation

6. Write and Read Interrupt

    6.1 Write Interrupted by a Write

    6.2 Write Interrupted by Read

7. Burst Write & Read with Auto-Precharge

    7.1 Burst Write with Auto-Precharge

    7.2 Burst Read with Auto-Precharge

8. Burst Termination

    8.1 Termination of a Burst Write Operation

    8.2 Termination of a Burst Write Operation

9. AC- Parameters

    9.1 AC Parameters for a Write Timing

    9.2 AC Parameters for a Read Timing

10. Mode Register Set

11. Power on Sequence and Auto Refresh (CBR)

12. Power Down Mode

13. Self Refresh (Entry and Exit)

14. Auto Refresh (CBR)

***Timing Diagrams*** (Cont'd)

15. Random Column Read ( Page within same Bank)

    15.1 $\overline{\text{CAS}}$ Latency = 2

    15.2 $\overline{\text{CAS}}$ Latency = 3

16. Random Column Write ( Page within same Bank)

    16.1 $\overline{\text{CAS}}$ Latency = 2

    16.2 $\overline{\text{CAS}}$ Latency = 3

17. Random Row Read ( Interleaving Banks) with Precharge

    17.1 $\overline{\text{CAS}}$ Latency = 2

    17.2 $\overline{\text{CAS}}$ Latency = 3

18. Random Row Write ( Interleaving Banks) with Precharge

    18.1 $\overline{\text{CAS}}$ Latency = 2

    18.2 $\overline{\text{CAS}}$ Latency = 3

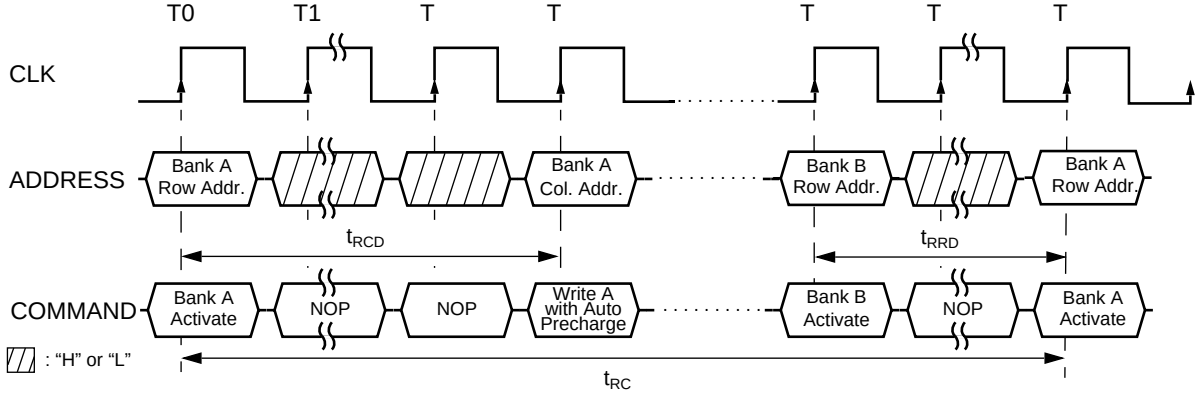
19. Precharge Termination of a Burst

    19.1 $\overline{\text{CAS}}$ Latency = 2

    19.2 $\overline{\text{CAS}}$ Latency = 3

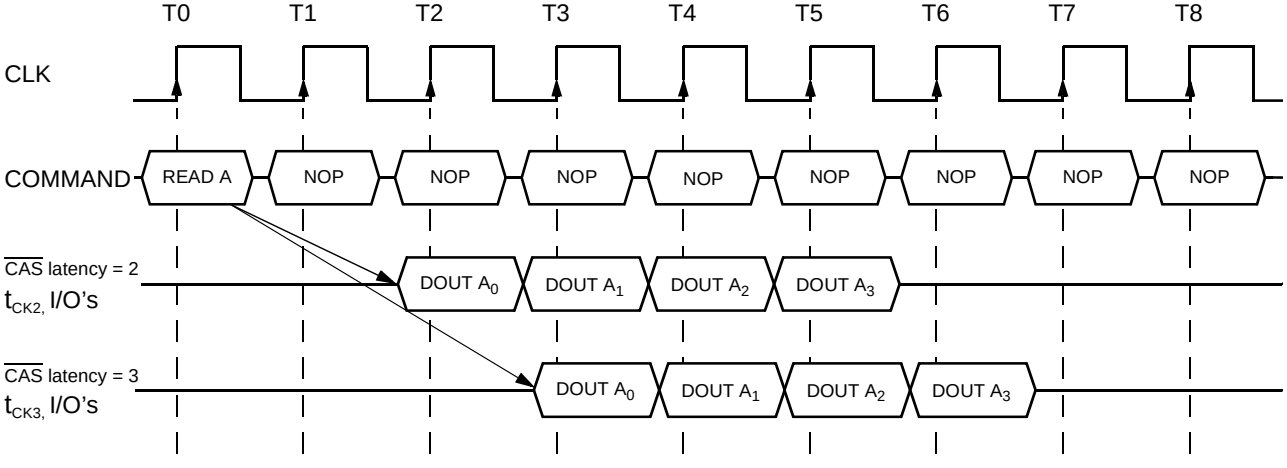
### *1. Bank Activate Command Cycle*

### *($\overline{CAS}$ latency = 3)*



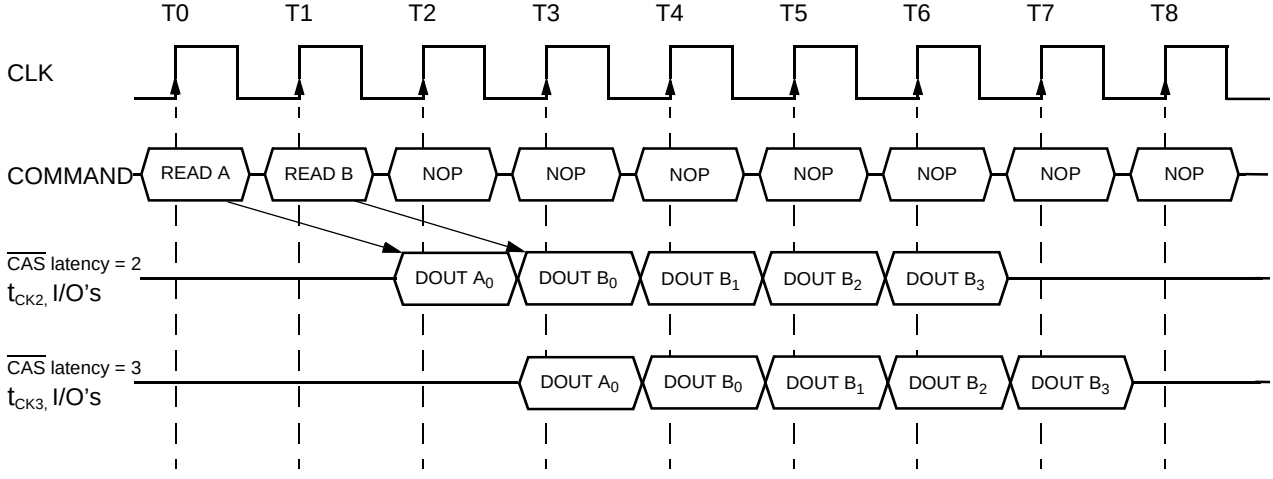

### *2. Burst Read Operation*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



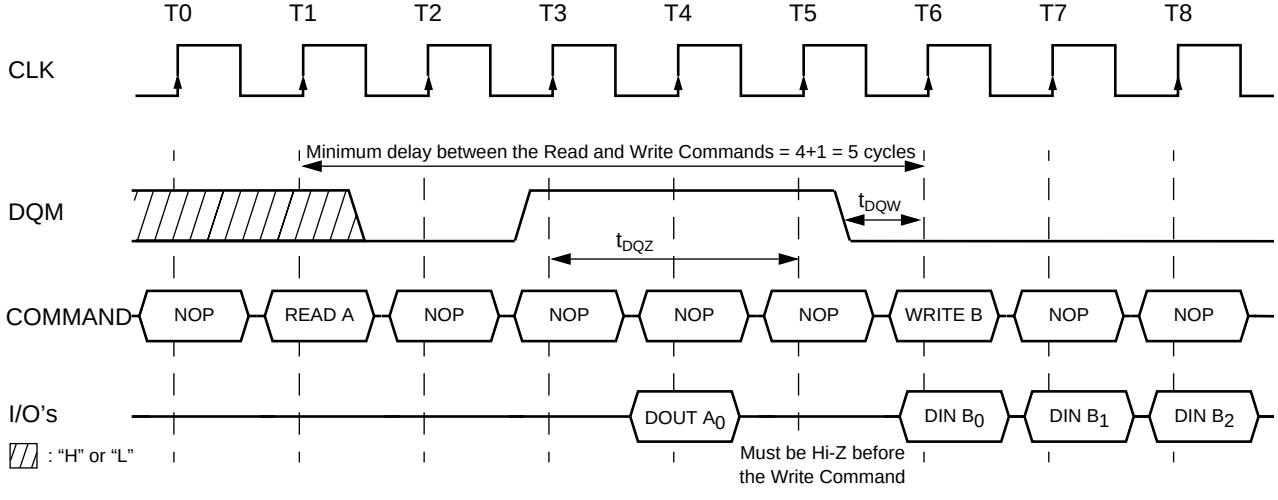
### *3. Read Interrupted by a Read*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



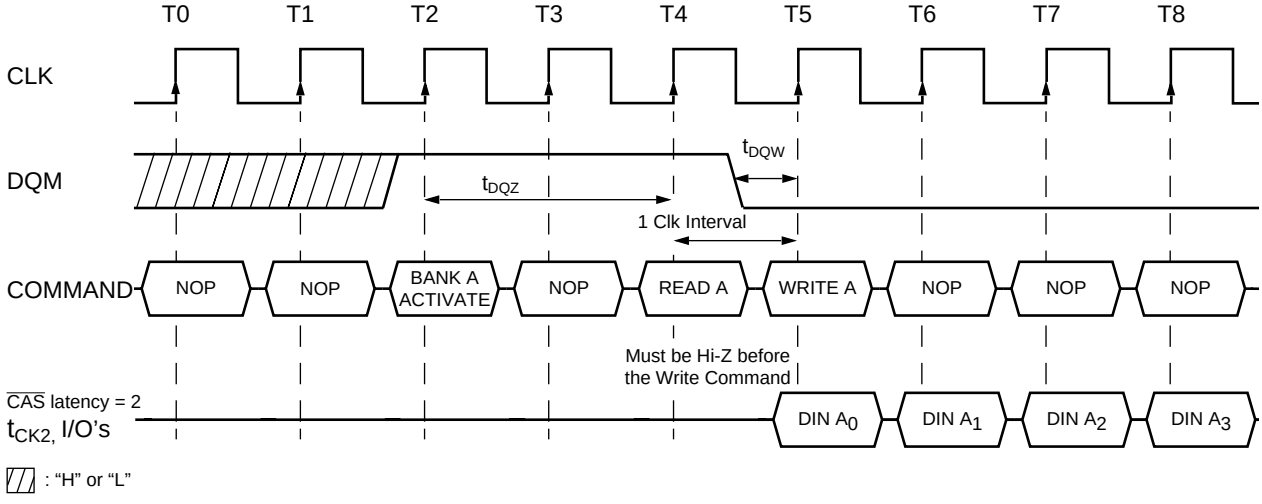

### *4.1 Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 3)*



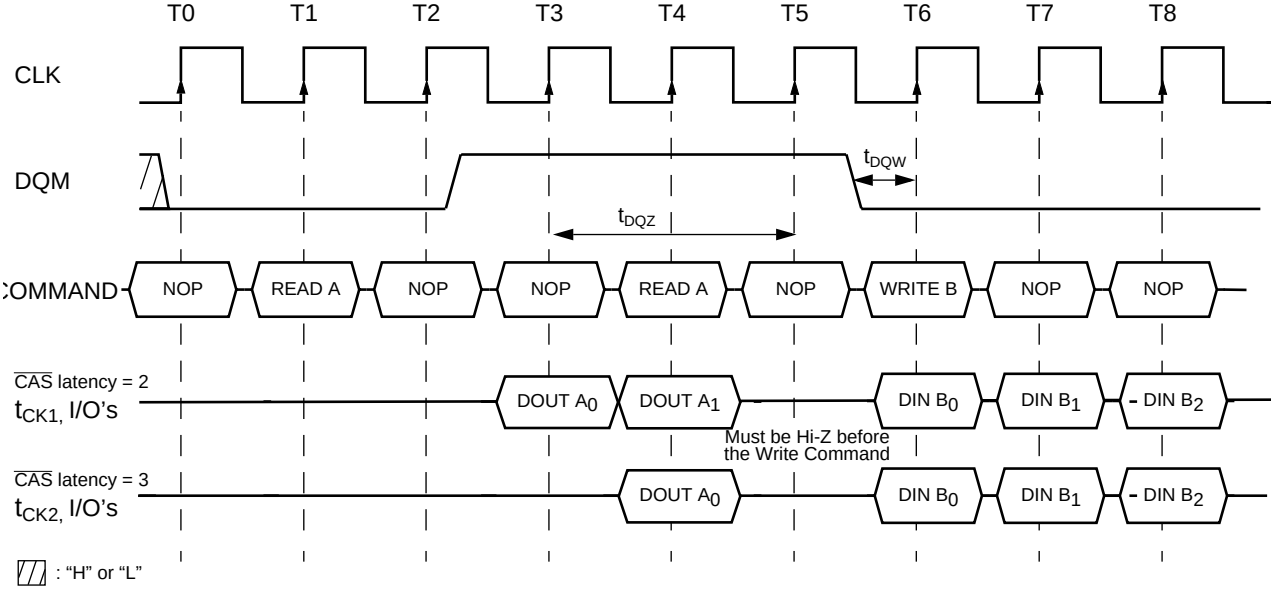
### *4.2 Minimum Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2)*



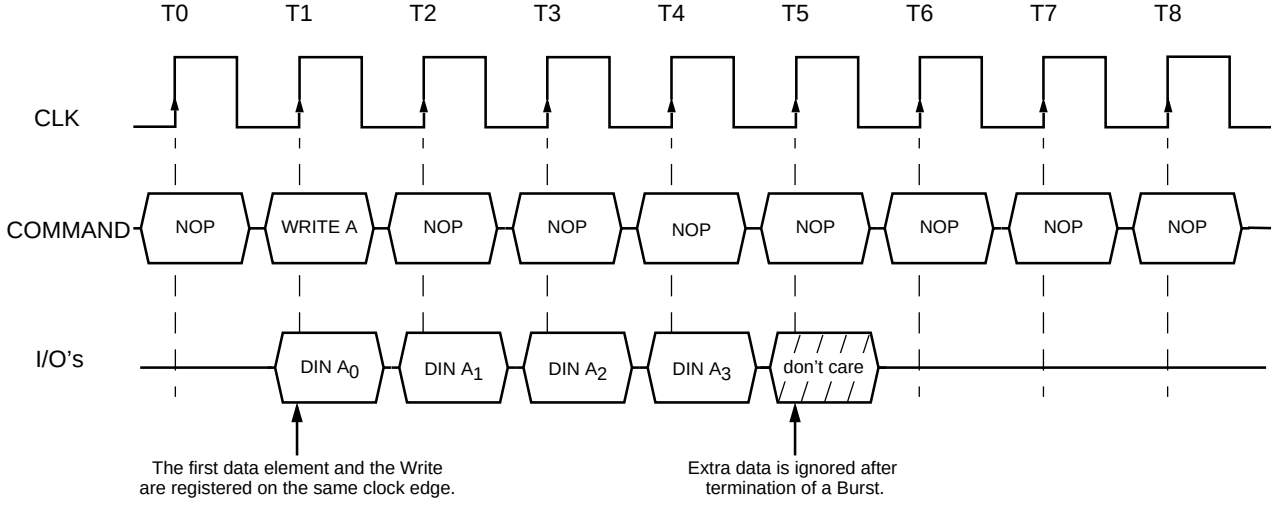

### *4.3 Non-Minimum Read to Write Interval*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



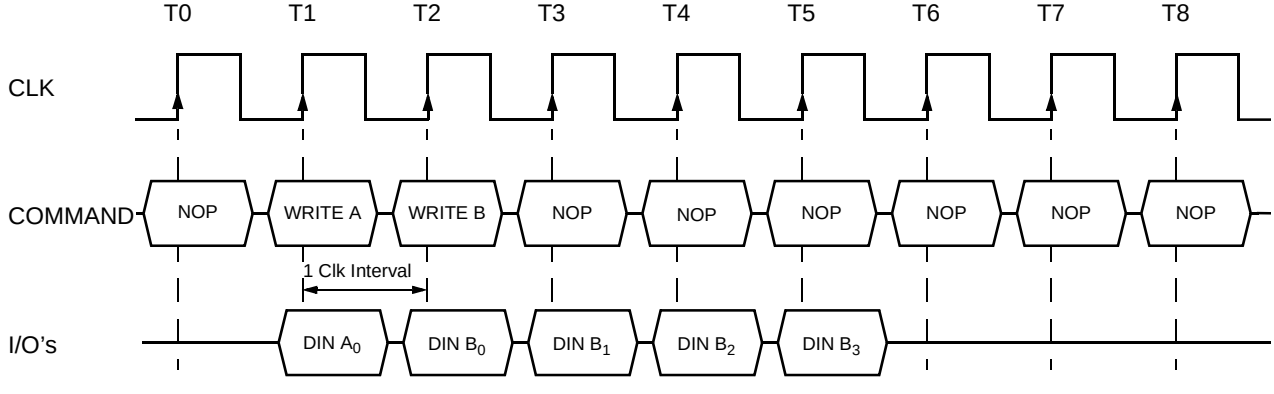
### *5. Burst Write Operation*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



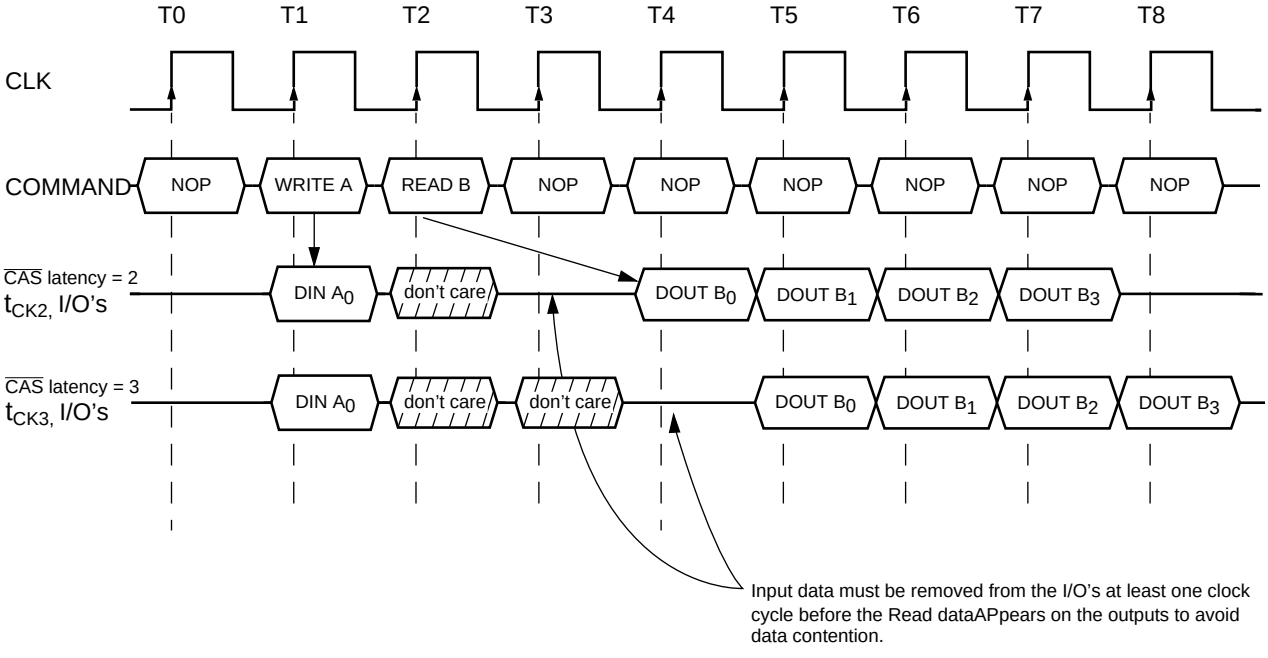

### *6.1 Write Interrupted by a Write*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



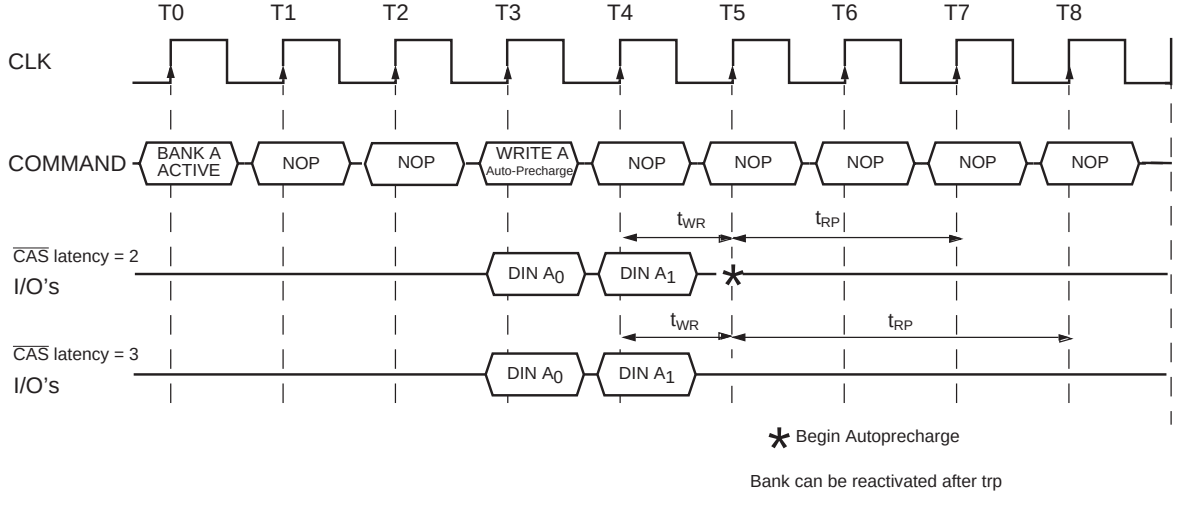
### *6.2 Write Interrupted by a Read*

### *(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)*



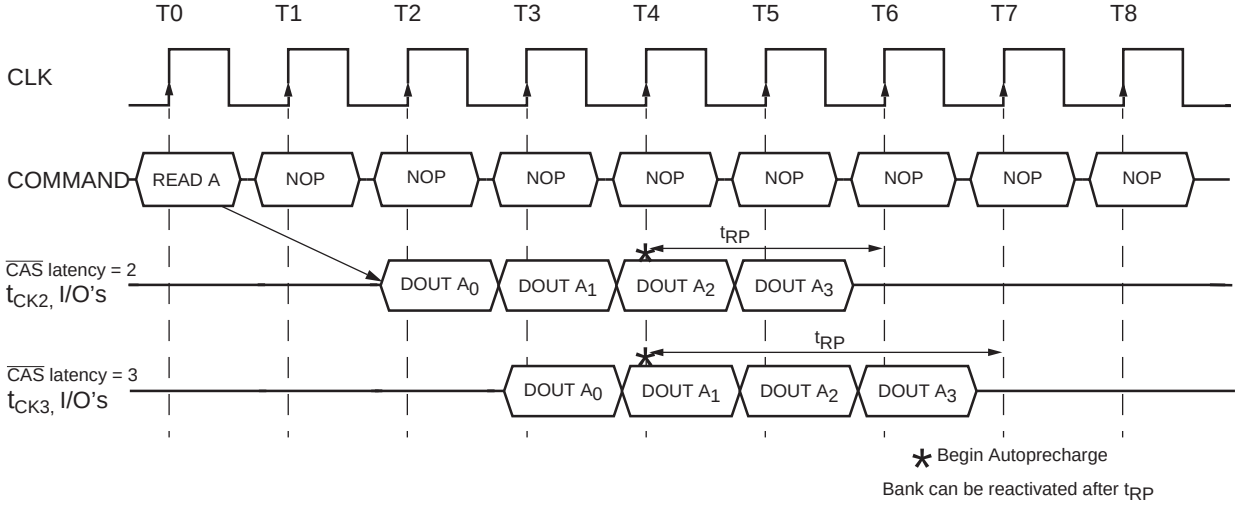

### *7. Burst Write with Auto-Precharge*

### *Burst Length = 2, $\overline{CAS}$ latency = 2, 3)*



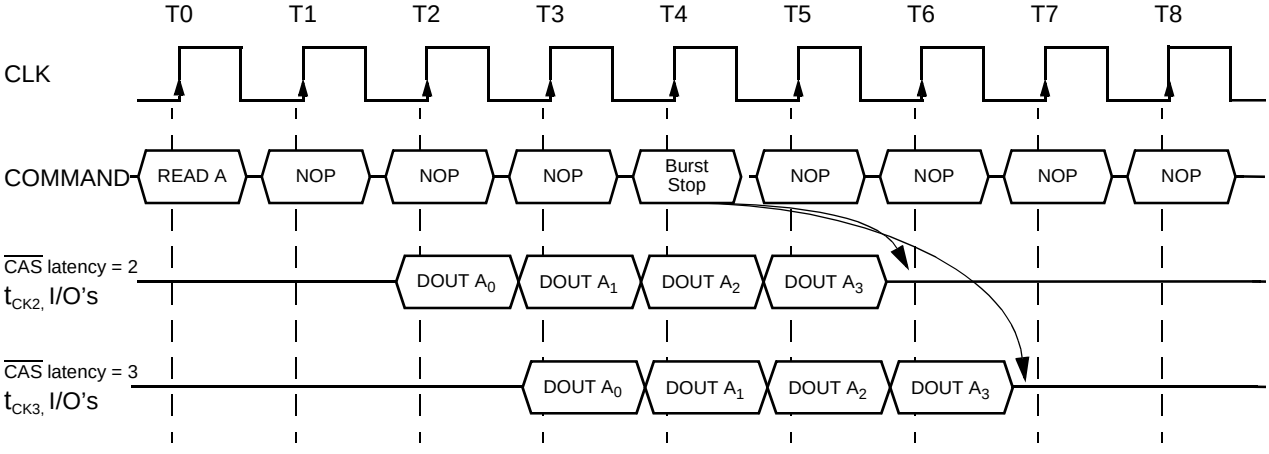
### *7.2 Burst Read with Auto-Precharge*

### *Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)*



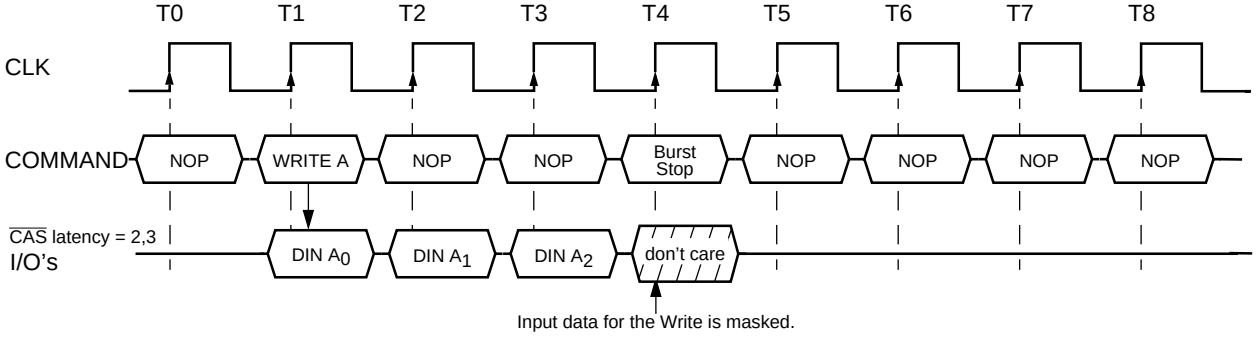
### 8.1 Termination of a Burst Read Operation

### (CAS latency = 2, 3)

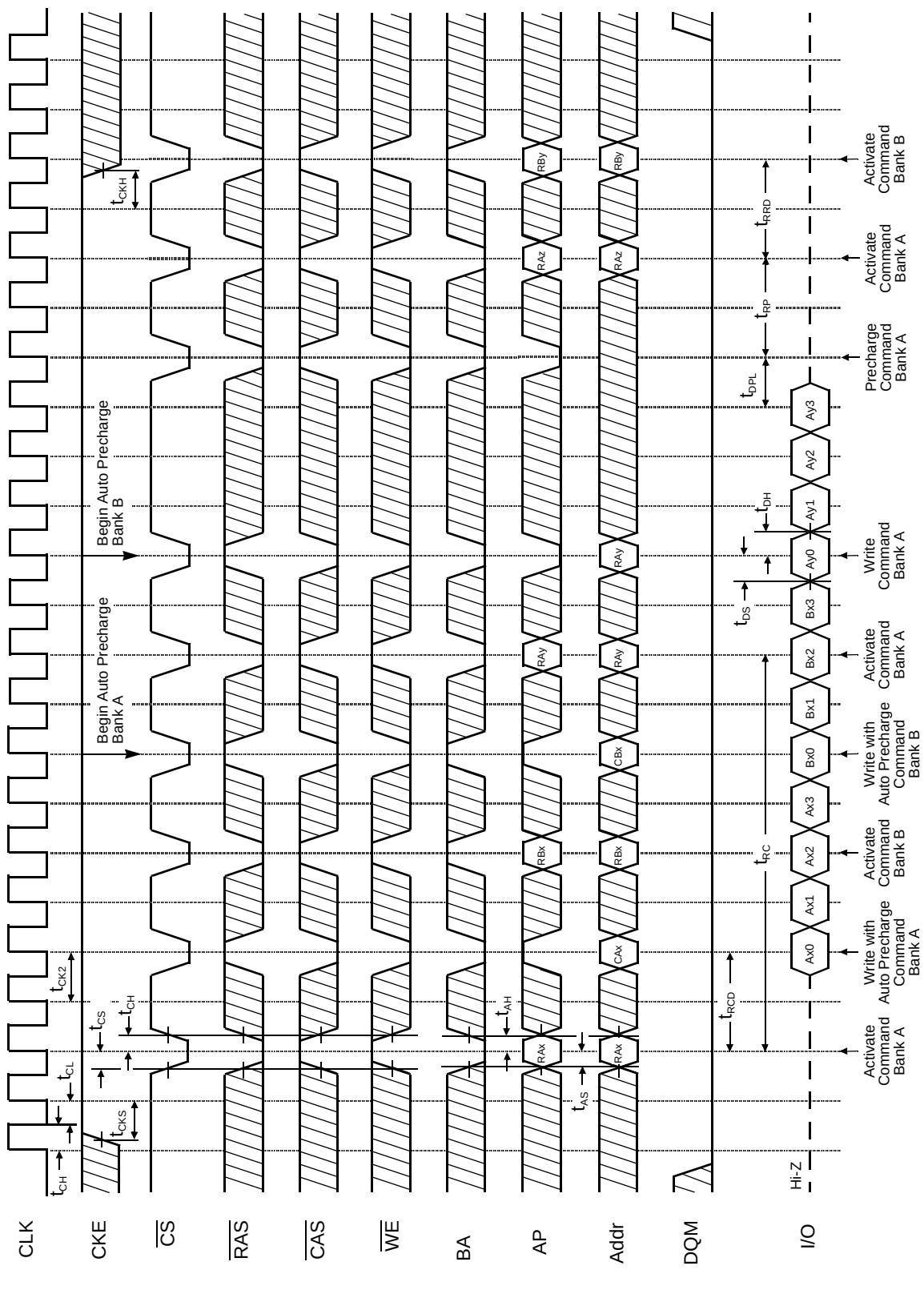



### 8.2 Termination of a Burst Write Operation

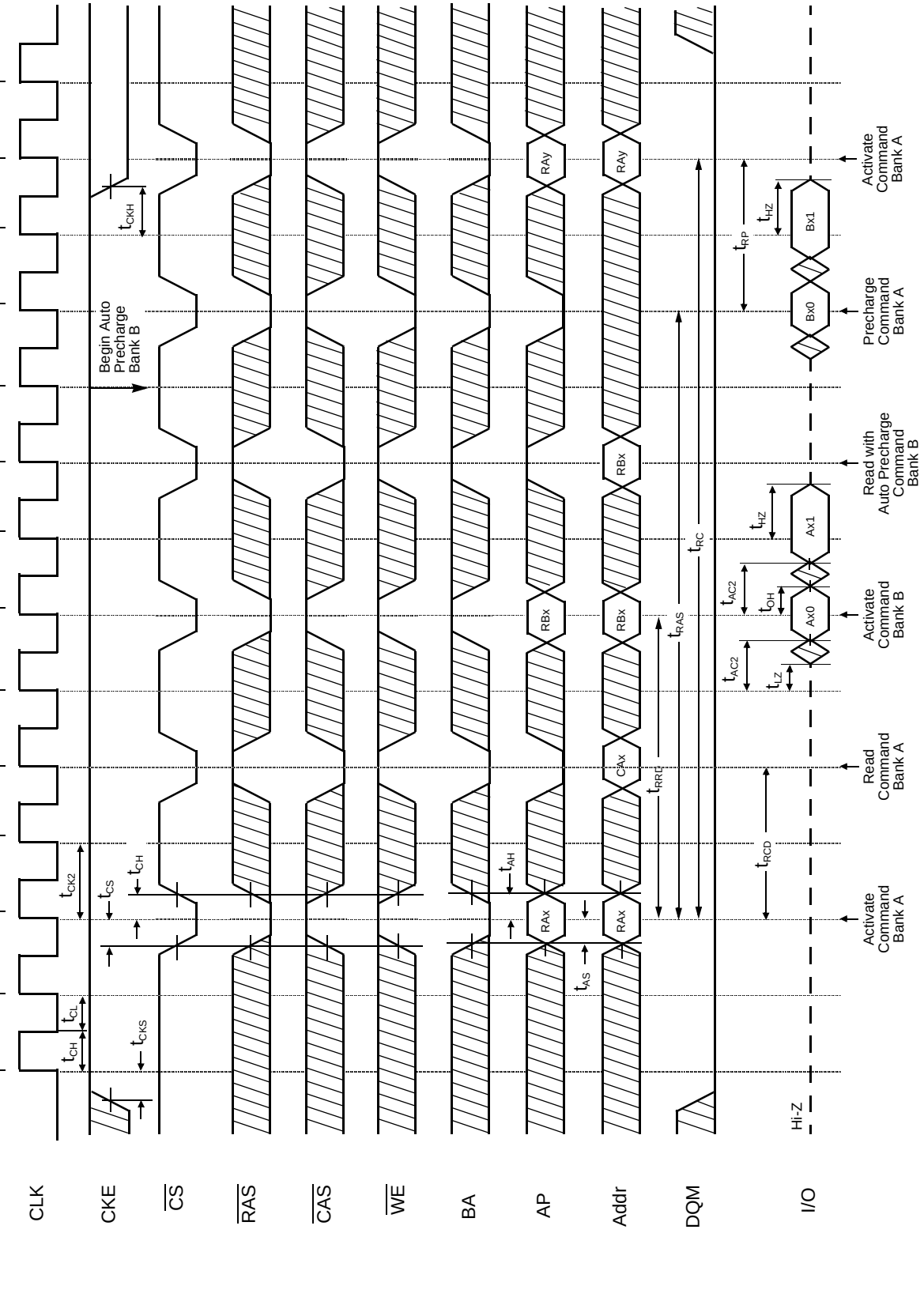
### (CAS latency = 2, 3)



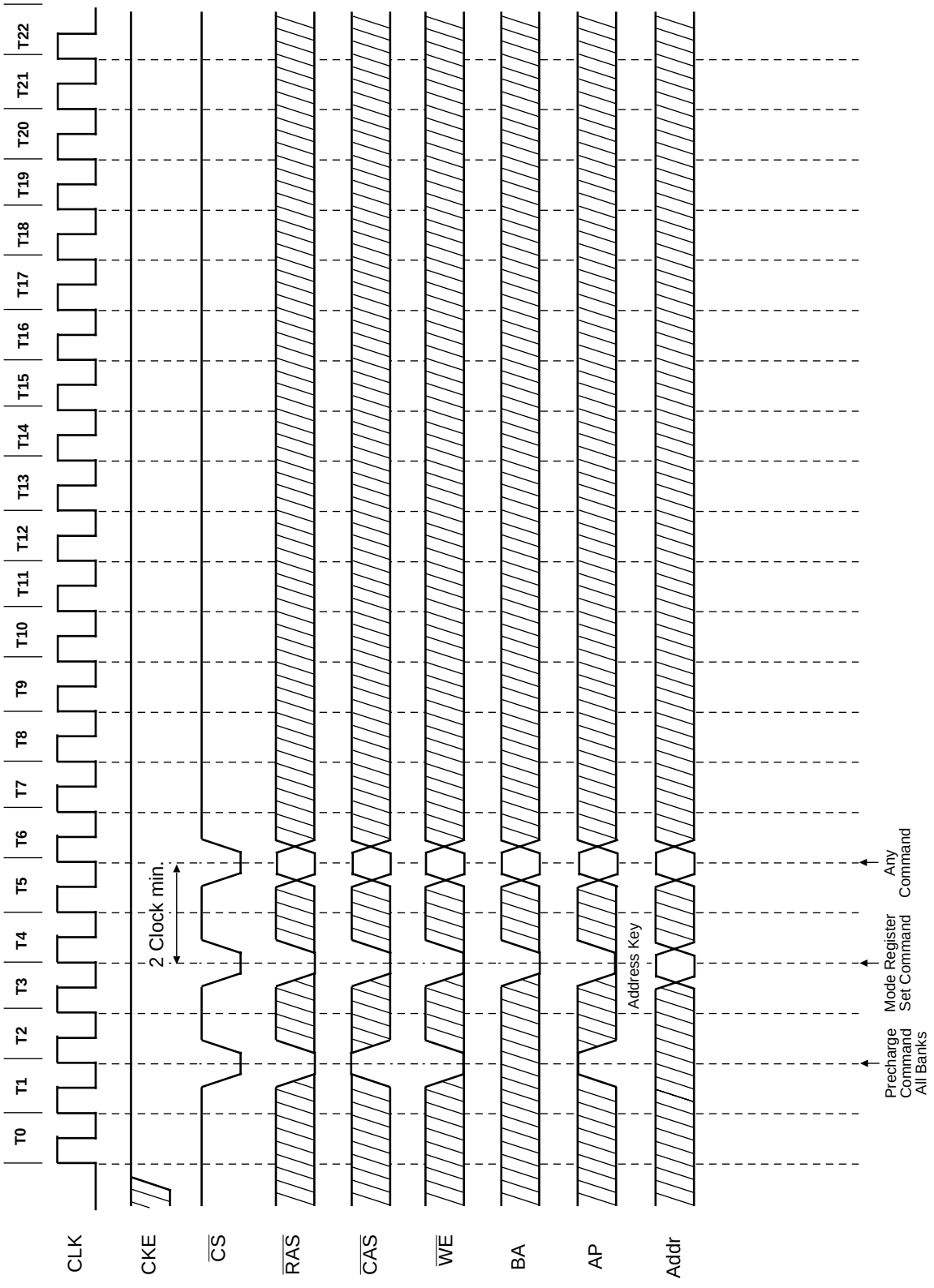
## 9.1 AC Parameters for Write Timing



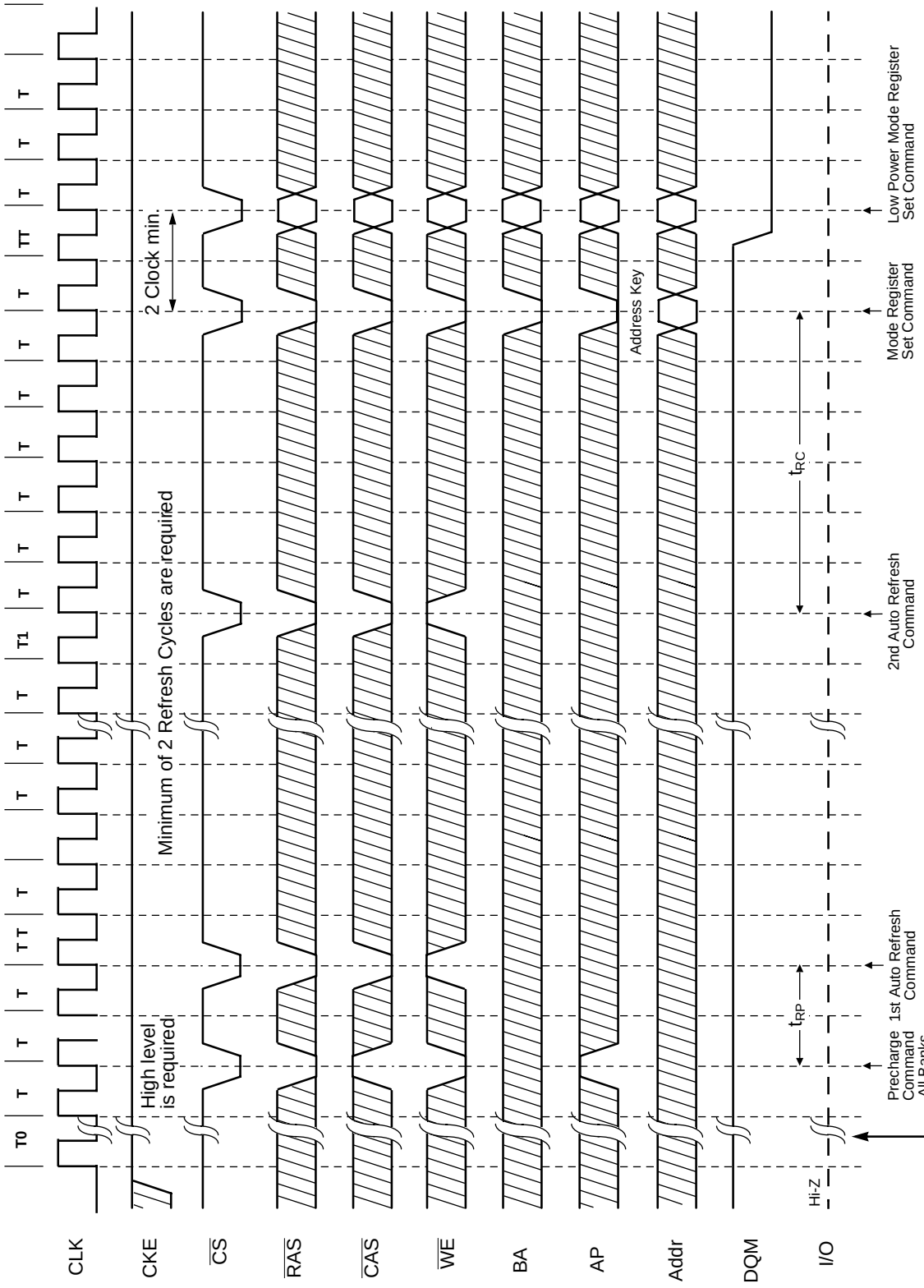
## 9.2 AC Parameters for Read Timing



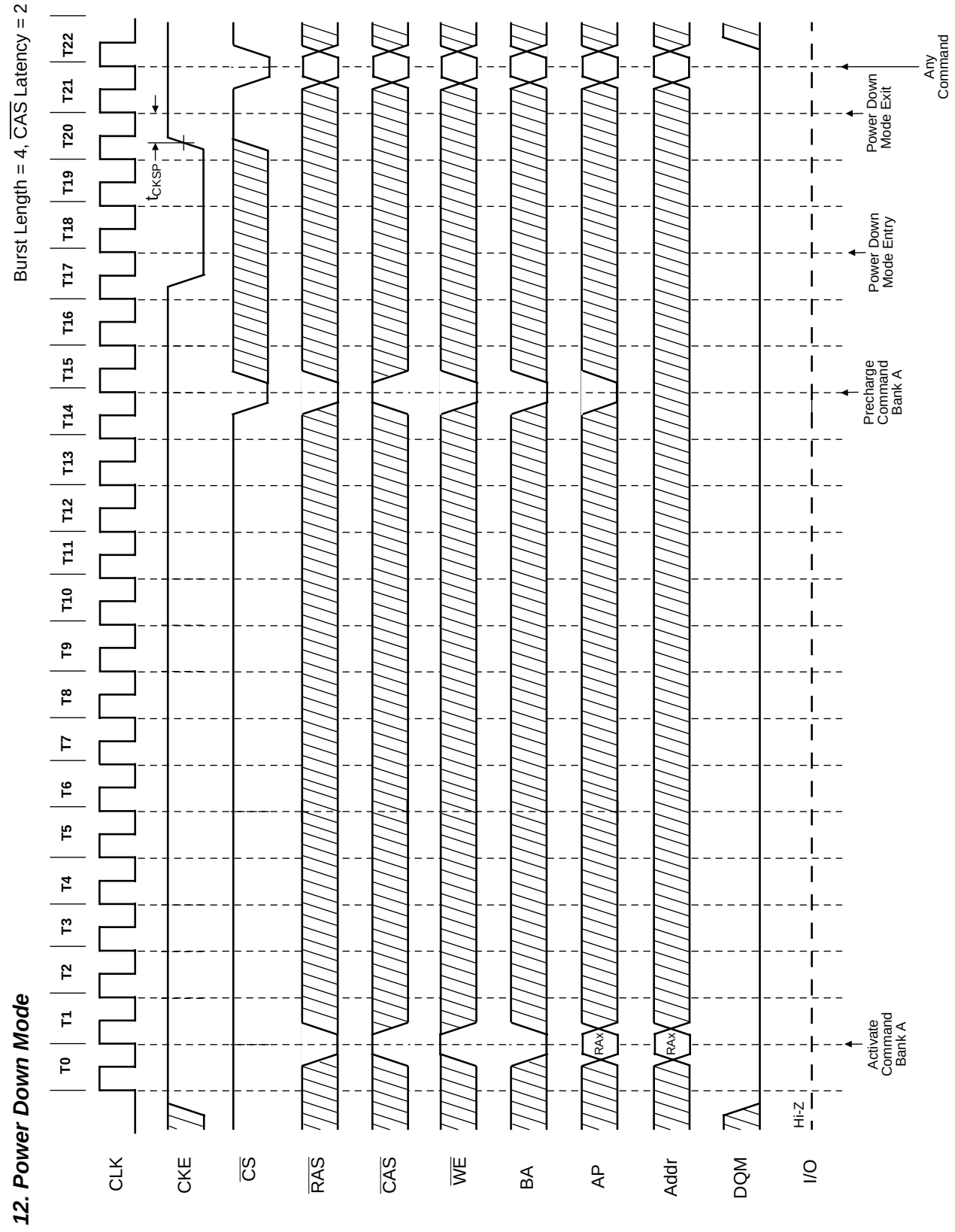
### 10. Mode Register Set



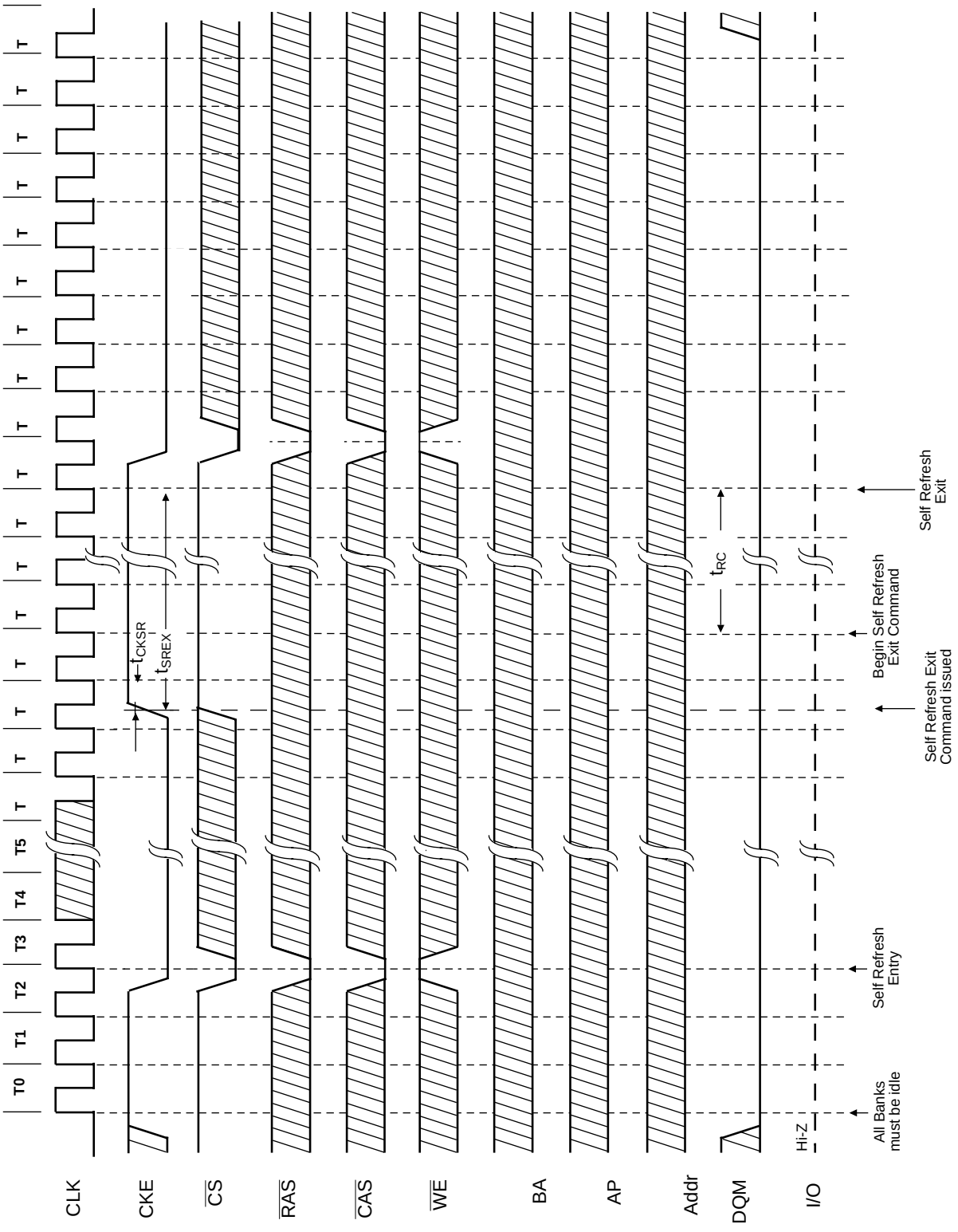
***11. Power on Sequence and Auto Refresh (CBR)***



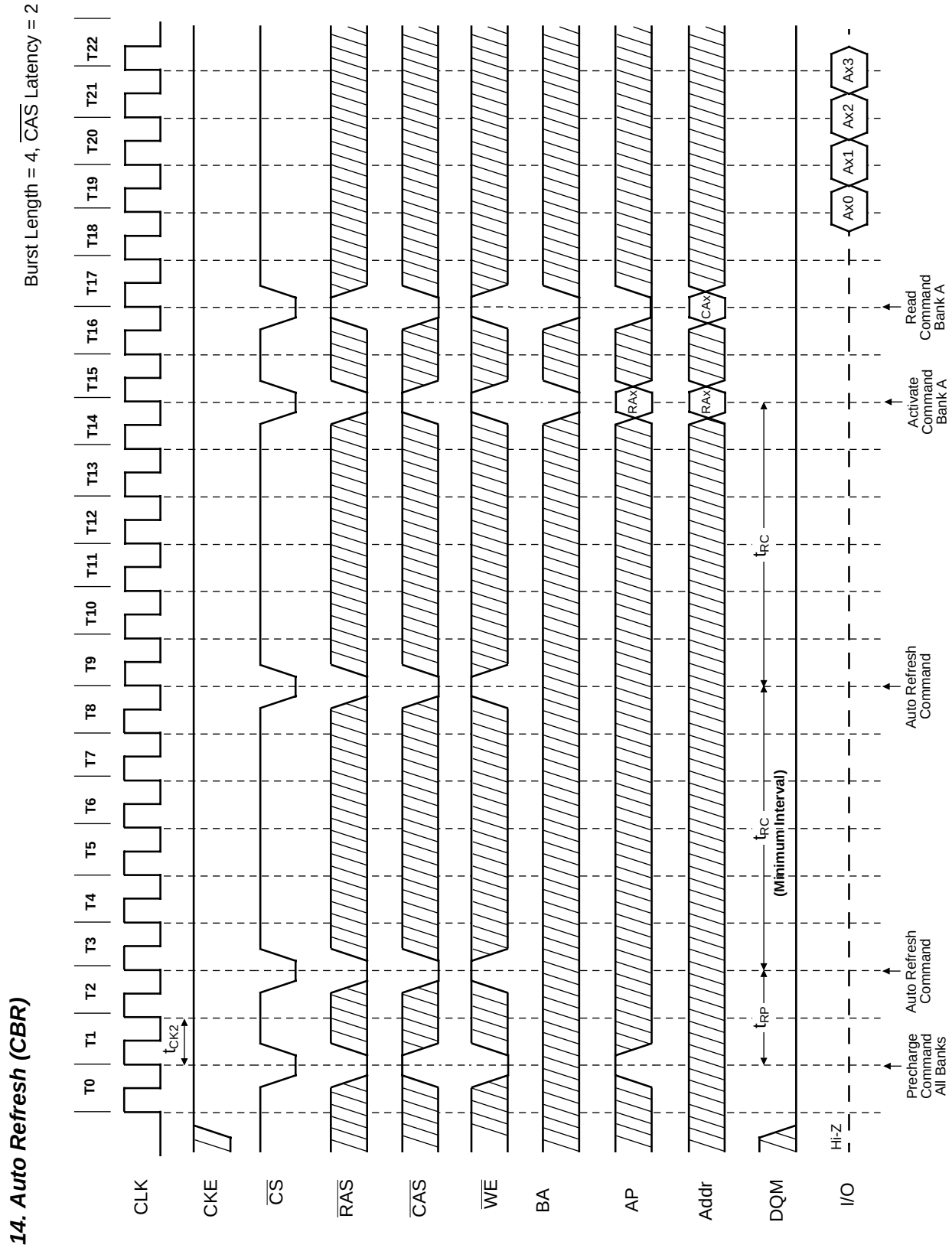
## 12. Power Down Mode



### 13. Self Refresh (Entry and Exit)

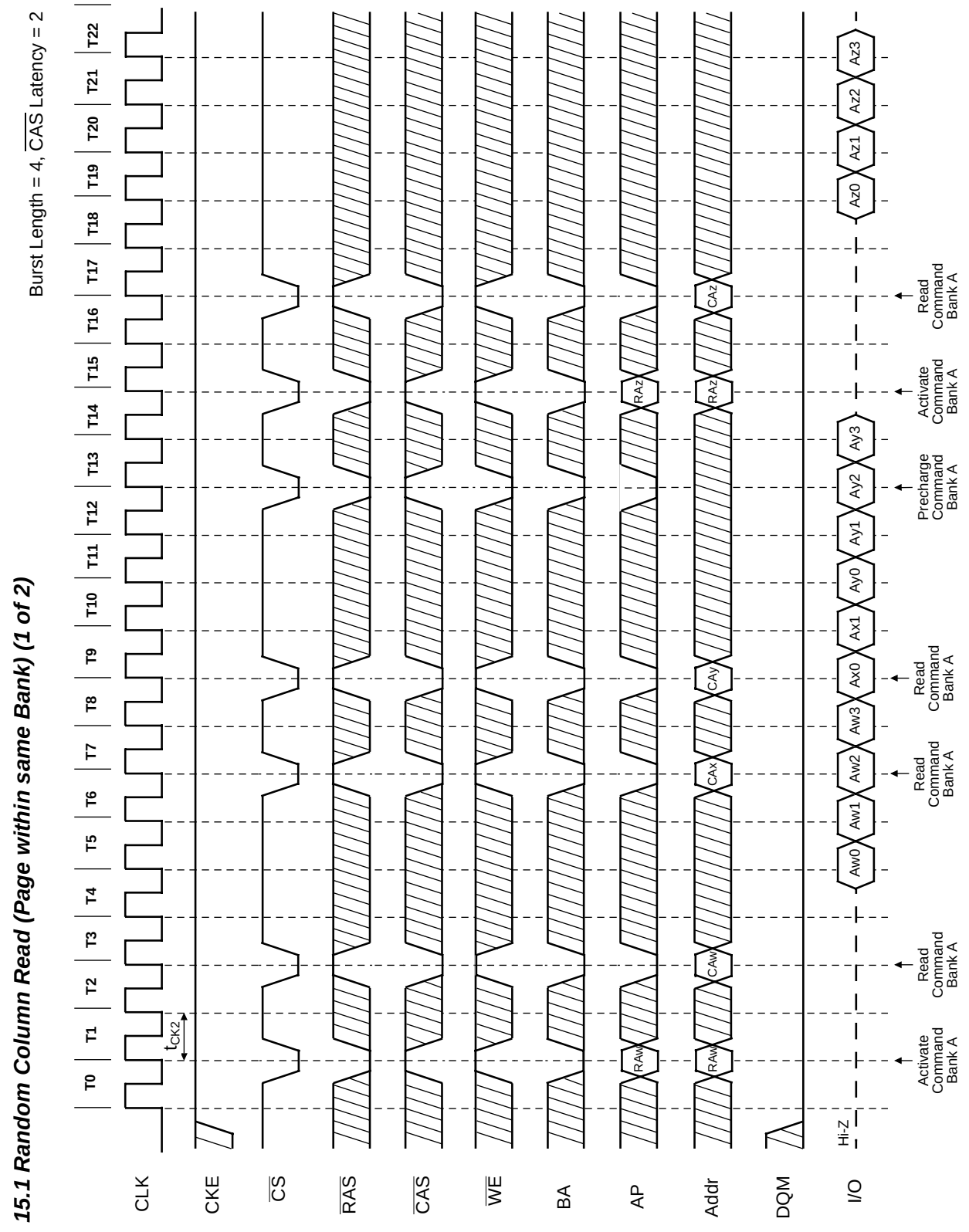


## 14. Auto Refresh (CBR)

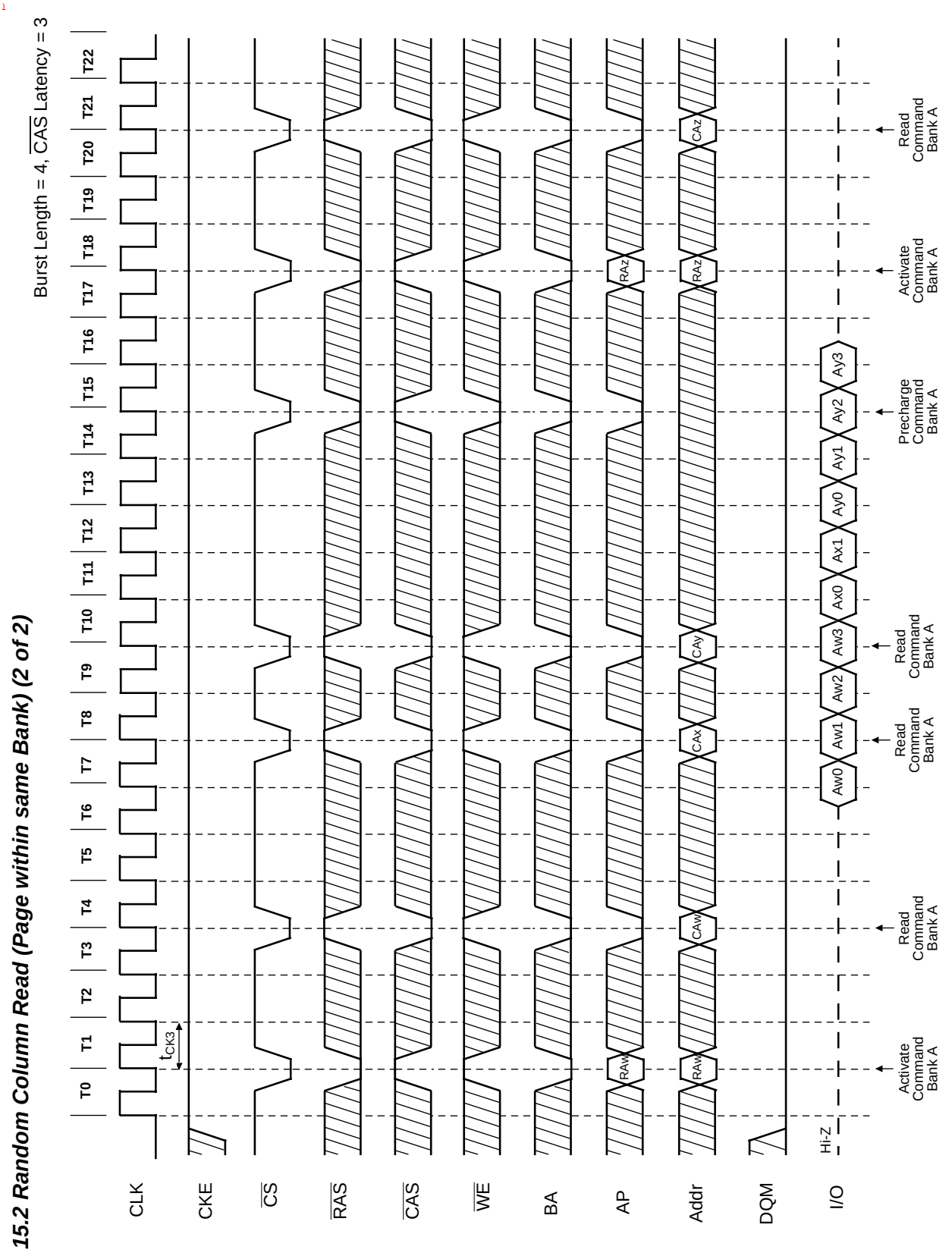


## 15.1 Random Column Read (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2

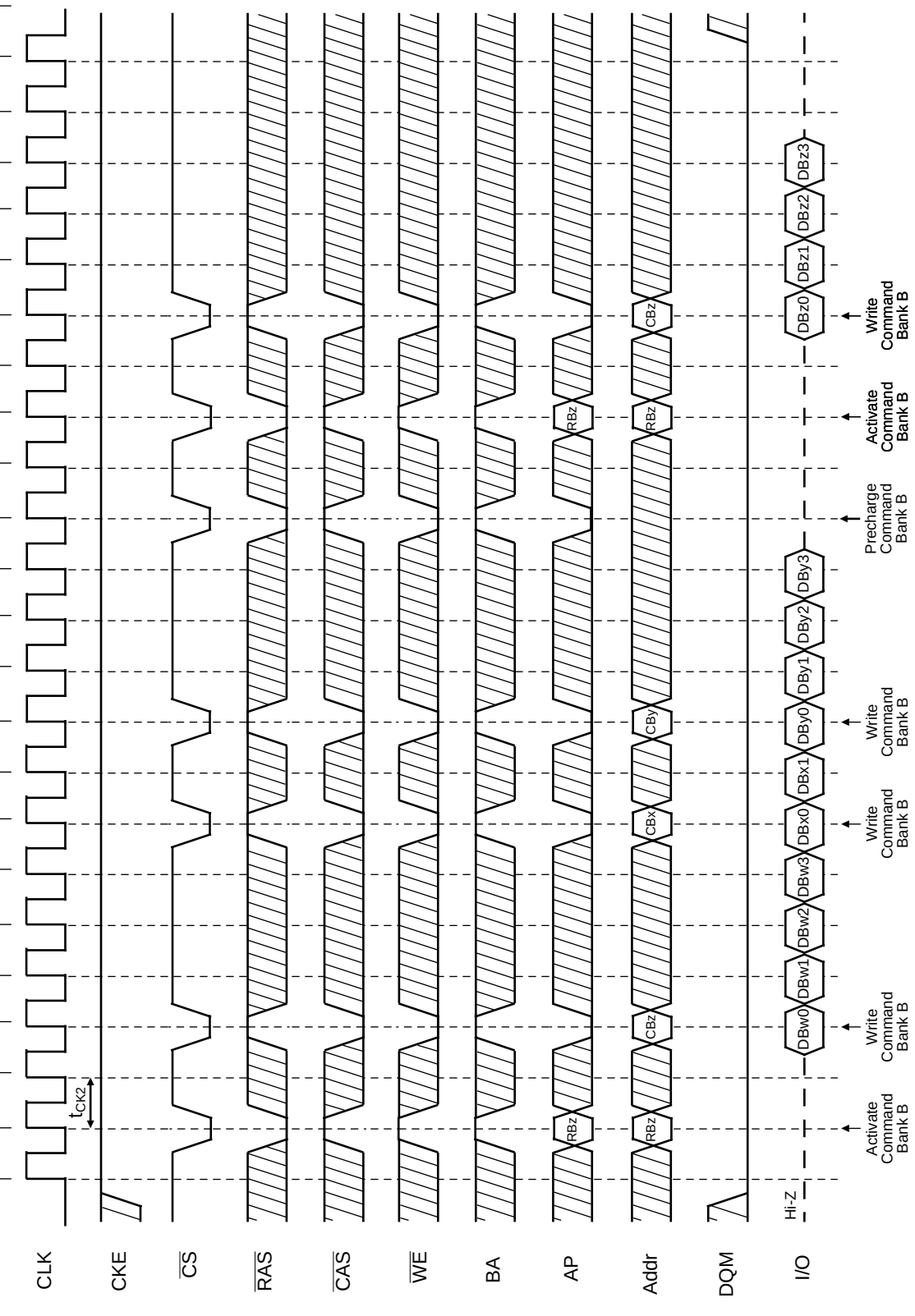


## 15.2 Random Column Read (Page within same Bank) (2 of 2)



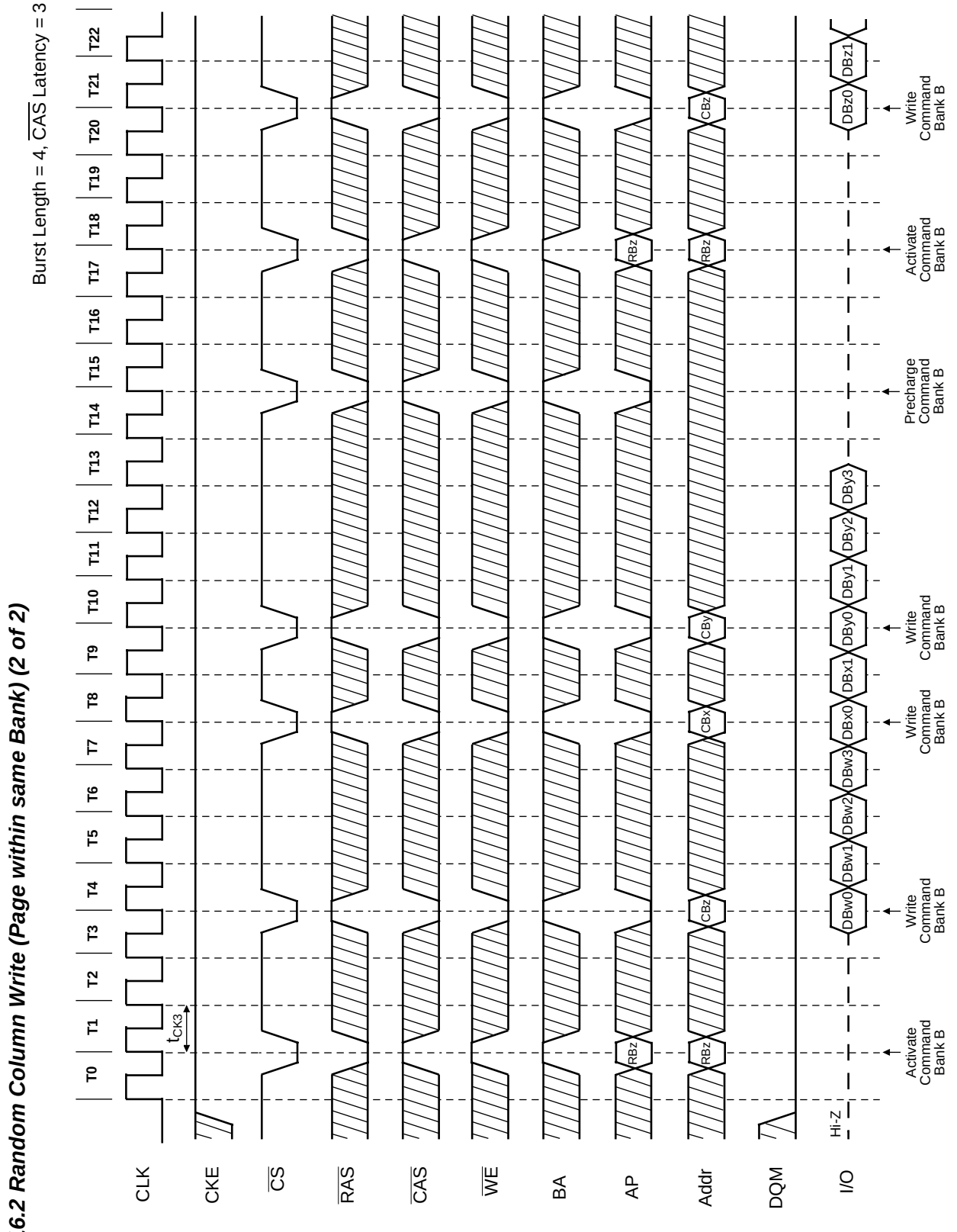
## 16.1 Random Column Write (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2



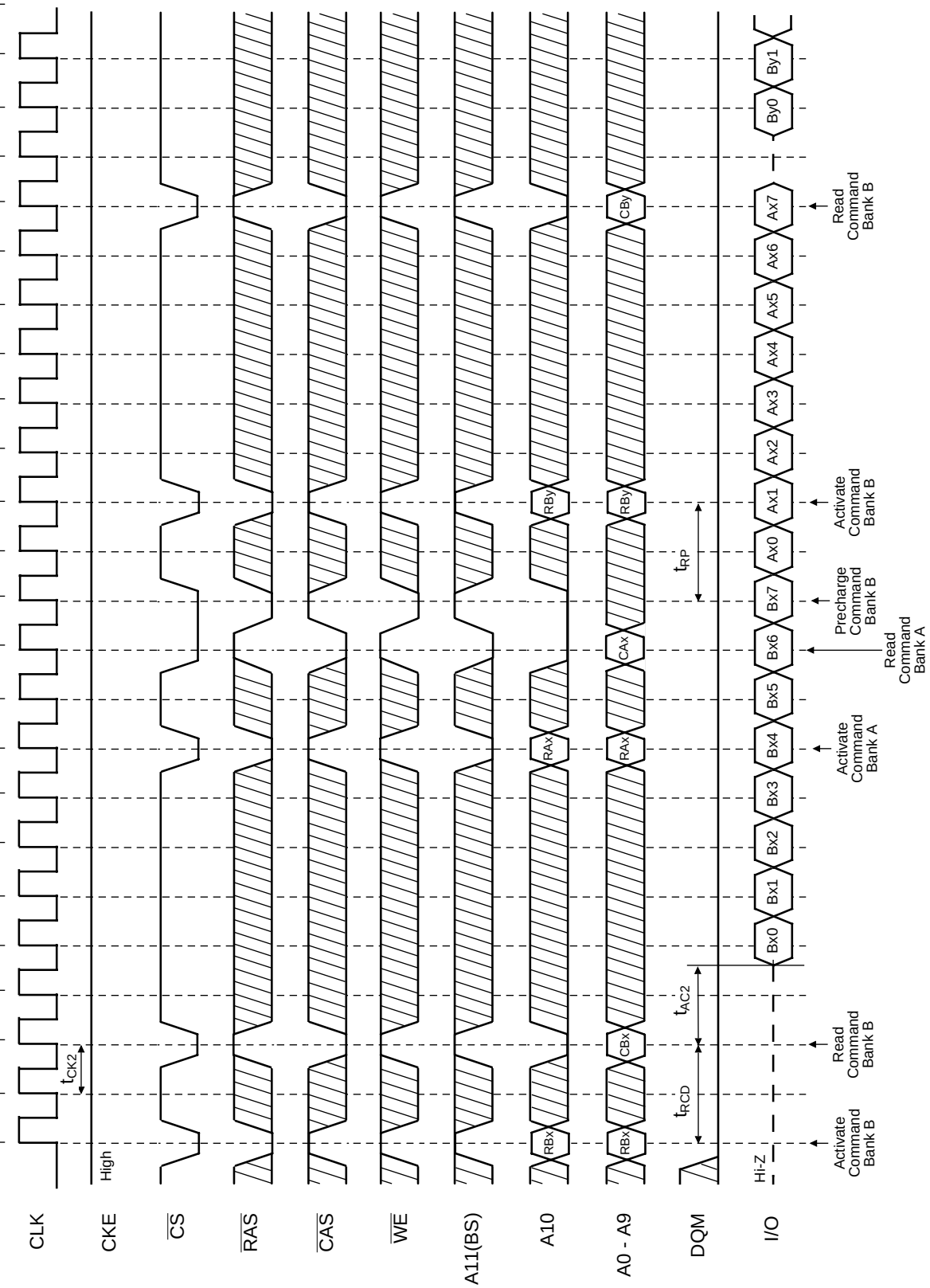
## 16.2 Random Column Write (Page within same Bank) (2 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 3



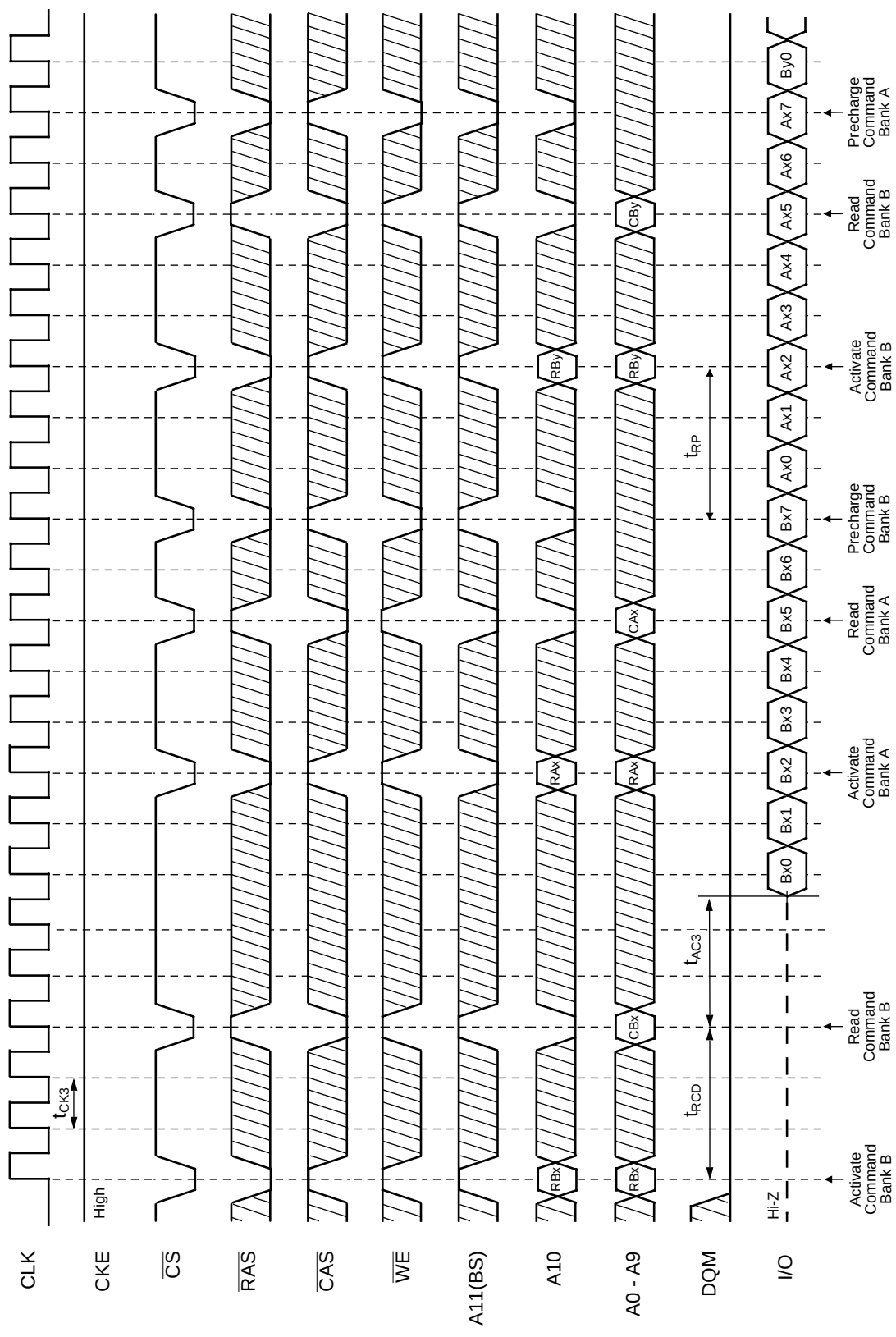
## 17.1 Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2



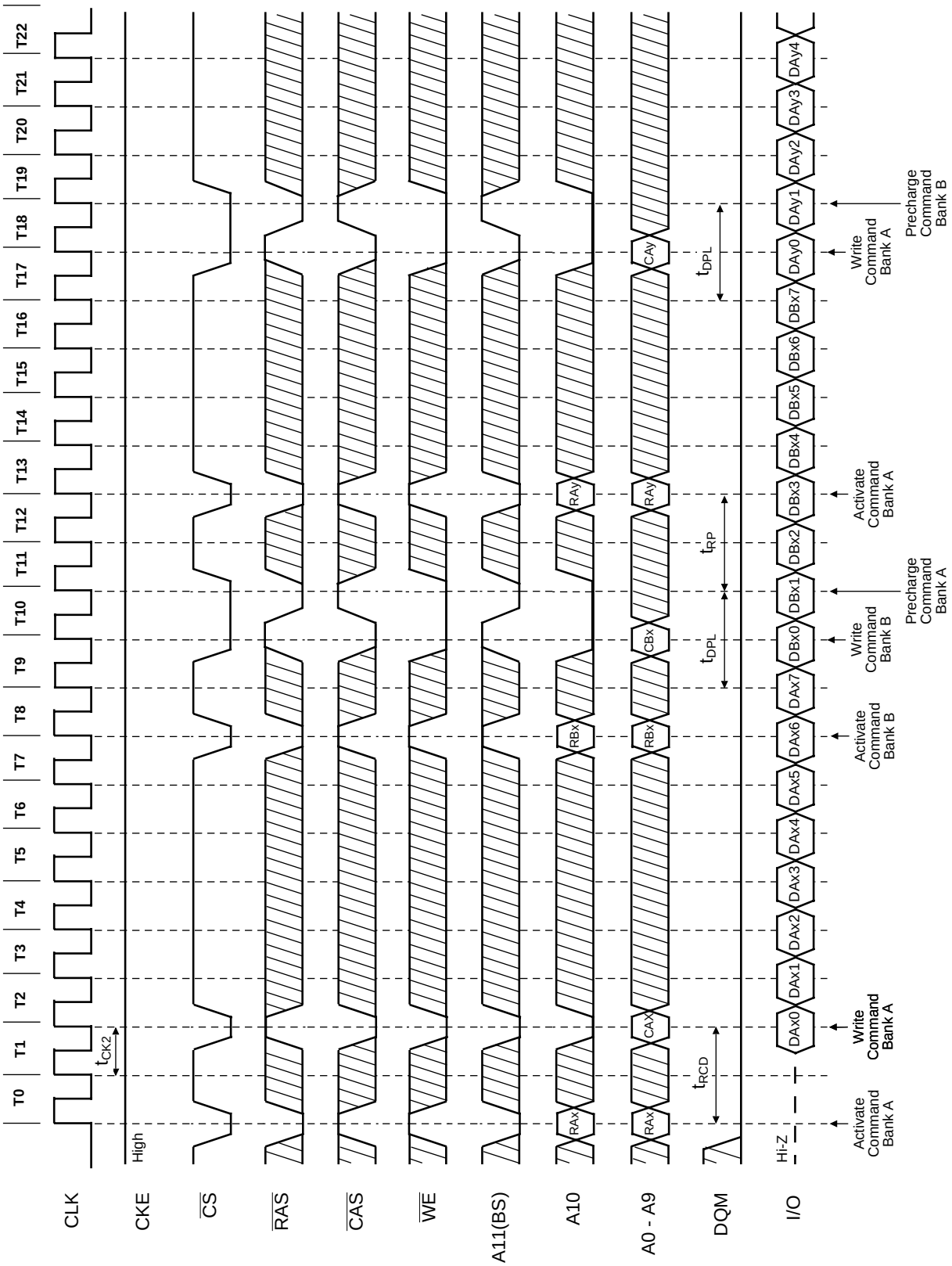
## 17. 2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



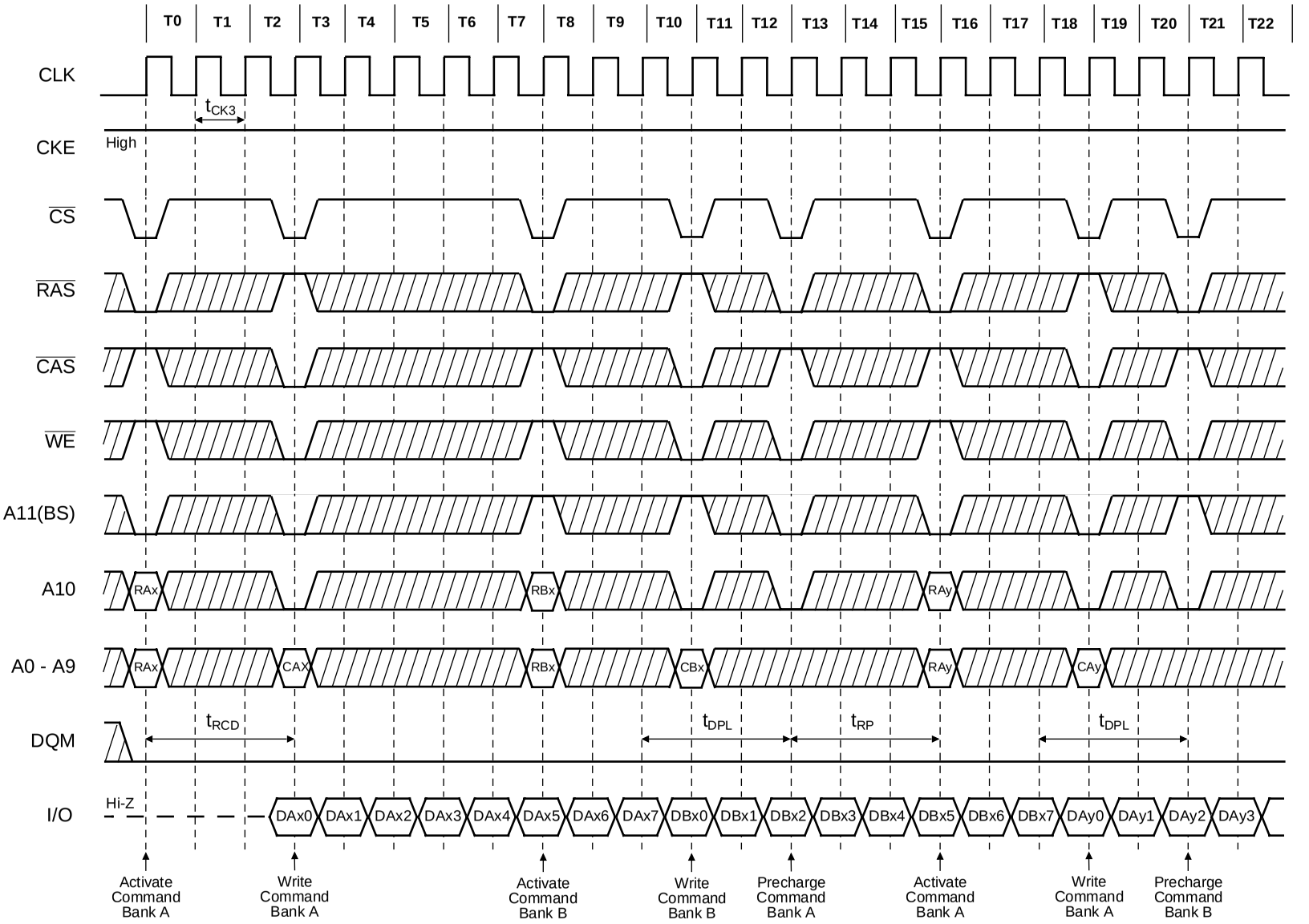
## 18.1 Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2



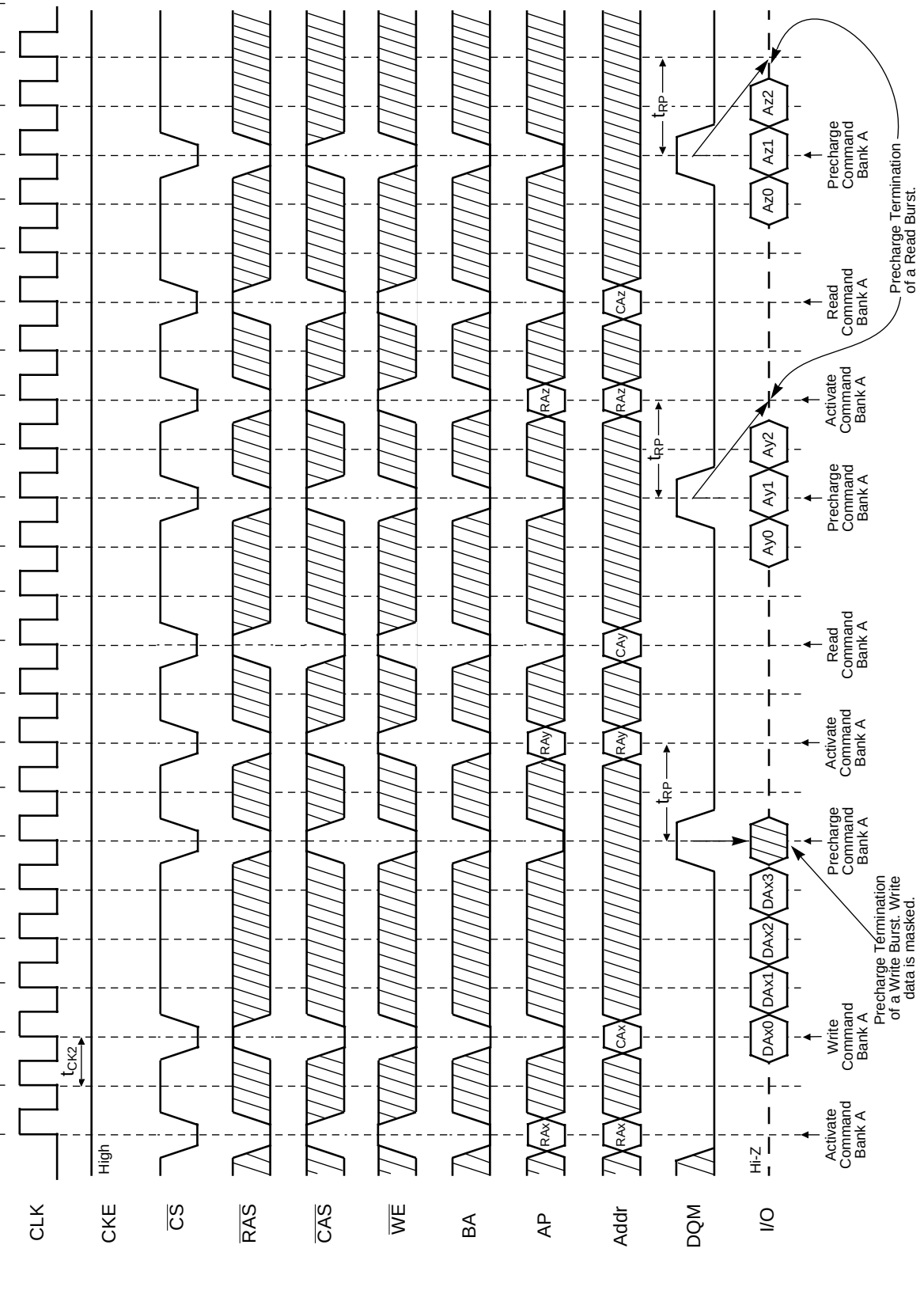
## 18.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



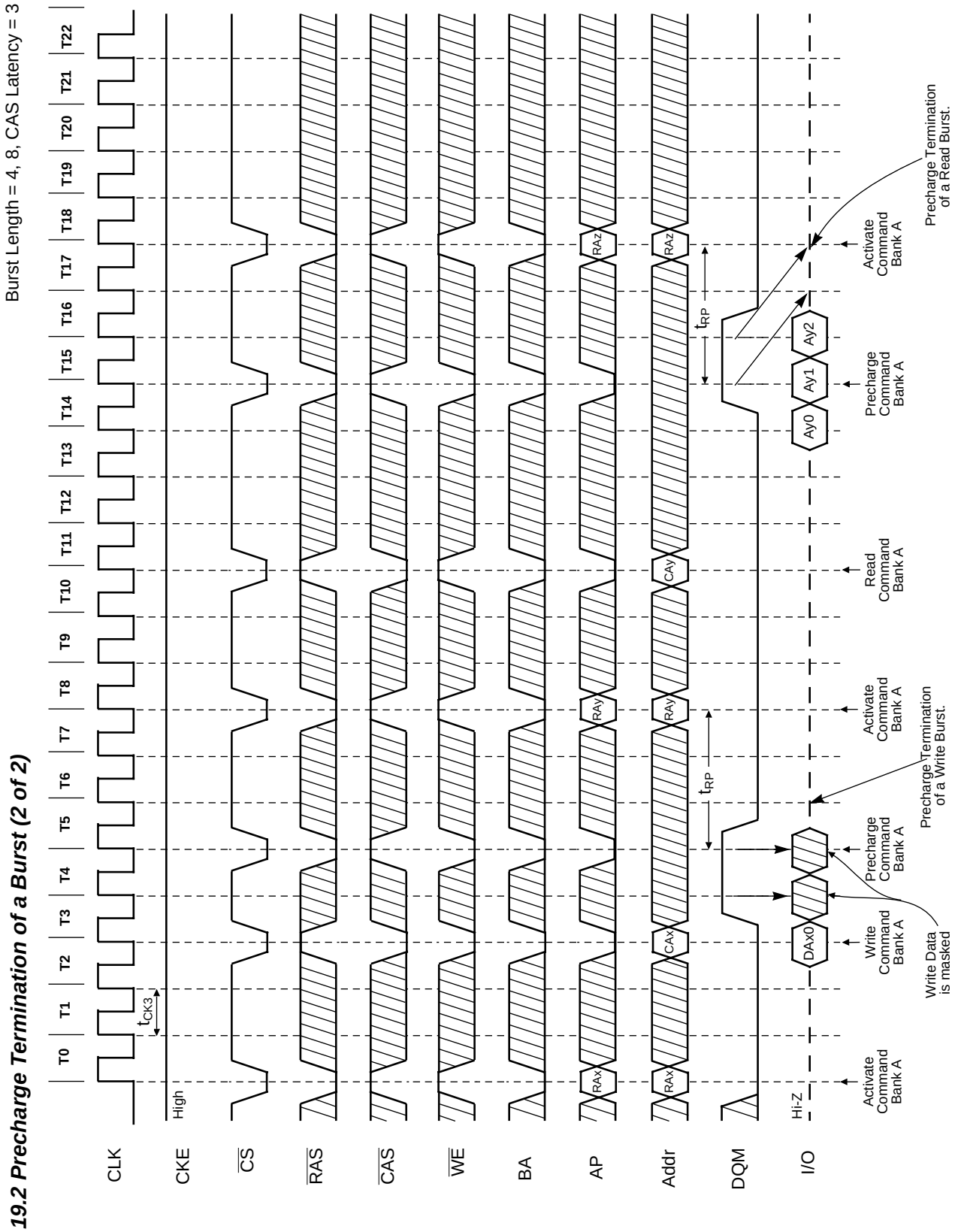
## 19.1 Precharge Termination of a Burst (1 of 2)

Burst Length = 8, CAS Latency = 2

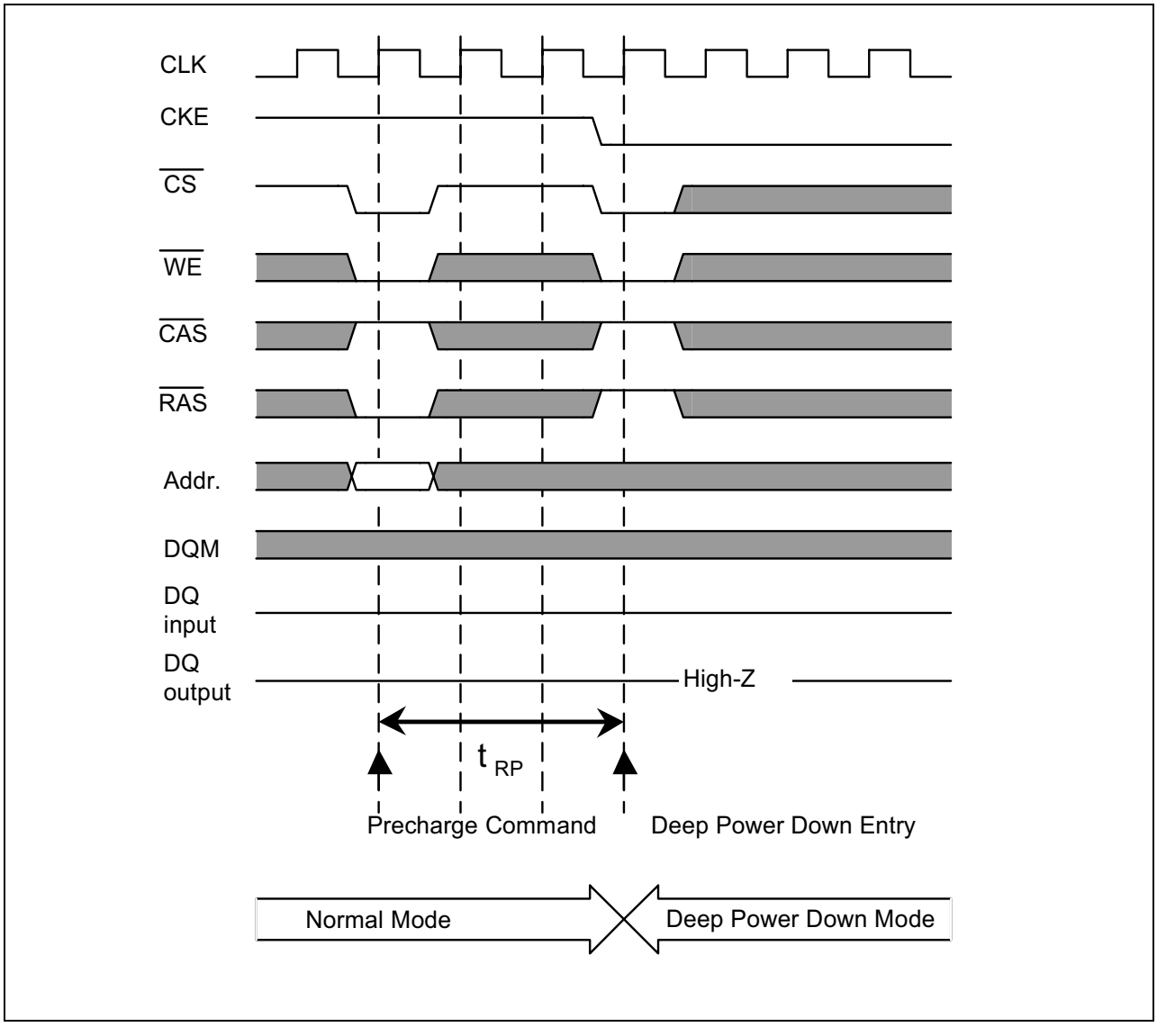


## 19.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8, CAS Latency = 3



### Deep Power Down Mode Entry

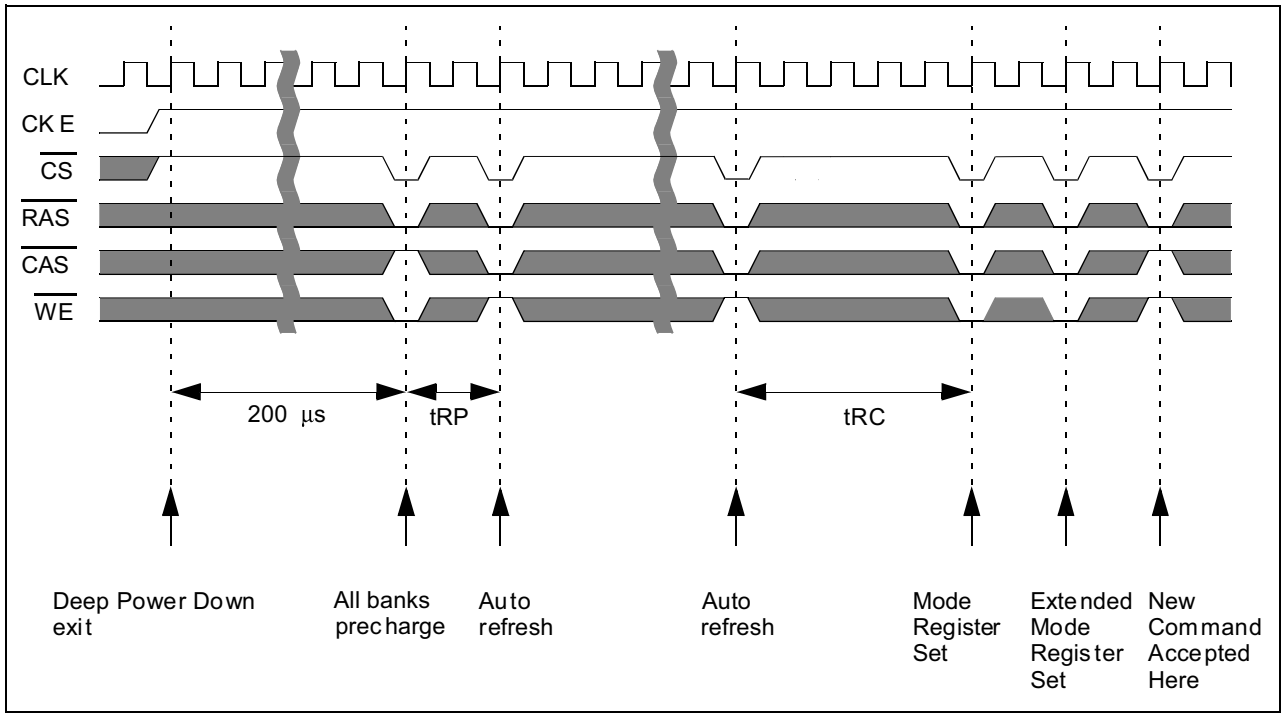



The deep power down mode has to be maintained for a minimum of 100µs.

### Deep Power Down Exit

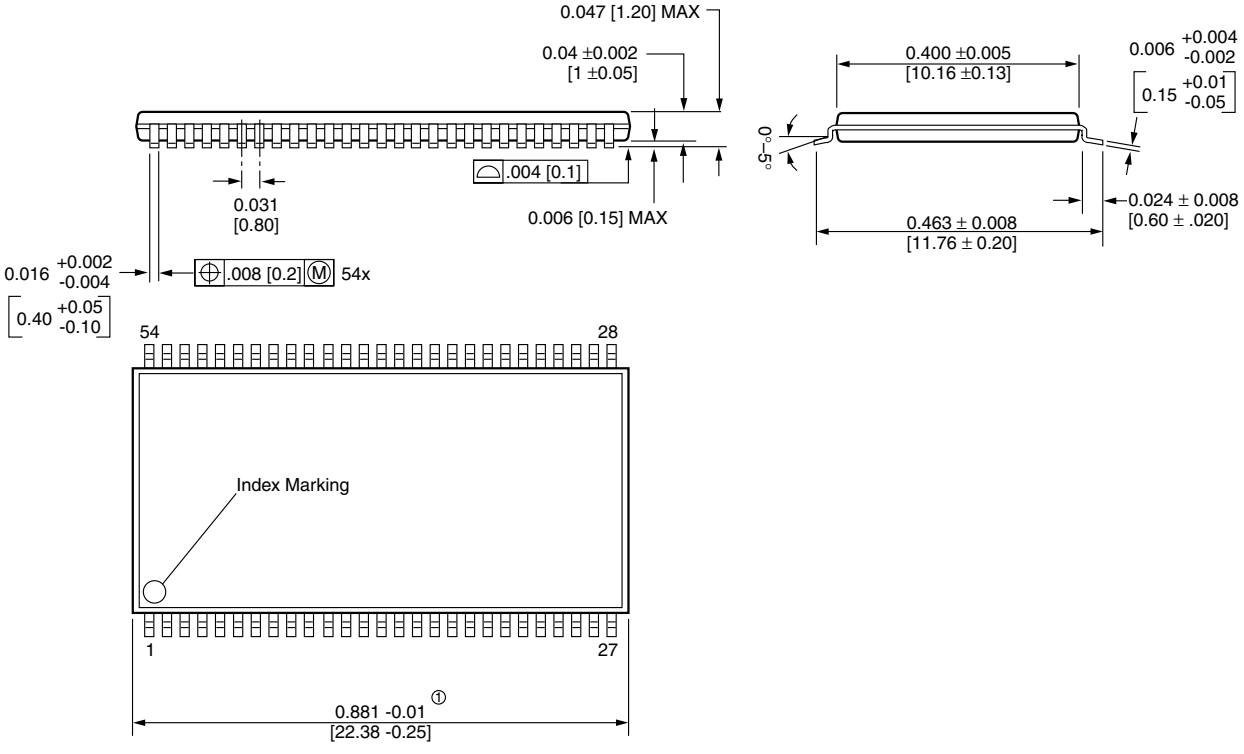
The deep power down mode is exited by asserting CKE high. After the exit, the following sequence is needed to enter a new command:

1. Maintain NOP input conditions for a minimum of 200 µs
2. Issue precharge commands for all banks of the device
3. Issue eight or more autorefresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extende mode register



## *Package Diagram*

### 54-Pin Plastic TSOP-II (400 mil)

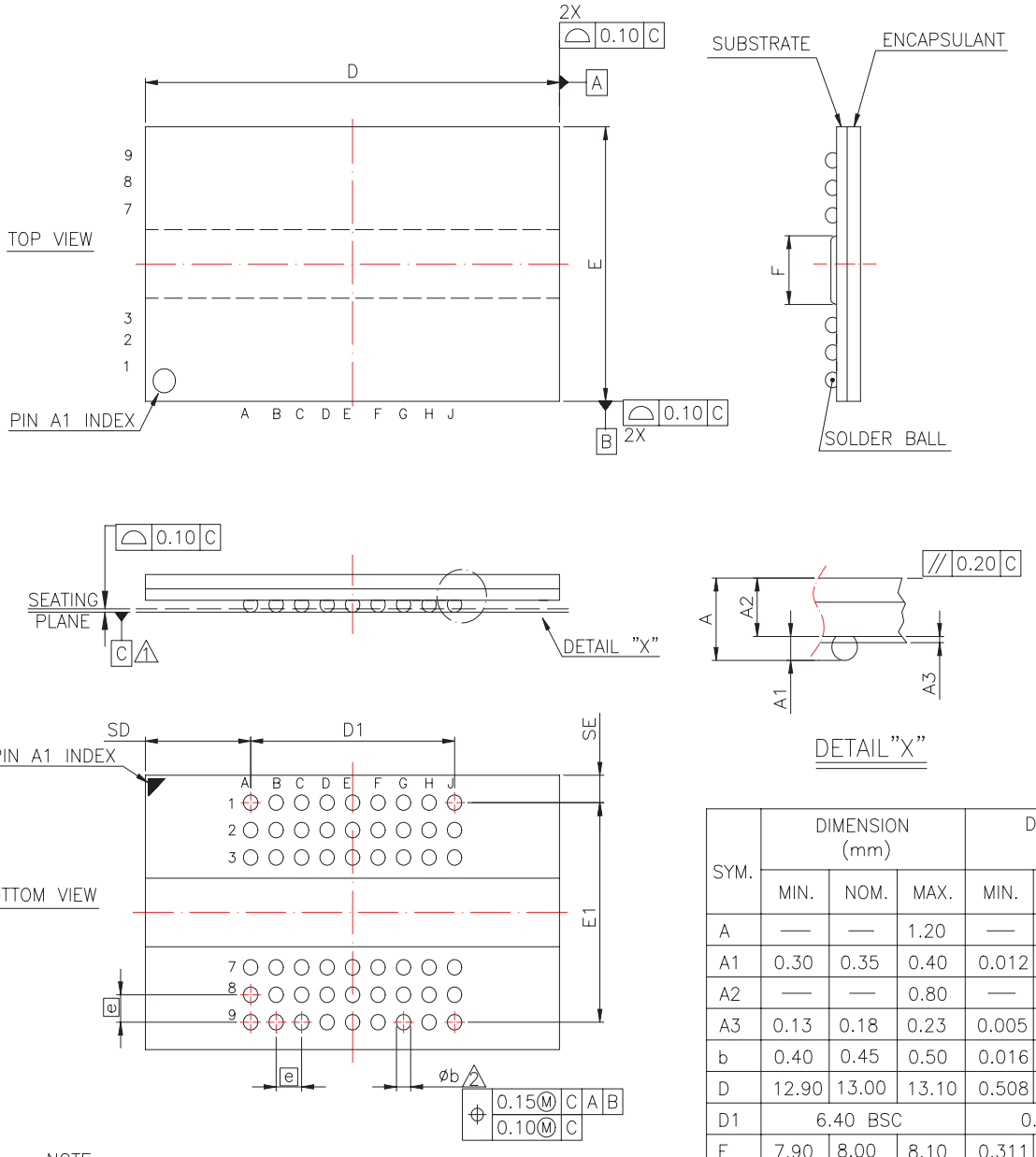



① Does not include plastic or metal protrusion of 0.15 max. per side

Unit in inches [mm]

## *Package Diagram*

### 54-Ball FBGA




NOTE:

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
2. DIMENSION 'b' IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. CONTROLLING DIMENSION : MILLIMETER.
4. REFERENCE DOCUMENT : JEDEC MO-210.

| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| A2 | — | — | 0.80 | — | — | 0.031 |
| A3 | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| D | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| D1 | 6.40 BSC | | | 0.252 BSC | | |
| E | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| E1 | 6.40 BSC | | | 0.252 BSC | | |
| F | 2.00 BSC | | | 0.079 BSC | | |
| SD | 3.30 BSC | | | 0.130 BSC | | |
| SE | 0.80 BSC | | | 0.031 BSC | | |
| e | 0.80 BSC | | | 0.031 BSC | | |

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