



N-Channel Enhancement-Mode Transistors

Characteristics

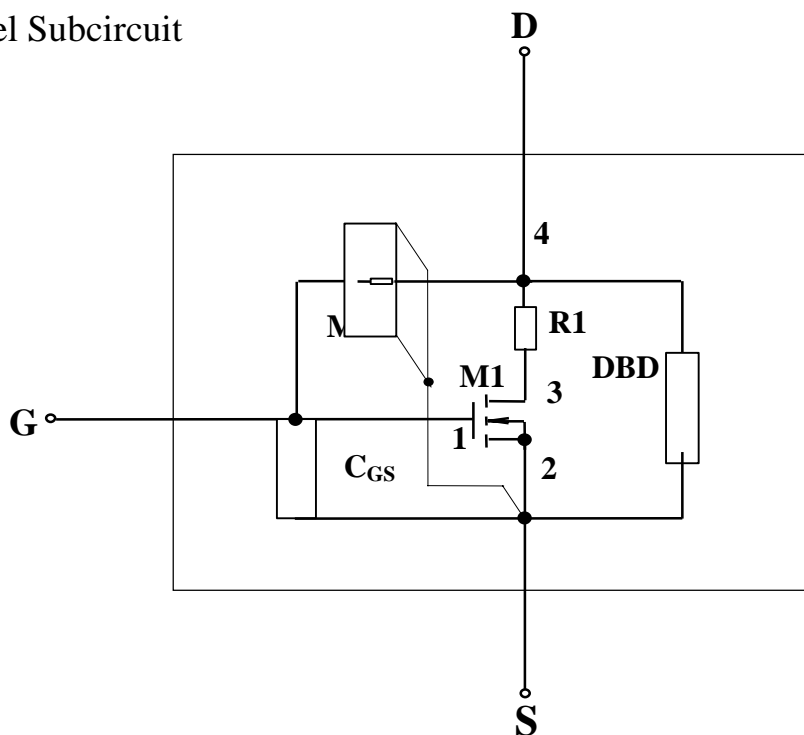
- N-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback

capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



Model Evaluation

N-Channel Device ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	3.12	V
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{V}, V_{GS} = 10\text{V}$	416	A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	0.011	Ω
		$V_{GS} = 10\text{V}, I_D = 30\text{A},$ $T_J = 125^\circ\text{C}$	0.018	
		$V_{GS} = 10\text{V}, I_D = 30\text{A},$ $T_J = 175^\circ\text{C}$	0.022	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{V}, I_D = 30\text{A}$	60	S
Forward Voltage ^b	V_{SD}	$I_F = 75\text{A}, V_{GS} = 0\text{V}$	0.92	V
Dynamic^a				
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1\text{MHz}$	4890	pF
Output Capacitance	C_{oss}		963	
Reverse Transfer Capacitance	C_{rss}		221	
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{V}, V_{GS} = 10\text{V},$ $I_D = 75\text{A}$	83	nC
Gate-Source Charge ^c	Q_{gs}		31	
Gate-Drain Charge ^c	Q_{gd}		24	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{V}, R_L = 0.47\Omega$ $I_D \cong 75\text{A}, V_{GEN} = 10\text{V},$ $R_G = 2.5\Omega$	57	ns
Rise Time ^c	t_r		31	
Turn-Off Delay Time ^c	$t_{d(off)}$		62	
Fall Time ^c	t_f		20	
Reverse Recovery Time	t_{rr}	$I_F = 75\text{A}, di/dt = 100\text{A}/\mu\text{s}$	100	ns

Notes:

- a) Guaranteed by design, not subject to production testing
- b) Pulse test: pulse width $\leq 300 \mu\text{sec}$, duty cycle $\leq 2\%$
- c) Independent of operating temperature



SPICE Device Model SUP/SUB75N08-10

Comparison of Model with Measured Data
($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

