High Voltage Latch-Up Proof, Single SPDT Switch

Data Sheet

ADG5419

FEATURES

- Latch-up immune under all circumstances
- Human body model (HBM) ESD rating: 8 kV
- Low on resistance: 13.5 Ω
- ±9 V to ±22 V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at ±15 V, ±20 V, +12 V, and +36 V
- V_{DD} to V_{SS} analog signal range

APPLICATIONS

- High voltage signal routing
- Automatic test equipment
- Analog front-end circuits
- Precision data acquisition
- Industrial instrumentation
- Amplifier gain select
- Relay replacement

FUNCTIONAL BLOCK DIAGRAMS

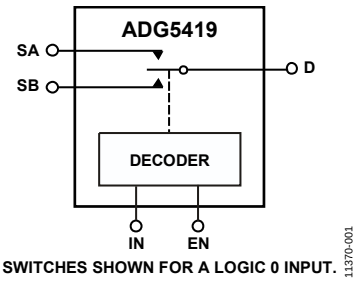

Figure 1. 8-Lead LFCSP

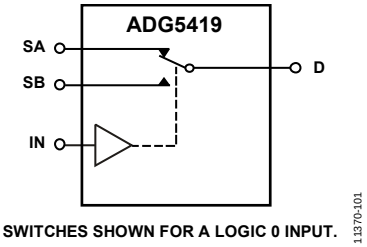

Figure 2. 8-Lead MSOP

GENERAL DESCRIPTION

The ADG5419 is a monolithic industrial, complementary metal oxide semiconductor (CMOS) analog switch containing a latch-up immune single-pole/double-throw (SPDT) switch.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. The ADG5419 exhibits break-before-make switching action for use in multiplexer applications.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. The latch-up immune construction and high ESD rating make these switches more robust in harsh environments.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P channel and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} of 13.5 Ω.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5419 can be operated from dual supplies up to ±22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5419 can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.
7. Available in 8-lead MSOP and 8-lead, 2 mm × 3 mm LFCSP packages.

Rev. A
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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Evaluation Board for 8 lead MSOP Devices in the Switch/ Mux Portfolio

DOCUMENTATION

Data Sheet

- ADG5419: High Voltage Latch-Up Proof, Single SPDT Switch Data Sheet

User Guides

- UG-893: Evaluating the 8-Lead MSOP Devices in the Switch/Mux Portfolio

REFERENCE MATERIALS

Press

- Latch-up Immune, High ESD Switches, Expands ADI Offerings in High-Voltage Industrial Applications

DESIGN RESOURCES

- ADG5419 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG5419 EngineerZone Discussions.

SAMPLE AND BUY

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9/13—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 27
	15	19	23	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.8			Ω typ	V_S = ±10 V, I_S = −10 mA
	2.2	2.7	3.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 24 and Figure 25
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 25
	±0.4	±4	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 24 and Figure 26
	±0.4	±4	±10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	217			ns typ	R_L = 300 Ω, C_L = 35 pF
	260	310	336	ns max	V_S = 10 V; see Figure 32
t_{ON} (EN)	179			ns typ	R_L = 300 Ω, C_L = 35 pF
	212	261	298	ns max	V_S = 10 V; see Figure 33
t_{OFF} (EN)	153			ns typ	R_L = 300 Ω, C_L = 35 pF
	176	195	209	ns max	V_S = 10 V; see Figure 33
Break-Before-Make Time Delay, t_D	86			ns typ	R_L = 300 Ω, C_L = 35 pF
			45	ns min	V_S = 10 V; see Figure 34
Charge Injection, Q_{INJ}	130			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	190			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	12			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	55			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 27
	14	18	22	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	2.3			Ω typ	V_S = ±15 V, I_S = −10 mA
	2.7	3.3	3.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 24 and Figure 25
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 25
	±0.4	±4	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 24 and Figure 26
	±0.4	±4	±10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	235	279	294	ns max	V_S = 10 V; see Figure 32
t_{ON} (EN)	199			ns typ	R_L = 300 Ω, C_L = 35 pF
	239	300	344	ns max	V_S = 10 V; see Figure 33
t_{OFF} (EN)	157			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	208	227	ns max	V_S = 10 V; see Figure 33
Break-Before-Make Time Delay, t_D	77			ns typ	R_L = 300 Ω, C_L = 35 pF
			46	ns min	V_S = 10 V; see Figure 34
Charge Injection, Q_{INJ}	160			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	190			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	22			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	55			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			μA typ	Digital inputs = 0 V or V_{DD}
	70		110	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 27
	30	38	44	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	5.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	6.8	8.3	12.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V; see Figure 24 and Figure 25
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	VS = 1V to10 V, VD = 10 V to 1V; see Figure 25
	±0.4	±4	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V to 10 V; see Figure 24 and Figure 26
	±0.4	±4	±10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	333			ns typ	R_L = 300 Ω, C_L = 35 pF
	414	508	567	ns max	V_S = 8 V; see Figure 32
t_{ON} (EN)	327			ns typ	R_L = 300 Ω, C_L = 35 pF
	410	526	612	ns max	V_S = 8 V; see Figure 33
t_{OFF} (EN)	166			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	528	611	ns max	V_S = 8 V; see Figure 33
Break-Before-Make Time Delay, t_D	176			ns typ	R_L = 300 Ω, C_L = 35 pF
			97	ns min	V_S = 8 V; see Figure 34
Charge Injection, Q_{INJ}	55			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	170			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−1.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	15			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	29			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	50			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			μA typ	Digital inputs = 0 V or V_{DD}
	50		65	μA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 27
	16	20	24	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	3.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	4.3	5.5	6.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V; see Figure 24 and Figure 25
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1V to 30 V, V_D = 30 V to 1V; see Figure 25
	±0.4	±4	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V to 30 V; see Figure 24 and Figure 26
	±0.4	±4	±10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	216			ns typ	R_L = 300 Ω, C_L = 35 pF
	250	286	310	ns max	V_S = 18 V; see Figure 32
t_{ON} (EN)	199			ns typ	R_L = 300 Ω, C_L = 35 pF
	232	279	315	ns max	V_S = 18 V; see Figure 33
t_{OFF} (EN)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	193	284	315	ns max	V_S = 18 V; see Figure 33
Break-Before-Make Time Delay, t_D	80			ns typ	R_L = 300 Ω, C_L = 35 pF
			47	ns min	V_S = 18 V; see Figure 34
Charge Injection, Q_{INJ}	135			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	170			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−1			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	14			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	26			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	50			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			μA typ	Digital inputs = 0 V or V_{DD}
	100		130	μA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
8-LEAD MSOP					θ_{JA} = 133.1°C/W
V_{DD} = 15 V, V_{SS} = −15 V	113	73	46	mA maximum	
V_{DD} = 20 V, V_{SS} = −20 V	118	76	47	mA maximum	
V_{DD} = 12 V, V_{SS} = 0 V	90	60	41	mA maximum	
V_{DD} = 36 V, V_{SS} = 0 V	116	74	46	mA maximum	
8-LEAD LFCSP					θ_{JA} = 60.88°C/W
V_{DD} = 15 V, V_{SS} = −15 V	156	92	52	mA maximum	
V_{DD} = 20 V, V_{SS} = −20 V	163	95	53	mA maximum	
V_{DD} = 12 V, V_{SS} = 0 V	126	78	48	mA maximum	
V_{DD} = 36 V, V_{SS} = 0 V	160	93	53	mA maximum	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	410 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
8-Lead MSOP (4-Layer Board)	133.1°C/W
8-Lead LFCSP	60.88°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
Human Body Model (HBM) ESD	8 kV

[1] Overvoltages at the IN, Sx, and D pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

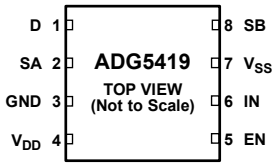

Figure 3. 8-Lead LFCSP Pin Configuration

Figure 4. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
LFCSP	**MSOP**	**Mnemonic**	**Description**
1	1	D	Drain Terminal. This pin can be an input or output.
2	2	SA	Source Terminal. This pin can be an input or an output.
3	3	GND	Ground (0 V) Reference.
4	4	V_{DD}	Most Positive Power Supply Potential.
5		EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the IN logic input determines the state of the switch.
6	6	IN	Logic Control Input.
7	7	V_{SS}	Most Negative Power Supply Potential.
8	8	SB	Source Terminal. This pin can be an input or an output.
	5	NC	No Connect. Not internally connected.
	Not applicable	EPAD	Exposed Pad. Exposed pad tied to substrate, V_{SS}.

Table 8. LFCSP Truth Table

EN	IN	Switch A	Switch B
0	X[1]	Off	Off
1	0	On	Off
1	1	Off	On

[1] X = don't care.

Table 9. MSOP Truth Table

IN	Switch A	Switch B
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

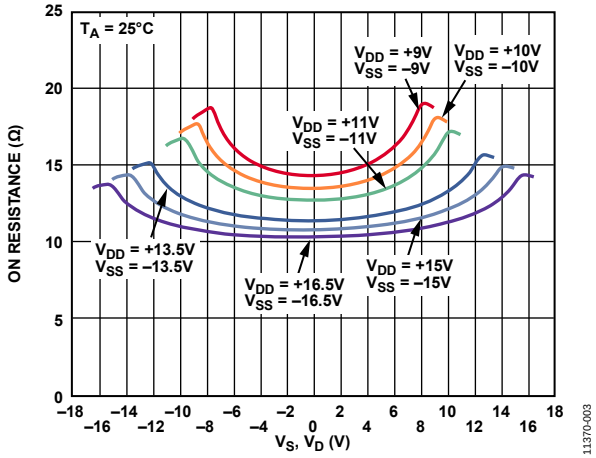

Figure 5. On Resistance as a Function of V_S, V_D Dual Supply

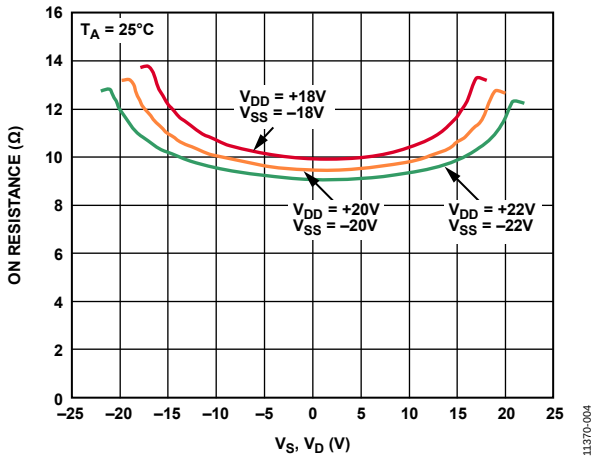

Figure 6. On Resistance as a Function of V_S, V_D Dual Supply)

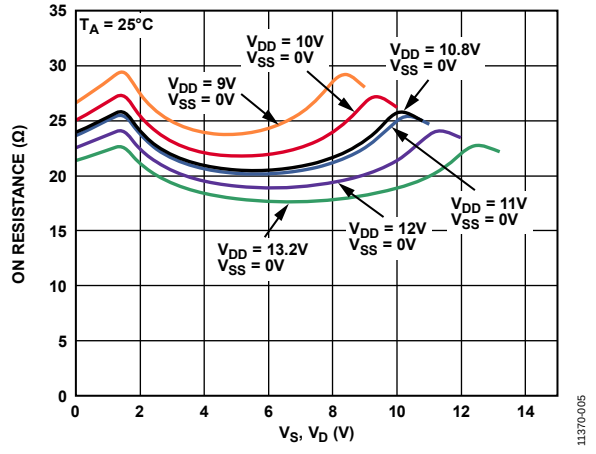

Figure 7. On Resistance as a Function of V_S, V_D (Single Supply)

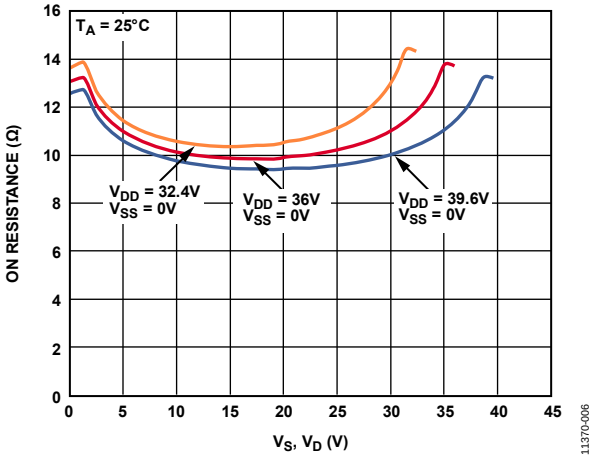

Figure 8. On Resistance as a Function of V_S, V_D (Single Supply)

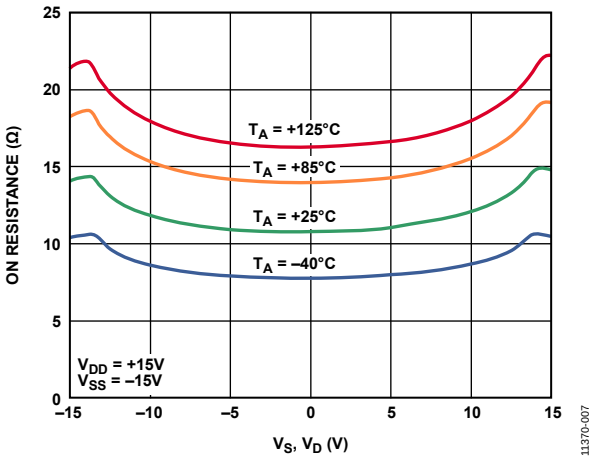

Figure 9. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

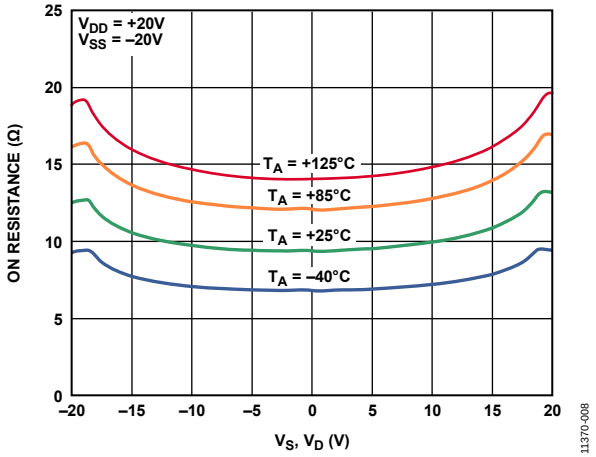

Figure 10. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

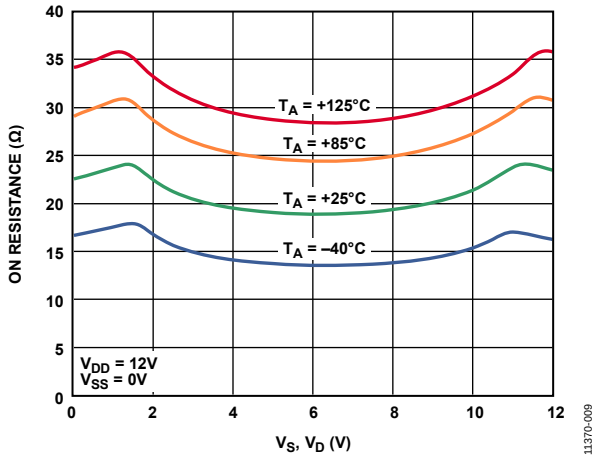

Figure 11. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

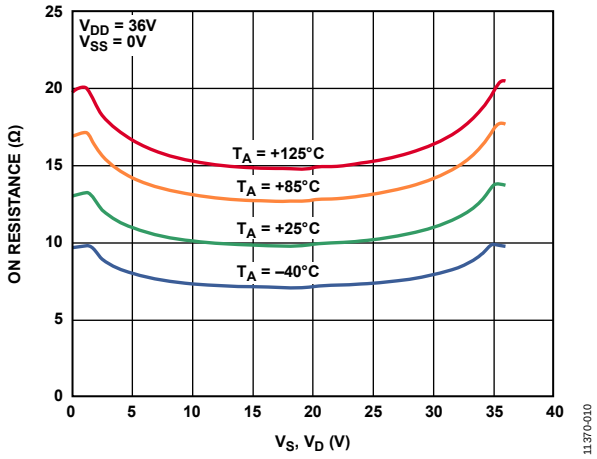

Figure 12. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

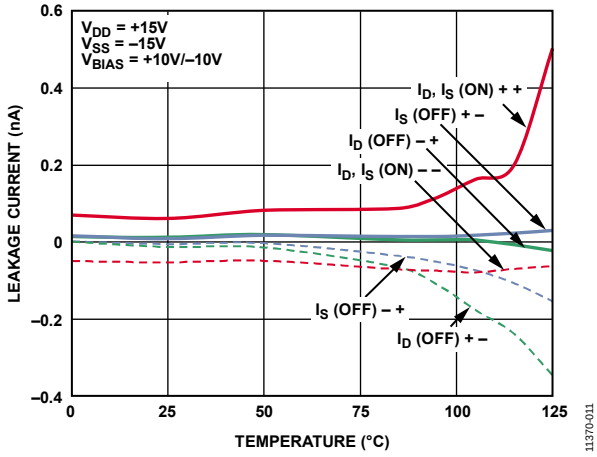

Figure 13. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

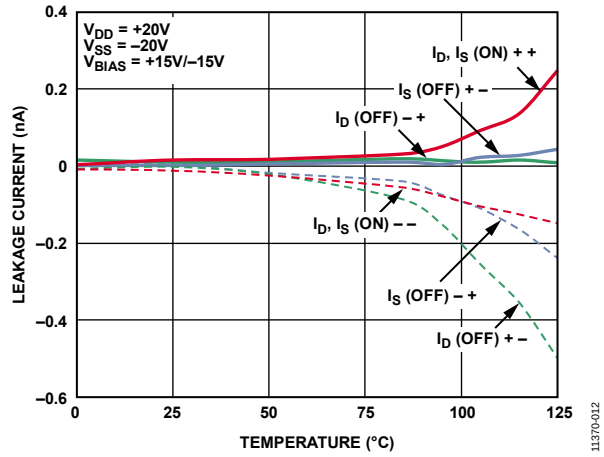

Figure 14. Leakage Currents as a Function of Temperature, ±20 V Dual Supply

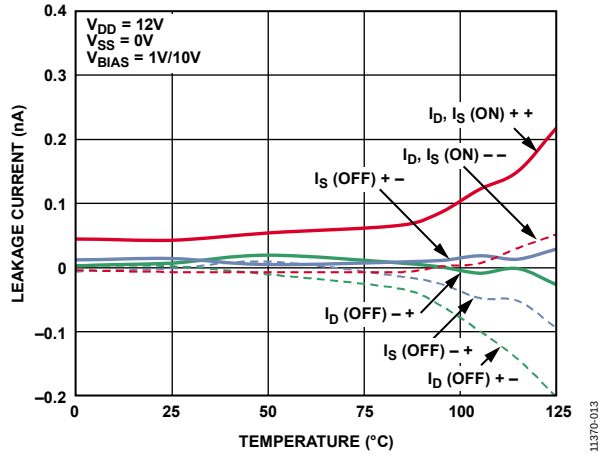

Figure 15. Leakage Currents as a Function of Temperature, 12 V Single Supply

Figure 16. Leakage Currents as a Function of Temperature, 36 V Single Supply

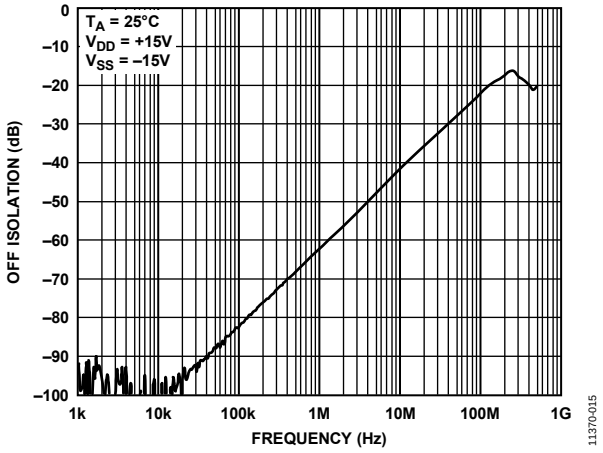

Figure 17. Off Isolation vs. Frequency

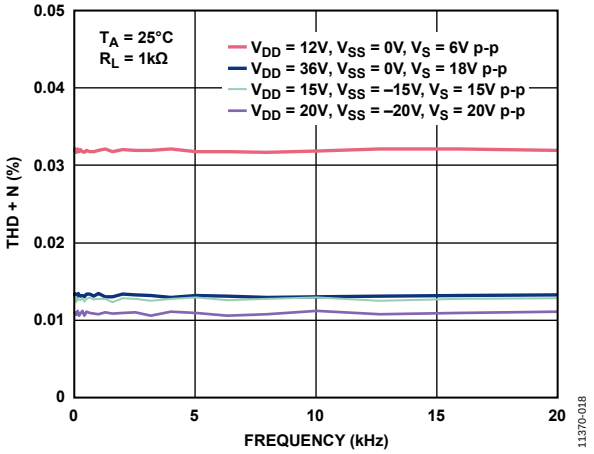

Figure 20. THD + N vs. Frequency

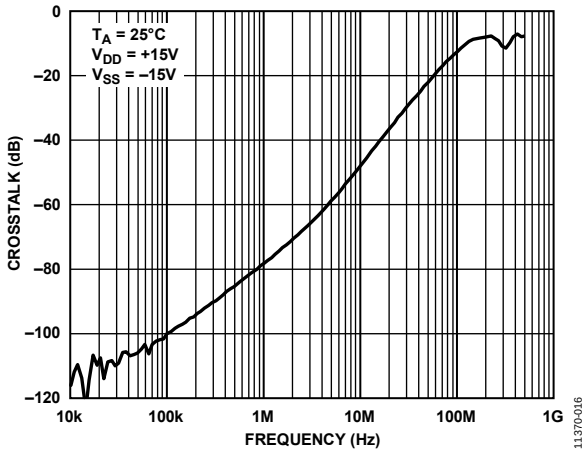

Figure 18. Crosstalk vs. Frequency

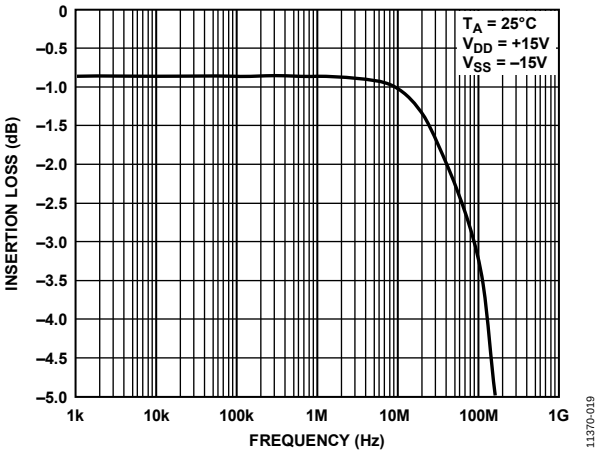

Figure 21. Bandwidth

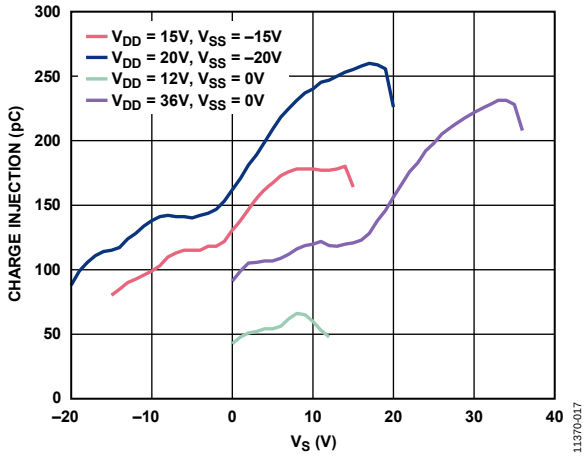

Figure 19. Charge Injection vs. Source Voltage

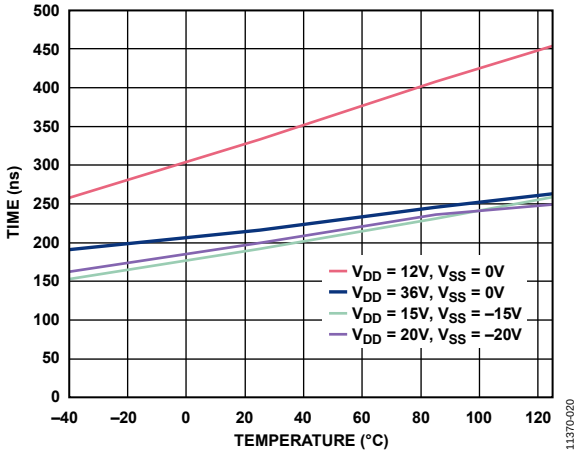

Figure 22. $t_{TRANSITION}$ Times vs. Temperature

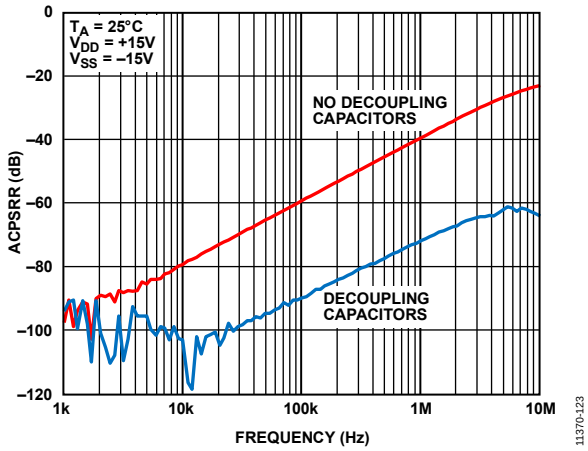

Figure 23. ACPSRR vs. Frequency

TEST CIRCUITS

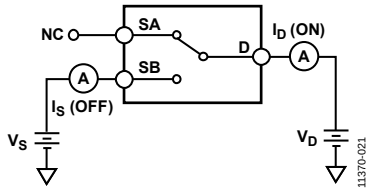

Figure 24. Channel On and Source Off Leakage (MSOP Only)

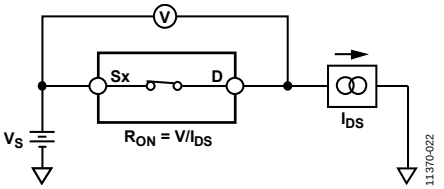

Figure 27. On Resistance

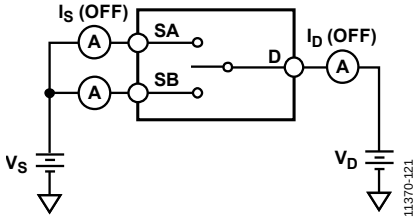

Figure 25. Off Leakage (LFCSP Only)

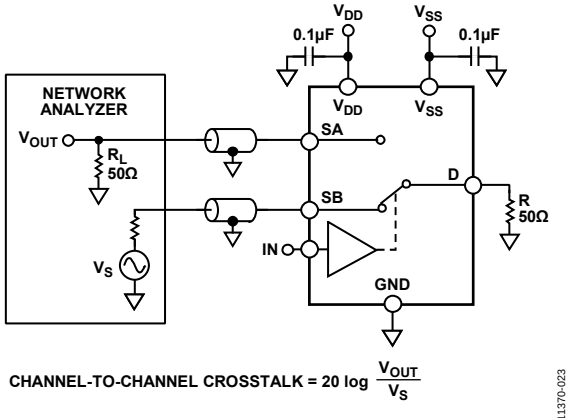

Figure 28. Channel-to-Channel Crosstalk

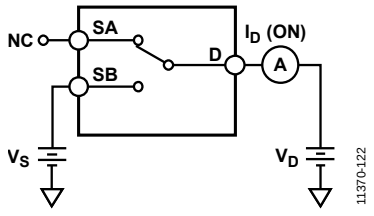

Figure 26. On Leakage (LFCSP Only)

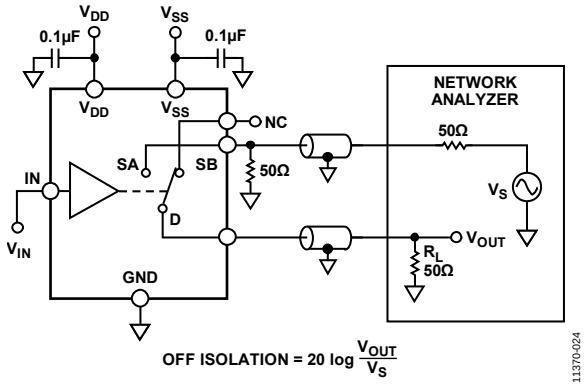

Figure 29. Off Isolation

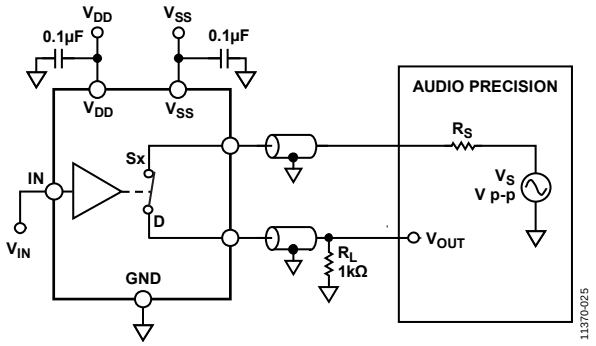

Figure 30. THD + Noise

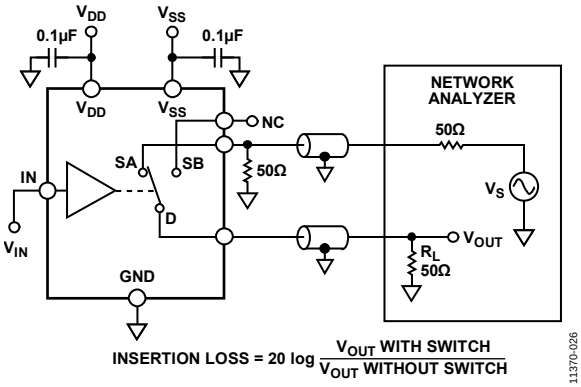

Figure 31. Bandwidth

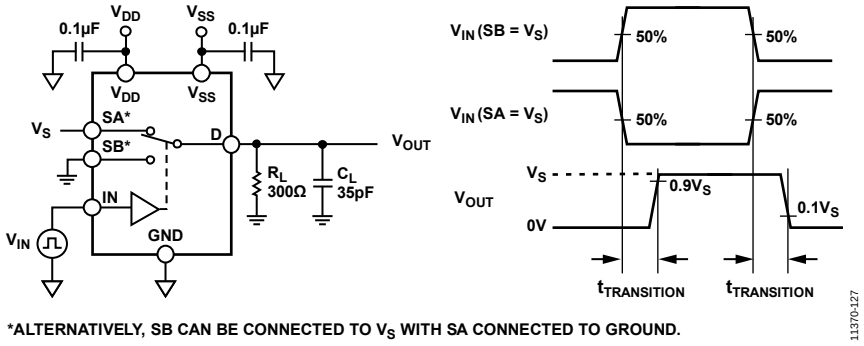

Figure 32. Transition Time, $t_{TRANSITION}$

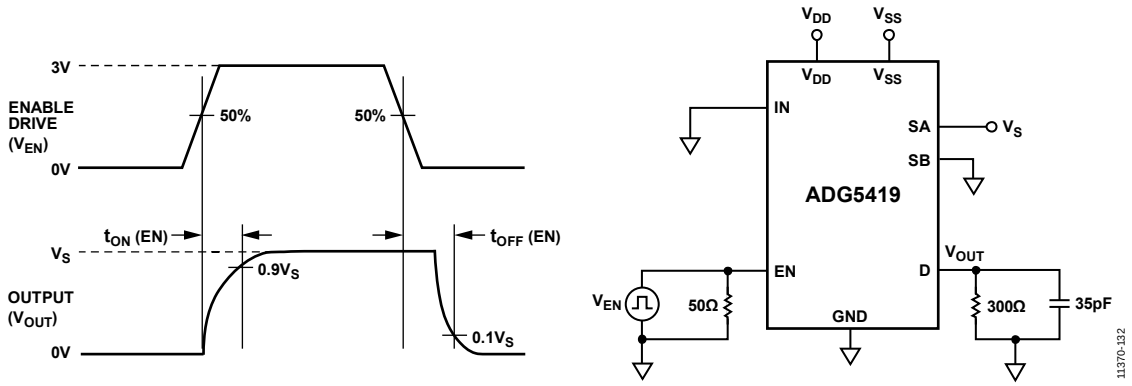

Figure 33. Enable Delay, t_{ON} (EN), t_{OFF} (EN) (LFCSP Only)

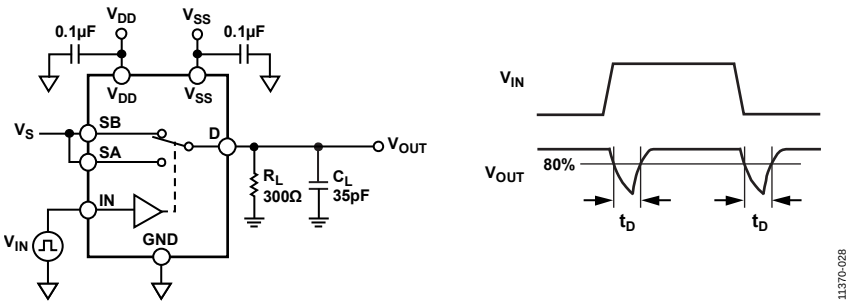

Figure 34. Break-Before-Make Delay, t_D

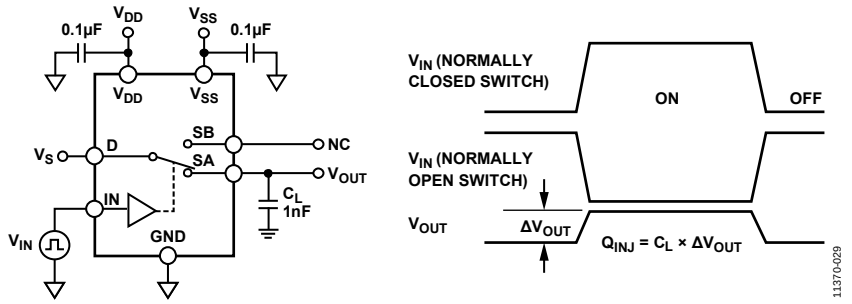

Figure 35. Charge Injection

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents digital input capacitance.

t_{ON} (EN)
t_{ON} represents the delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 33.

t_{OFF} (EN)
t_{OFF} represents the delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 33.

$t_{TRANSITION}$
$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB, from its dc level.

Total Harmonic Distortion + Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 23.

APPLICATIONS INFORMATION

The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5419 high voltage switch allows single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V. The ADG5419 (as well as other select devices within this family) achieves an 8 kV human body model ESD rating, which provides a robust solution, eliminating the need for separate protection circuitry designs in some applications.

TRENCH ISOLATION

In the ADG5419, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a completely latch-up immune switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. The two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up immune switch.

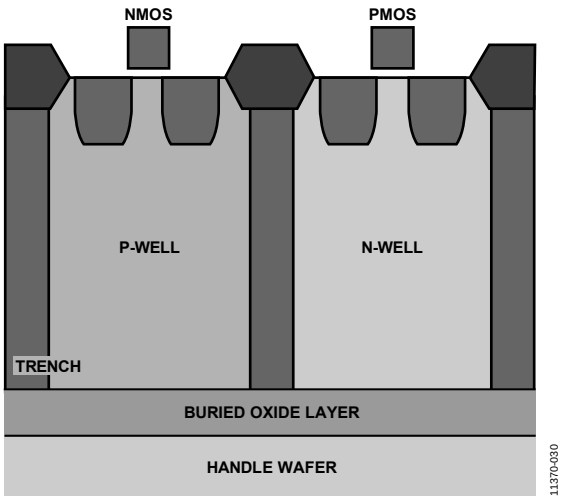

Figure 36. Trench Isolation

OUTLINE DIMENSIONS

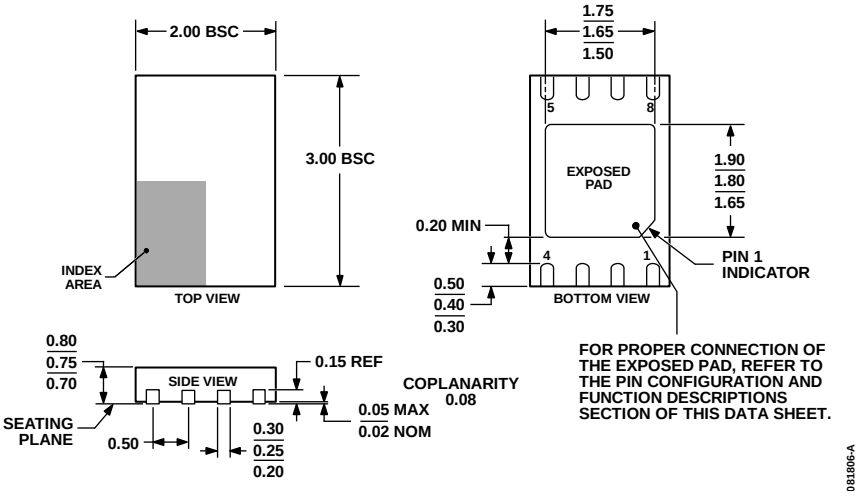

Figure 37. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
2 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-4)
Dimensions shown in millimeters

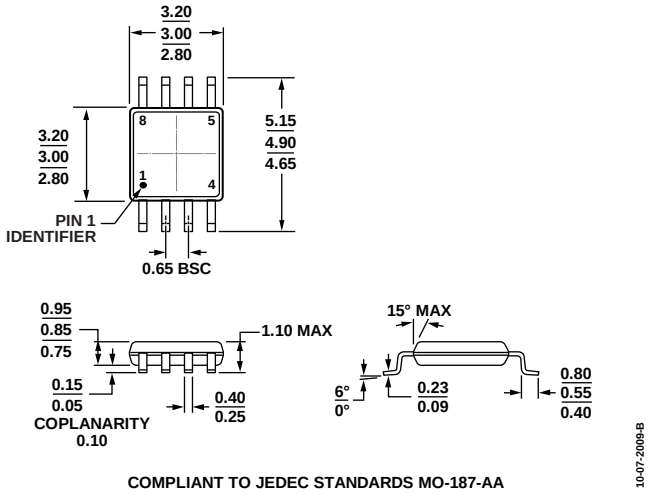

Figure 38. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG5419BCPZ-RL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-4	BL
ADG5419BRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S48
ADG5419BRMZ-RL7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S48

[1] Z = RoHS Compliant Part.

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D11370-0-3/15(A)