MP2212

16V, 3A, 600kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2212 is an internally compensated 600kHz fixed frequency PWM synchronous step-down regulator. With a 3V to 6V bias supply (V_{CC}), MP2212 operates from a 3V to 16V input and generates an adjustable output voltage from 0.8V to 0.9xV_{IN} at up to 3A load current.

The MP2212 integrates an 80mΩ high-side switch and an 80mΩ synchronous rectifier for high efficiency without an external Schottky diode. With peak current mode control and internal compensation, it is stable with a ceramic output capacitor and a small inductor. Fault protection includes hiccup short-circuit protection, cycle-by-cycle current limiting and thermal shutdown. Other features include frequency synchronization input and internal soft-start.

The MP2212 is available in small 3mm x 3mm 10-lead QFN and 8-lead SOIC with exposed pad packages.

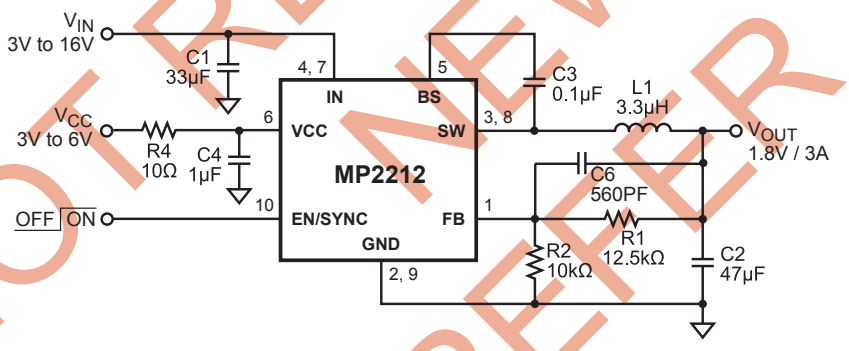
FEATURES

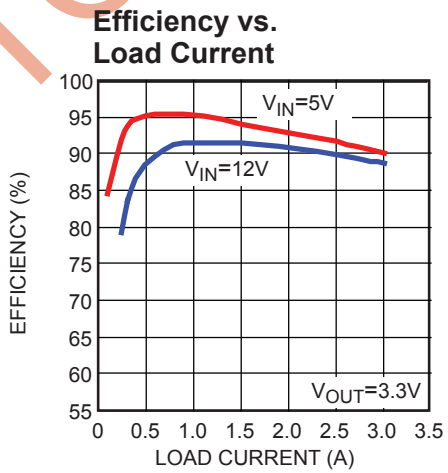
- 3A Output Current
- Input Supply Range: 3V to 16V
- 80mΩ Internal Power MOSFET Switches
- All Ceramic Output Capacitors Design
- Up to 95% Efficiency
- 600kHz Fixed Switching Frequency
- Adjustable Output from 0.8V to 0.9xV_{IN}
- Internal Soft-Start
- Frequency Synchronization Input
- Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Hiccup Short Circuit Protection
- 10-lead, 3mm x 3mm QFN Package and 8-lead SOICE package

APPLICATIONS

- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Printers and LCD TVs
- Network and Telecom Equipment
- Point of Load Regulators

TYPICAL APPLICATION





ORDERING INFORMATION

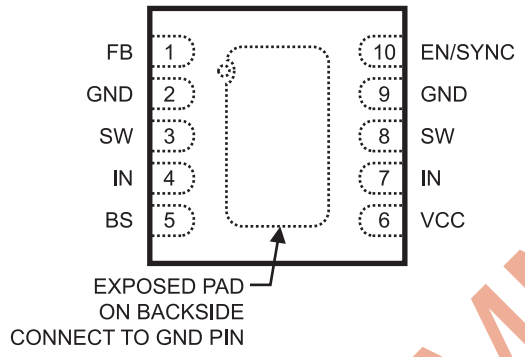
Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2212DQ*	QFN10 (3mm x 3mm)	Z7	-40°C to +85°C
MP2212DN**	SOIC8E	MP2212DN	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2212DQ–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2212DQ–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP2212DN–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2212DN–LF–Z)

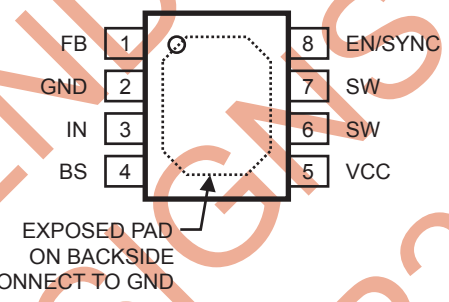
PACKAGE REFERENCE

TOP VIEW



QFN10 (3mm x 3mm)

TOP VIEW



SOIC8E

ABSOLUTE MAXIMUM RATINGS (1)

IN to GND ..... -0.3V to +18V
SW to GND ..... -0.3V to V_{IN} + 0.3V
..... -2.5V to V_{IN} + 2.5V for < 50ns
FB, EN/SYNC, VCC to GND ..... -0.3V to +6.5V
BS to SW ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN10 (3mm x 3mm) 2.5W
SOIC8E 2.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 3V to 16V
Bias Voltage V_{CC} ..... 3V to 6V
EN/SYNC Voltage ..... no more than V_{CC}
Output Voltage V_{OUT} ..... 0.8V to 0.9x V_{IN}
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN10 (3mm x 3mm)	50	12	°C/W
SOIC8E	50	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{CC} = 3.6V, V_{IN}=12V, T_A = +25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
VCC Supply Current	V_{EN} = VCC V_{FB} = 0.85V		750		µA
VCC Shutdown Current	V_{EN} = 0V, V_{CC}= 6V		1		µA
VCC Under Voltage Lockout Threshold	Rising Edge		2.8	3	V
VCC Under Voltage Lockout Hysteresis			200		mV
IN Shutdown Current	V_{EN} = 0V		4		µA
IN Under Voltage Lockout Threshold, Rising Edge			2.85	2.95	V
IN Under Voltage Lockout Hysteresis			300		mV
Regulated FB Voltage	T_A = +25°C	0.780	0.800	0.820	V
	-40°C ≤ TA ≤ +85°C	0.772		0.828	V
FB Input Current	V_{FB} = 0.85V	-50		50	nA
EN High Threshold	-40°C ≤ T_A ≤ +85°C	1.6			V
EN Low Threshold	-40°C ≤ T_A ≤ +85°C			0.4	V
Internal Soft-Start Time			120		µs
High-Side Switch On-Resistance	I_{SW} = 300mA		80		mΩ
Low-Side Switch On-Resistance	I_{SW} = –300mA		80		mΩ
SW Leakage Current	V_{EN} = 0V; V_{IN} = 12V V_{SW} = 0V or 12V	-10		10	µA
BS Under Voltage Lockout Threshold			1.8		V
High-Side Switch Current Limit	Sourcing		6		A
Low-Side Switch Current Limit	Sinking		3		A
Oscillator Frequency		450	600	750	kHz
Synch Frequency		0.5		2	MHz
Minimum On Time			50		ns
Maximum Duty Cycle			90		%
Thermal Shutdown Threshold	Hysteresis = 20°C		150		°C

Note:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

PIN FUNCTIONS

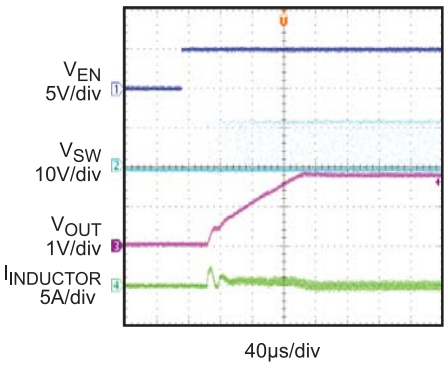
8-SOICE Pin #	10-QFN Pin #	Name	Description
5	6	VCC	Bias Supply. This supplies power to both the internal control circuit and the gate drivers. A decoupling capacitor to ground is required close to this pin.
3	4, 7	IN	Input Supply. This supplies power to the high side switch. A decoupling capacitor to ground is required close to this pin to reduce switching spikes.
6，7	3, 8	SW	Switch Node Connection to the Inductor. These pins connect to the internal high and low-side power MOSFET switches. All SW pins must be connected together externally.
2	2, 9	GND, Exposed Pad	Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors. Connect Exposed Pad and GND pin to the same plane.
4	5	BS	Bootstrap. A capacitor between this pin and SW provides a floating supply for the high-side gate driver.
1	1	FB	Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal 0.8V reference to set the regulation voltage.
8	10	EN/SYNC	Enable and Frequency Synchronization Input Pin. Forcing this pin below 0.4V shuts down the part. Forcing this pin above 1.6V but no more than V_{CC} turns on the part. Attach to V_{CC} with a 100kΩ pull up resistor for automatic start-up. Applying a 500kHz to 2MHz clock signal to this pin synchronizes the internal oscillator frequency to the external source. Don't apply a voltage more than V_{CC} to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, V_{OUT} = 1.8V, T_A = +25°C, unless otherwise noted.

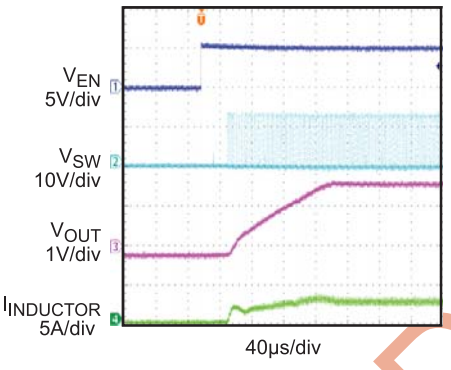
Enable Startup

V_{IN}=12V, I_{OUT}=0A



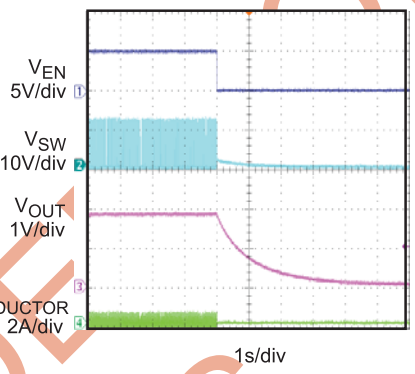
Enable Startup

V_{IN}=12V, I_{OUT}=3A



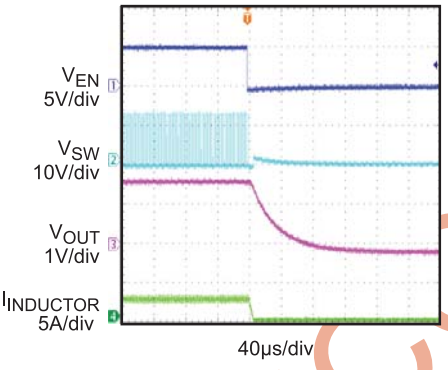
Enable Shut Down

V_{IN}=12V, I_{OUT}=0A



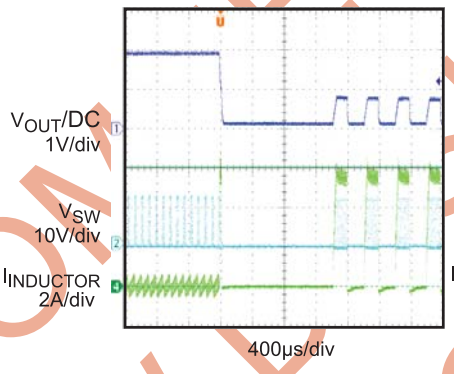
Enable Shut Down

V_{IN}=12V, I_{OUT}=3A



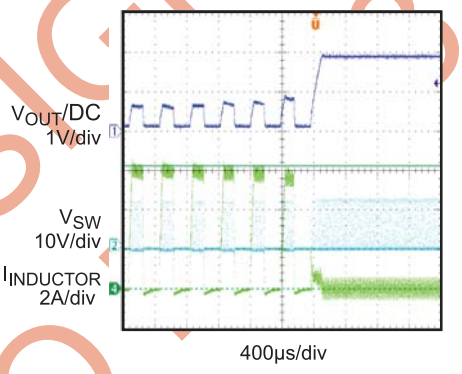
Short Circuit Protection

V_{IN}=12V



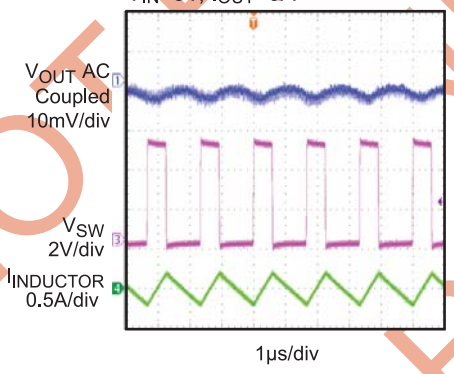
Short Circuit Recovery

V_{IN}=12V



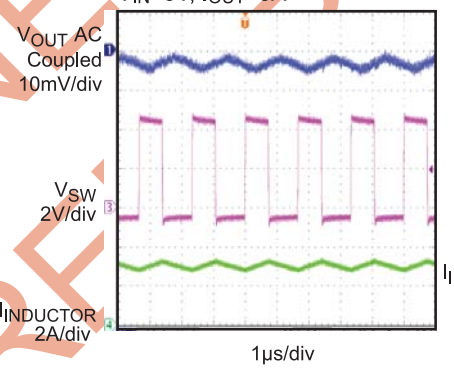
Switching Waveform

V_{IN}=5V, I_{OUT}=0A



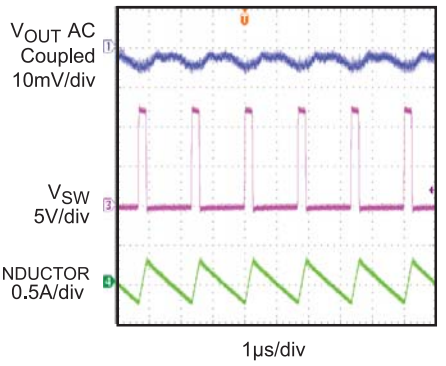
Switching Waveform

V_{IN}=5V, I_{OUT}=3A



Switching Waveform

V_{IN}=12V, I_{OUT}=0A

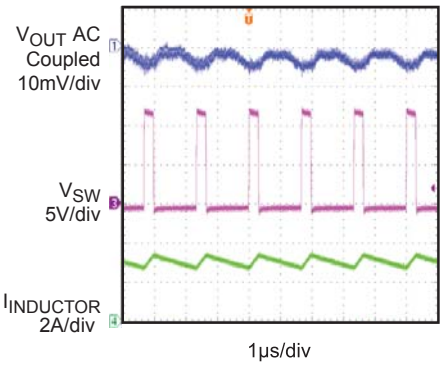


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, V_{OUT} = 1.8V, T_A = +25°C, unless otherwise noted (*continued*)

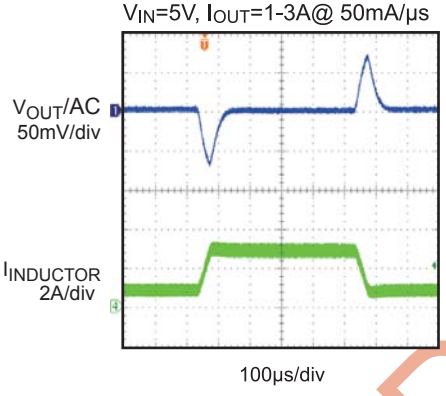
Switching Waveform

V_{IN}=12V, I_{OUT}=3A



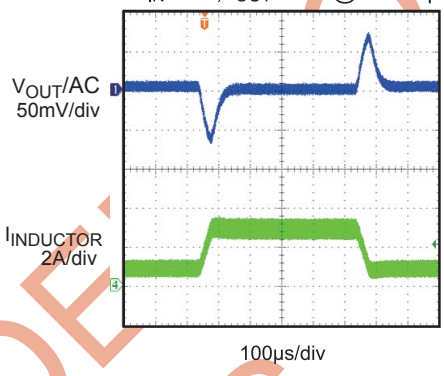
Load Transient

V_{IN}=5V, I_{OUT}=1-3A@ 50mA/µs



Load Transient

V_{IN}=12V, I_{OUT}=1-3A@ 50mA/µs



FUNCTIONAL BLOCK DIAGRAM

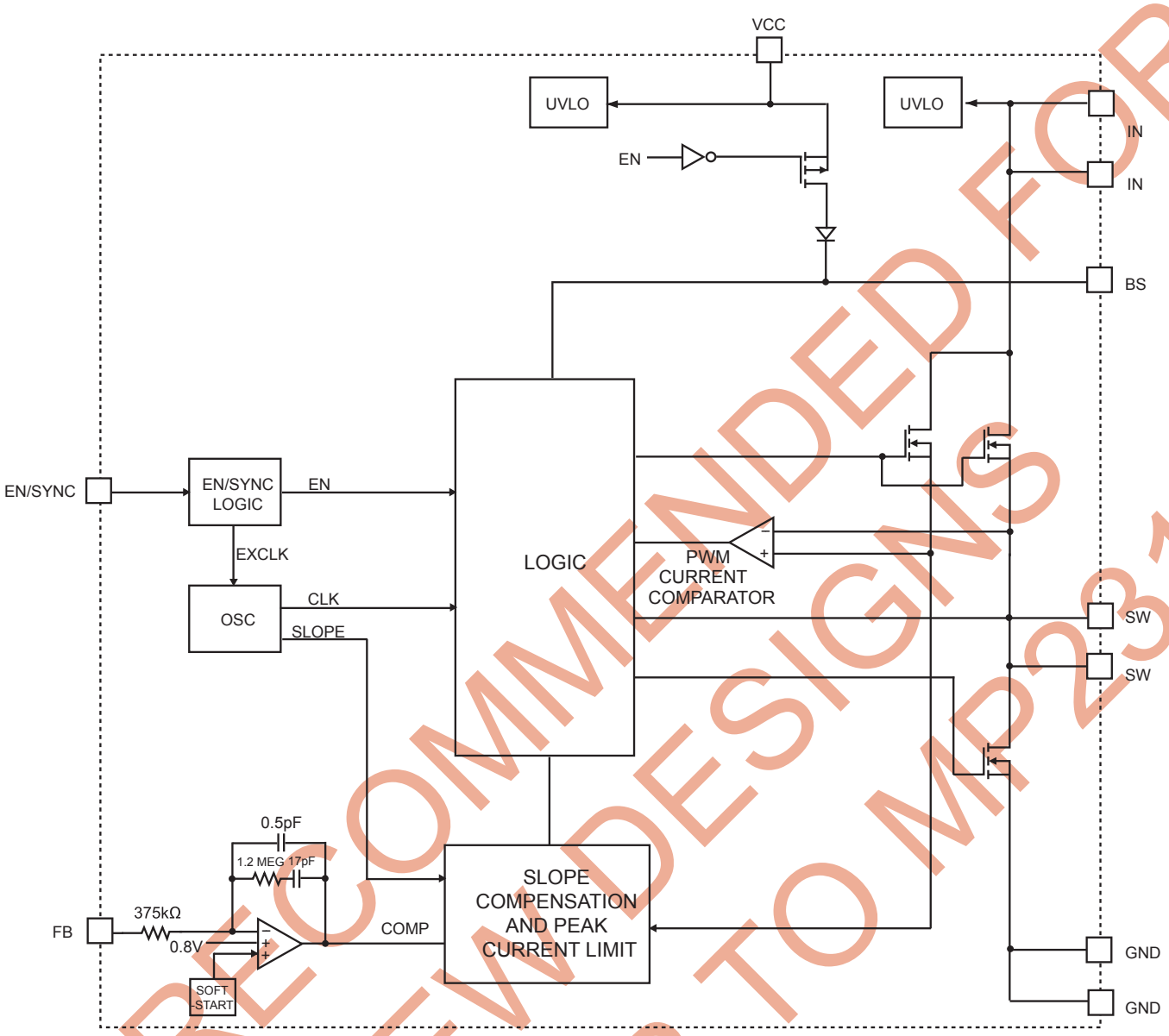


Figure 1—Functional Block Diagram

FUNCTIONAL DESCRIPTION

PWM Control

The MP2212 is a constant frequency peak-current-mode control PWM switching regulator. Refer to the functional block diagram. The high side N-Channel DMOS power switch turns on at the beginning of each clock cycle. The current in the inductor increases until the PWM current comparator trips to turn off the high side DMOS switch. The peak inductor current at which the current comparator shuts off the high side power switch is controlled by the COMP voltage at the output of feedback error amplifier. The transconductance from the COMP voltage to the output current is set at 11.25A/V.

This current-mode control greatly simplifies the feedback compensation design by approximating the switching converter as a single-pole system. Only Type II compensation network is needed, which is integrated into the MP2212. The internal compensation in the MP2212 simplifies the compensation design, minimizes external component counts. The loop bandwidth can be adjusted by adding a feed-forward capacitor which is in parallel with the feedback resistor from output to FB pin.

Enable and Frequency Synchronization (EN/SYNC PIN)

This is a dual function input pin. Forcing this pin below 0.4V for longer than 4μs shuts down the part; forcing this pin above 1.6V for longer than 4μs turns on the part. Applying a 500kHz to 2MHz clock signal to this pin also synchronizes the internal oscillator frequency to the external clock. When the external clock is used, the part turns on after detecting the first few clocks regardless of duty cycles. If any ON or OFF period of the clock is longer than 4μs, the signal will be intercepted as an enable input and disables the synchronization. For automatic startup, connect this pin to V_{CC} with a pull-up resistor. Don't apply a voltage more than V_{CC} to this pin.

Soft-Start and Output Pre-Bias Startup

When the soft-start period starts, an internal current source begins charging an internal soft-start capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V.

At this point the reference voltage takes over at the non-inverting error amplifier input. The soft-start time is internally set at 120μs. If the output of the MP2212 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Over Current Protection

The MP2212 offers cycle-to-cycle current limiting for both high-side and low-side switches. The high-side current limit is relatively constant regardless of duty cycles. When the output is shorted to ground, causing the output voltage to drop below 50% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. It will restart with a full soft-start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Bootstrap (BST PIN)

The gate driver for the high-side N-channel DMOS power switch is supplied by a bootstrap capacitor connected between the BS and SW pins. When the low-side switch is on, the capacitor is charged through an internal boost diode. When the high-side switch is on and the low-side switch turns off, the voltage on the bootstrap capacitor is boosted above the input voltage and the internal bootstrap diode prevents the capacitor from discharging.

Input UVLO

Both VCC and IN pins have input UVLO detection. Until both VCC and IN voltage exceed under voltage lockout threshold, the parts remain in shutdown condition. There are also under voltage lockout hysesteres at both VCC and IN pins.

VCC Power Supply

V_{CC} is the power supply of both the internal control circuit and the gate drivers.

Generally, the V_{CC} power supply could be provided directly by a proper power rail or generated from other V_{CC} generation circuits. For instance, Figure6 shows a typical V_{CC} generation circuit for VOUT=5V application.

It is noteworthy that the voltage applied on the V_{CC} pin should never be higher than 6V.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Figure 1). For typical applications, choose R2 to be 10k Ω. R1 is then given by:

$$R1 = R2 \times (\frac{V_{OUT}}{0.8V} - 1)$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (ceramic)
1.2	5	10	1μH-4.7μH	47μF
1.5	8.75	10	1μH-4.7μH	47μF
1.8	12.5	10	1μH-4.7μH	47μF
2.5	21.25	10	1μH-4.7μH	47μF
3.3	31.25	10	1μH-4.7μH	47μF

Feed-forward capacitor

For applications with V_{OUT} other than 0.8V, adding a feed-forward capacitor in parallel with the feedback resistor from output to FB pin can increase loop bandwidth, help reducing transient overshoot and undershoot and startup overshoot if any. Figure 2 shows typical 5 V_{OUT} application circuit with a 390pF feed-forward capacitor.

Selecting the Inductor

A 1μH to 4.7μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <10mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x \Delta I_L x f_{OSC}}$$

where ΔI_L is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current, 3A.The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved efficiency

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47μF capacitor is sufficient.

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance (μH)	Max DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm3)
TOKO					
	FDA1055-3R3M	3.3	7.3	11.7	10.8x11.6x5.5
Wurth Electronics					
	744314330	3.3	9.6	8	7x6.9x5
TDK					
	ULF100457-3R3N6R9	3.3	11.6	7.5	10x9.7x4.5

Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. If electrolytic capacitor is used, pay attention to output ripple voltage, extra heating, and the selection of feedback resistor R1 (refer to "Output Voltage Setting" section) due to large ESR of electrolytic capacitor. The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x f_{OSC} x L} x (ESR + \frac{1}{8 x f_{OSC} x C3})$$

The output capacitance is recommended to be less than 100μF.

External Schottky Diode

For this part, an external schottky diode is recommended to be placed close to "SW" and "GND" pins, especially when the output current is larger than 2A.

With the external schottky diode, the voltage spike and negative kick on "SW" pin can be minimized; moreover, the conversion efficiency can also be improved a little.

For the external schottky diode selection, it's noteworthy that the maximum reverse voltage rating of the external diode should be larger than the maximum input voltage. As for the current rating of this diode, 0.5A rating should be sufficient.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines as follows. Here, the typical application circuit is taken as an example to illustrate the key layout rules should be followed.

1) For MP2212DQ, a PCB layout with more than (or) four layers is recommended.

2) The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces.

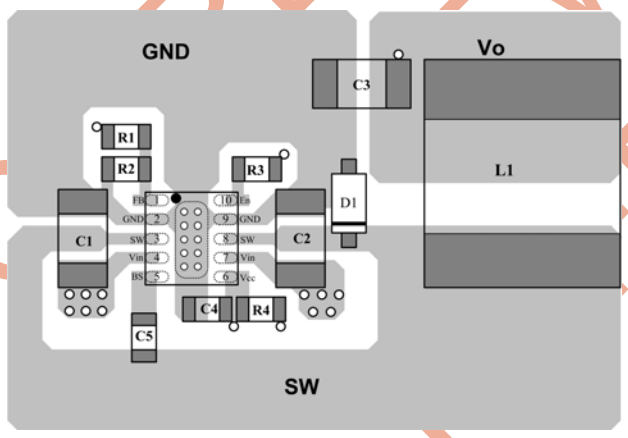
3) For MP2212DQ, two input ceramic capacitors (2 x (10μF~22μF)) are strongly recommended to be placed on both sides of the MP2212DQ package and keep them as close as possible to the "IN" and "GND" pins.

For MP2212DN, an input ceramic capacitor should be placed as close as possible to "IN" and "GND" pins.

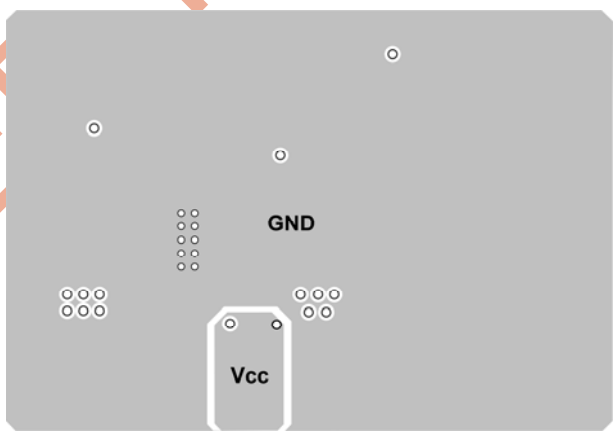
4) A RC low pass filter is recommended for VCC supply. The V_{CC} decoupling capacitor must be placed as close as possible to "VCC" pin and "GND" pin.

5) The external feedback resistors shall be placed next to the FB pin. Keep the FB trace as short as possible.

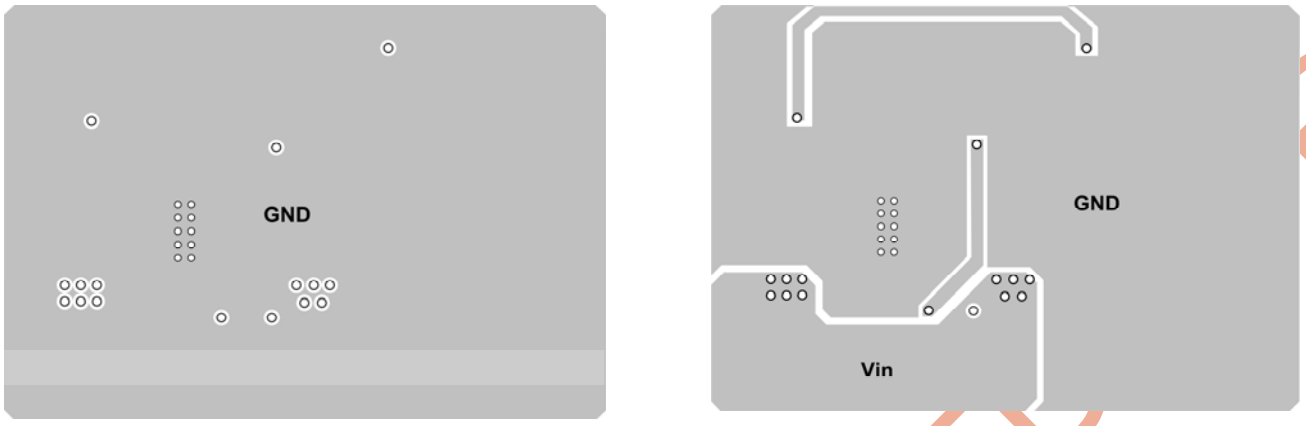
6) Keep the switching node SW short and away from the feedback network.



Top Layer

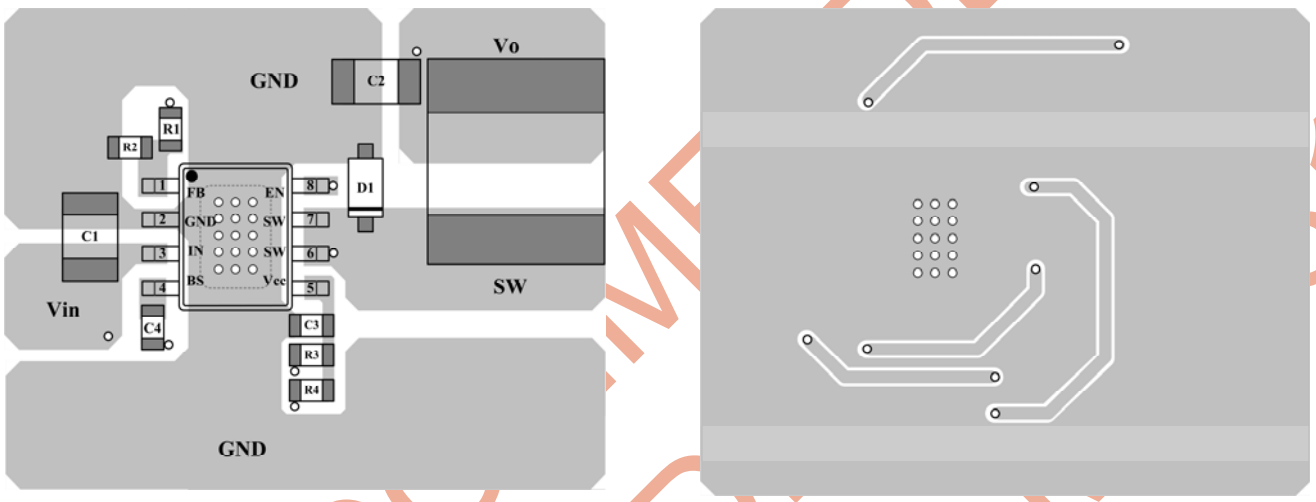


Inner Layer1



Inner Layer2 Bottom Layer

Figure2—Recommended PCB Layout of MP2212DQ



Top Layer Bottom Layer

Figure 3—Recommended PCB Layout of MP2212DN

TYPICAL APPLICATION CIRCUITS

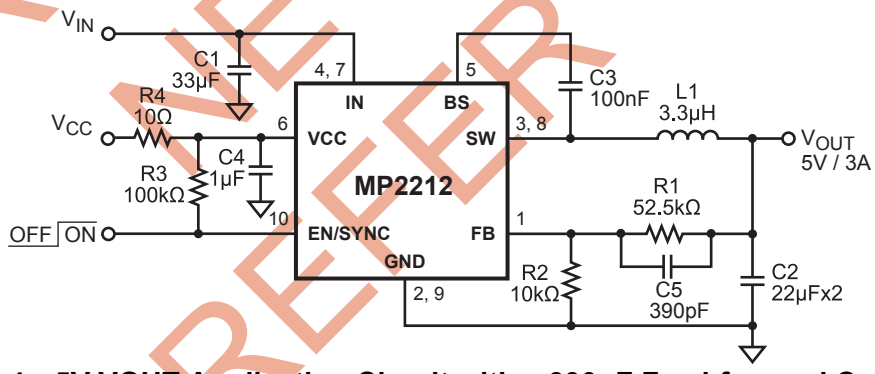


Figure 4—5V VOUT Application Circuit with a 390pF Feed-forward Capacitor

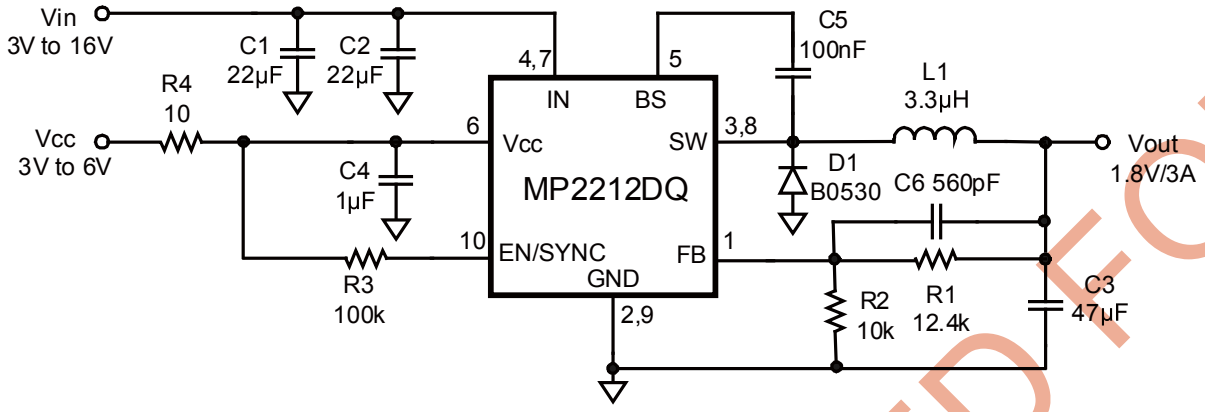


Figure 5—Typical Application Circuit of MP2212DQ

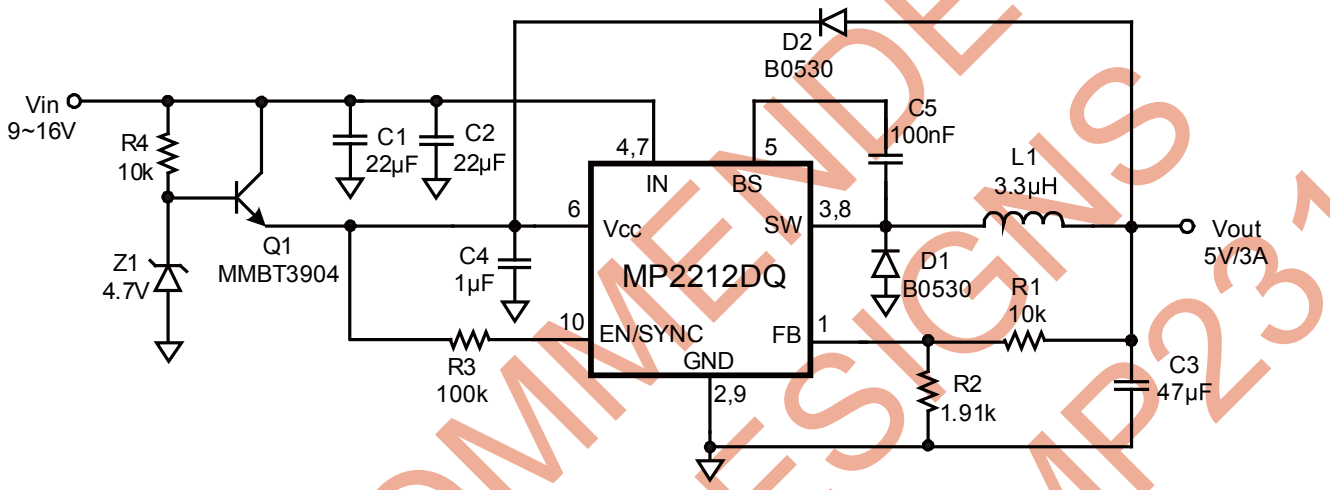


Figure6—MP2212DQ with A V_{cc} Generation Circuit

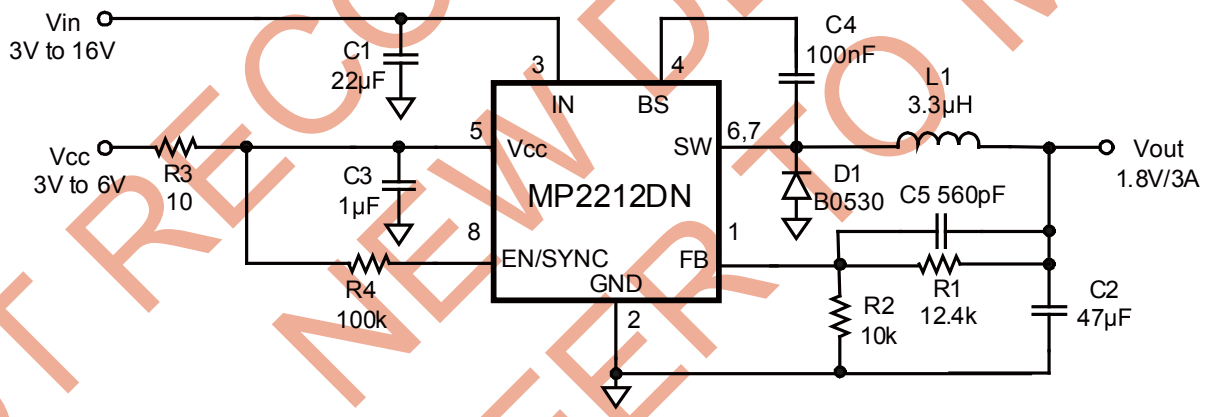
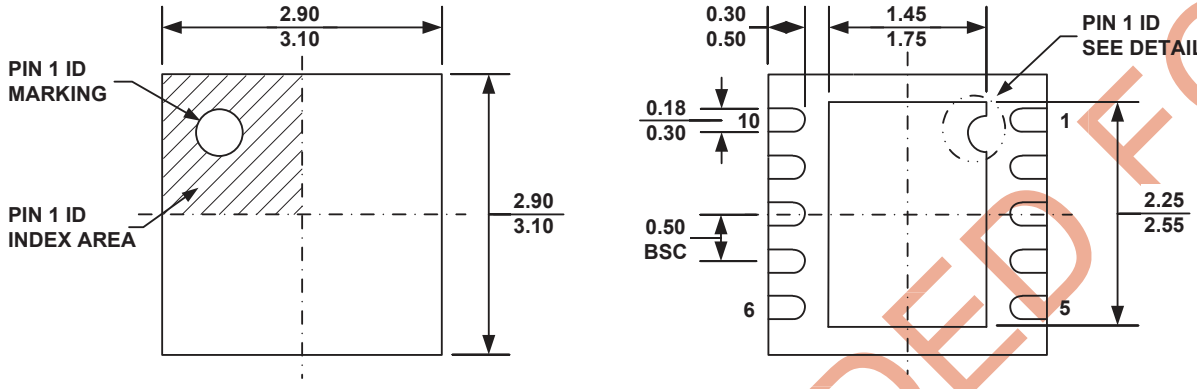


Figure 7 —Typical Application Circuit of MP2212DN

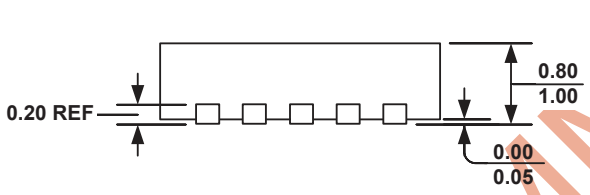
PACKAGE INFORMATION

QFN10 (3mm x 3mm)

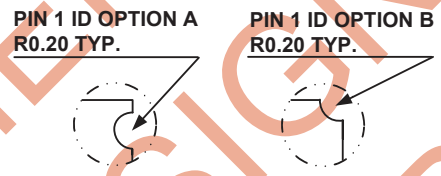


TOP VIEW

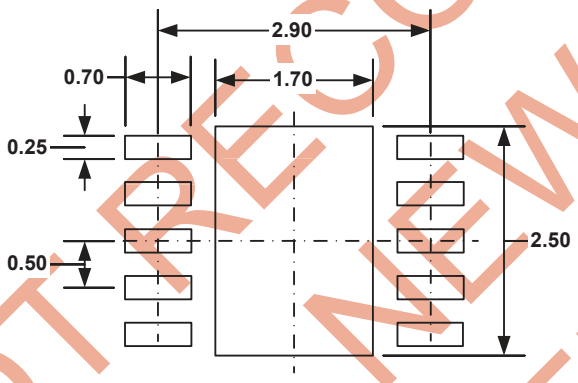
BOTTOM VIEW



SIDE VIEW



DETAIL A

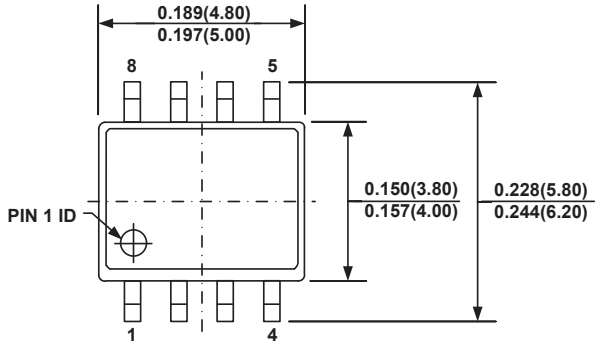


RECOMMENDED LAND PATTERN

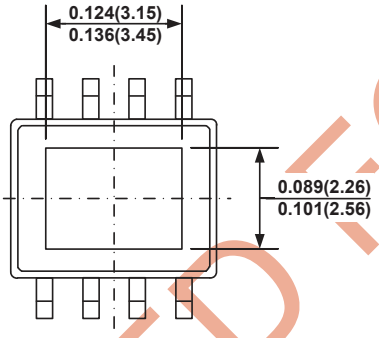
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

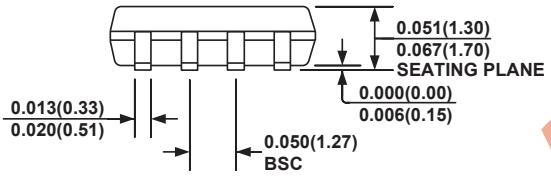
SOIC8E (EXPOSED PAD)



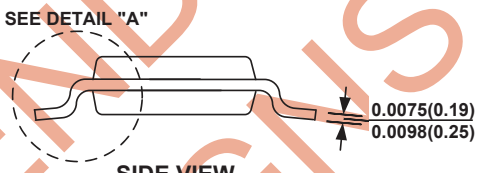
TOP VIEW



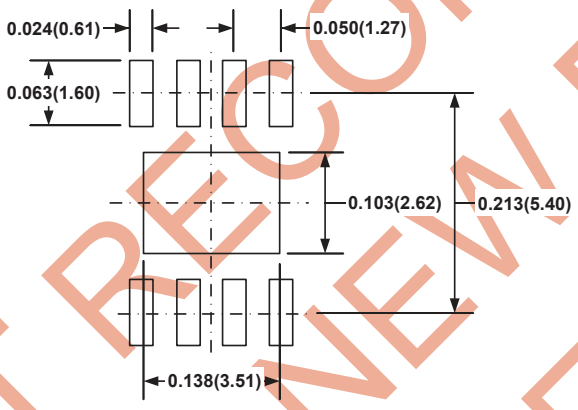
BOTTOM VIEW



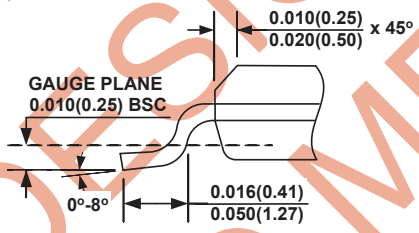
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.