ISM Band FSK Receiver IC

ADF7902

FEATURES

Single-chip, low power UHF receiver
Companion receiver to ADF7901 transmitter
Frequency range: 369.5 MHz to 395.9 MHz
Eight RF channels selectable with three digital inputs
Modulation parameters supported
- **FSK demodulation**
- **2 kbps data rate**
- **34.8 kHz frequency deviation**

5.0 V supply voltage
Low power consumption
- **18.5 mA with receiver enabled**
- **1 µA standby current**

24-lead TSSOP

GENERAL DESCRIPTION

The ADF7902 is a low power UHF receiver. The device demodulates frequency shift keyed (FSK) signals with 34.8 kHz frequency deviation and at data rates of up to 2 kbps. There are eight specific RF channels ranging from 369.5 MHz to 395.9 MHz on which the receiver can operate. Each channel is selectable by configuring three digital control lines.

The ADF7902 is designed for low power applications, consuming 18.5 mA (typical) during normal operation and 1 µA (maximum) in standby mode.

FUNCTIONAL BLOCK DIAGRAM

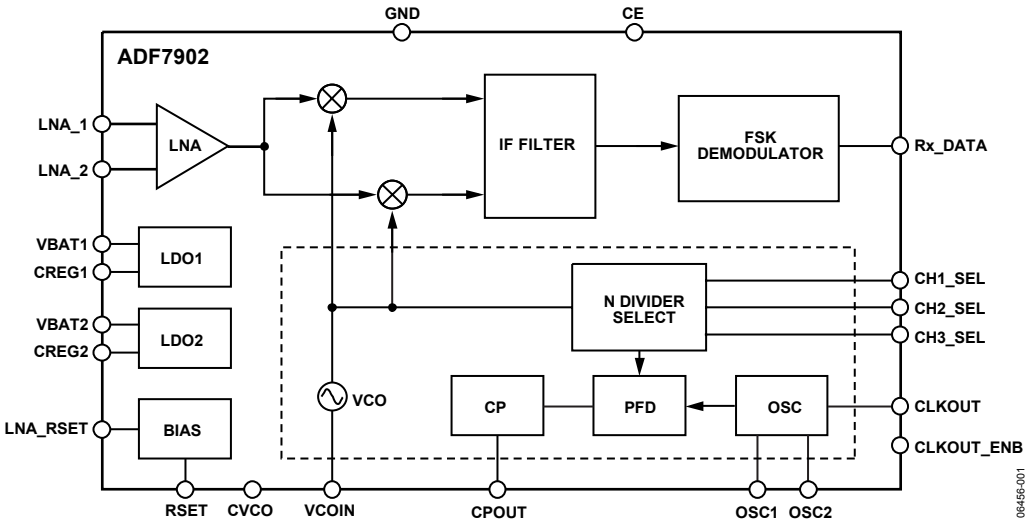

Figure 1.

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REVISION HISTORY

1/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} =5.0 V; GND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications T_A = 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
CHANNEL FREQUENCIES					
Channel 1		369.5		MHz	
Channel 2		371.1		MHz	
Channel 3		375.3		MHz	
Channel 4		376.9		MHz	
Channel 5		388.3		MHz	
Channel 6		391.5		MHz	
Channel 7		394.3		MHz	
Channel 8		395.9		MHz	
RECEIVER PARAMETERS					
Data Rate		2		kbps	
Frequency Deviation		−34.8		kHz	Data = 0
		+34.8		kHz	Data = 1
Input Sensitivity		−110		dBm	
LNA Input Impedance		128 − j125		Ω	f_{RF} = 388.3 MHz
CHANNEL FILTERING					
IF Filter Bandwidth		200		kHz	−3 dB bandwidth
Adjacent Channel Rejection		60		dB	1 MHz offset Desired signal 3 dB above input sensitivity level, with interferer power increased until BER = 10^{-3}
PHASE-LOCKED LOOP					
CE High to Receive Data		4		ms	
REFERENCE INPUT					
Crystal Reference		9.8304		MHz	±25 ppm frequency accuracy
INPUT LOGIC LEVELS					
Input High Voltage, V_{IH}	0.7 × V_{DD}			V	
Input Low Voltage, V_{IL}			0.2 × V_{DD}	V	
OUTPUT LOGIC LEVELS					
Output High Voltage, V_{OH}	4.5			V	
Output Low Voltage, V_{OL}			0.4	V	
Output Drive Level			2	mA	
POWER SUPPLY					
Voltage Supply					
V_{DD}		5		V	
Current Consumption					
Receiver Enabled		18.5		mA	CE = 1
Low Power Sleep Mode			1	µA	CE = 0

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
VBAT to GND[1]	−0.3 V to +6.0 V
Digital I/O Voltage to GND	−0.3 V to VBAT + 0.3 V
LNA_1, LNA_2	0 dBm
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−40°C to +125°C
Maximum Junction Temperature	125°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	235°C
Infrared (15 sec)	240°C

[1] GND = GND1 = GND1B = GND2 = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

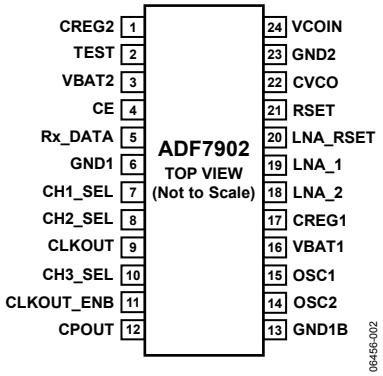

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CREG2	A 0.1 µF capacitor should be added at CREG2 to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time but may cause higher spurs.
2	TEST	Test Output Pin. Leave as no connect.
3	VBAT2	5 V Power Supply for RF Circuitry. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
4	CE	Chip Enable Input. Driving CE low puts the part into power-down mode, drawing <1 µA.
5	Rx_DATA	Receiver Output. Demodulated data appears on this pin.
6	GND1	Ground for Digital Circuitry.
7	CH1_SEL	Channel Select Pin. This represents the LSB of the channel select pins.
8	CH2_SEL	Channel Select Pin.
9	CLKOUT	Square Wave Clock Output at the Crystal Frequency. This can be used to drive the OSC2 pin of a partnering ADF7902. The output has a 50:50 mark-space ratio and switches between 0 V and 2.2 V. If CLKOUT is disabled by setting Pin 11 high, then CLKOUT must be tied low.
10	CH3_SEL	Channel Select Pin.
11	CLKOUT_ENB	CLKOUT Enable Input. This should be driven low to enable the reference clock signal to appear on the CLKOUT pin. Driving the pin high removes the clock signal on CLKOUT. It should be driven high when an external reference is used.
12	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
13	GND1B	Ground for Digital Circuitry.
14	OSC2	The reference crystal should be connected between this pin and OSC1. The necessary crystal load capacitor should be tied between this pin and ground. A square wave signal can be applied to this pin as an external reference source.
15	OSC1	The reference crystal should be connected between this pin and OSC2. The necessary crystal load capacitor should be tied between this pin and ground. This pin should be connected to ground when OSC2 is driven by an external reference.
16	VBAT1	5 V Power Supply for Digital Circuitry. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
17	CREG1	A 0.1 µF capacitor should be added at CREG1 to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time but may cause higher spurs.
18	LNA_2	LNA Input. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer.
19	LNA_1	Complementary LNA Input.
20	LNA_RSET	External Bias Resistor for LNA. A value of 1.1 kΩ is recommended.
21	RSET	External Resistor to Set Charge Pump Current and Some Internal Bias Currents. A value of 3.6 kΩ is recommended.
22	CVCO	Voltage Controlled Oscillator (VCO) Capacitor. A 22 nF capacitor should be placed between this pin and CREG2 to reduce VCO noise.
23	GND2	Ground for RF Circuitry.
24	VCOIN	The tuning voltage on this pin determines the output frequency of the VCO. The higher the tuning voltage, the higher the output frequency. The output of the loop filter is connected here.

TYPICAL PERFORMANCE CHARACTERISTICS

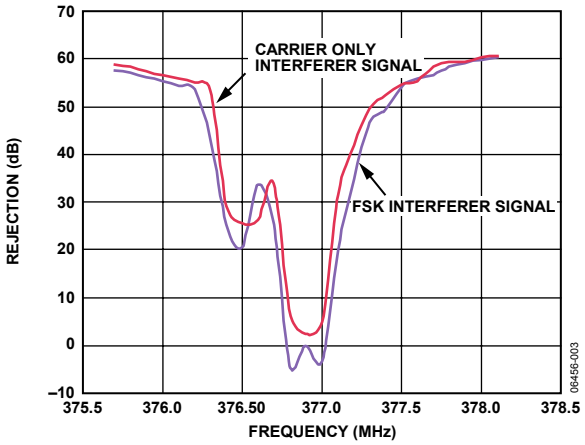

Figure 3. Narrow-Band Interference Rejection Plot

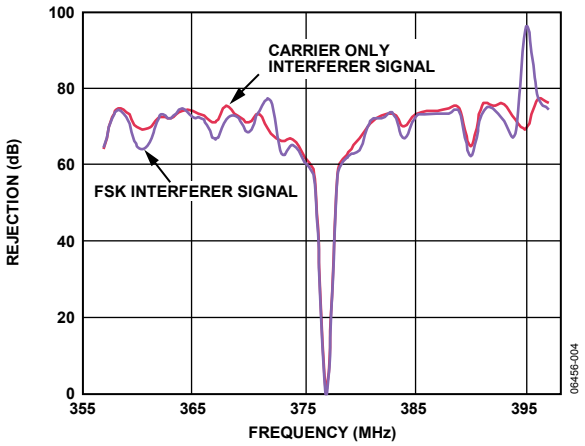

Figure 4. Wideband Interference Rejection Plot

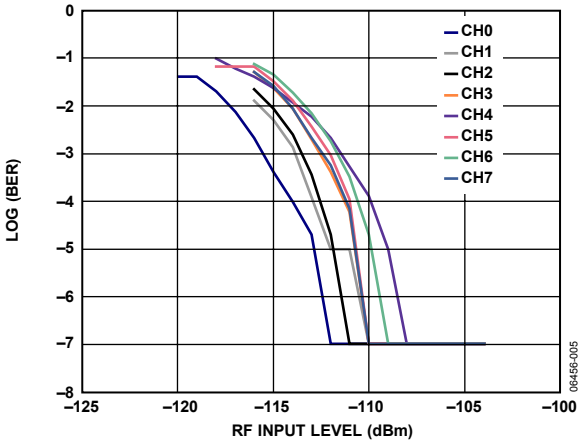

Figure 5. Sensitivity Plot

APPLICATIONS INFORMATION

Table 4. Channel Frequency Truth Table

CH1_SEL	CH2_SEL	CH3_SEL	Channel Frequency (MHz)
0	0	0	369.5
1	0	0	371.1
0	0	1	375.3
1	1	0	376.9
0	1	0	388.3
1	0	1	391.5
0	1	1	394.3
1	1	1	395.9

APPLICATIONS CIRCUITS

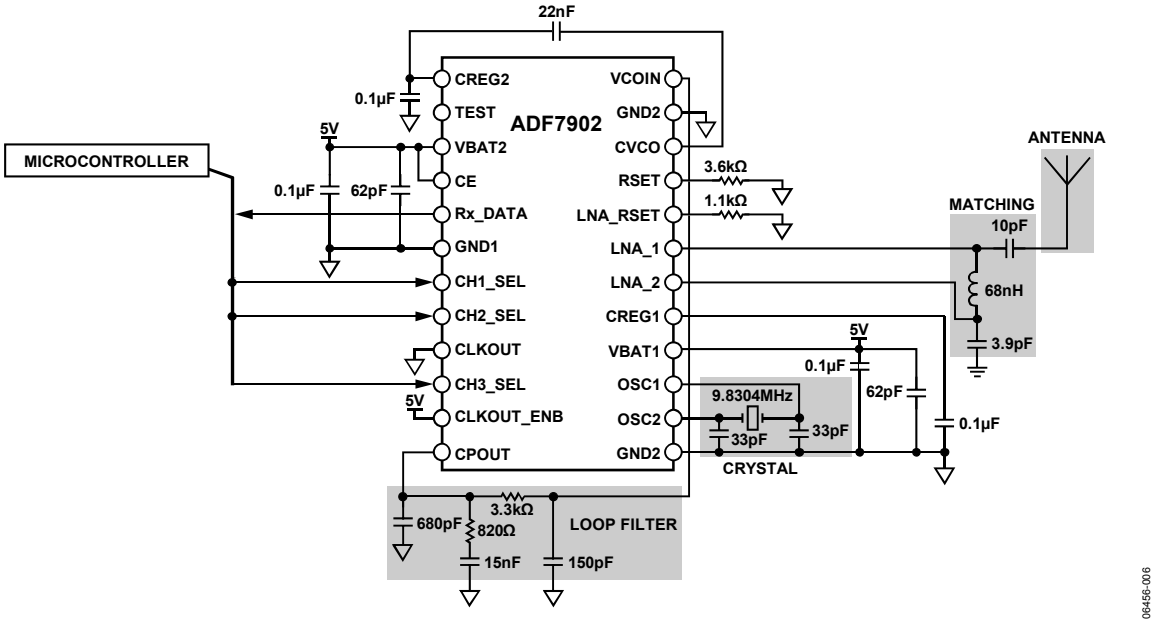

Figure 6. Single Receiver Applications Circuit

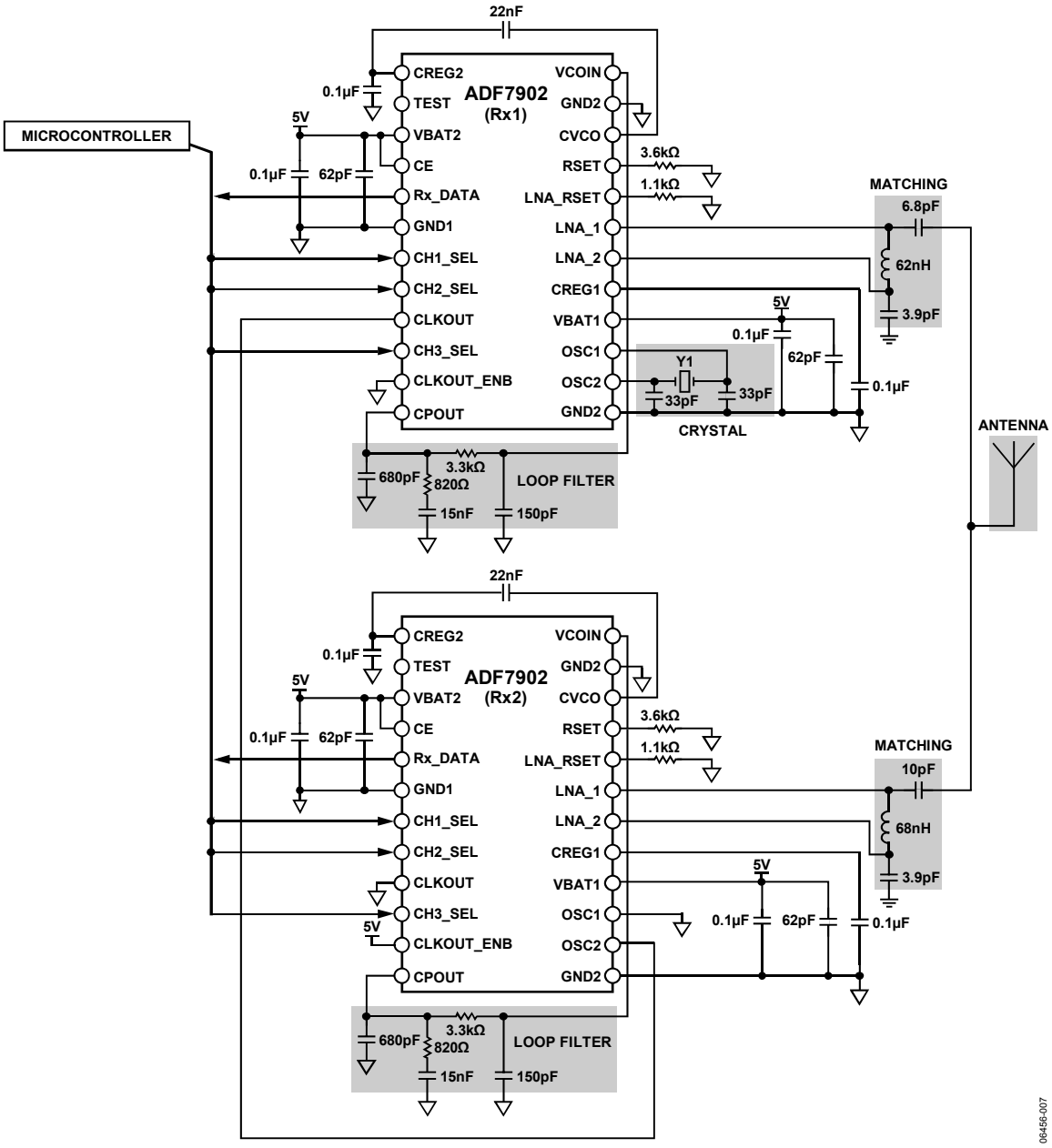

Figure 7. Dual Receiver Applications Circuit

TEST MODES

If CLKOUT_ENB is tied high, CLKOUT is disabled. The CLKOUT pin is reconfigured as a test enable input. If the CLKOUT pin is then tied low, the part operates as is normal with CLKOUT off. If it is tied high (2.2 V), the part is in test mode. Test mode is described in Table 5.

When CLKOUT_ENB = 0, RSSI appears on the test output pin (Pin 2), and CLKOUT is configured as an output with a 9.8 MHz clock coming out.

When test mode is enabled, the channel frequency is set to 369.5 MHz (Channel 1).

Table 5. Test Modes

CH1_SEL	CH2_SEL	CH3_SEL	Test Mode
0	0	0	agc gain is set to maximum (filti is also set to maximum on test output pin)
0	0	1	filti on test output pin
0	1	0	filtq on test output pin
0	1	1	Charge pump output is set to maximum (test pin is also tri-state)
1	0	0	Charge pump output is set to minimum (also n-divider output ÷ 2 on test output pin)
1	0	1	Charge pump is tri-state (test pin is also tri-state)
1	1	0	n-divider output ÷ 2 on test output pin
1	1	1	Recovered data clock on test output pin

OUTLINE DIMENSIONS

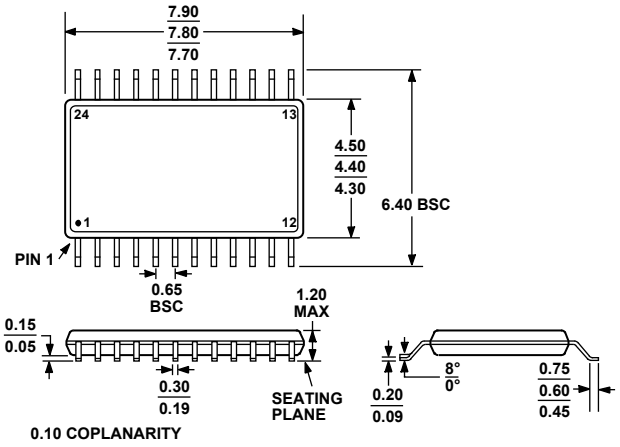

Figure 8. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7902BRUZ[1]	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADF7902BRUZ-RL[1]	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 13″ REEL	RU-24
ADF7902BRUZ-RL7[1]	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 7″ REEL	RU-24

[1] Z = Pb-free part.

NOTES

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