Programmable High-Frequency Crystal Oscillator (XO)

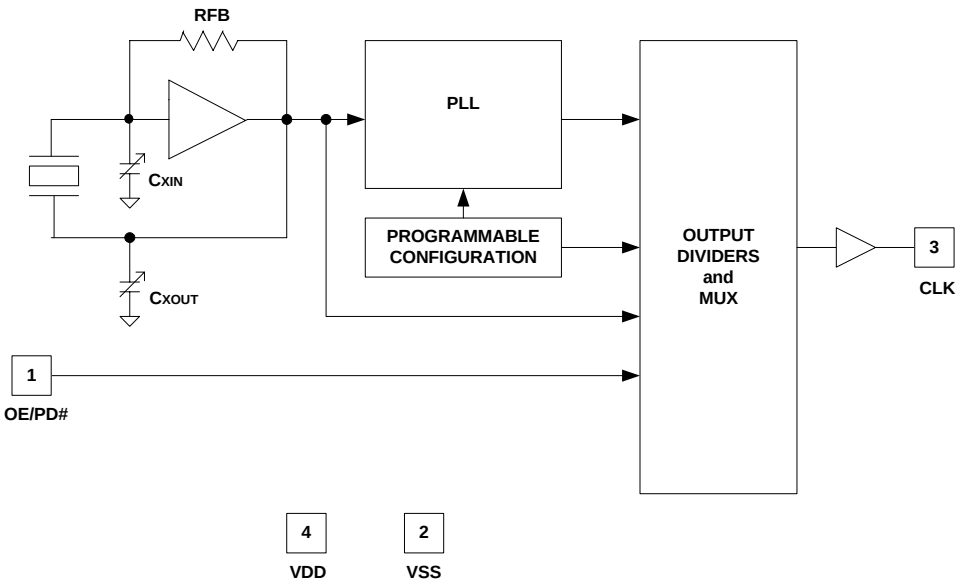
Features

- Programmable High-frequency Crystal Oscillator (XO)
- Wide operating output clock frequency range of 1–166 MHz
- Integrated phase-locked loop (PLL)
- 85 ps typical cycle-to-cycle Jitter with CLK = 133 MHz
- 3.3V operation
- Output Enable and Power-down functions
- Package available in 4-Pin Ceramic LCC SMD
- Pb-free package
- Industrial Temperature from –40°C to 85°C
- For SSCG functionality refer to CY25701 data sheet

Benefits

- Internal PLL to generate up to 166 MHz output
- Suitable for most PC, consumer, and networking applications
- Application compatibility in standard and low-power systems
- CY25701 can be used as a direct replacement without any PCB modification if spread spectrum clock (SSC) is required for EMI reduction.
- In-house programming of samples and prototype quantities is available using CY3672 programming kit and CY3724 socket adapters. Production quantities are available through Cypress's value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others.

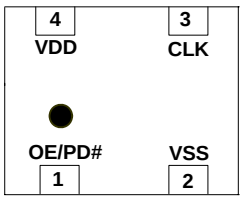
Logic Block Diagram



Pin Configuration

CY25702

4-pin Ceramic SMD



Pin Definition

Pin	Name	Description
1	OE/PD#	Output Enable pin: Active HIGH. If OE = 1, CLK is enabled. Power Down pin: Active LOW. If PD# = 0, Power Down is enabled.
2	VSS	Power supply ground.
3	CLK	Clock output.
4	VDD	3.3V power supply.

Table 1. Programming Data Requirement

Pin Function	Output Frequency	Output Enable/Power Down
Pin Name	CLK	OE/PD#
Pin#	3	1
Units	MHz	N/A
Program Value	**ENTER DATA**	**ENTER DATA**

Functional Description

The CY25702 is a programmable high-frequency Crystal Oscillator (XO) that uses a Cypress proprietary PLL to synthesize the frequency of the embedded input crystal.

The CY25702 uses a programmable configuration memory array to synthesize output frequency. The frequency CLK output can be programmed from 1 MHz to 166 MHz.

The CY25702 is available in a 4-pin ceramic SMD package with an operating temperature range of –40 to 85°C.

Programming Description

Field/Factory-Programmable CY25702

Field/Factory programming is available for samples and manufacturing by Cypress and its distributors. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Additional information on the CY25702 can be obtained from the Cypress web site at www.cypress.com.

Output Frequency, CLK Output (CLK, pin 3)

The frequency at the CLK output is produced by synthesizing the embedded crystal oscillator frequency input. The range of the synthesized clock is from 1 MHz to 166 MHz.

Output Enable or Power Down (OE/PD#, pin 1)

Pin 1 can be programmed as either output enable (OE) or Power Down (PD#).

Absolute Maximum Rating

Supply Voltage (V_{DD}).....–0.5V to +7.0V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V

Storage Temperature (Non-condensing) ..... –55°C to 100°C

Junction Temperature..... –40°C to 125°C

Data Retention @ Tj = 125°C.....> 10 years

Package Power Dissipation..... 350 mW

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.00	3.30	3.60	V
T_A	Ambient Temperature (Commercial)	–20	–	70	°C
T_A	Ambient Temperature (Industrial)	–40	–	85	°C
C_{LOAD}	Max. Load Capacitance @ pin 3	–	–	15	pF
F_{CLK}	CLK output frequency, C_{LOAD} = 15 pF	1	–	166	MHz
T_{PU}	Power-up time for VDD to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current (pin 3)	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V (source)	10	12	–	mA
I_{OL}	Output Low Current (pin 3)	V_{OL} = 0.5, V_{DD} = 3.3V (sink)	10	12	–	mA
V_{IH}	Input High Voltage (pin 1)	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	Input Low Voltage (pin 1)	CMOS levels, 30% of V_{DD}	–	–	$0.3V_{DD}$	V
I_{IH}	Input High Current (pin 1)	$V_{in} = V_{DD}$	–	–	10	µA
I_{IL}	Input Low Current (pin 1)	$V_{in} = V_{SS}$	–	–	10	µA
I_{OZ}	Output Leakage Current (pin 3)	Three-state output, OE = 0	–10	–	10	µA
C_{IN}[1]	Input Capacitance (pin 1)	Pin 1, or OE	–	5	7	pF
I_{VDD}	Supply Current	V_{DD} = 3.3V, CLK = 1 to 166 MHz, C_{LOAD} = 0, OE = V_{DD}	–	–	50	mA
Δf/f	Initial Accuracy at Room Temp.	T_A = 25°C, 3.3V	–25	–	25	ppm
	Freq. Stability over Temp. Range	T_A = –20°C to 70°C, 3.3V	–25	–	25	ppm
	Freq. Stability over Voltage Range	3.0 to 3.6V	–12	–	12	ppm
	Aging	T_A = 25°C, First year	–5	–	5	ppm

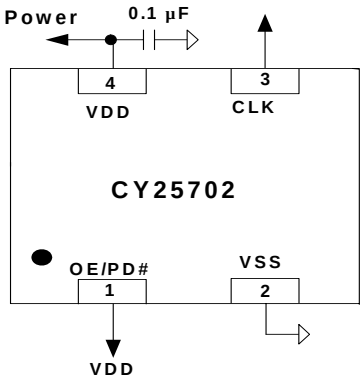
AC Electrical Characteristics[1]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	CLK, Measured at $V_{DD}/2$	45	50	55	%
t_R	Output Rise Time	20%–80% of V_{DD}, C_L=15 pF	–	–	2.7	ns
t_F	Output Fall Time	20%–80% of V_{DD}, C_L=15 pF	–	–	2.7	ns
T_{CCJ1}[2]	Cycle-to-Cycle Jitter CLK (Pin 3)	CLK ≥ 133 MHz, Measured at $V_{DD}/2$	–	85	200	ps
		25 MHz ≤ CLK < 133 MHz, Measured at $V_{DD}/2$	–	215	400	ps
		CLK < 25 MHz, Measured at $V_{DD}/2$	–	–	500	ps
T_{OE1}	Output Disable Time (pin1 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin1 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
T_{LOCK}	PLL Lock Time	Time for CLK to reach valid frequency	–	–	10	ms

Note
1. Guaranteed by characterization, not 100% tested.
2. Jitter is configuration dependent. Actual jitter is dependent on output frequencies, spread percentage, temperature, and output load. For more information, refer to the application note, “Jitter in PLL Based Systems: Causes, Effects, and Solutions” available at http://www.cypress.com/clock/appnotes.html, or contact your local Cypress Field Application Engineer.

Application Circuit

Figure 1. Application Circuit Diagram



Switching Waveforms

Figure 2. Duty Cycle Waveform

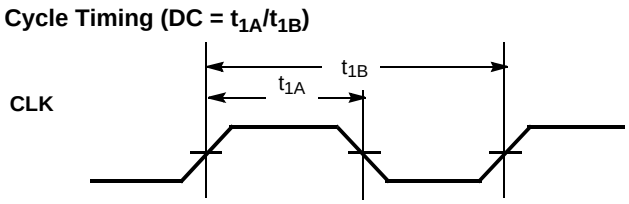
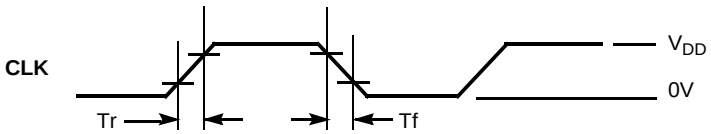
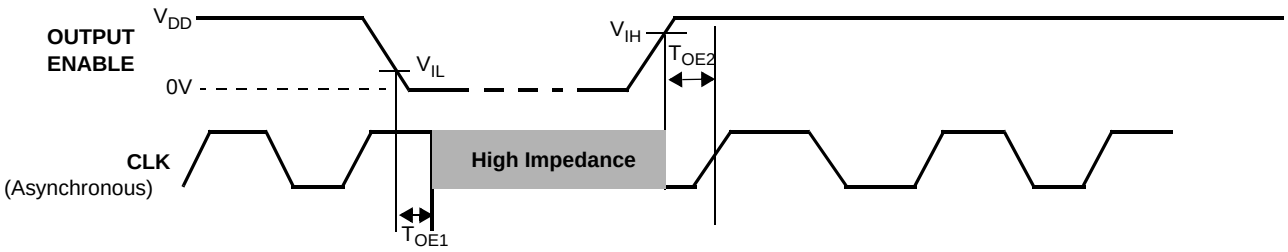


Figure 3. Output Rise/Fall Time Waveform



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 4. Output Enable/Disable Timing Waveforms

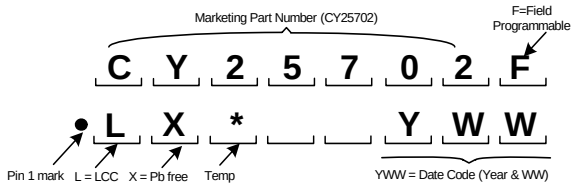


Ordering Information

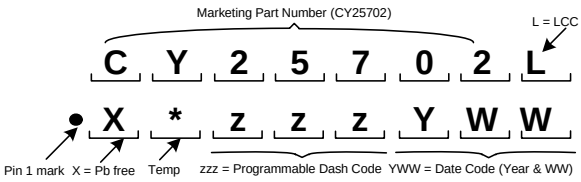
Part Number	Package Description	Product Flow
Lead-free (Pb-free)		
CY25702FLXCT[3]	4-Lead Ceramic LCC SMD -Tape and Reel	Commercial, –20° to 70°C
CY25702FLXIT[3]	4-Lead Ceramic LCC SMD -Tape and Reel	Industrial, –40° to 85°C
CY25702LXCZZZT[4]	4-Lead Ceramic LCC SMD -Tape and Reel	Commercial, –20° to 70°C
CY25702LXIZZZT[4]	4-Lead Ceramic LCC SMD -Tape and Reel	Industrial, –40° to 85°C

Actual Marking[5]

CY25702FLX*

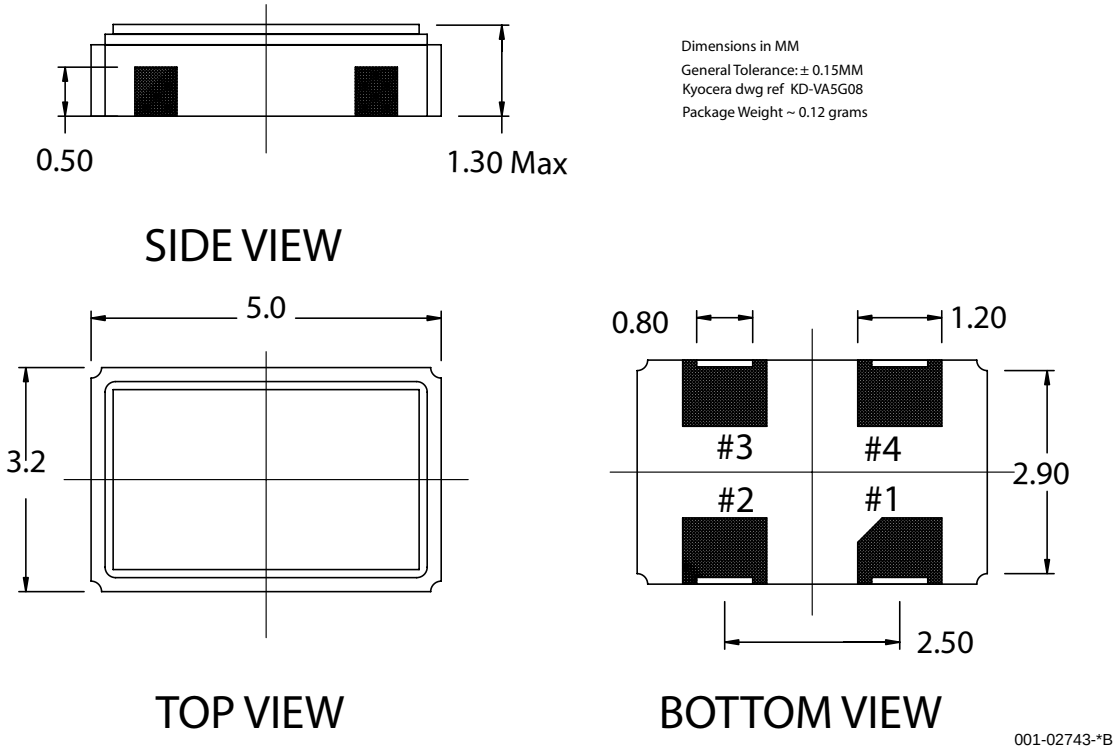


CY25702LX*



Package Drawings and Dimensions

Figure 5. 4-Lead (5.0x3.2 mm) Ceramic LCC LZ04A



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Notes
3. "FLX" suffix is used for products programmed in field by Cypress Distributors.
4. "ZZZ" denotes the assigned product dash number. This number will be assigned by factory after the output frequency programming data is received from the customer.
5. Temp can be C (Commercial) or I (Industrial).

Document History Page

Document Title: CY25702 Programmable High-Frequency Crystal Oscillator (XO) Document Number: 38-07721				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	296081	See ECN	RGL	New data sheet
*A	333298	See ECN	RGL	Added Jitter Specifications Corrected the Ordering Information table to match the DevMaster
*B	390406	See ECN	RGL	Removed CY25702FXC and CY25702XCZZZ
*C	595857	See ECN	RGL	Complete data sheet rewrite