

## N- and P-Channel 1.8 V (G-S) MOSFET

### PRODUCT SUMMARY

	$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	12	0.235 at $V_{GS} = 4.5$ V	1.3
		0.280 at $V_{GS} = 2.5$ V	1.2
		0.340 at $V_{GS} = 1.8$ V	1.0
P-Channel	- 12	0.535 at $V_{GS} = - 4.5$ V	- 0.86
		0.880 at $V_{GS} = - 2.5$ V	- 0.67
		1.26 at $V_{GS} = - 1.8$ V	- 0.56

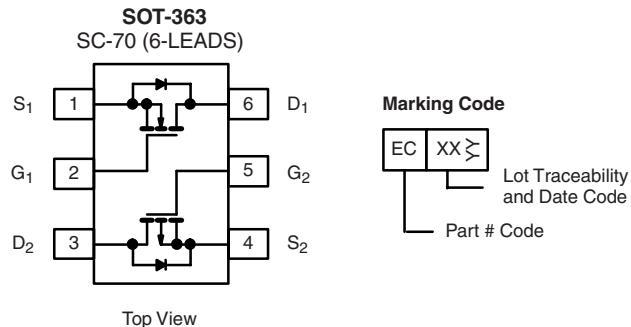
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Thermally Enhanced SC-70 Package
- Fast Switching to Minimize Gate and Switching Losses
- Compliant to RoHS Directive 2002/95/EC



### APPLICATIONS

- Baseband dc-to-dc Converter Switch for Portable Electronics



**Ordering Information:** Si1557DH-T1-E3 (Lead (Pb)-free)  
Si1557DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	N-Channel		P-Channel		Unit
		5 s	Steady State	5 s	Steady State	
Drain-Source Voltage	$V_{DS}$		12		- 12	V
Gate-Source Voltage	$V_{GS}$			$\pm 8$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	1.3	1.2	- 0.86	- 0.77	A
		0.9	0.8	- 0.62	- 0.55	
Pulsed Drain Current	$I_{DM}$	3		- 2		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	0.5	0.39	- 0.5	- 0.39	
Maximum Power Dissipation <sup>a</sup>	$P_D$	0.6	0.47	0.6	0.47	W
		0.3	0.25	0.3	0.25	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150				°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ s	170	210	°C/W
	Steady State	220	265	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	105	125

Notes:

a. Surface mounted on 1" x 1" FR4 board.

**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

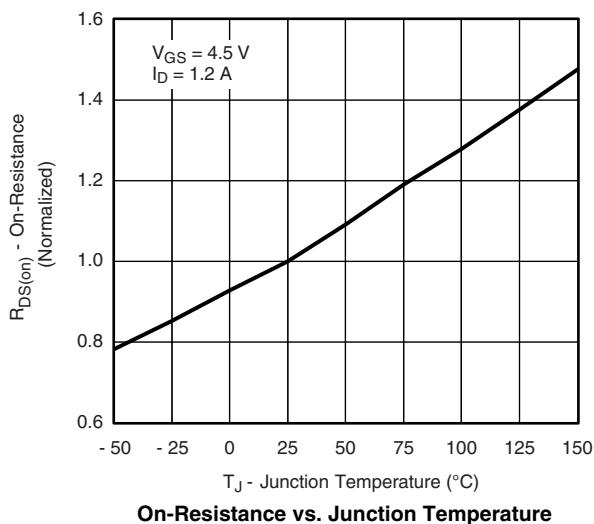
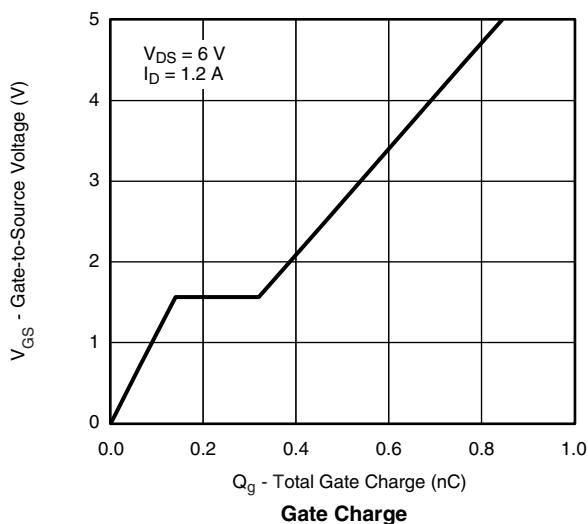
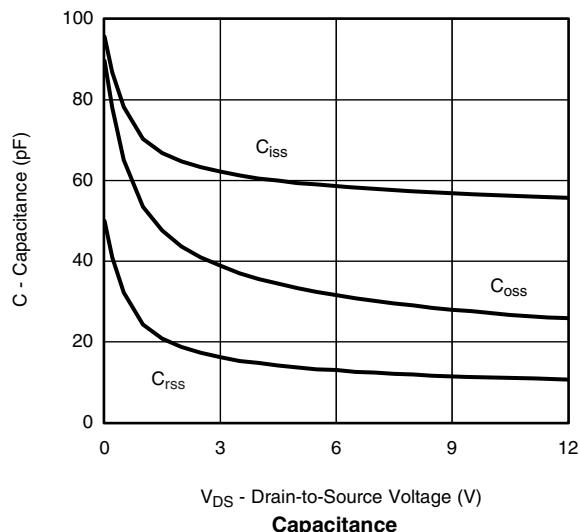
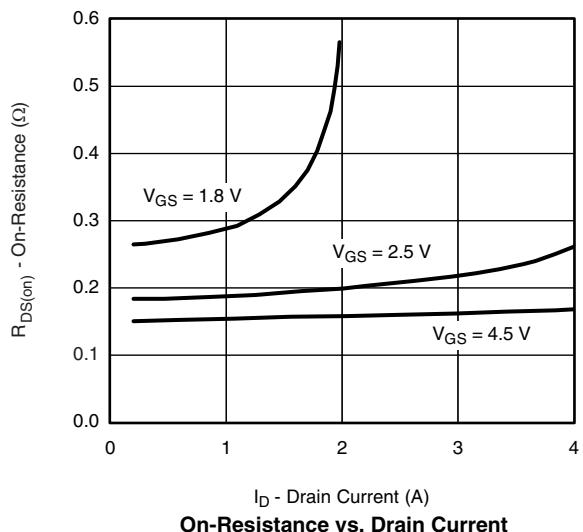
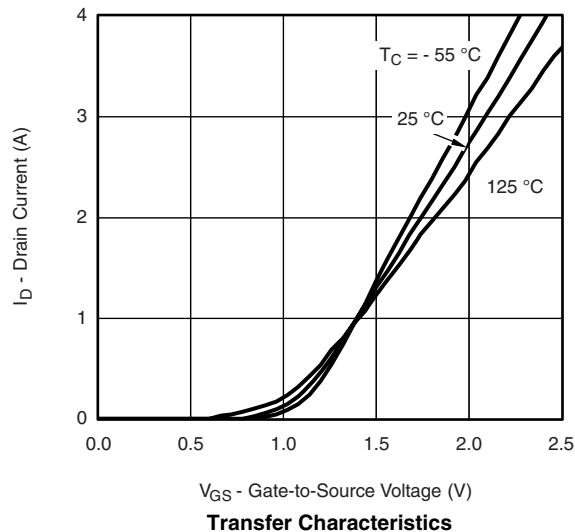
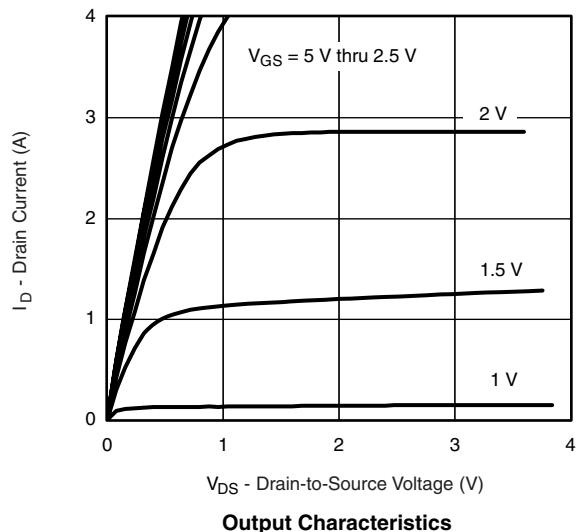
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
<b>Static</b>							
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 100 \mu\text{A}$	N-Ch	0.45		1	V
		$V_{DS} = V_{GS}$ , $I_D = -100 \mu\text{A}$	P-Ch	-0.45		1	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 8 \text{ V}$	N-Ch P-Ch			$\pm 100$ $\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 9.6 \text{ V}$ , $V_{GS} = 0 \text{ V}$	N-Ch			1	$\mu\text{A}$
		$V_{DS} = -9.6 \text{ V}$ , $V_{GS} = 0 \text{ V}$	P-Ch			-1	
		$V_{DS} = 9.6 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 85^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -9.6 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 85^\circ\text{C}$	P-Ch			-5	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$	N-Ch	3			A
		$V_{DS} \leq -5 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$	P-Ch	-2			
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$ , $I_D = 1.2 \text{ A}$	N-Ch		0.195	0.235	$\Omega$
		$V_{GS} = -4.5 \text{ V}$ , $I_D = -0.77 \text{ A}$	P-Ch		0.445	0.535	
		$V_{GS} = 2.5 \text{ V}$ , $I_D = 1.0 \text{ A}$	N-Ch		0.230	0.280	
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -0.6 \text{ A}$	P-Ch		0.735	0.880	
		$V_{GS} = 1.8 \text{ V}$ , $I_D = 0.2 \text{ A}$	N-Ch		0.284	0.340	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -0.2 \text{ A}$	P-Ch		1.05	1.26	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 5 \text{ V}$ , $I_D = 1.2 \text{ A}$	N-Ch		0.8		S
		$V_{DS} = -5 \text{ V}$ , $I_D = -0.77 \text{ A}$	P-Ch		1.2		
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 0.39 \text{ A}$ , $V_{GS} = 0 \text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -0.39 \text{ A}$ , $V_{GS} = 0 \text{ V}$	P-Ch		-0.8	-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	$Q_g$	N-Channel $V_{DS} = 6 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$ , $I_D = 1.2 \text{ A}$	N-Ch		0.8	1.2	nC
Gate-Source Charge	$Q_{gs}$		P-Ch		1.1	1.8	
Gate-Drain Charge	$Q_{gd}$		N-Ch		0.15		
Rise Time	$t_r$	P-Channel $V_{DS} = -6 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$ , $I_D = -0.1 \text{ A}$	P-Ch		0.3		ns
Turn-On Delay Time	$t_{d(\text{on})}$		N-Ch		0.20		
Turn-Off Delay Time	$t_{d(\text{off})}$		P-Ch		0.25		
Fall Time	$t_f$		N-Ch		15	25	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 0.39 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$	N-Ch		17	25	
		$I_F = -0.39 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$	P-Ch		25	40	
			N-Ch		30	45	
			P-Ch		15	25	
			N-Ch		10	15	
			P-Ch		10	15	
			N-Ch		20	40	
			P-Ch		25	40	

Notes:

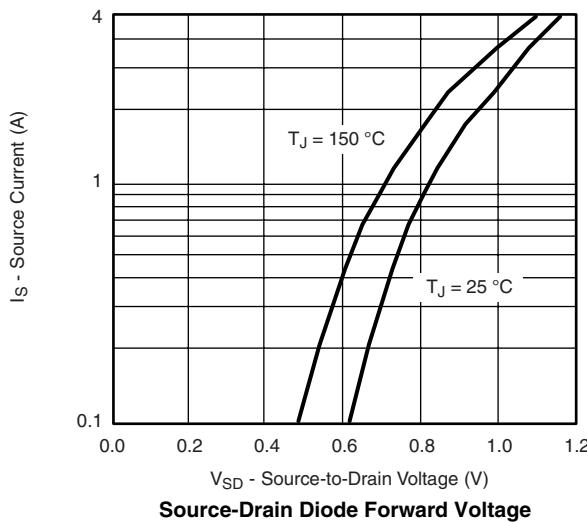
a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

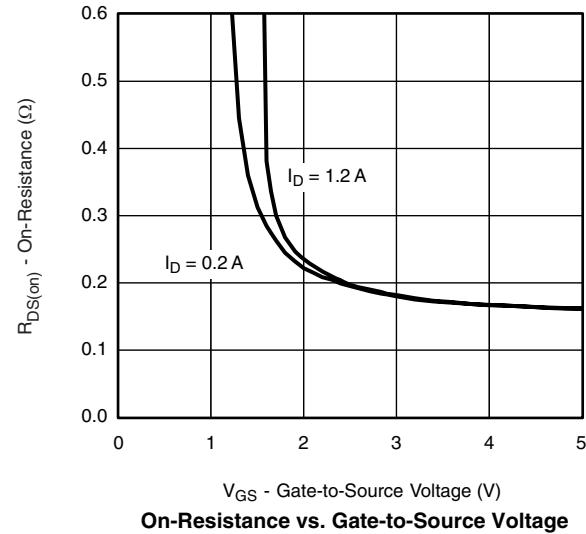
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


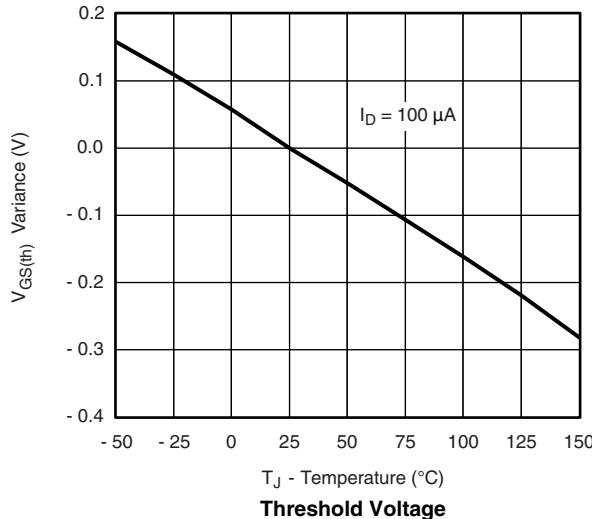
## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



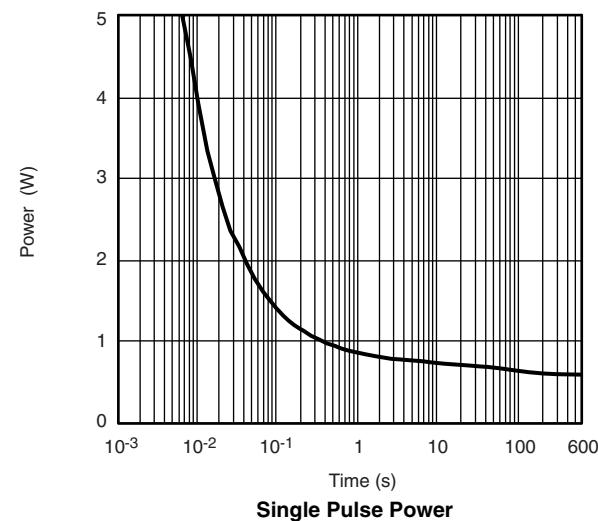
Source-Drain Diode Forward Voltage



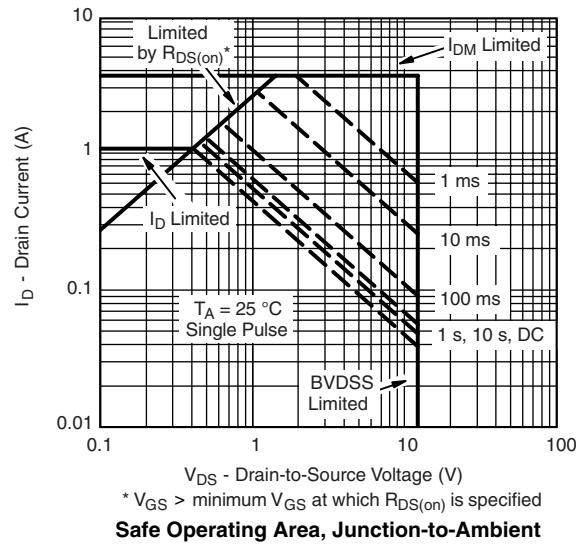
On-Resistance vs. Gate-to-Source Voltage



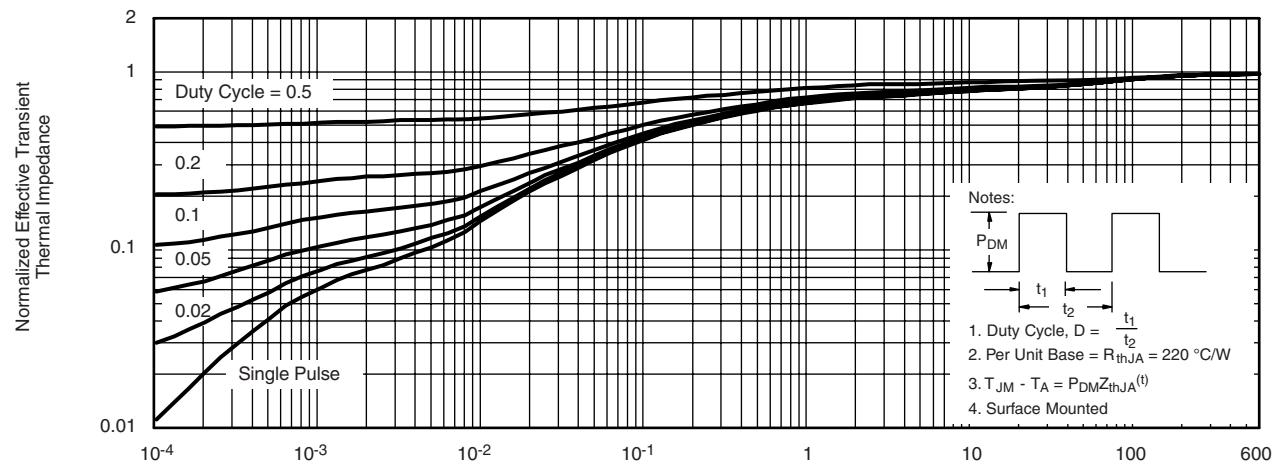
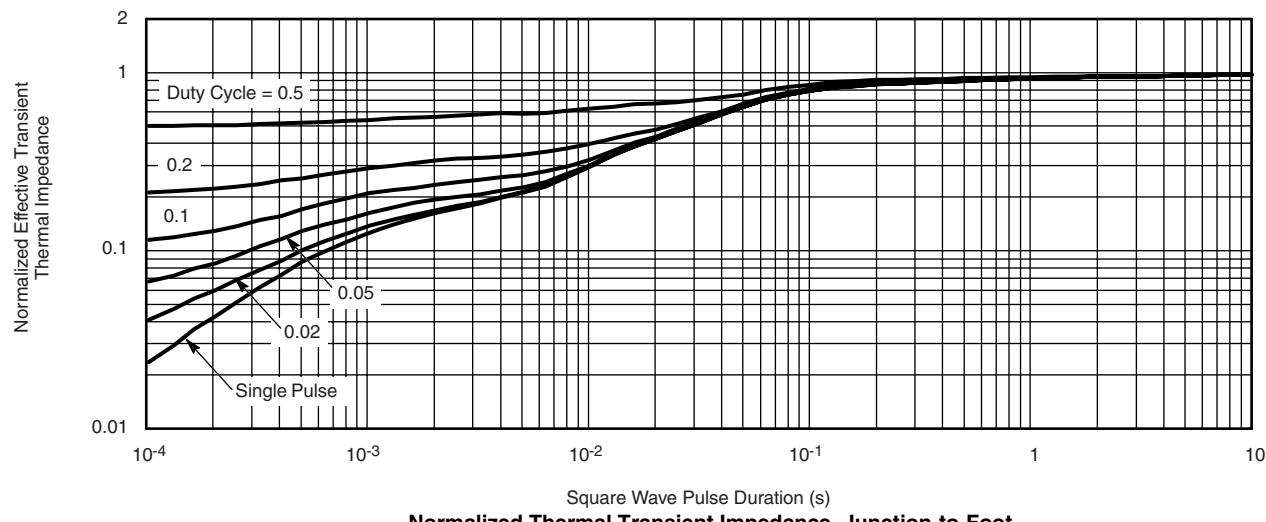
Threshold Voltage



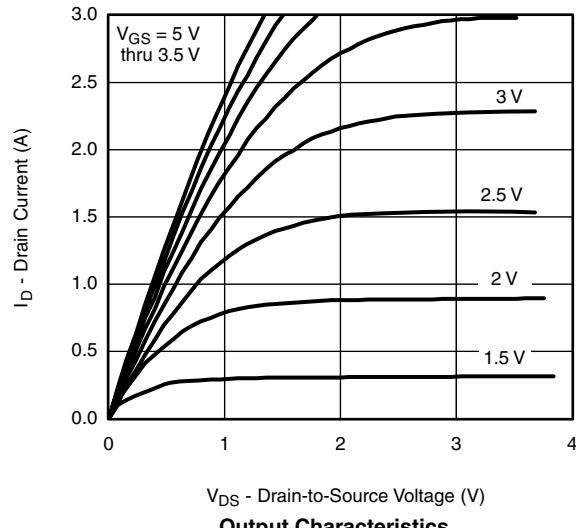
Single Pulse Power



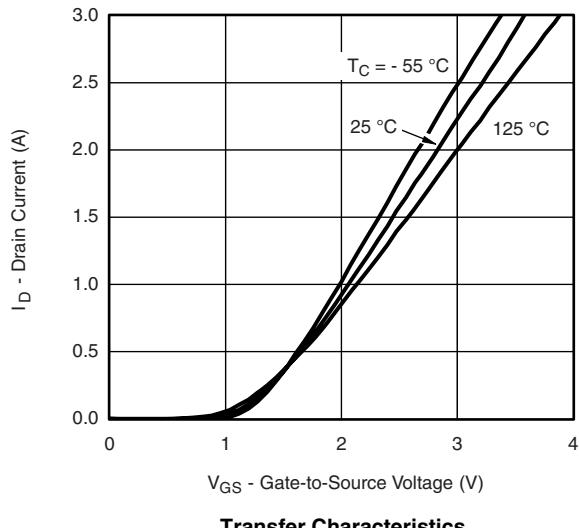
Safe Operating Area, Junction-to-Ambient

**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Foot**

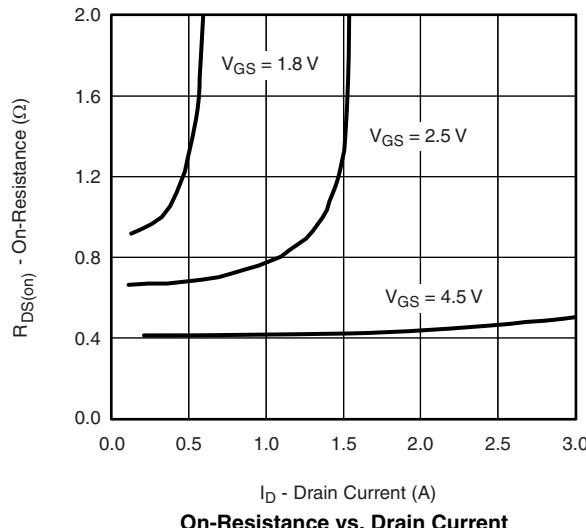
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



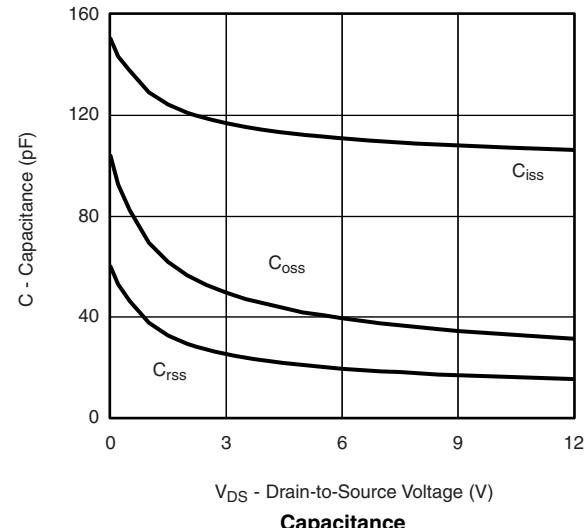
Output Characteristics



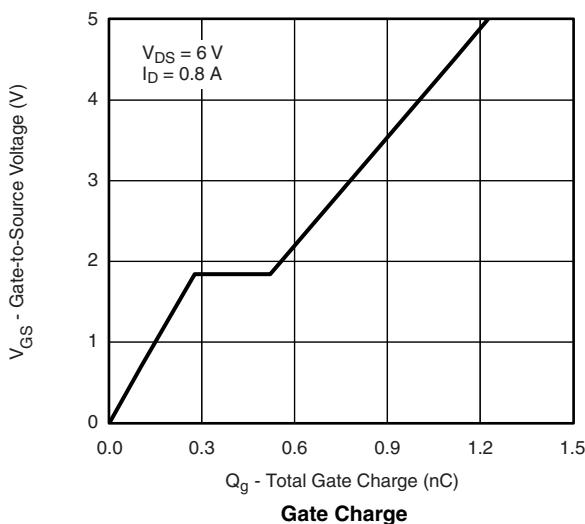
Transfer Characteristics



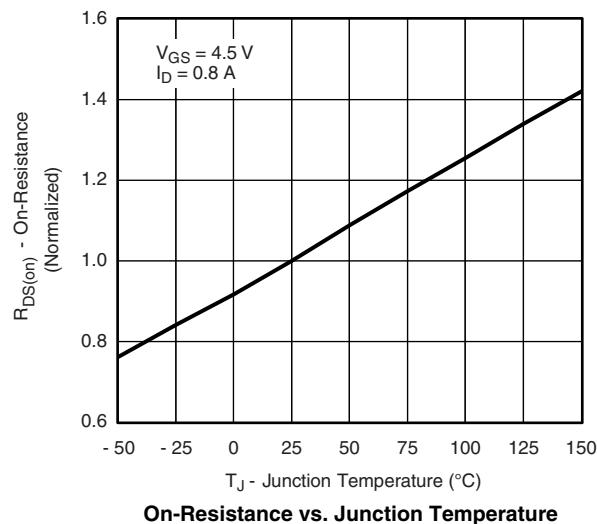
On-Resistance vs. Drain Current



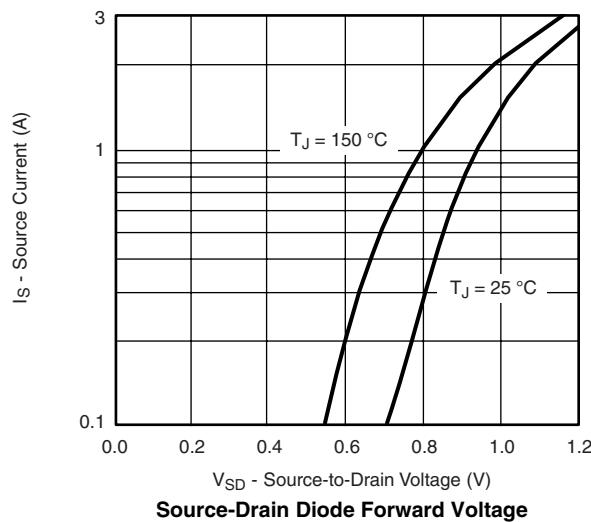
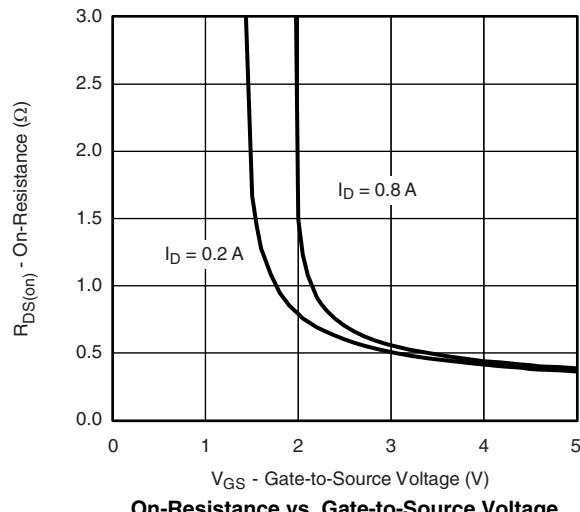
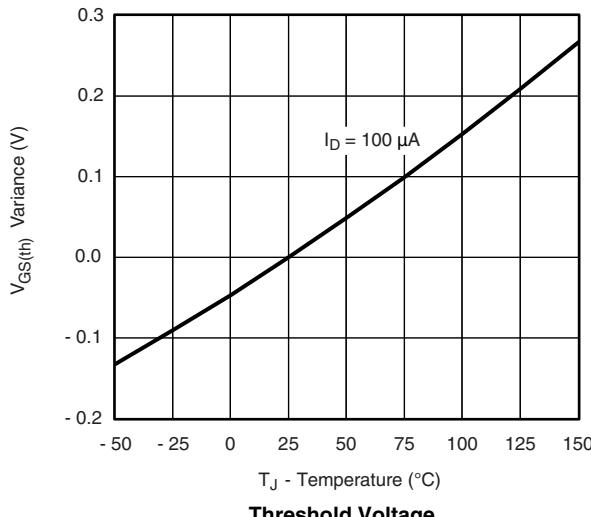
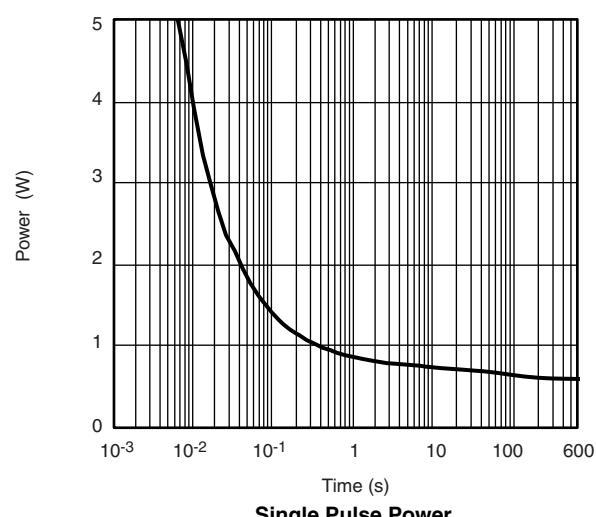
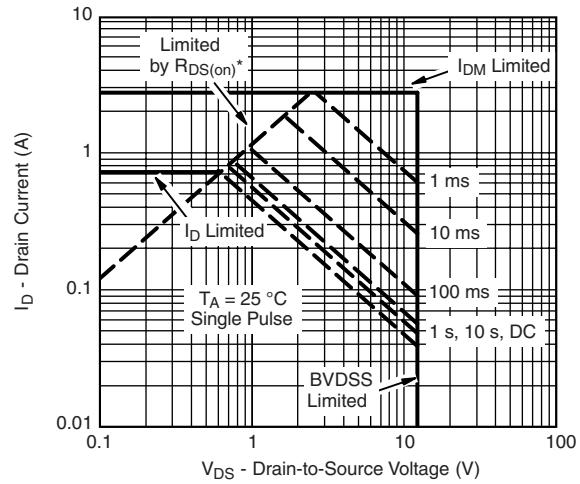
Capacitance

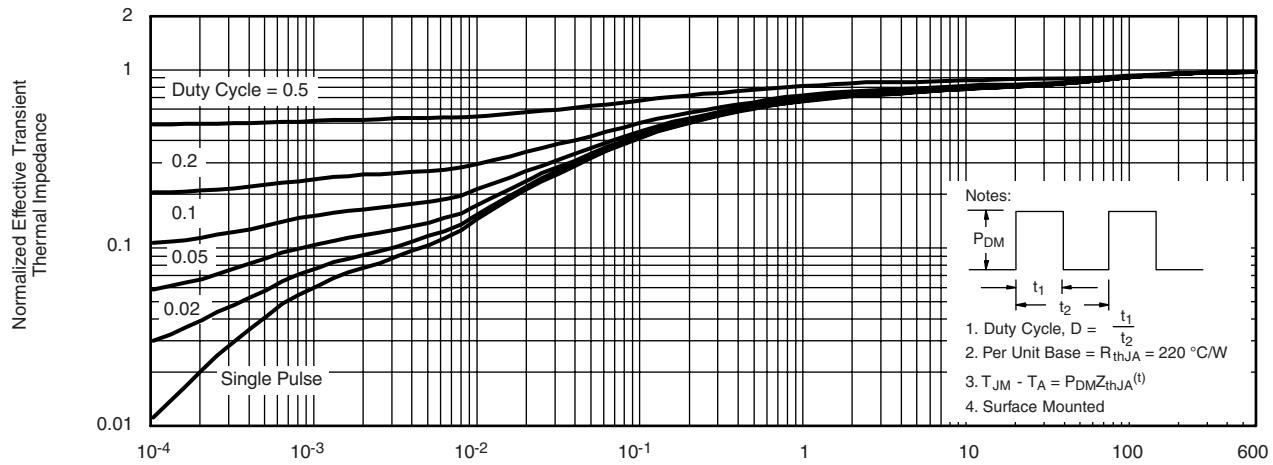
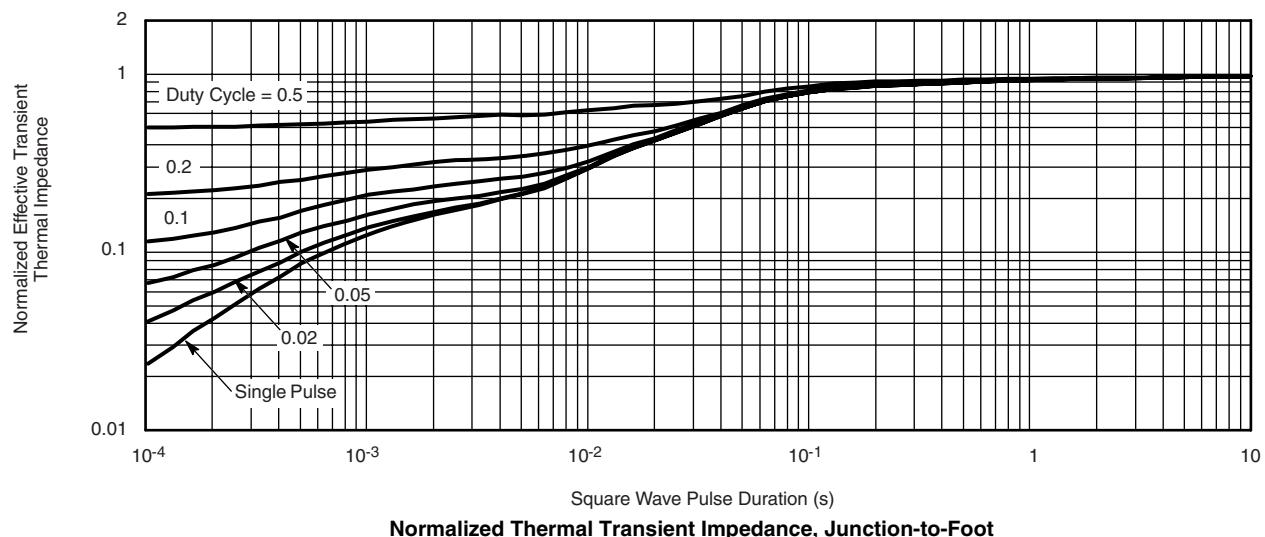


Gate Charge

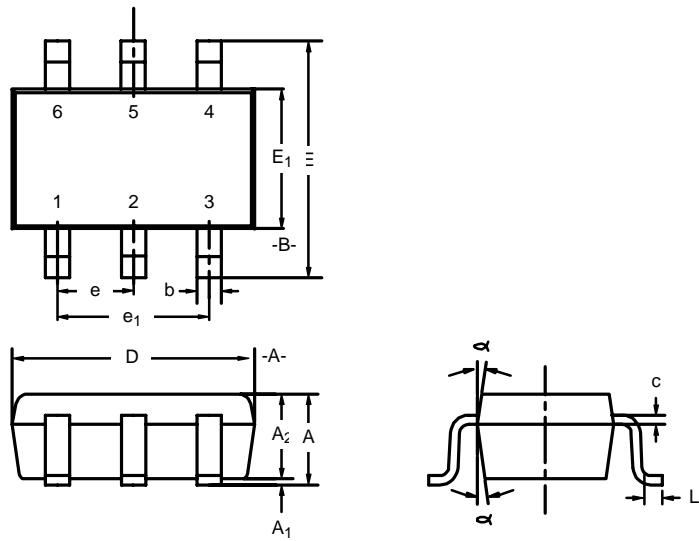


On-Resistance vs. Junction Temperature

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power**

**Safe Operating Area, Junction-to-Ambient**

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Foot**

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**SC-70: 6-LEADS**


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.90	—	1.10	0.035	—	0.043
<b>A<sub>1</sub></b>	—	—	0.10	—	—	0.004
<b>A<sub>2</sub></b>	0.80	—	1.00	0.031	—	0.039
<b>b</b>	0.15	—	0.30	0.006	—	0.012
<b>c</b>	0.10	—	0.25	0.004	—	0.010
<b>D</b>	1.80	2.00	2.20	0.071	0.079	0.087
<b>E</b>	1.80	2.10	2.40	0.071	0.083	0.094
<b>E<sub>1</sub></b>	1.15	1.25	1.35	0.045	0.049	0.053
<b>e</b>	0.65BSC			0.026BSC		
<b>e<sub>1</sub></b>	1.20	1.30	1.40	0.047	0.051	0.055
<b>L</b>	0.10	0.20	0.30	0.004	0.008	0.012
$\alpha$	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5550

# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET

## Copper Leadframe Version

### Recommended Pad Pattern and Thermal Performance

#### INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

#### PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

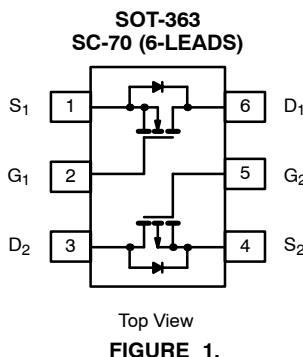


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

#### BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

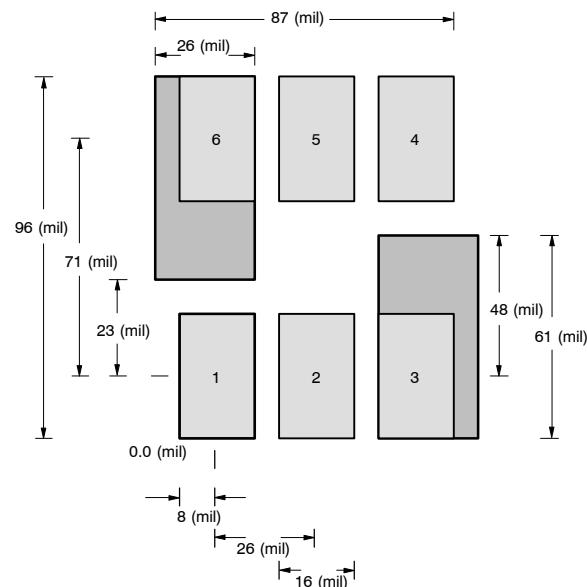


FIGURE 2. SC-70 (6 leads) Dual

#### EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch<sup>2</sup> PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

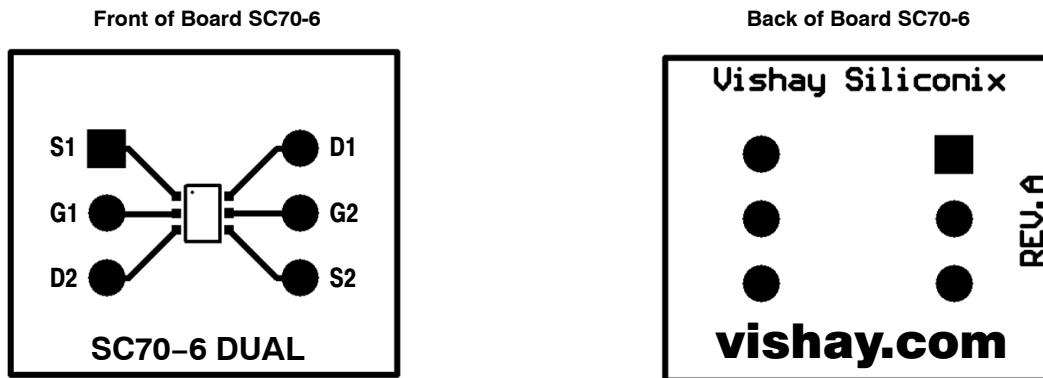


FIGURE 3.

## Thermal Performance

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the "foot" is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

### COOPER LEADFRAME

Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{224^\circ\text{C/W}}$	$P_D = \frac{150^\circ\text{C} - 60^\circ\text{C}}{224^\circ\text{C/W}}$
$P_D = 558 \text{ mW}$	$P_D = 402 \text{ mW}$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

## TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of  $R\theta_{JA}$  for the dual 6-pin SC-70 with varying leadframes are as follows:

### LITTLE FOOT 6-PIN SC-70

	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch <sup>2</sup> PCB with maximum copper both sides.	413°C/W	224°C/W

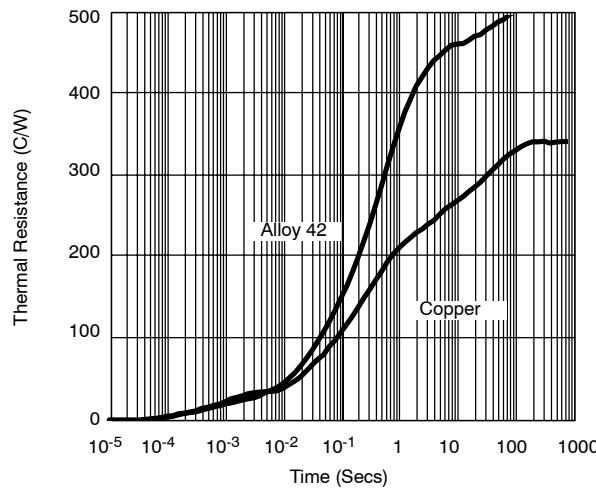
The results indicate that designers can reduce thermal resistance ( $\theta_{JA}$ ) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch<sup>2</sup> PCB area.

The Dual copper leadframe versions have the following suffix:

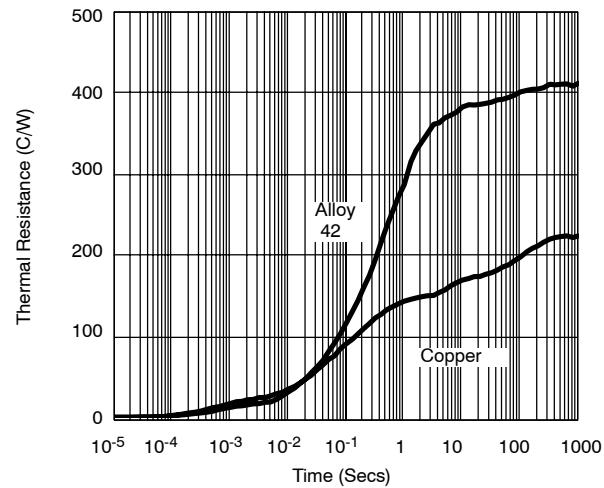
Dual: Si19xxEDH  
Compl.: Si15xxEDH

### Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{413^\circ\text{C/W}}$	$P_D = \frac{150^\circ\text{C} - 60^\circ\text{C}}{413^\circ\text{C/W}}$
$P_D = 303 \text{ mW}$	$P_D = 218 \text{ mW}$

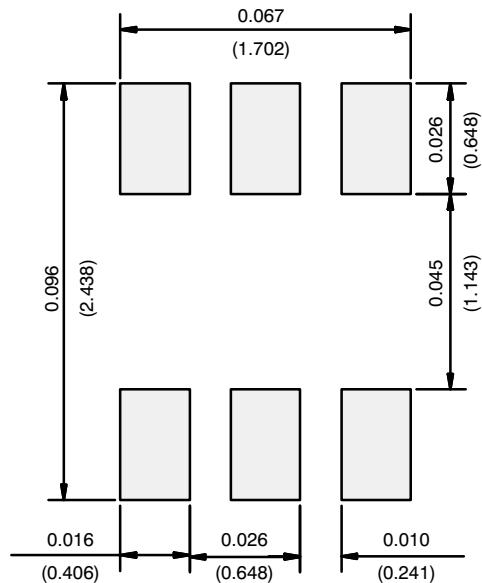


**FIGURE 4.** Dual SC70-6 Thermal Performance on EVB



**FIGURE 5.** Dual SC70-6 Comparison on 1-inch<sup>2</sup> PCB

## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



### Recommended Minimum Pads Dimensions in Inches/(mm)

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## Material Category Policy

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.**

**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**