USB2.0 High-Speed (480Mbps) Signal Switch With Vbus Short Protection

Features

- USB 2.0 compliant (high speed and full speed)
- R_{ON} is 4.0Ω typical @ V_{DD} = 3.0V
- Low bit-to-bit skew
- Low Crosstalk: -41dB @ 240 MHz
- Off Isolation: -37dB @ 240 MHz
- Wide -3db bandwidth: 770MHz
- Near-Zero propagation delay: 250ps
- Support for 1.8V/2.5V/3.3V Logic on Control pins
- Channel On Capacitance: 6.0pF
- VDD Operating Range: 1.8V to 4.3V ±10%
- Data pin I/O ESD: >8kV HBM protection per JESD22-A114D specification
- I/O pins have over-voltage protection and can tolerate a short to Vbus
- Packaging (Pb-free & Green): 10-pin UQFN (ZM10)

Applications

- Route signals for USB 2.0
- Cell phone, PDA, Digital camera and Notebook
- LCD Monitor ,TV, Set-top box
- Portable device

Pin Description

Pin No	Pin Name	Description
1	D+	USB Data bus
2	D-	USB Data bus
3	GND	Ground
4	D-A	Multiplexed Source Inputs
5	D+A	Multiplexed Source Inputs
6	D-B	Multiplexed Source Inputs
7	D+B	Multiplexed Source Inputs
8	/OE	Switch Enable
9	V_{DD}	Positive Power Supply
10	SEL	Switch Select

Logic Function Table

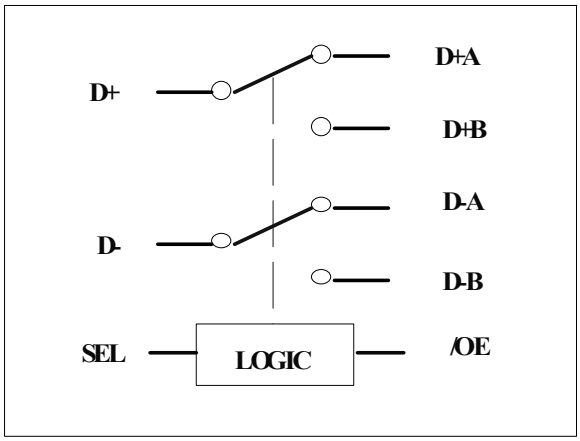
/OE	SEL	Function
H	X	I/O's = Hi-Z
L	L	D(+/-) to D(+/-)A
L	H	D(+/-) to D(+/-)B

Description

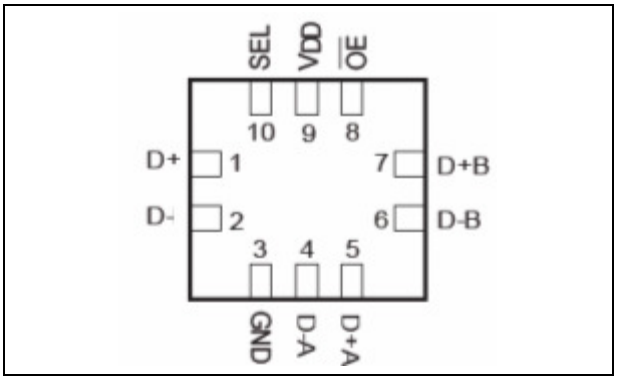
The PI3USB42 is a single differential channel 2:1 multiplexer/demultiplexer USB 2.0 Switch. Industry leading advantages include a propagation delay of less than 250ps, resulting from its low channel resistance and I/O capacitance. The device multiplexes differential outputs from a USB Host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew, high channel-to-channel noise isolation and is compatible with various standards, such as High Speed USB 2.0 (480 Mb/s).

The PI3USB42 offers overvoltage protection per the USB2.0 specification. With the chip powered on or off, all I/O pins can withstand a short to Vbus (5V +/-10%). If VDD=0V, the I/Os can still have signals present, and the signal will NOT leak through to VDD.

Functional Block Diagram



Pin Assignment



Maximum Ratings

Storage Temperature	65℃ to +150℃
Supply Voltage to Ground Potential	-0.5V to +4.6V
Control Input Voltage	-0.5V to 4.6V
DC Switch Voltage (D+, D-, D+A, D-A, D+B and D-B)	-0.5V to 5.25V
DC Output Current	120mA
Power Dissipation	0.5W
ESD(HBM)	>8kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	1.8	-	4.3	V
V_{CNTRL} (1)	Control Input Voltage	0	-	4.3	
V_{INPUT}	Switch Input Voltage	-0.5	-	4.3	
T_A	Operating Temperature	-40	-	85	°C

Notes:
1. The control input must be held high or low and it must not float.

DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = 3.0V - 4.4V)

Parameter	Description	Test Conditions(1)	Min	Typ(2)	Max	Unit
V_{IH}	Input High Voltage	Guaranteed High Level	1.2	-	-	V
V_{IL}	Input Low Voltage	Guaranteed Low Level	-	-	0.60	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., I_{SEL} = -18mA	-	-0.7	-1.2	
I_{IH}	Input High Current	V_{DD} = Max., V_{SEL} = V_{DD}	-	-	±100	nA
I_{IL}	Input Low Current	V_{DD} = Max., V_{SEL} = GND	-	-	±100	
R_{ON}	Switch On-Resistance(3)	V_{DD} = Min., 0 ≤ V_{INPUT} ≤0.4V, I_{INPUT}= -40mA	-	4.0	5.5	Ω
$R_{FLAT(ON)}$	On-Resistance Flatness(3)	V_{DD} = Min., 0 ≤ V_{INPUT} ≤0.4V, I_{INPUT} = -40mA	-	0.25	-	
△R_{ON}	On-Resistance match from center ports to any other port(3)	V_{DD} = Min., 0 ≤ V_{INPUT} ≤0.4V, I_{INPUT} = -40mA	-	0.1	1.0	
I_{OZ}	Output leakage current when port is off	V_{DD} = 4.3V, 0 ≤ V_{INPUT} ≤0.4V	-	-	±100	nA
I_{OFF}	Power-Off Leakage Current	V_{INPUT} =0V~4.3V, V_{DD}=0V	-	-	100	nA

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. V_{DD} = 3.0 - 4.4V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between D and Dn pin at indicated current through the Switch On-Resistance is determined by the lower of the voltages on the two (D, Dn) pins.

Power Supply Characteristics

(T_A = -40°C to +85°C, V_{DD} = 3.0V - 4.4V)

Parameter	Description	Test Conditions[1]	Min	Typ	Max	Unit
I_{CC}	Quiescent Power Supply current	V_{DD} = Max., V_{SEL} = V_{DD} or GND	-	-	100	nA
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{DD}	V_{CNTRL} =1.8V, V_{DD}=4.3V	-	5.8	15	µA

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

Capacitance

(T_A = 25°C, V_{DD} = 3.0V, f = 1MHz)

Parameters	Description	Test Conditions	Min.	Typ	Max.	Units
C_{CNTRL}	Control logic pin Input Capacitance	V_{SEL} = 0V	-	6.0	-	pF
C_{OFF}	Switch Capacitance, Switch OFF		-	1.9	-	
C_{ON}	Switch Capacitance, Switch ON		-	6.0	-	

Dynamic Electrical Characteristics Over the Operating Range

(T_A = 25°C, V_{DD} = 3.0V)

Parameters	Description	Test Conditions(1)	Min.	Typ	Max.	Units
XTALK	Crosstalk	R_L = 50Ω, f = 240 MHz	-	-41	-	dB
OIRR	OFF Isolation		-	-37	-	
BW	–3dB Bandwidth	R_L = 50Ω	-	770	-	MHz

Switching Characteristics

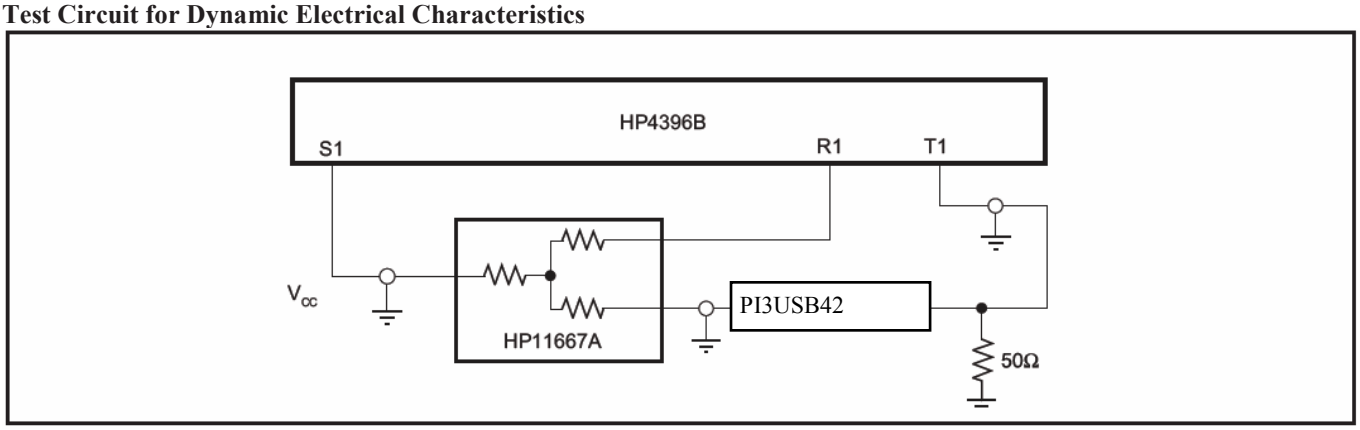
(T_A = 25°C, V_{DD} = 3.0V)

Parameters	Description	Test Conditions[1]	Min	Typ	Max	Units
t_{PD}	Propagation Delay[2,3]	See Test Circuit for Electrical Characteristics	-	0.25	-	ns
t_{PZH}, t_{PZL}	Line Enable Time - SEL to D(+/-), D(+/-)n		-	25	-	
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to D(+/-), D(+/-)n		-	4	-	
t_{BBM}	Break-Before-Make	-	-	7	-	ns
t_{SKb-b}	Output skew, bit-to-bit (opposite transition of the same output (t_{PHL} -t_{PLH})[2]	V_{DD} = 3V	-	-	35	ps
		V_{DD} = 4V	-	-	60	

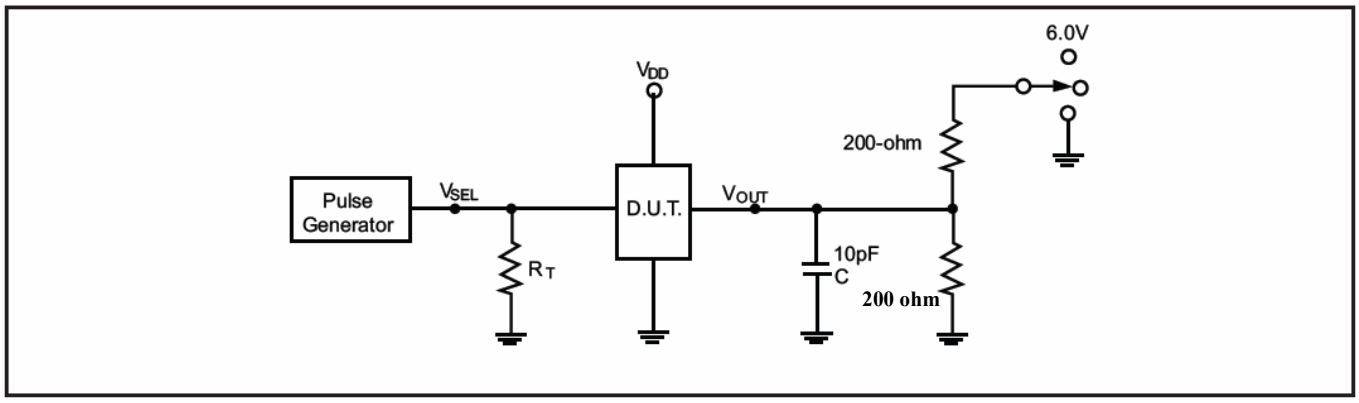
Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Guaranteed by design.
3. The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Test Circuits and Test Diagramming

Test Circuit for Dynamic Electrical Characteristics



Test Circuit for Electrical Characteristics

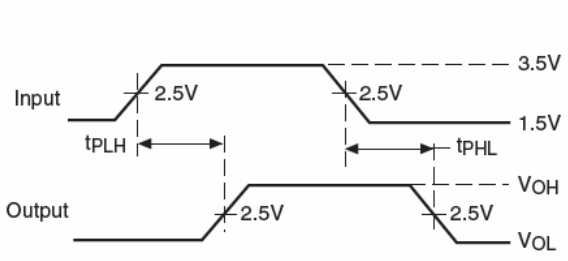


Notes:
C_L = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, ZO = 50Ω, tR ≤ 2.5ns, tF ≤ 2.5ns.
The outputs are measured one at a time with on transition per measurement.

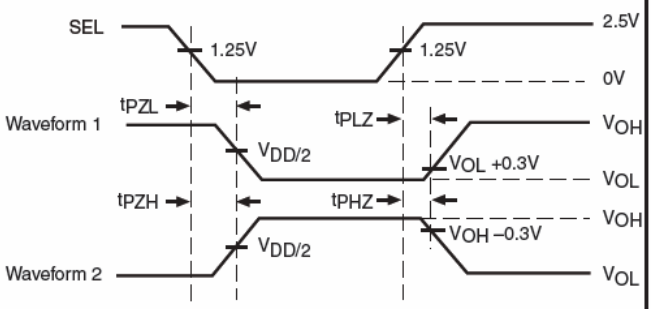
Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on I-side)	6.0V
t_{PHZ}, t_{PZH} (output on I-side)	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Propagation Delay Times



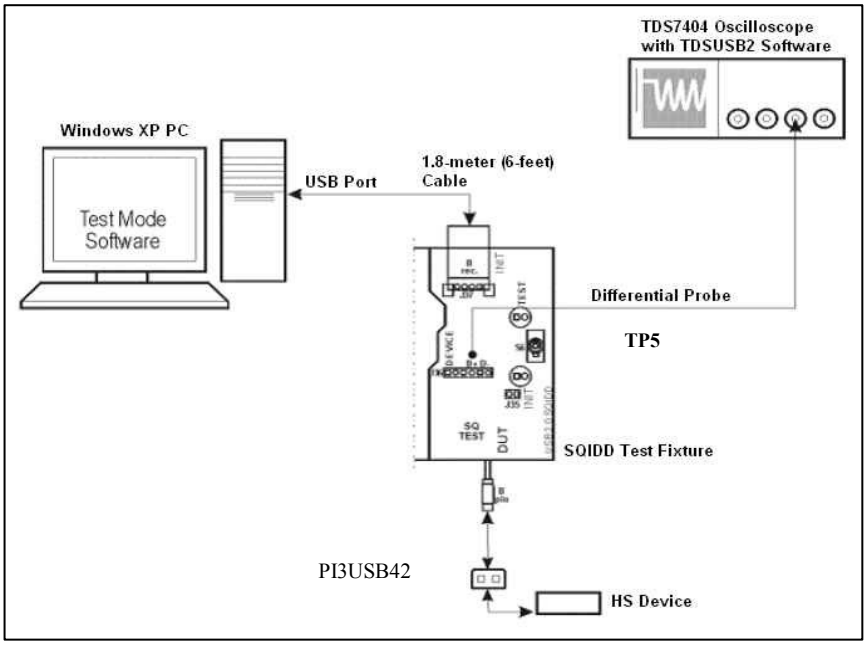
Voltage Waveforms Enable and Disable Times

Applications Information

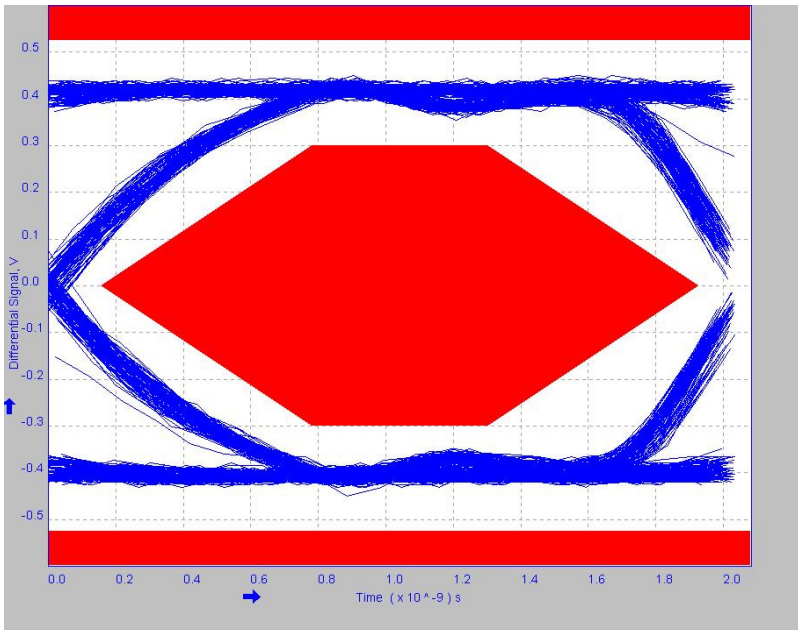
Logic Inputs
The logic control inputs can be driven up to +4.3V regardless of the supply voltage. For example, given a +3.3V supply, the output enables or select pins may be driven to low to 0V and high to 4.3V.

Power Supply Sequencing
Proper power supply sequencing is recommended for all CMOS devices. Always apply VDD and GND before applying signals to input/output or control pin.

Eye Diagram measurement:

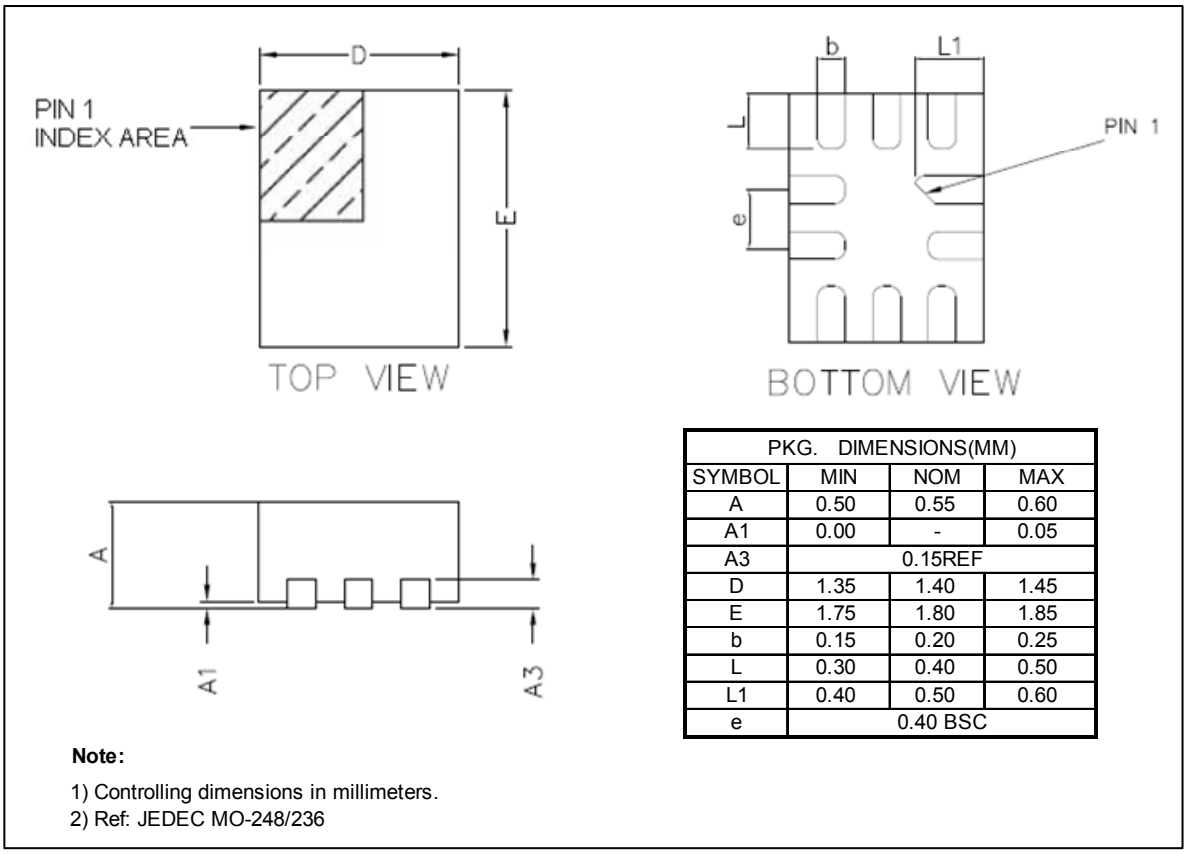


USB2.0 High-speed (480Mbps) Signal Integrity Test Setup



High Speed Signal Quality Eye Diagram Test (V_{DD} = 3.3V)

Mechanical Information 10-pin UQFN (ZM10)

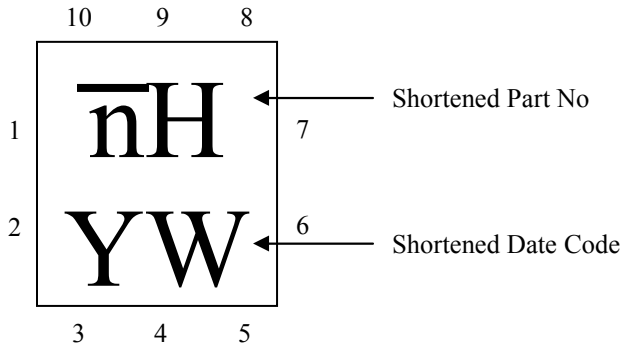


PKG. DIMENSIONS(MM)			
SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3		0.15REF	
D	1.35	1.40	1.45
E	1.75	1.80	1.85
b	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.40	0.50	0.60
e		0.40 BSC	

Note:

1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-248/236

Marking Description



Ordering Information

Part Number	Package Code	Package
PI3USB42ZME	ZM	Lead Free and Green UQFN-10

Notes:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel