# 74LVT374

## 3.3 V octal D-type flip-flop; 3-state

Rev. 4 — 22 November 2011 Product data sheet

## 1. General description

The 74LVT374 is a high-performance product designed for $V_{CC}$ operation at 3.3 V.

This device is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock (pin CP) and output enable (pin $\overline{OE}$) control gates. The state of each Dn input (one setup time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flops Qn output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active LOW output enable (pin $\overline{OE}$) controls all eight 3-state buffers independent of the clock operation.

When pin $\overline{OE}$ is LOW, the stored data appears at the outputs. When pin $\overline{OE}$ is HIGH, the outputs are in the high-impedance OFF-state, which means they will neither drive nor load the bus.

## 2. Features and benefits

- Inputs and outputs arranged for easy interfacing to microprocessors
- 3-state outputs for bus interfacing
- Common output enable control
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection
  - JESD78 class II exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVT374D | –40 °C to +85 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LVT374DB | –40 °C to +85 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74LVT374PW | –40 °C to +85 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |

## 4. Functional diagram

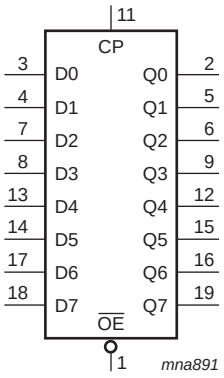



**Fig 1. Logic symbol**

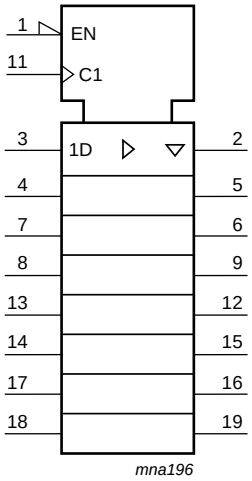



**Fig 2. IEC logic symbol**

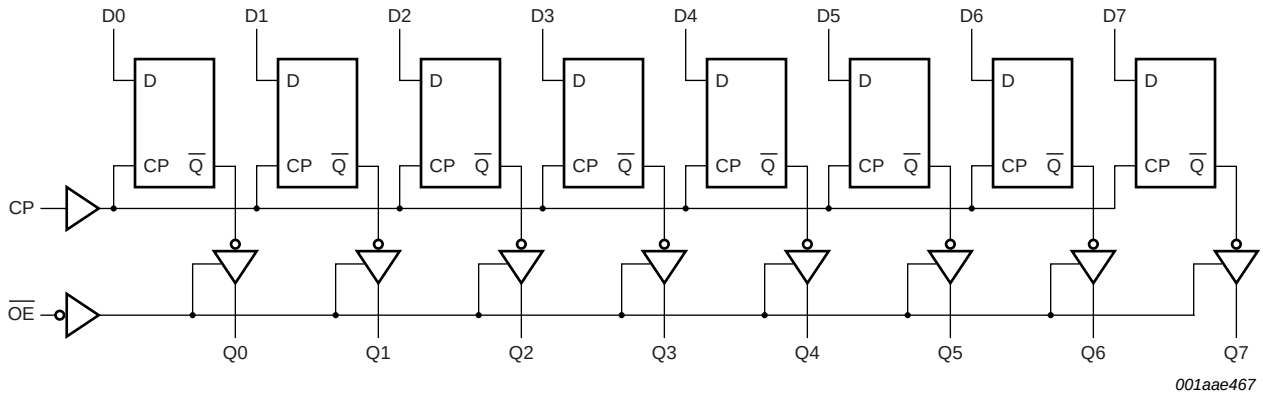



**Fig 3. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

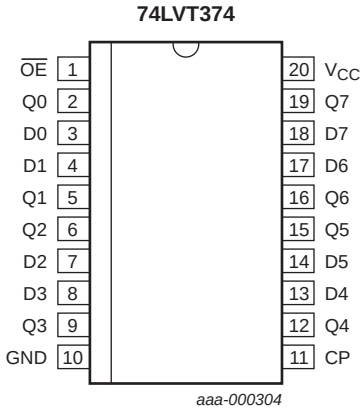



**Fig 4. Pin configuration for SO20, and (T)SSOP20)**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}$ | 1 | output enable input (active LOW) |
| D0 to D7 | 3, 4, 7, 8, 13, 14, 17, 18 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock pulse input (active rising edge) |
| Q0 to Q7 | 2, 5, 6, 9, 12, 15, 16, 19 | data output |
| $V_{CC}$ | 20 | supply voltage |

# 6. Functional description

## 6.1 Function table

**Table 3. Function table [1]**

| Operating mode | Control | | Input | Internal register | Output |
|---|---|---|---|---|---|
| | $\overline{OE}$ | CP | Dn | | Qn |
| Load and read register | L | ↑ | l | L | L |
| | | | h | H | H |
| Hold | L | NC | X | NC | NC |
| Disable outputs | H | L or H | X | NC | Z |
| | | ↑ | Dn | Dn | Z |

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH clock transition;
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition;
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition;
Z = high-impedance OFF-state;
NC = no change;
X = don't care.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +4.6 | V |
| $V_I$ | input voltage | | [1] | −0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | −0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | - | −50 | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | - | −50 | mA |
| $I_O$ | output current | output in LOW-state | | - | 128 | mA |
| | | output in HIGH-state | | - | −64 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_j$ | junction temperature | | [2] | - | 150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +85 °C | [3] | - | 500 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.7 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | 0.8 | V |
| $I_{OH}$ | HIGH-level output current | | - | –32 | mA |
| $I_{OL}$ | LOW-level output current | | - | 32 | mA |
| | | current duty cycle ≤ 50 %; $f_i \geq 1$ kHz | - | 64 | mA |
| $T_{amb}$ | ambient temperature | in free air | –40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.7 V; $I_{IK}$ = –18 mA | –1.2 | –0.9 | - | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = 2.7 V to 3.6 V; $I_{OH}$ = –100 µA | $V_{CC}$ – 0.2 | $V_{CC}$ – 0.1 | - | V |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = –8 mA | 2.4 | 2.5 | - | V |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = –32 mA | 2.0 | 2.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.7 V | | | | |
| | | $I_{OL}$ = 100 µA | - | 0.1 | 0.2 | V |
| | | $I_{OL}$ = 24 mA | - | 0.3 | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | | | | |
| | | $I_{OL}$ = 16 mA | - | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 32 mA | - | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 64 mA | - | 0.4 | 0.55 | V |
| $V_{OL(pu)}$ | power-up LOW-level output voltage | $V_{CC}$ = 3.6 V; $I_O$ = 1 mA; $V_I$ = GND or $V_{CC}$ [2] | - | 0.13 | 0.55 | V |
| $I_I$ | input leakage current | all input pins; $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | - | 1 | 10 | µA |
| | | control pins; $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | - | ±0.1 | ±1 | µA |
| | | data pins; $V_{CC}$ = 3.6 V [3] | | | | |
| | | $V_I$ = $V_{CC}$ | - | 0.1 | 1 | µA |
| | | $V_I$ = 0 V | –5 | –1 | - | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | - | 1 | ±100 | µA |
| $I_{LO}$ | output leakage current | $V_O$ = 5.5 V and $V_{CC}$ = 3.0 V; output HIGH [4] | - | 60 | 125 | µA |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 3.0 V; $V_I$ = 0.8 V | 75 | 150 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 3.0 V; $V_I$ = 2.0 V [4] | - | –150 | –75 | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6; $V_I$ = 0 V to 3.6 V [4] | - | - | 500 | µA |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6; $V_I$ = 0 V to 3.6 V | | –500 | - | - | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq$ 1.2 V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; $\overline{OE}$ = don't care | [5] | - | 1 | ±100 | μA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | output HIGH: $V_O$ = 3.0 V | | - | 1 | 5 | μA |
| | | output LOW: $V_O$ = 0.5 V | | –5 | 1 | - | μA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | | |
| | | outputs HIGH | | - | 0.13 | 0.19 | mA |
| | | outputs LOW | | - | 3 | 12 | mA |
| | | outputs disabled | [6] | - | 0.13 | 0.19 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3 V to 3.6 V; one input at $V_{CC}$ – 0.6 V and other inputs at $V_{CC}$ or GND | [7] | - | 0.1 | 0.2 | mA |
| $C_I$ | input capacitance | $V_I$ = 0 V or 3.0 V | | - | 4 | - | pF |
| $C_O$ | output capacitance | outputs disabled; $V_O$ = 0 V or 3.0 V | | - | 7 | - | pF |

[1] Typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at $V_{CC}$ or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC}$ = 1.2 V to $V_{CC}$ = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.

[6] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to ground (GND = 0 V); for test circuit see Figure 9.*

| Symbol | Parameter | Conditions | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $t_{PLH}$ | LOW to HIGH propagation delay | CP to Qn; see Table 6 | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.7 | 3.2 | 5.1 | ns |
| | | $V_{CC}$ = 2.7 V | - | - | 5.8 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | CP to Qn; see Table 6 | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.2 | 3.5 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | - | - | 5.5 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $\overline{OE}$ to Qn; see Figure 6 | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.2 | 5.3 | ns |
| | | $V_{CC}$ = 2.7 V | - | - | 7.3 | ns |

**Table 7. Dynamic characteristics** *...continued*

*Voltages are referenced to ground (GND = 0 V); for test circuit see Figure 9.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $t_{PZL}$ | OFF-state to LOW propagation delay | $\overline{OE}$ to Qn; see Figure 7 | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 2.0 | 3.4 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | | - | - | 6.1 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $\overline{OE}$ to Qn; see Figure 6 | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.9 | 4.3 | 6.7 | ns |
| | | $V_{CC}$ = 2.7 V | | - | - | 7.1 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $\overline{OE}$ to Qn; see Figure 7 | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 2.0 | 3.4 | 5.1 | ns |
| | | $V_{CC}$ = 2.7 V | | - | - | 5.1 | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 2.0 | 0.7 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 2.0 | - | - | ns |
| $t_h$ | hold time | Dn to CP; see Figure 8 | [3] | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 0.3 | –0.5 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 0 | - | - | ns |
| $t_W$ | pulse width | CP input HIGH; see Figure 5 | [4] | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.5 | 0.8 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | - | - | ns |
| | | CP input LOW; see Figure 5 | [4] | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 2.5 | 1.7 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 3.0 | - | - | ns |
| $f_{max}$ | maximum frequency | CP input; see Figure 5 | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 125 | 200 | - | MHz |
| | | $V_{CC}$ = 2.7 V | | 125 | - | - | MHz |

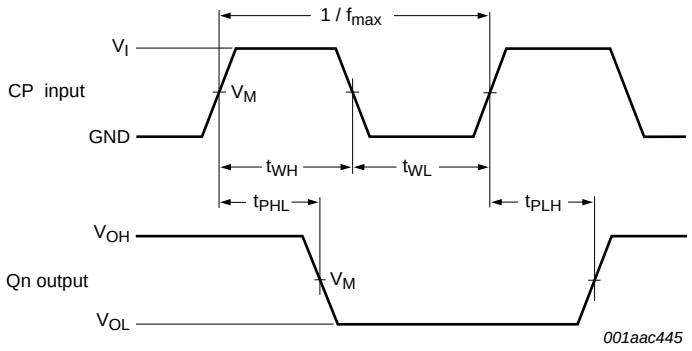
[1] Typical values are at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] $t_{su}$ is the same as $t_{su(H)}$ and $t_{su(L)}$

[3] $t_h$ is the same as $t_{h(H)}$ and $t_{h(L)}$

[4] $t_W$ is the same as $t_{WH}$ and $t_{WL}$

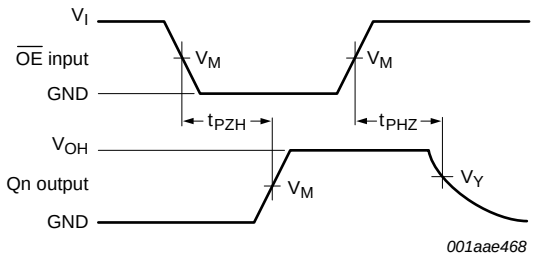
## 11. Waveforms




Measurement points are given in Table 8

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

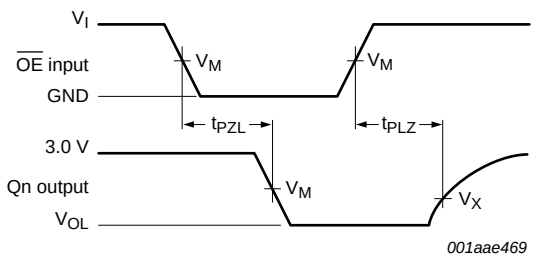
**Fig 5. Propagation delay clock input (CP) to output (Qn), pulse width clock (CP) and maximum clock frequency**




Measurement points are given in Table 8

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

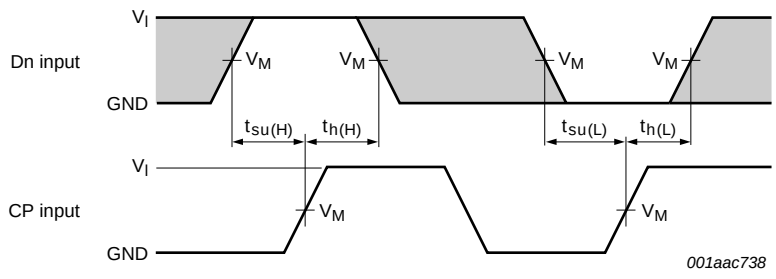
**Fig 6. Output enable time to HIGH-state and output disable time from HIGH-state**




Measurement points are given in Table 8

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. Output enable time to LOW-state and output disable time from LOW-state**



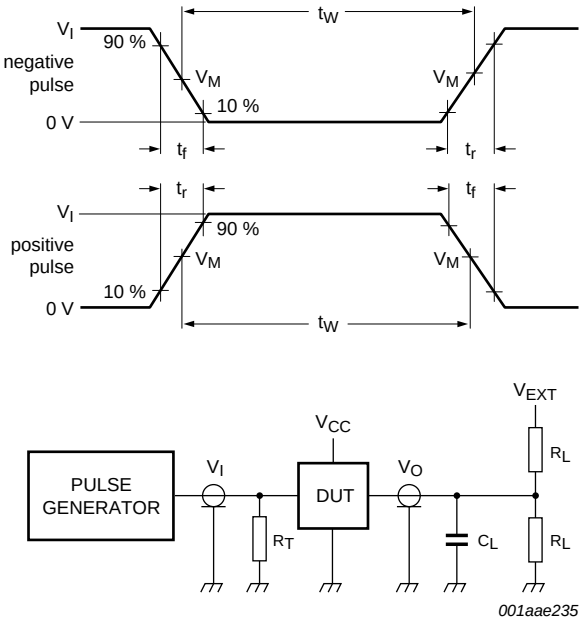

Measurement points are given in Table 8

**Remark:** The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 8. Data setup and hold times**

**Table 8. Measurement points**

| Input | Output | | |
|---|---|---|---|
| $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = Test voltage for switching times.

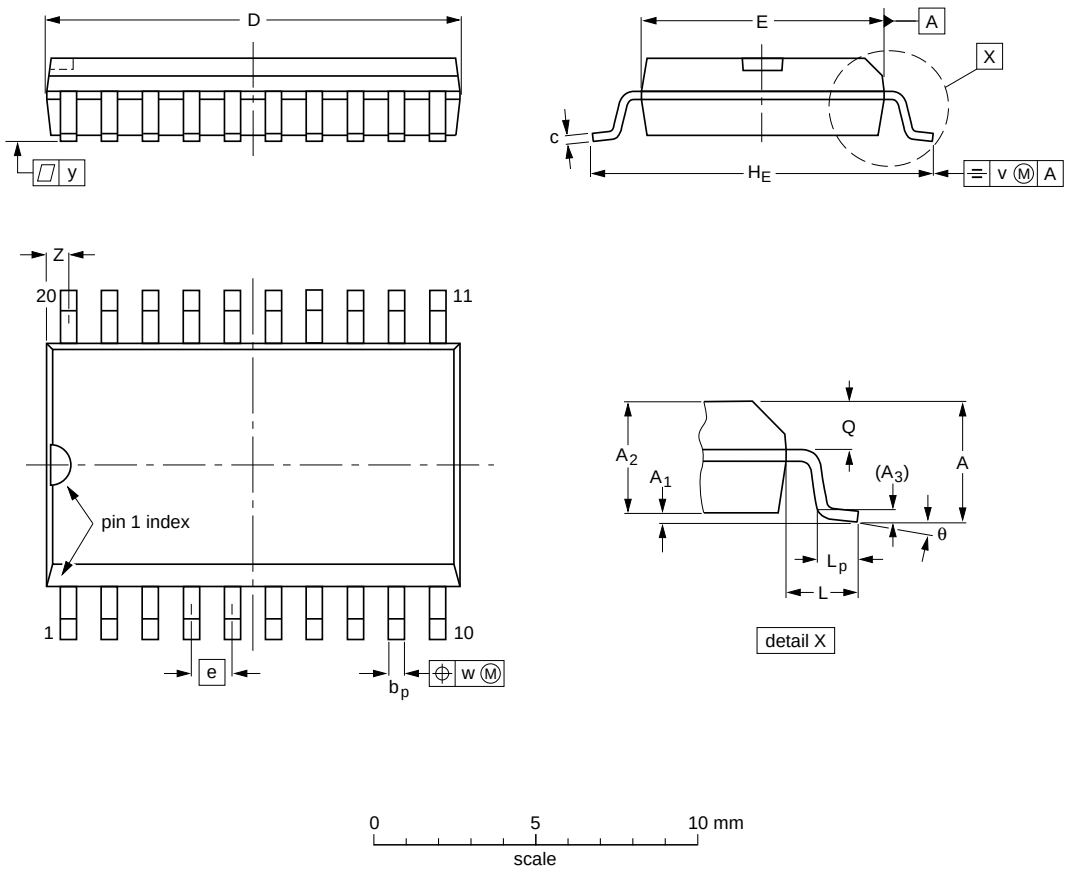
**Fig 9. Load circuitry for switching times**

**Table 9. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

## 12. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

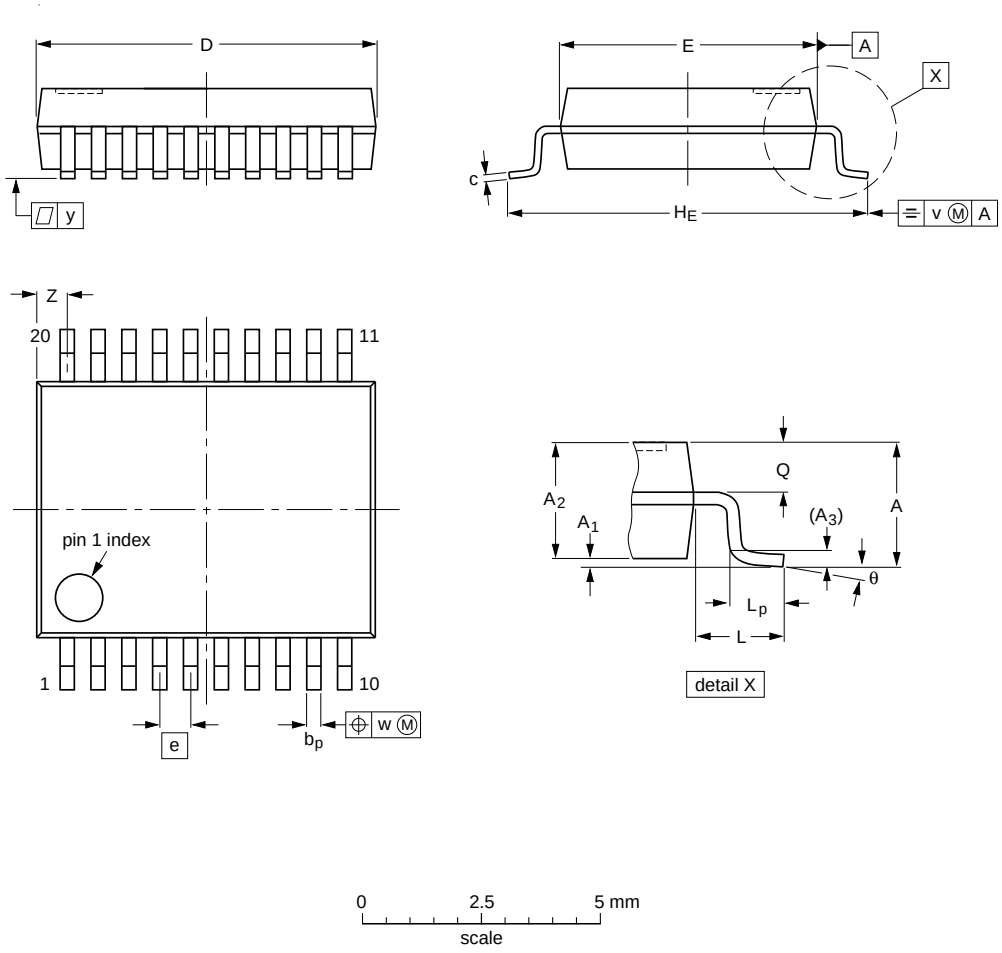
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT163-1 (SO20)**

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm** **SOT339-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 7.4<br>7.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5 | $8^o$<br>$0^o$ |

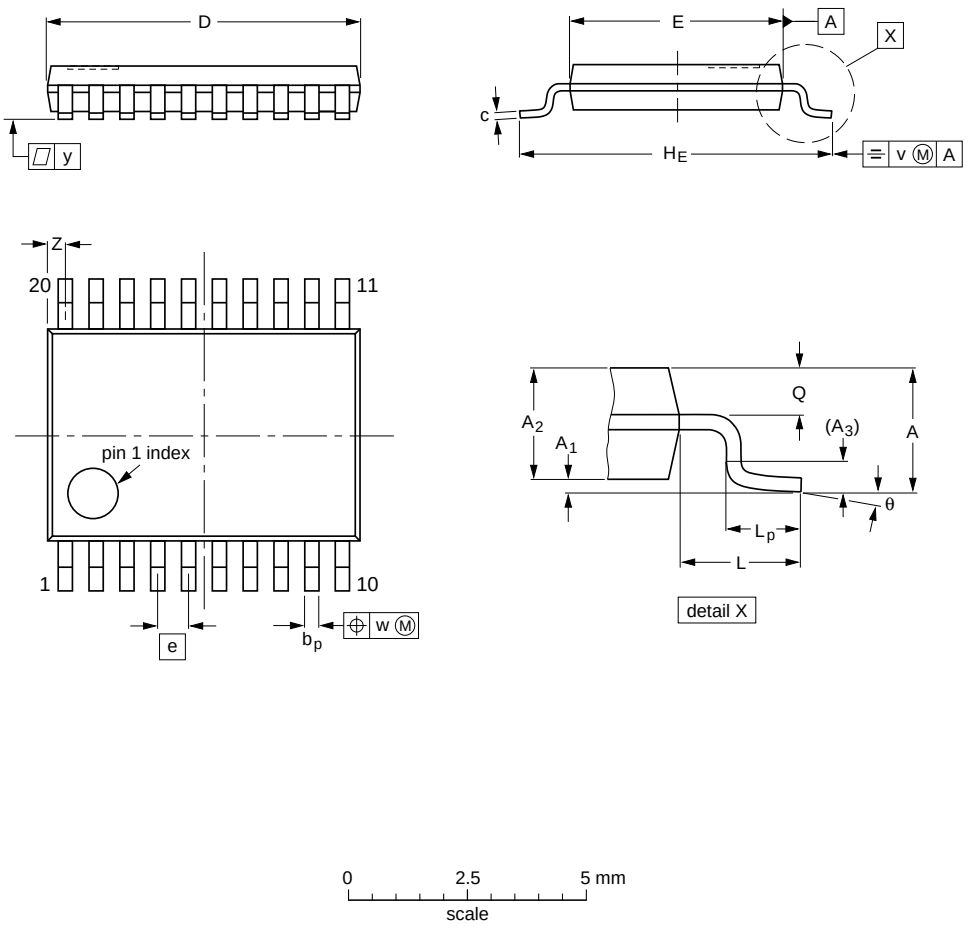
**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT339-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 11. Package outline SOT339-1 (SSOP20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT360-1 (TSSOP20)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| MOS | Metal Oxide Semiconductor |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVT374 v.4 | 20111122 | Product data sheet | - | 74LVT374 v.3 |
| Modifications: | • Legal pages updated. | | | |
| 74LVT374 v.3 | 20110914 | Product data sheet | - | 74LVT374 v.2 |
| 74LVT374 v.2 | 19980219 | product specification | - | 74LVT374 v.1 |
| 74LVT374 v.1 | 19960208 | product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 15.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 15.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 17. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 22 November 2011**
**Document identifier: 74LVT374**

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

74LVT374D 74LVT374D-T 74LVT374DB 74LVT374DB-T 74LVT374PW 74LVT374PW-T