

TSW4200 Demonstration Kit

Contents

1	Introduction	2
2	Software	5
3	Quick Setup	6
4	Adapter Reference	7
5	Notes on Interfacing with Xilinx 7-Series FPGA	7

List of Figures

1	TSW4200 Demonstration Kit	2
2	DAC3283 EVM Block Diagram.....	3
3	ADS62P49 EVM Block Diagram	4
4	DAC3283 EVM Software Configuration.....	6

List of Tables

1	TSW4200 Demonstration Kit Reference Materials	2
2	TSW4200-DAC Default Jumper Setting	4
3	TSW4200-ADC Default Jumper Setting	5

1 Introduction

1.1 Overview

This is the user's guide for the TSW4200 Demonstration Kit. The kit includes two EVMs: TSW4200-DAC and TSW4200-ADC, and they provide evaluation to TI's DAC3283 and ADS62P49, respectively. Through the included FMC adapter boards, the EVMs are ideally suited for mating with a FPGA development board to evaluate the DAC and the ADC as a basic transmitter and receiver system. For more information regarding the individual device or EVM, refer to [Table 1](#) for the respective device's datasheet and EVM user's guide.

Table 1. TSW4200 Demonstration Kit Reference Materials

	Device	Data Sheet	EVM	User's Guide
TSW4200-DAC	DAC3283	SLAS693	DAC328xEVM	SLAU311
TSW4200-ADC	ADS62P49	SLAS635	ADS62PxxEVM	SLAU237

The included FMC adapters are the FMC-DAC-Adapter and the FMC-ADC-Adapter. They are a type of passive interconnect board enabling direct connection of the output of TI's LVDS high speed DACs or ADCs to a standard FMC interconnect header. The FMC interconnect header is a typical input on the latest Xilinx FPGA EVMs. The TSW4200-DAC EVM uses the FMC-DAC-Adapter, and the TSW4200-ADC uses the FMC-ADC-Adapter.

Note: Use the adapters with the latest revision update:

FMC-DAC-Adapter (rev. A or later)
FMC-ADC-Adapter (rev. C or later)
HSMC-ADC-Bridge (rev. B or later)

1.2 TSW2400 Demonstration Kit Block Diagram

[Figure 1](#) shows the configurations of the TSW4200-DAC and TSW4200-ADC EVM with the FPGA development board. [Section 3](#) covers the setup information of the EVMs.

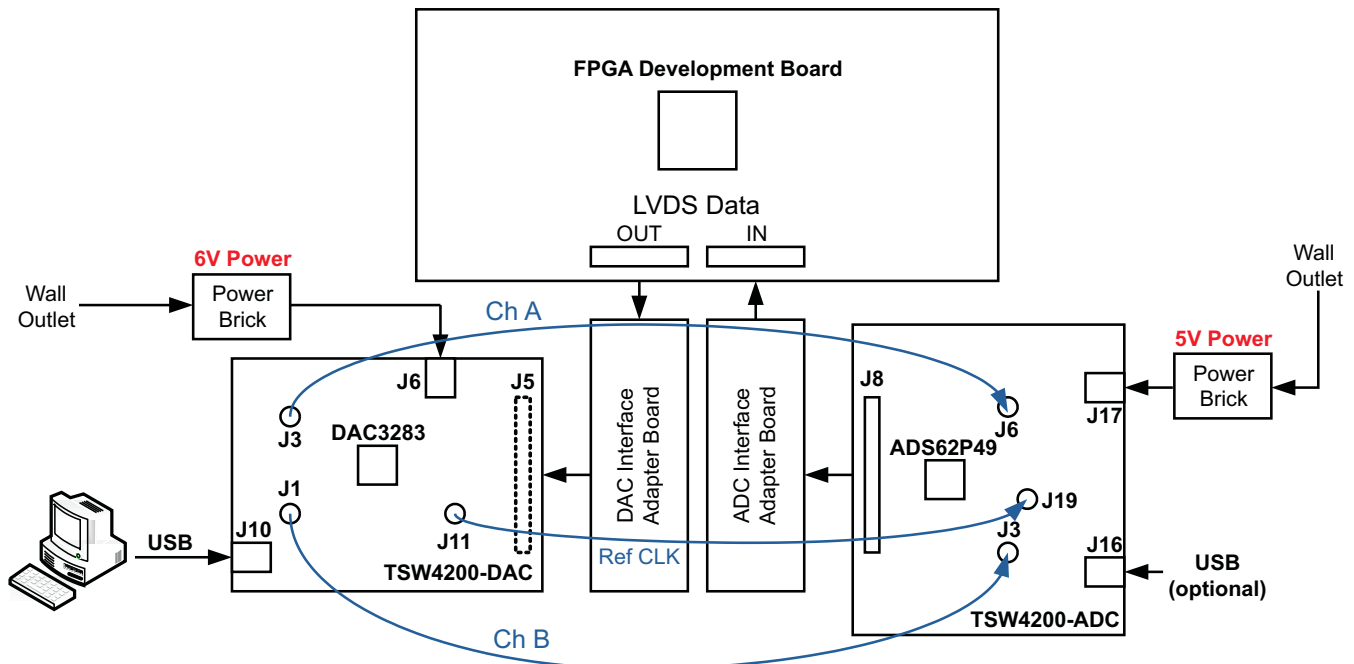


Figure 1. TSW4200 Demonstration Kit

1.3 TSW4200-DAC Configuration

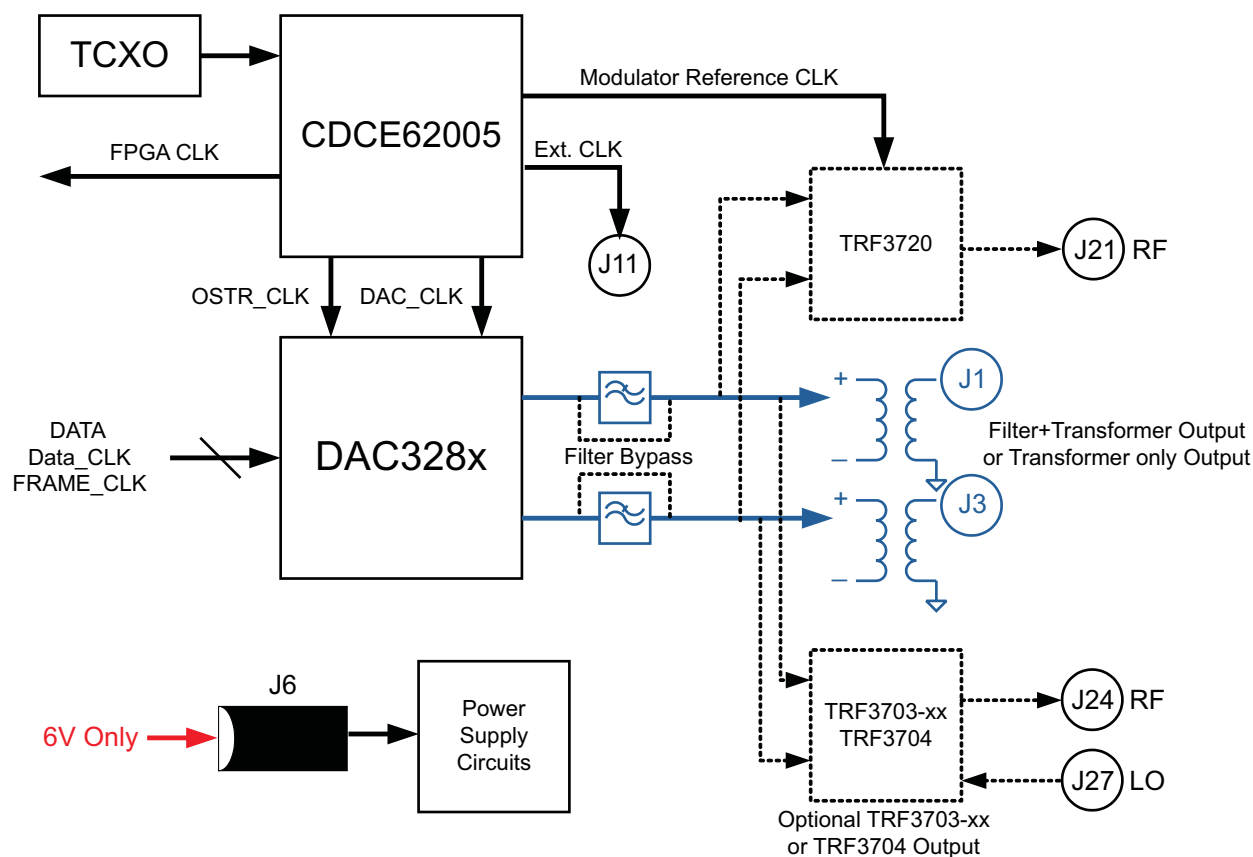


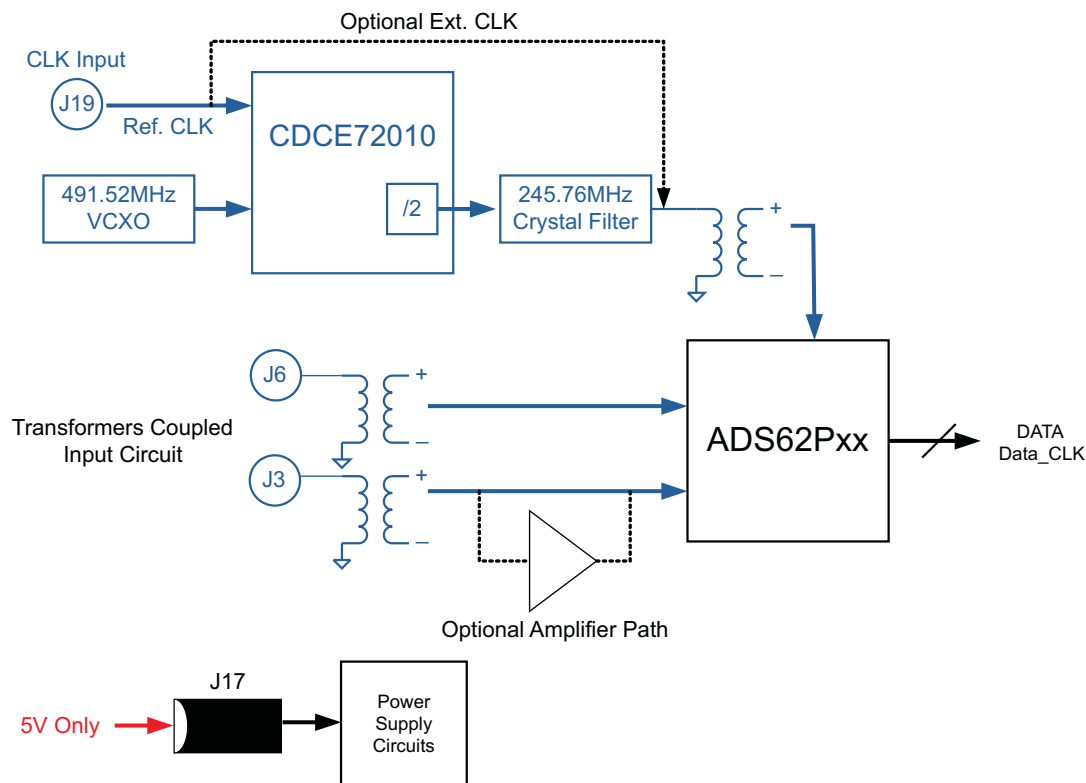
Figure 2. DAC3283 EVM Block Diagram

1. The TSW4200-DAC kit is a DAC3283EVM configured as follow:
 - (a) Power Supply Option: The kit includes a **6-V power supply** input to power supply jack J6. For proper EVM operation and to prevent damage to the EVM, only use a 6-V power supply.
 - (b) Analog Output Option: The on-board DAC3283 has dual-channel outputs that go through a filter network and transformer to J3 (Ch. A) and J1 (Ch. B).
 - (c) Clock Option: The on-board CDC62005 provides clocks to all the on-board devices.
 - (i) The default DAC clock is configured at 614.4 MHz. The DAC interpolation, FPGA clock (TSW3100 CLK), and the FIFO OSTR clock can be configured based on the data rate, FPGA configuration, and system requirement. For more information, please refer to the [DAC3283](#) datasheet.
 - (ii) The TSW4200-DAC has a clock output at J11 that provides the reference clock for the CDC62005 on the TSW4200-ADC at J19. The default reference clock should be configured as 19.2 MHz.
2. The EVM has the default jumper setting listed on [Table 2](#).
3. For more details, refer to the DAC3283EVM User's Guide ([SLAU311](#)).

Table 2. TSW4200-DAC Default Jumper Setting

Jumper	Default Position	Purpose
JP22	2-3	CDCE62005 (U4) external reference clock bias
JP19	Shorted	Enable TCXO (U7)
JP9	1-2	DAC3283 (U1) TXENABLE
JP20	1-2	CDCE62005 (U4) power down
JP21	1-2	CDCE62005 (U4) reference select
JP13	2-3	TRF3720 (U3) power save
JP17	1-2 (TRF3720)	TRF3720 (U3) or TRF3703 (U10) Power Path

1.4 TSW4200-ADC Configuration


Figure 3. ADS62P49 EVM Block Diagram

- TSW4200-ADC Configuration:
 - Power Supply Option:** The kit includes a **5-V power supply** input to power supply jack J17. For proper EVM operation and to prevent damage to the EVM, only use a 5-V power supply.
 - Analog Input Option:** The on-board ADS62P49 has dual-channel transformer-coupled inputs from J3 (Ch. A) and J6 (Ch. B).
 - Clock Option:** The on-board CDCE72010 provides a crystal-filtered LVCMOS clock at 245.76 MHz to the on-board ADS62P49. The reference clock input of 19.2 MHz to the TSW4200-ADC is at J19. The CDCE72010 is configured in PLL mode by default using the on-board 491.52-MHz VCXO. The CDCE72010's output has the divider configured to be divide-by-2, dividing the 491.52-MHz VCXO clock to the required 245.76-MHz clock.
- The EVM has the default jumper setting listed on [Table 3](#).
- For more details, refer to the ADS62PXXEVM User's Guide ([SLAU237](#)).

Table 3. TSW4200-ADC Default Jumper Setting

Jumper	Default Position	Purpose
JP11	1-2 (parallel)	ADS62P49 (U2) parallel or serial mode option
JP8	1-2 (parallel)	SCLK parallel or serial mode option
JP12	1-2 (0dB gain, int. ref.)	SCLK parallel mode select
JP9	1-2 (parallel)	SDATA parallel or serial mode option
JP13	Open	SDATA parallel mode option
JP10	1-2 (parallel)	SEN parallel or serial mode select
JP14	1-2 (2's complement & DDR LVDS)	SEN parallel mode option
JP20	1-2	CDCE72010 (U10) AUX select
JP21	1-2	CDCE72010 (U10) MODE select
J14	Open	CDCE72010 (U10) power down
J15	Open	CDCE72010 (U10) reset
JP3	2-3 (Off)	THS4509 (U1) power down
JP23	1-2	USB microcontroller (U6) power select
J18	Open	VCXO (VCXO1) enable
JP16	1-2	Power option (see schematic or ADS62PXX EVM user's guide)
JP17	Open	Power option (see schematic or ADS62PXX EVM user's guide)
JP19	1-2	Power option (see schematic or ADS62PXX EVM user's guide)
JP15	1-2	Power option (see schematic or ADS62PXX EVM user's guide)
JP18	1-2	Power option (see schematic or ADS62PXX EVM user's guide)
JP22	1-2	FPGA SDOUT path
JP5	1-2 (Low)	ADS62P49 (U2) CTRL3
JP6	1-2 (Low)	ADS62P49 (U2) CTRL2
JP7	1-2 (Low)	ADS62P49 (U2) CTRL1

2 Software

See the DAC3283 and the ADS62P49 EVM user's guide for more detailed explanations of the EVM setup and operation. This document assumes that EVM software applications are installed and functioning properly.

Be sure to use the latest EVM software available at www.ti.com. For the TSW4200 Demonstration Kit evaluation, only the DAC3283 EVM software is needed. The ADS62P49 EVM software is optional since the on-board jumpers provide sufficient control of the ADC.

3 Quick Setup

1. For the DAC EVM, connect the 6-V supply to J6. Connect the EVM to a PC through a USB cable to utilize the EVM software.
 - (a) Start the DAC3283 EVM software, select the *Top Level* tab and press the **Reset USB Port** button.
 - (b) Configure the *Top Level* tab the same as shown in [Figure 4](#). Set *Test Port Div* to 32 to set the reference frequency of 19.2 MHz. All other settings remain in default values. Configure the DAC interpolation, FPGA clock (TSW3100 CLK), and the FIFO OSTR clock based on the data rate, FPGA configuration, and system requirement. For more information, please refer to the [DAC3283](#) datasheet.

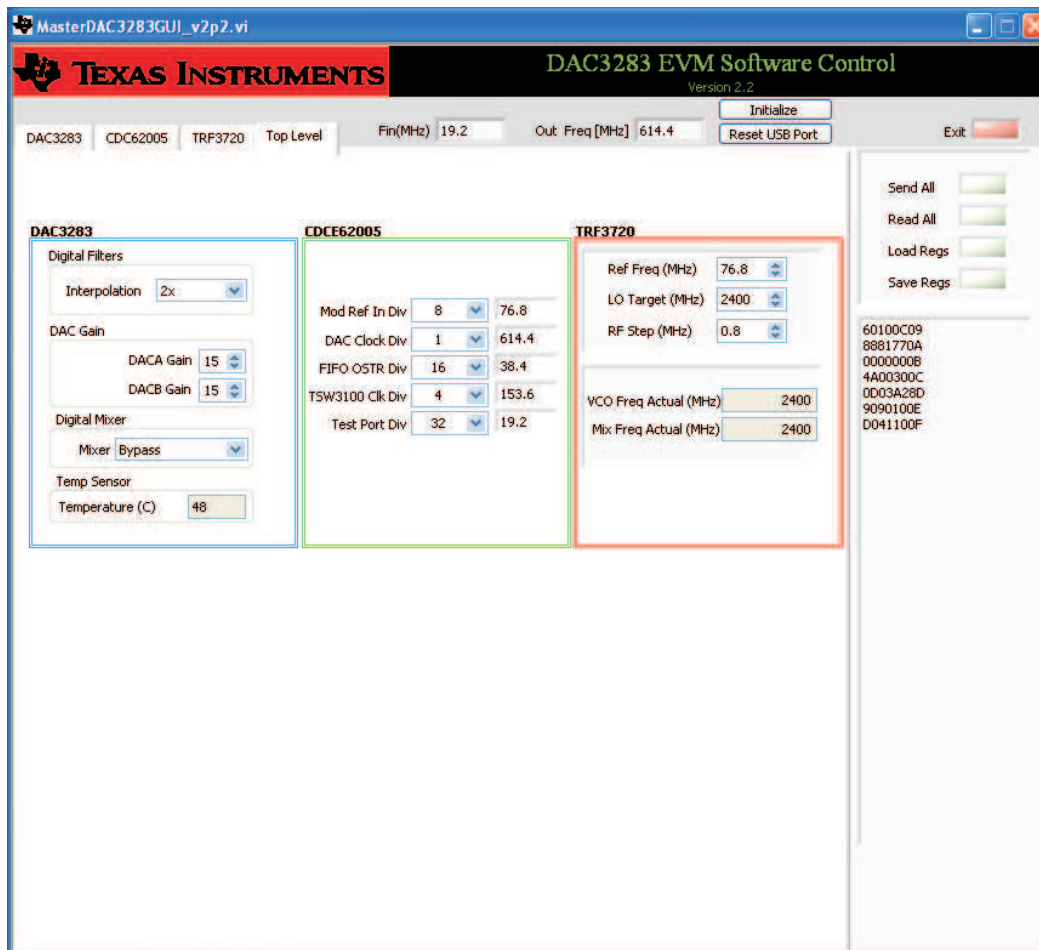


Figure 4. DAC3283 EVM Software Configuration

- (c) Pressing *Send All*, sends all the instructions to the DAC3283 EVM.
 - (d) Toggle the **Initialize** button. This initializes the CDC62005 clock.
 - (e) Verify that the CDC62005 LED (D4) is illuminated, indicating lock.
2. For the ADC EVM, connect the 5-V supply to J17. The USB connection to ADC EVM is optional. The default ADS62P49 operates with internal reference and has 2's complement, LVDS output.
3. Connect the ADC and DAC EVMs to the FPGA solution through the provided adapter boards. See [Section 4](#), the Adapter Reference section, for details.
4. Connect the external reference clock output of the DAC EVM at J11 to the reference clock input of the ADC EVM at J19. The reference clock should be at 19.2 MHz.
5. Connect the DAC EVM output at J1 and J3 to the ADC EVM input at J3 and J6. See [Figure 1](#) for details.

6. Start evaluating the TSW4200 Demonstration Kit by configuring the FPGA to transmit data to the DAC EVM and receive data from the ADC EVM.

4 Adapter Reference

Visit www.ti.com for more information on the following adapter board options.

- FMC-ADC-Adapter, <http://focus.ti.com/docs/toolsw/folders/print/fmc-adc-adapter.html>
- FMC-DAC-Adapter, <http://focus.ti.com/docs/toolsw/folders/print/fmc-dac-adapter.html>
- HSMC-ADC-Bridge, <http://focus.ti.com/docs/toolsw/folders/print/hsmc-adc-bridge.html>

5 Notes on Interfacing with Xilinx 7-Series FPGA

The connections between the TSW4200 kit and FMC (HPC or LPC) connectors on a Xilinx 7-Series FPGA EVM spread the input/output buses of the ADC/DAC over two IO-banks. This makes it necessary to use the BUFMR clock buffer in the FPGA in order to clock data in multiple clock regions.

For detailed information about this clock buffer, refer to the *7-Series FPGA Clocking Resources User Guide* (Xilinx UG472, Multi-Region Clocking). The use case *Driving Multiple BUFMRs (with Divide) and BUFIO* in particular, provides extensive details over the implementation.

In an actual end-user system implementation, ADC and DAC connections to the FPGA should utilize a single FPGA IO-bank for a simpler approach.

For an ADC with serial LVDS output implementation, half of an IO-bank can handle all connections from the ADC:

- Connect the bit clock DCLK_p/n to a MRCC differential clock input.
- Connect the frame clock FCLK_p/n to the neighbor SRCC differential clock input.
- Connect all data inputs to normal differential inputs starting from the FCLK_p/n.

For a DAC with parallel LVDS input implementation, connections to the FPGA often use several data buses, and an optimal connection can be made as:

- Connect the clock coming from the DAC, from the VCXO, or other clocking device to a MRCC differential input.
- Connect the clock and data connections to the DAC in the same IO-bank and neighbor (above and below) IO-banks.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

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This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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