B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

MC14001B Series

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to $+125$	°C
T_{stg}	Storage Temperature Range	-65 to $+150$	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C
V_{ESD}	ESD Withstand Voltage Human Body Model Machine Model Charged Device Model	> 3000 > 300 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65 °C to 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SOIC-14
D SUFFIX
CASE 751A

TSSOP-14
DT SUFFIX
CASE 948G

MARKING DIAGRAMS

14	140xxBG AWLYWW
1	

SOIC-14

14	14 0xxB ALYW▪
1	
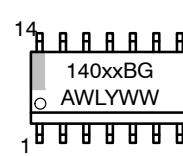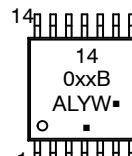
TSSOP-14

xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

DEVICE INFORMATION

Device	Description
MC14001B	Quad 2-Input NOR Gate
MC14011B	Quad 2-Input NAND Gate
MC14023B	Triple 3-Input NAND Gate
MC14025B	Triple 3-Input NOR Gate
MC14071B	Quad 2-Input OR Gate
MC14073B	Triple 3-Input AND Gate
MC14081B	Quad 2-Input AND Gate
MC14082B	Dual 4-Input AND Gate

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MC14001B Series

LOGIC DIAGRAMS

NOR	NAND	OR	AND

MC14001B
Quad 2-Input NOR Gate

MC14011B
Quad 2-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14081B
Quad 2-Input AND Gate

2 INPUT

MC14025B
Triple 3-Input NOR Gate

MC14023B
Triple 3-Input NAND Gate

MC14073B
Triple 3-Input AND Gate

MC14082B
Dual 4-Input AND Gate

3 INPUT

NC = 6, 8
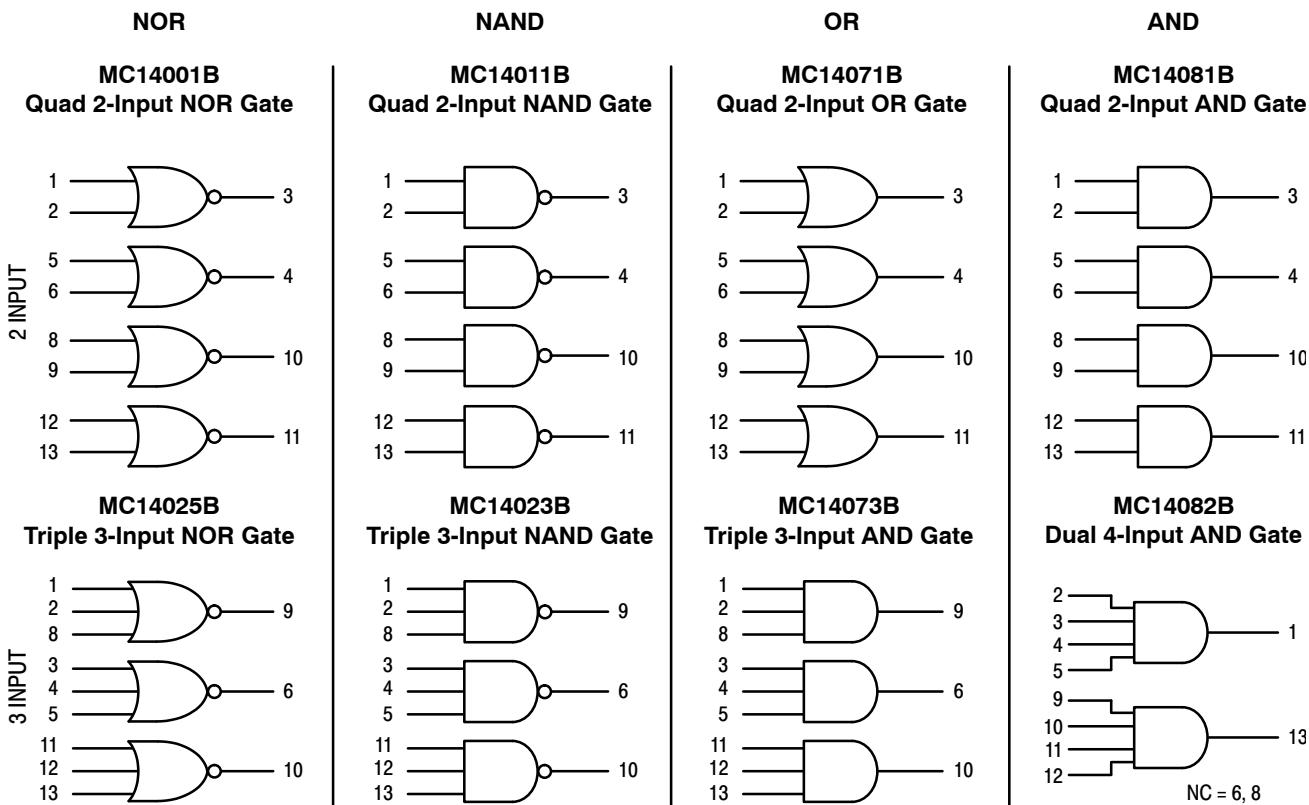
V_{DD} = PIN 14
V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

MC14001B
Quad 2-Input NOR Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 2_D
OUT_A	3	12	IN 1_D
OUT_B	4	11	OUT_D
IN 1_B	5	10	OUT_C
IN 2_B	6	9	IN 2_C
V_{SS}	7	8	IN 1_C

MC14011B
Quad 2-Input NAND Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 2_D
OUT_A	3	12	IN 1_D
OUT_B	4	11	OUT_D
IN 1_B	5	10	OUT_C
IN 2_B	6	9	IN 2_C
V_{SS}	7	8	IN 1_C

MC14023B
Triple 3-Input NAND Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 3_C
IN 1_B	3	12	IN 2_C
IN 2_B	4	11	IN 1_C
IN 3_B	5	10	OUT_C
OUT_B	6	9	OUT_A
V_{SS}	7	8	IN 3_A

MC14025B
Triple 3-Input NOR Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 3_C
IN 1_B	3	12	IN 2_C
IN 2_B	4	11	IN 1_C
IN 3_B	5	10	OUT_C
OUT_B	6	9	OUT_A
V_{SS}	7	8	IN 3_A

MC14071B
Quad 2-Input OR Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 2_D
OUT_A	3	12	IN 1_D
OUT_B	4	11	OUT_D
IN 1_B	5	10	OUT_C
IN 2_B	6	9	IN 2_C
V_{SS}	7	8	IN 1_C

MC14073B
Triple 3-Input AND Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 3_C
IN 1_B	3	12	IN 2_C
IN 2_B	4	11	IN 1_C
IN 3_B	5	10	OUT_C
OUT_B	6	9	OUT_A
V_{SS}	7	8	IN 3_A

MC14081B
Quad 2-Input AND Gate

IN 1_A	1 ●	14	V_{DD}
IN 2_A	2	13	IN 2_D
OUT_A	3	12	IN 1_D
OUT_B	4	11	OUT_D
IN 1_B	5	10	OUT_C
IN 2_B	6	9	IN 2_C
V_{SS}	7	8	IN 1_C

MC14082B
Dual 4-Input AND Gate

OUT_A	1 ●	14	V_{DD}
IN 1_A	2	13	OUT_B
IN 2_A	3	12	IN 4_B
IN 3_A	4	11	IN 3_B
IN 4_A	5	10	IN 2_B
NC	6	9	IN 1_B
V_{SS}	7	8	NC

NC = NO CONNECTION

MC14001B Series

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55 °C Min	−55 °C Max	25 °C Min	25 °C Typ (Note 2)	25 °C Max	125 °C Min	125 °C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current Source (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	– – – –	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	– – – –	−1.7 −0.36 −0.9 −2.4	– – – –	mAdc
Sink (V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	µAdc
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0 10 15	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/N$ $I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/N$ $I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/N$							µAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25 °C.
4. To calculate total supply current at loads other than 50 pF:
   $I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$
   where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} − V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

B-SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25 °C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time, All B-Series Gates t_{TLH} = (1.35 ns/pF) C_L + 33 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/PF) C_L + 20 ns	t_{TLH}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Output Fall Time, All B-Series Gates t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns

Propagation Delay Time
MC14001B, MC14011B only
    t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns
    t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns
    t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns
All Other 2, 3, and 4 Input Gates
    t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns
    t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns
    t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns
8–Input Gates (MC14068B, MC14078B)
    t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns
    t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns
    t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns
	t_{PLH}, t_{PHL}	
		
		5.0
		10
		15
		
		5.0
		10
		15
		
		5.0
		10
		15
			
			–
			–
			–
			
			–
			–
			–
			
			–
			–
			–
				
				125
				50
				40
				
				160
				65
				50
				
				200
				80
				60
					
					250
					100
					80
					
					300
					130
					100
					
					350
					150
					110
						ns

5. The formulas given are for the typical characteristics only at 25 °C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
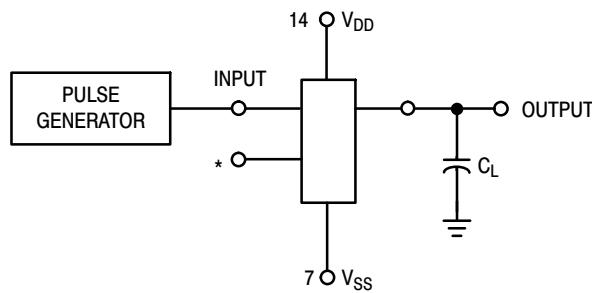
* All unused inputs of AND, NAND gates must be connected to V_{DD}.
  All unused inputs of OR, NOR gates must be connected to V_{SS}.
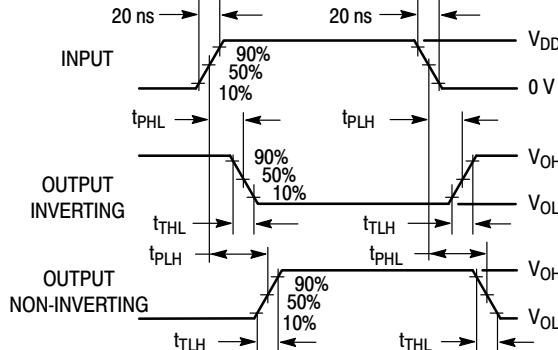
Figure 1. Switching Time Test Circuit and Waveforms

MC14001B Series

CIRCUIT SCHEMATIC
NOR, OR GATES

MC14001B, MC14071B
One of Four Gates Shown

* Inverter omitted in MC14001B
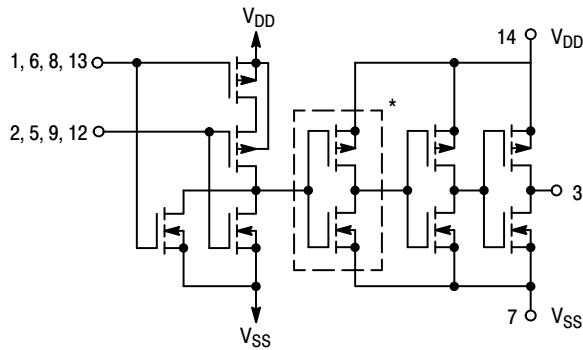
MC14025B
One of Three Gates Shown

* Inverter omitted in MC14025B
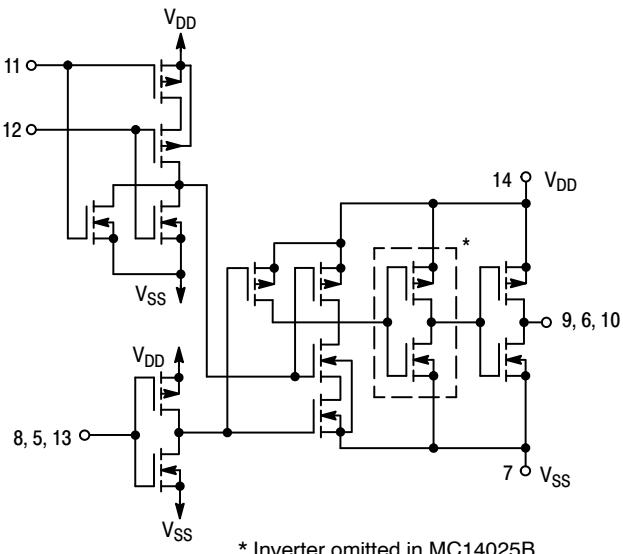
CIRCUIT SCHEMATIC
NAND, AND GATES

MC14023B, MC14073B
One of Three Gates Shown

* Inverter omitted in MC14023B
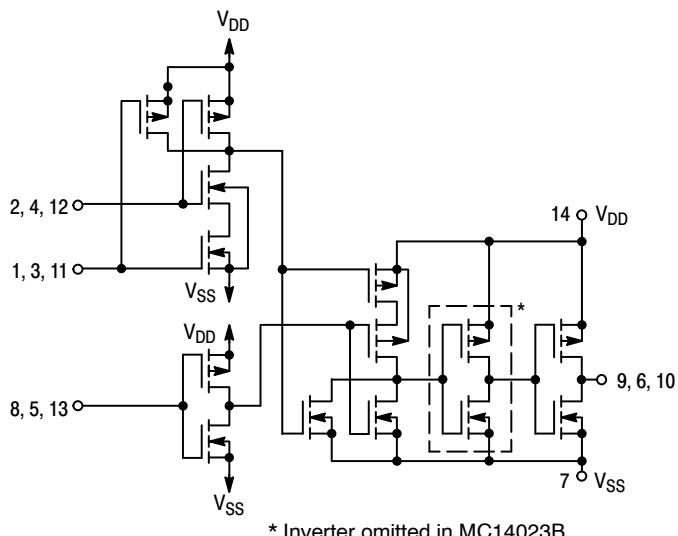
MC14011B, MC14081B
One of Four Gates Shown

* Inverter omitted in MC14011B

MC14001B Series

TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)
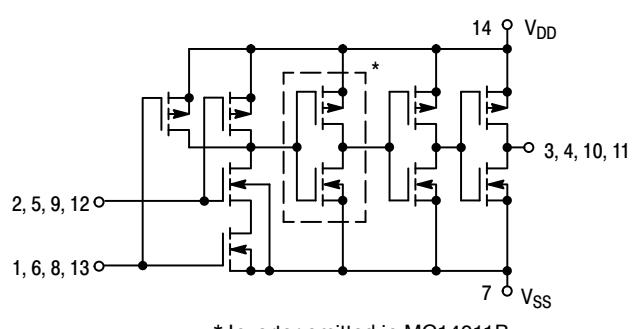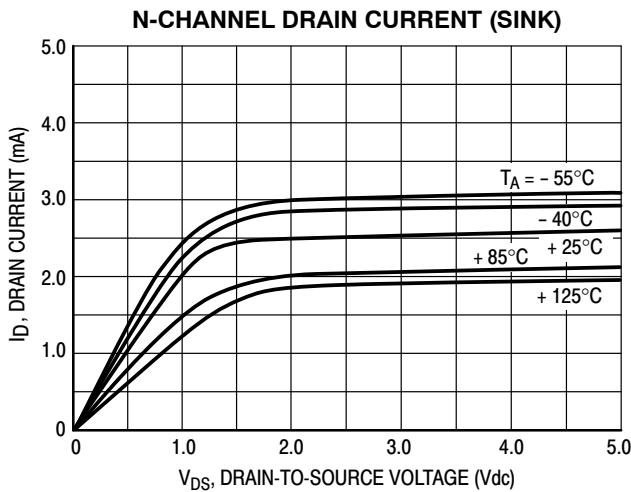
Figure 2. V_{GS} = 5.0 Vdc
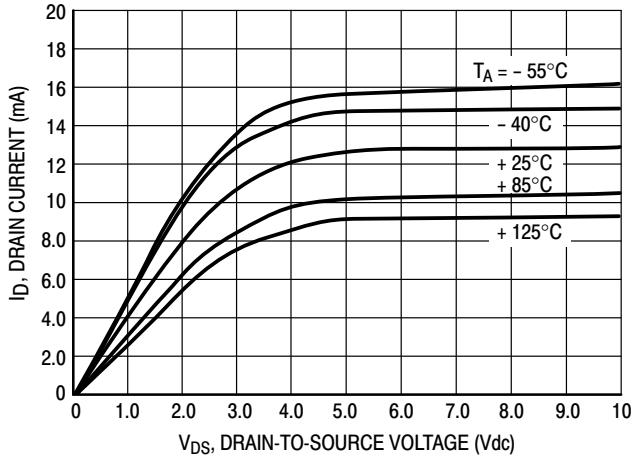
Figure 4. V_{GS} = 10 Vdc

Figure 6. V_{GS} = 15 Vdc

P-CHANNEL DRAIN CURRENT (SOURCE)

Figure 3. V_{GS} = −5.0 Vdc
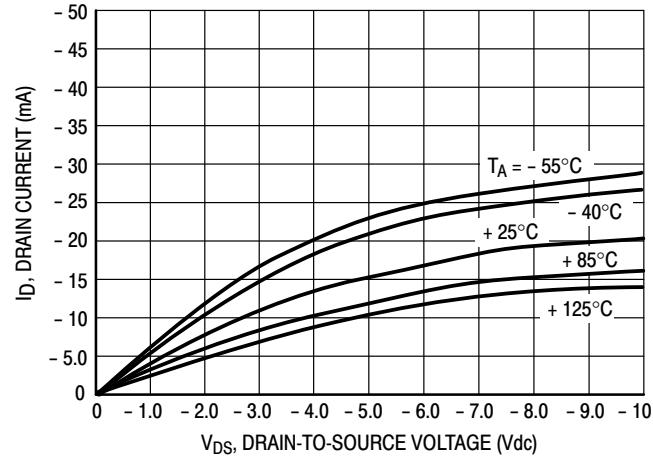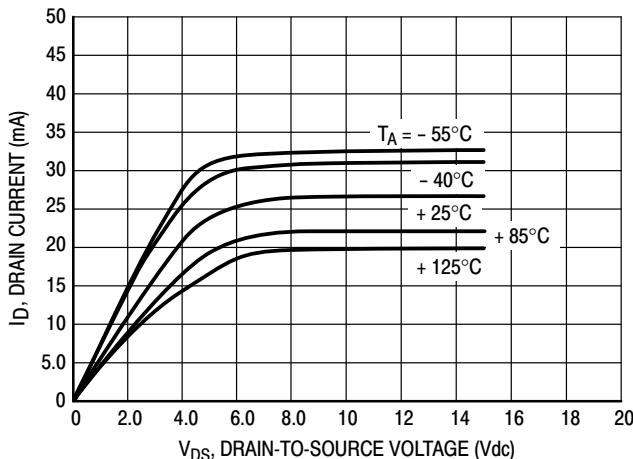
Figure 5. V_{GS} = −10 Vdc
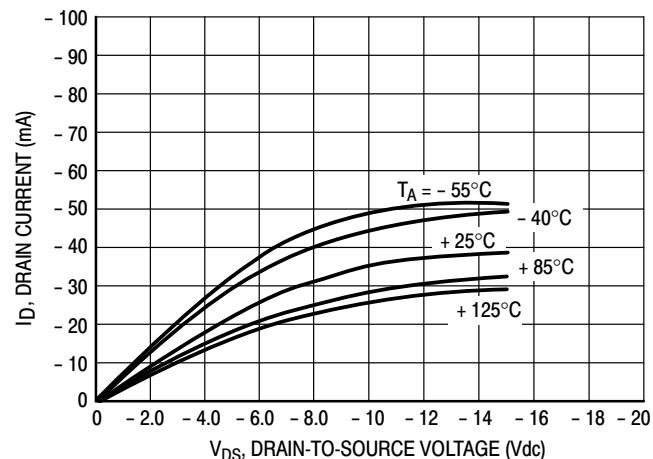
Figure 7. V_{GS} = −15 Vdc

These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B−SERIES GATE CHARACTERISTICS (CONT'D)

VOLTAGE TRANSFER CHARACTERISTICS

Figure 8. V$_{DD}$ = 5.0 Vdc

Figure 9. V$_{DD}$ = 10 Vdc

Figure 10. V$_{DD}$ = 15 Vdc
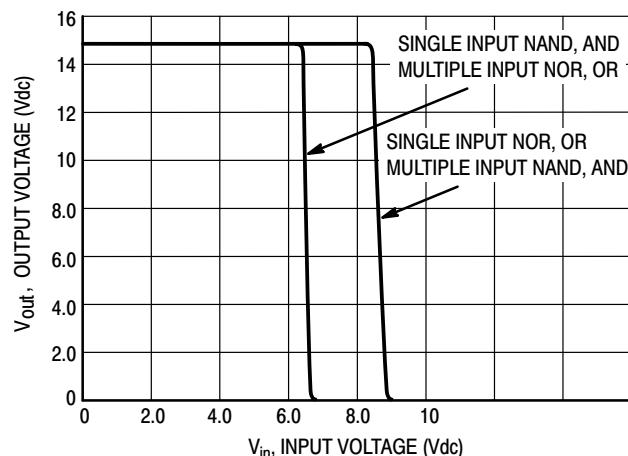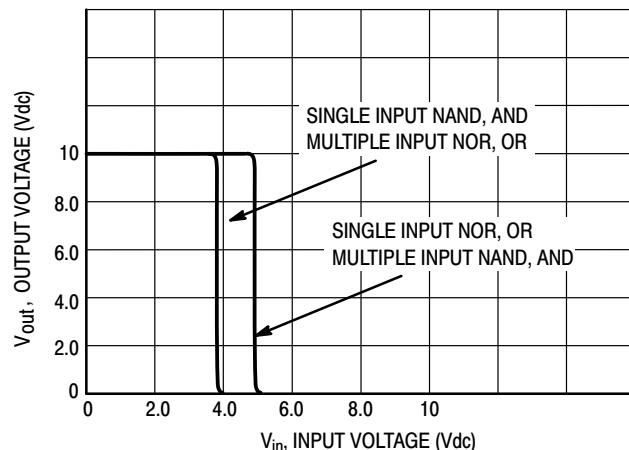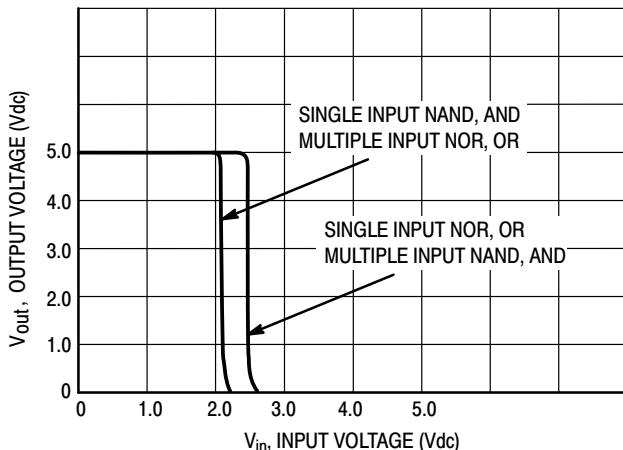
DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

    1.0 V with a 5.0 V supply
    2.0 V with a 10.0 V supply
    2.5 V with a 15.0 V supply

(a) Inverting Function   **(b) Non-Inverting Function**
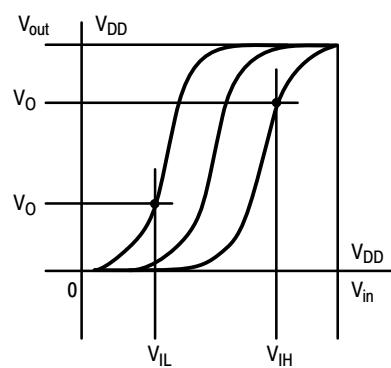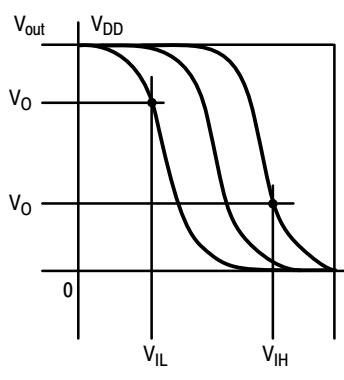
Figure 11. DC Noise Immunity

ORDERING INFORMATION

Device	Package	Shipping†
MC14001BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14001BDG*		
MC14001BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14001BDR2G*		
MC14001BDTR2G	TSSOP-14 (Pb-Free)	
NLV14001BDTR2G*		
MC14001BFELG	SOEIAJ-14 (Pb-Free)	2000 Units / Tape & Reel

Device	Package	Shipping†
MC14011BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14011BDG*		
MC14011BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14011BDR2G*		
MC14011BDTR2G	TSSOP-14 (Pb-Free)	
NLV14011BDTR2G*		
MC14011BFG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC14011BFELG		2000 Units / Tape & Reel

Device	Package	Shipping†
MC14023BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14023BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14023BDR2G*		
MC14023BFELG	SOEIAJ-14 (Pb-Free)	2000 Units / Tape & Reel

Device	Package	Shipping†
MC14025BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14025BDG*		
MC14025BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14025BDR2G*		

Device	Package	Shipping†
MC14071BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14071BDG*		
MC14071BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14071BDR2G*		
MC14071BDTG	TSSOP-14 (Pb-Free)	96 Units per Rail
MC14071BDTR2G		2500 Units / Tape & Reel
NLV14071BDTR2G*		

Device	Package	Shipping†
MC14073BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14073BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel

ORDERING INFORMATION (continued)

Device	Package	Shipping†
MC14081BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14081BDG*		
MC14081BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14081BDR2G*		
MC14081BDTR2G	TSSOP-14 (Pb-Free)	
NLV14081BDTR2G*		

Device	Package	Shipping†
MC14082BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14082BDG*		
MC14082BDR2G		2500 Units / Tape & Reel
NLV14082BDR2G*		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

REVISION HISTORY

Revision	Description of Changes	Date
13	Adding NLV14082BDR2G device into Ordering Information table.	11/14/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.
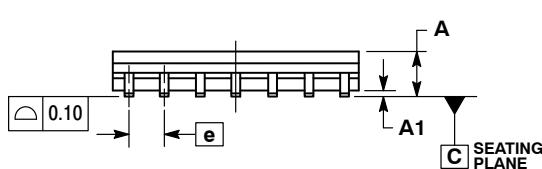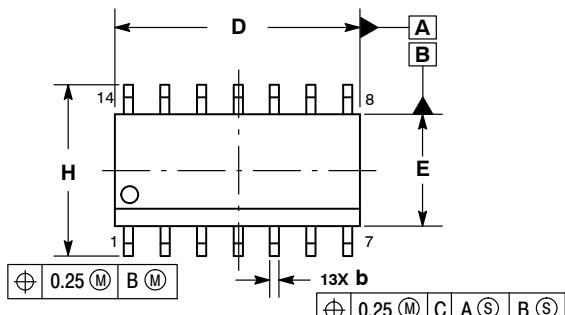
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

13X b

0.25 (M) C A (S) B (S)

DETAIL A

X 45°

DETAIL A

SEATING PLANE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°
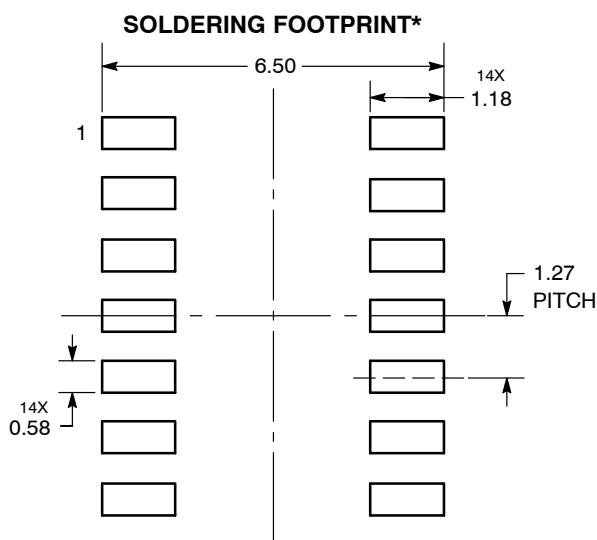
SOLDERING FOOTPRINT*

6.50

14X 1.18

1.27 PITCH

14X 0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*
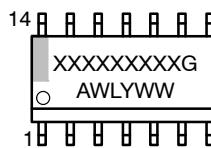
XXXXXXXXXG
AWLYWW

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "∎", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

| DOCUMENT NUMBER:	98ASB42565B		
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X K REF

$\bigoplus$ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

0.15 (0.006) | T | U Ⓢ

2X L/2

L

PIN 1 IDENT.

14   8

1   7

A

−V−

0.15 (0.006) | T | U Ⓢ

B
−U−

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1

SECTION N−N

C

0.10 (0.004)

−T− SEATING PLANE

D   G   H

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*

7.06

1

0.65 PITCH

14X 0.36

14X 1.26

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXX
XXXX
ALYW▪

○   ▪

1
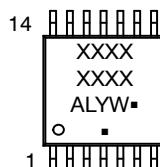
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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