VITESSE

VSC7959
Data Sheet

CML Limiting Amplifier with LOS Detect

FEATURES

- +3.3V or +5V Power Supply
- Typical Supply Current of 29mA
- Current-Mode Logic Outputs
- Optional Output Squelch
- Loss of Signal Detect
- Output Offset Correction
- Typical Rise/Fall Times of 80ps
- Available in 24-Pin QFP-N, TSSOP-16, and Bare Die

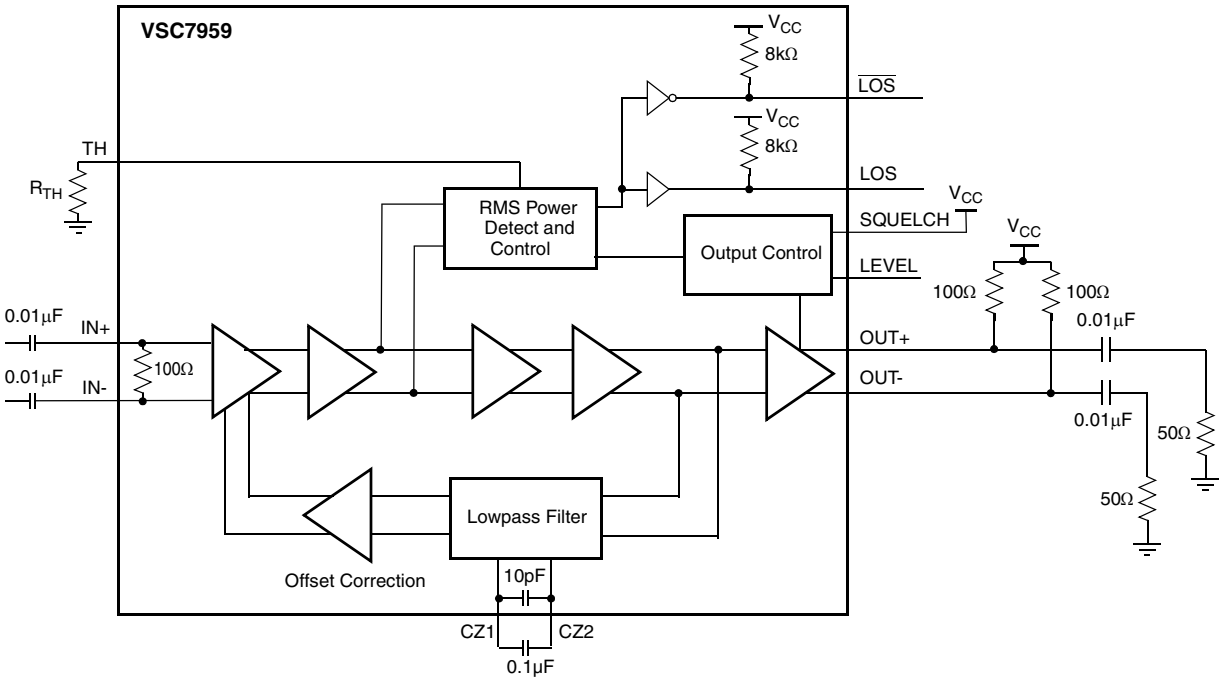
APPLICATIONS

- SONET/SDH at 155MHz, 622Mb/s, 1.244Gb/s, 2.488Gb/s
- Full-Speed Fibre Channel (1.062Gb/s/2.124Gb/s)
- Small Form Factor Transceivers
- ATM Optical Receivers

GENERAL DESCRIPTION

The VSC7959 is a single-supply limiting amplifier with Loss of Signal (LOS) detect for SONET/SDH and Fibre Channel applications up to 2.5Gb/s. The VSC7959 provides a constant output signal swing for a wide range of input voltages and has Common-Mode Logic (CML) outputs. Key features of the VSC7959 include the rms power detectors for programmable LOS detection, optional output squelch, excellent jitter performance, and fast edge rates. The VSC7959 is available in die form, a TSSOP-16 package, or a 24-pin QFP-N package.

VSC7959 Block Diagram



ELECTRICAL SPECIFICATIONS

DC Characteristics

Over Recommended Operating Conditions.

Table 1. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}	Power supply voltage	3.135		5.5	V	
I_{CC}	Power supply current[1]		29	37	mA	V_{CC} = 3.3V.
			33	43	mA	V_{CC} = 5V.
I_{EE}	Power supply current including load current[1]		37	45	mA	V_{CC} = 3.3V.
			41	61	mA	V_{CC} = 5V.
I_{CCSQ}	Power supply current when squelched[1]		17	29	mA	V_{CC} = 3.3V.
			20	35	mA	V_{CC} = 5V.
I_{EESQ}	Power supply current including load current when squelched[1]		18	30	mA	V_{CC} = 3.3V.
			21	36	mA	V_{CC} = 5V.
I_{SQ}	Squelch input current	0		400	µA	
PSRR	Power supply rejection ratio	20	30		dB	f < 2MHz, V_{IN} = 100mV.

1. *See Figure 1 for supply current measurement setup.*

AC Characteristics

Over Recommended Operating Conditions. All AC voltage measurements are differential peak-to-peak, unless otherwise noted.

Table 2. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
	Maximum data rate	2.5			Gb/s	
V_{IN}	Input voltage range	5		1200	mV	
J_D	Deterministic jitter[1]			30	ps	V_{IN} >10mV.
			45		ps	V_{IN} = 5mV differential, V_{CC} = +3.3V.
J_R	Random jitter[2]			8	ps	RMS, V_{IN} > 10mV.
			10		ps	V_{IN} = 5mV differential, V_{CC} = +3.3V.
t_R, t_F	Rise and fall times		80	110	ps	20% to 80%, V_{IN} >10mV.
			130		ps	20% to 80%, V_{IN} = 5mV differential.
V_N	Input referred noise		100		µV	RMS, IN+ to IN–.
R_{DIFF}	Differential input resistance		100		Ω	IN+ to IN–.
f_L	Low frequency cut-off		210		kHz	C_Z open.
				10	kHz	C_Z = 0.1µF.
V_{SQ}	Output signal when squelched		20		mV	Output AC-coupled.

Table 2. AC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CML}	CML output voltage	550	700	1200	mV	LEVEL = open, $R_L = 50\Omega$[3]. V_{IN} >10mV. See "Voltage Inputs vs.Voltage Output" in "Typical Operating Characteristics" on page 7.
		1100		1800	mV	LEVEL = GND, $R_L = 75\Omega$.
				20	mV	Squelched.
			560		mV	V_{IN} = 5mV differential, V_{CC} = +3.3V.
Z_O	Output tesistance		100		Ω	Single-ended.

1. *Deterministic jitter measured peak-to-peak with K28.5 pattern.*
2. *Random jitter measured with minimum input.*
3. *Connect LEVEL to GND for higher output voltage.*

Table 3. Loss of Signal Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Condition
H_{LOS}	LOS hystersis	2.2	4.0	5.5	dB	H_{LOS} = 20 log (V_{THD}/V_{THA}) K28.5 pattern.
t_{LOS}	LOS assert/deassert time		1.0		µs	Response time for a 10dB change in input power.
V_{THA}	LOS assert threshold	15			mV	R_{TH} = 5.6kΩ, f = 2.5Gb/s, K28.5 pattern.
V_{THD}	LOS deassert threshold			35	mV	R_{TH} = 5.6kΩ, f = 2.5Gb/s, K28.5 pattern.
V_{LOSH}	LOS output HIGH voltage	2.4	3.5		V	I_{LOS} = –30µA.
V_{LOSL}	LOS output LOW voltage			0.3	V	I_{LOS} = 1.2mA.

Table 4. Loss of Signal Truth Table

SQUELCH	LOS	Output
HIGH	LOW	On
LOW	HIGH	On
HIGH	HIGH	Off
LOW	LOW	On

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$V_{CC\_3.3}$	Power supply voltage for 3.3V operation	+3.135	+3.3	+5.5	V	
V_{CC_5}	Power supply voltage for 5V operation	+3.135	+5.0	+5.5	V	
T_J	Junction temperature range	–40		+100	°C	
T	Operating temperature range[1]	–40		+85	°C	

1. Lower limit of specification is ambient temperature and upper limit is case temperature

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power supply voltage	–0.5	+6	V
	Voltage at IN+, IN–	V_{CC} – 3	V_{CC} + 0.5	V
	Voltage at SQUELCH, LOS, $\overline{LOS}$, TH, LEVEL	–0.5	V_{CC} + 0.5	V
	Differential input voltage (IN+, IN–)		2.5	V
	Continuous current at CML outputs (OUT+, OUT–)		25	mA
	Current into LOS, $\overline{LOS}$	–2	+3	mA
T_J	Junction temperature	–55	+125	°C
T_S	Storage temperature	–55	+150	°C
V_{ESD}	ESD voltage (Human Body Model)	–2500	+2500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

FUNCTIONAL DESCRIPTION

The VSC7959 is a high-speed limiting amplifier with LOS detect. The VSC7959 is designed to operate with a +3.3V or +5V supply in SONET/SDH and Fibre Channel applications up to 2.5Gb/s. The VSC7959 has CML outputs. Key features of the VSC7959 are LOS detect, output offset correction, output squelch, low power supply current, and fast rise/fall times.

The inputs of the VSC7959 provide 100Ω input impedance between IN+ and IN– and are intended to be AC-coupled. The CML output circuits are designed to tolerate output impedance mismatches and may be AC- or DC-coupled.

LOS Detect

LOS Detect utilizes an RMS power detector with programmable LOS indicator to provide two outputs, LOS and $\overline{\text{LOS}}$. The input, TH, is used to set the threshold at which the LOS detector outputs (LOS and $\overline{\text{LOS}}$) change state. See Table 3, "Loss of Signal Specifications" on page 3 for setting the resistor value between TH and ground. Table 4, "Loss of Signal Truth Table" on page 3 clarifies the interaction of LOS and SQUELCH.

Optional Squelch

Squelch is disabled when SQUELCH is not connected or is set to TTL low level. When SQUELCH is set to a TTL high level and LOS is asserted, the data outputs, OUT+ and OUT– are forced to static levels. If LOS is not asserted, the outputs will not be squelched.

Offset Correction

The offset correction feature is provided to ensure that the offsets in the limiting amplifier coupled with its gain do not cause the output buffer to give a false output. Because of the high gain of the amplifier, offset correction using a low-frequency feedback loop reduces input offset. If no component is placed between pins CZ1 and CZ2, the low frequency cut-off is 200kHz. If a 0.1µF capacitor is placed between CZ1 and CZ2, the low frequency cut-off is lowered to approximately 2kHz. For Fibre Channel and Gigabit Ethernet applications, leave pins CZ1 and CZ2 open. For ATM/SONET and other scrambled non-return-to-zero (NRZ) applications, place a 0.1µF capacitor between CZ1 and CZ2. This maintains a one-decade separation between the lowest input frequency and the low frequency cut-off. The low frequency cut-off of the offset correction loop is given by the following equation:

$$\begin{aligned} f_{OC} &= 43 / [2\pi * 35k\,(C_Z + 100pF)] \\ &= 196 \bullet 10^{-6} / (C_Z + 100pF) \\ &= 196 \bullet 10^{-6} / (0.1\mu F + 100pF) \\ &= 1.96kHz \end{aligned} \qquad \textbf{(EQ 1)}$$

Output Level Control

The LEVEL pin adjusts the output levels to 20mA when grounded and to 16mA when left unconnected.

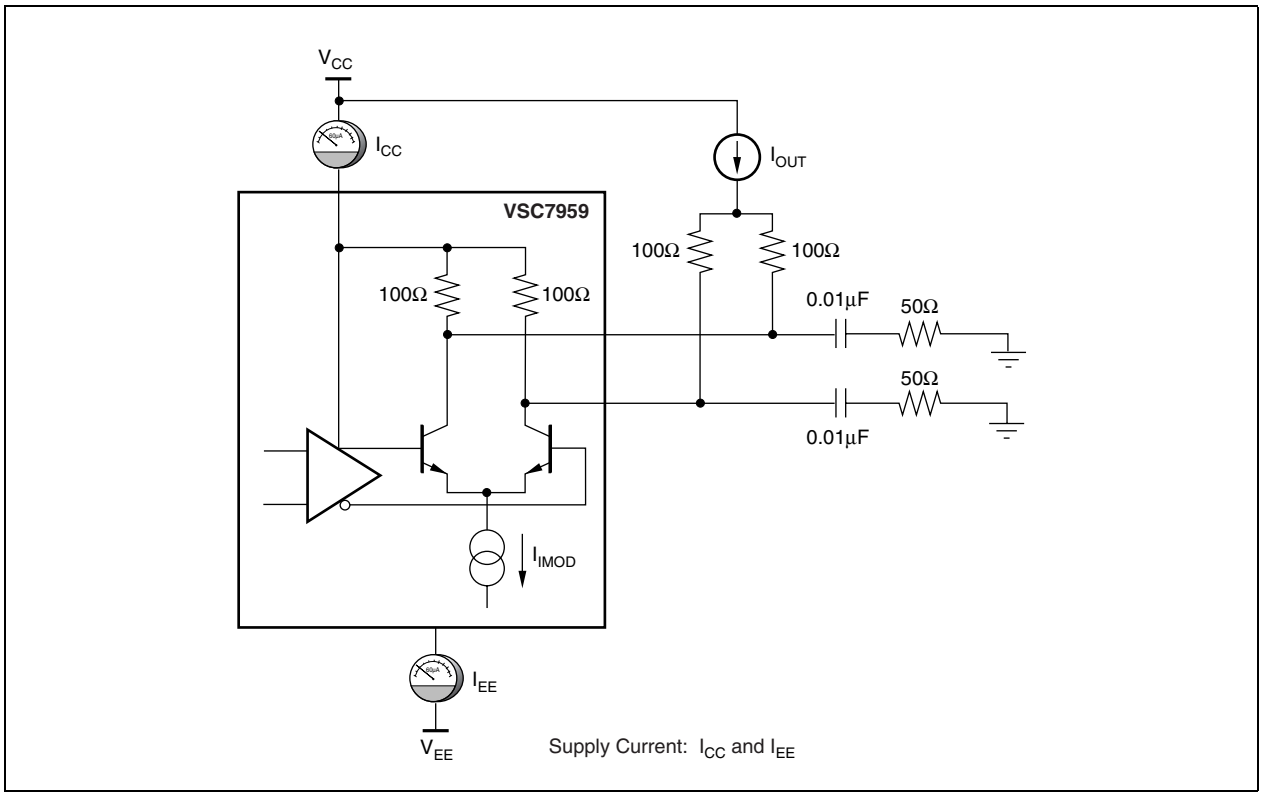


Figure 1. Supply Current Measurement

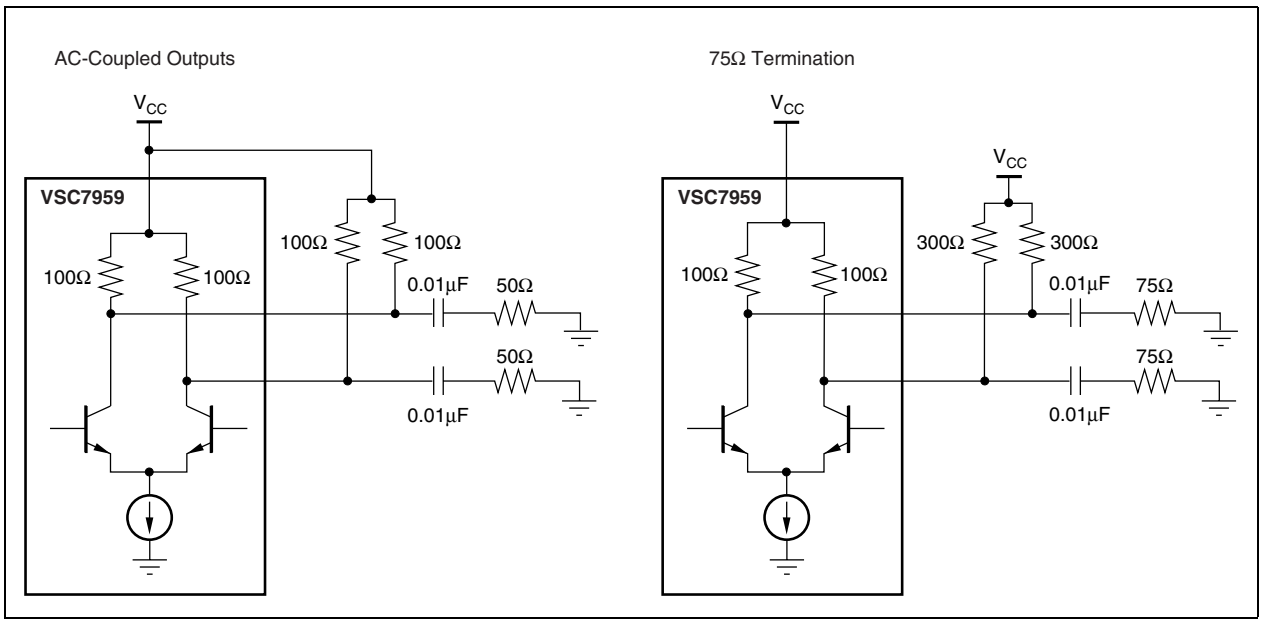
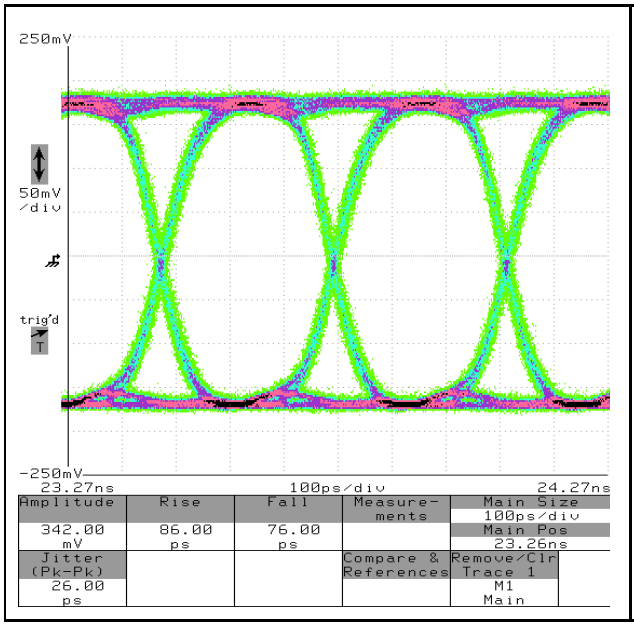


Figure 2. Output Terminations

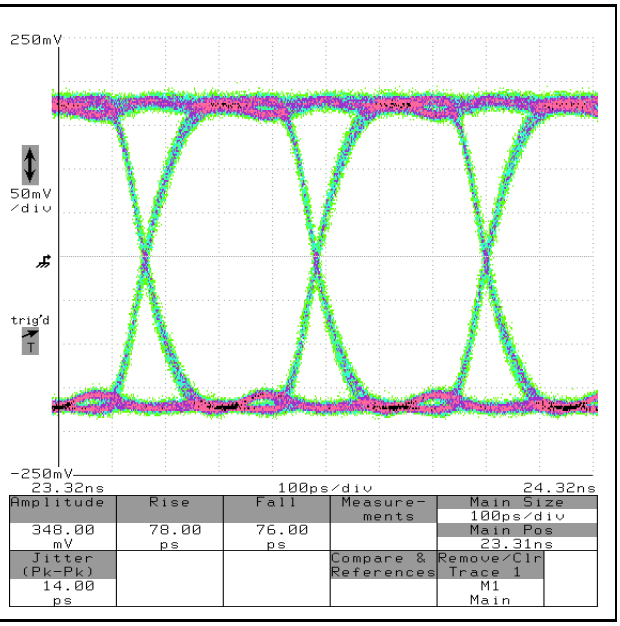
TYPICAL OPERATING CHARACTERISTICS

T_A = +25°C.

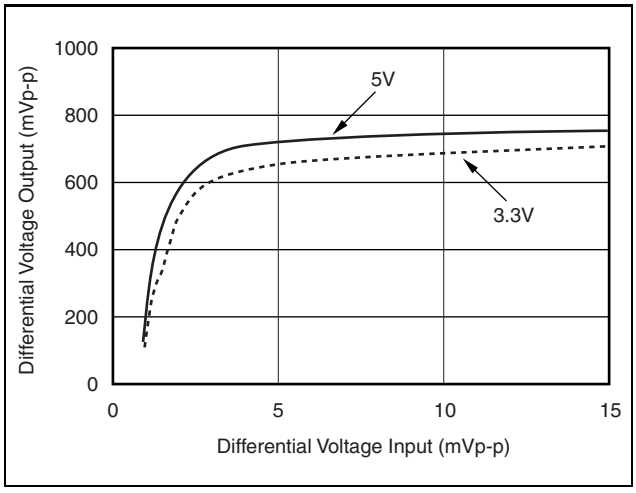
Differential Voltage Input = 10mVp-p
f = 3.125Gb/s, V_{SS} = +3.3V



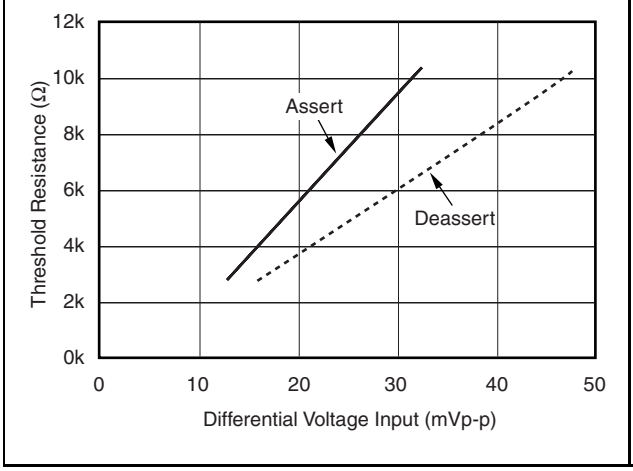
Differential Voltage Input = 1000mVp-p
f = 3.125Gb/s, V_{SS} = +3.3



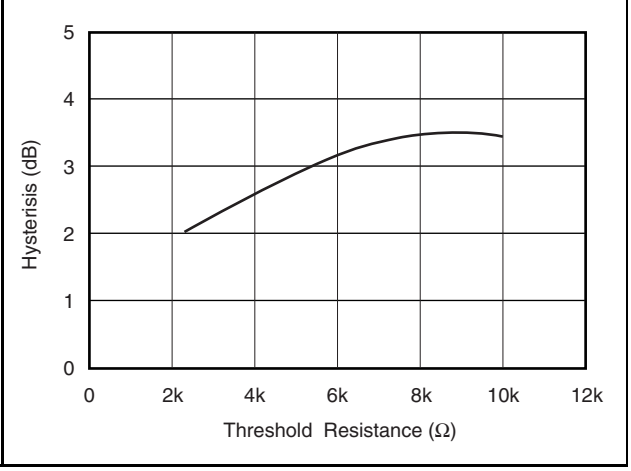
Differential Voltage Input vs. Voltage Output



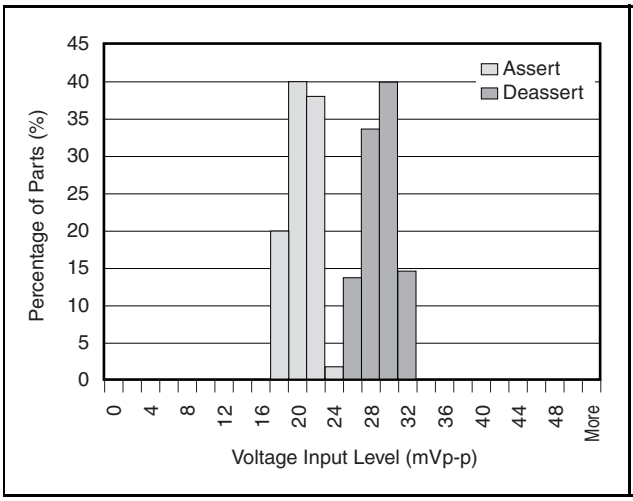
LOS Sensitivty
f = 2.5GHz, V_{SS} = +3.3V, K28.5 Pattern



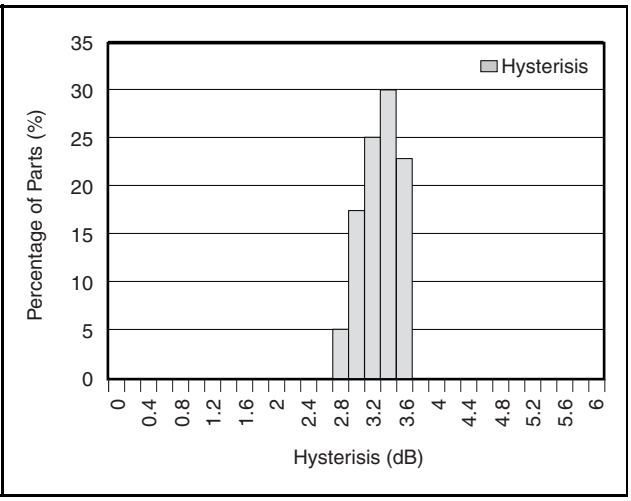
LOS Hysterisis
f = 2.5Gb/s, V_{SS} = +3.3V, K28.5 Pattern



LOS Typical Distribution
Assert/Deassert, R_{TH} = 5.6kΩ



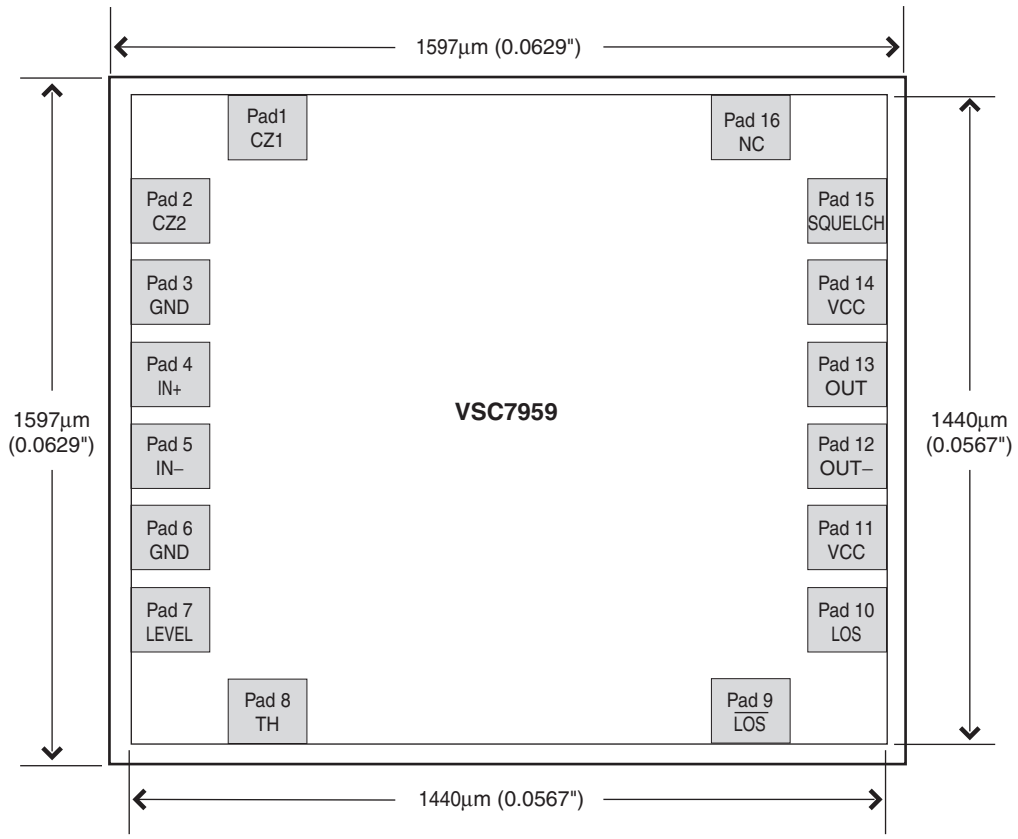
LOS Typical Distribution
Hysterisis, R_{TH} = 5.6kΩ



PCB LAYOUT GUIDELINES

Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. The output traces to the laser diode must be short to minimize inductance. Short output traces will provide best performance.

BARE DIE AND PACKAGE INFORMATION



Die Size Including Scribe:	1597µm x 1597µm (0.0629" x 0.0629")
Die Size Not Including Scribe:	1440µm x 1440µm (0.0567 x 0.0567")
Pad Pitch:	180µm (0.0071")
Pad Passivation Opening:	95µm x 95µm (0.0037" x 0.0037")
Die Thickness:	280µm (0.011")

The back side of the die may either be left floating or connected to the most negative potential.

Figure 3. Pad Diagram for Bare Die (-W)

Table 7. Coordinates for Bare Die (-W)

Pad Name	Pad Number	Coordinates (µm)		Description
		X	Y	
CZ1	1	270.525	1359.05	Offset correction loop capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop.
CZ2	2	80.95	1170.525	Offset correction loop capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop.
GND	3	80.95	990.525	Supply ground.
IN+	4	80.95	810.525	Noninverted data input.
IN-	5	80.95	630.525	Inverted data input.
GND	6	80.95	450.525	Supply ground.
LEVEL	7	80.95	270.525	Output current level. This pin may be either connected to ground or left unconnected. Connecting to ground causes output current to be 20mA. The output is 16mA when left unconnected.
TH	8	270.525	80.95	Loss of Signal (LOS) threshold. Connect a resistor from this pin to ground to set the input signal level at which LOS outputs will be asserted.
$\overline{\text{LOS}}$	9	1169.475	80.95	Inverted Loss of Signal output. LOS is HIGH for input signals above the threshold programmed by TH.
LOS	10	1359.05	270.525	Noninverted Loss of Signal output. LOS is LOW for input signals above the threshold programmed by TH.
VCC	11	1359.05	450.525	Power supply.
OUT-	12	1359.05	630.525	Inverted data output.
OUT+	13	1359.05	810.525	Noninverted data output.
VCC	14	1359.05	990.525	Power supply.
SQUELCH	15	1359.05	1170.525	Squelch input. Squelch is disabled if this pin is unconnected or set LOW. When SQUELCH is HIGH, OUT+ and OUT- are forced to static levels.
NC	16	1169.475	1359.05	No connection.

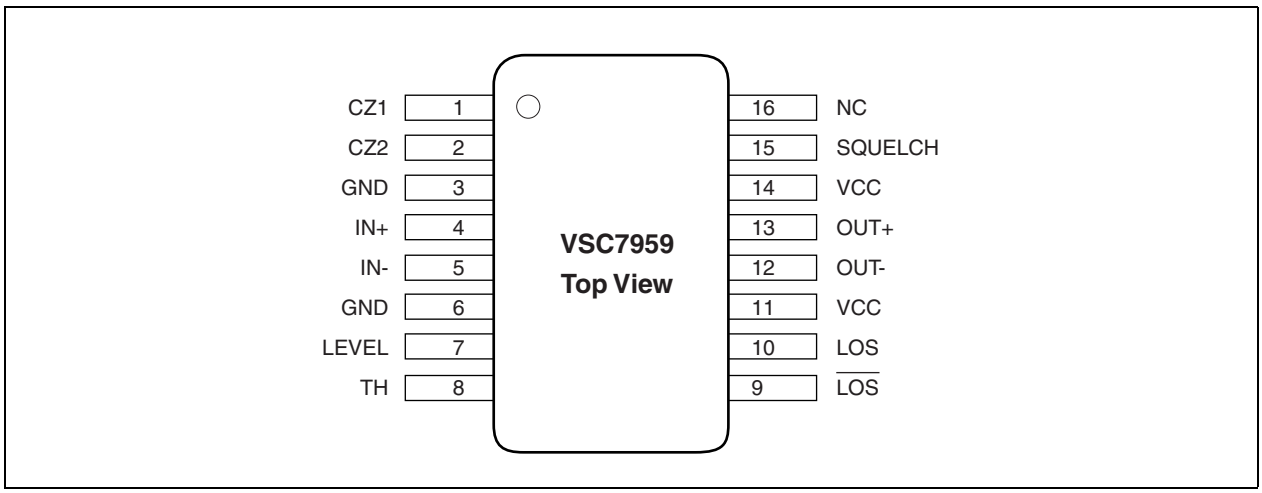


Figure 4. Pin Diagram for TSSOP-16 (YD)

Table 8: Pin Identifications for TSSOP-16 (YD)

Pin Name	Pin Number	Description
CZ1	1	Offset correction loop capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop.
CZ2	2	Offset correction loop capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop.
GND	3	Supply ground.
IN+	4	Noninverted input signal.
IN-	5	Inverted input signal.
GND	6	Supply ground.
LEVEL	7	Output current level. This pin may be either connected to ground or left unconnected. Connecting to ground causes output current to be 20mA. The output is 16mA when left unconnected.
TH	8	Loss of Signal (LOS) threshold. Connect a resistor from this pin to ground to set the input signal level at which LOS outputs will be asserted.
$\overline{\text{LOS}}$	9	Inverted Loss of Signal output. LOS is HIGH for input signals above the threshold programmed by TH.
LOS	10	Noninverted Loss of Signal output. LOS is LOW for input signals above the threshold programmed by TH.
VCC	11	Power supply.
OUT-	12	Inverted data output.
OUT+	13	Noninverted data output.
VCC	14	Power supply.
SQUELCH	15	Squelch input. Squelch is disabled if this pin is unconnected or set LOW. When SQUELCH is HIGH, OUT+ and OUT- are forced to static levels when LOS is HIGH.
NC	16	No connection.

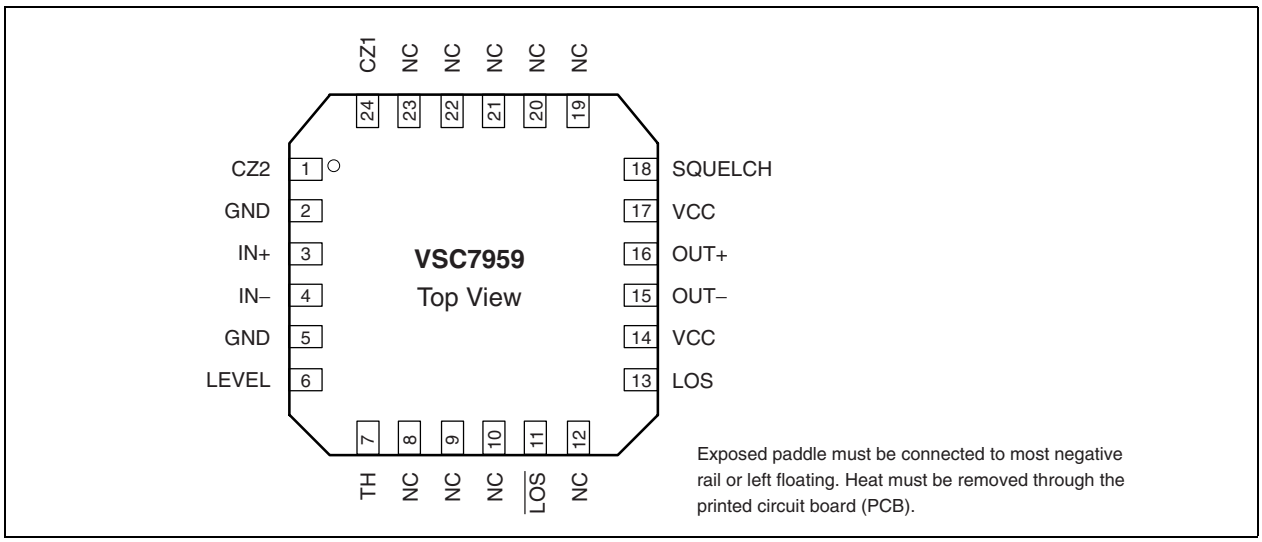
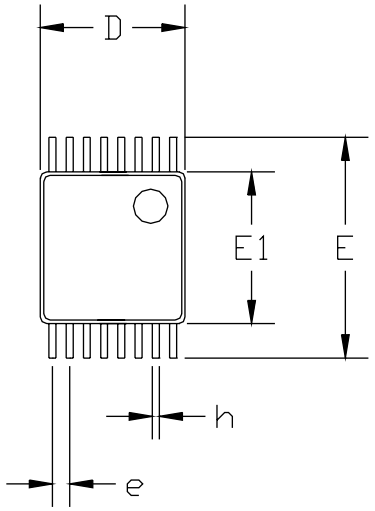


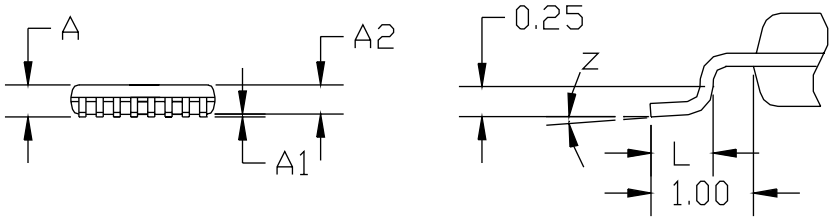
Figure 5. Pin Diagram for 24-Pin QFP-N (YF)

Table 9. Pin Identification for 24-Pin QFP-N (YF)

Pin Name	Pin Number	Description
CZ2	1	Offset correction loop capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop.
GND	2	Supply ground.
IN+	3	Noninverted data input.
IN–	4	Inverted data input.
GND	5	Supply ground.
LEVEL	6	Output current level. This pin may be either connected to ground or left unconnected. Connecting to ground causes output current to be 20mA. The output is 16mA when left unconnected.
TH	7	Loss of Signal (LOS) threshold. Connect a resistor from this pin to ground to set the input signal level at which LOS outputs will be asserted.
NC	8	No connection.
NC	9	No connection.
NC	10	No connection.
$\overline{\text{LOS}}$	11	Inverted Loss of Signal output. LOS is HIGH for input signals above the threshold programmed by TH.
NC	12	No connection.
LOS	13	Noninverted Loss of Signal Output. LOS is LOW for input signals above the threshold programmed by TH.
VCC	14	Power supply.
OUT–	15	Inverted data output.
OUT+	16	Noninverted data output.
VCC	17	Power supply.
SQUELCH	18	Squelch input. Squelch is disabled if this pin is unconnected or set LOW. When SQUELCH is HIGH, OUT+ and OUT– are forced to static levels when LOS is HIGH.
NC	19	No connection.
NC	20	No connection.
NC	21	No connection.
NC	22	No connection.
NC	23	No connection.
CZ1	24	Offset correction loop capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop.

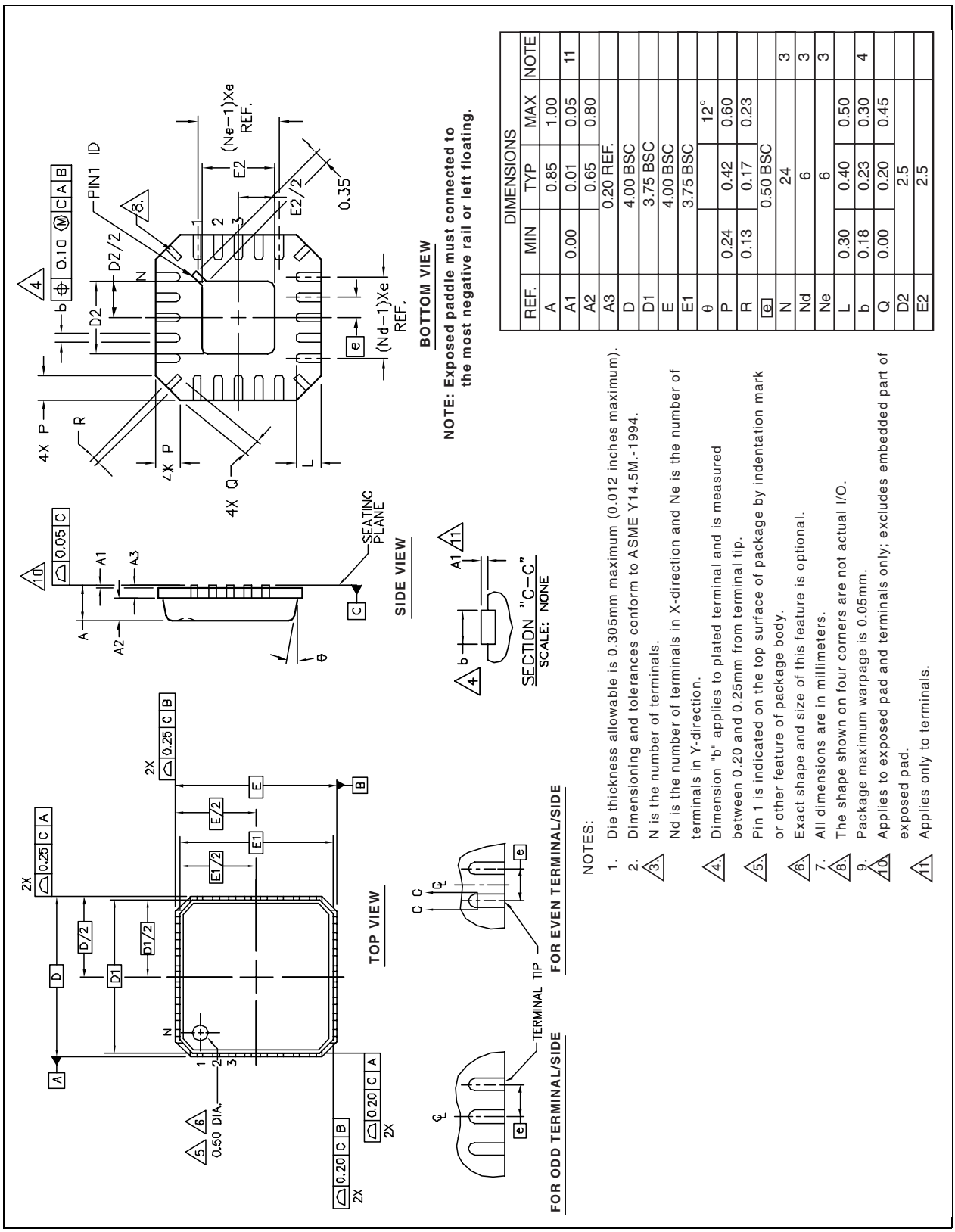


SYMBOL	TSSOP		
	MIN.	NOM.	MAX.
A			1.10
A_1	0.05		0.15
A_2	0.85	0.90	0.95
D		5.00 BSC.	
E		6.40 BSC.	
E_1	4.30	4.40	4.50
L	0.50	0.60	0.70
e		0.65 BSC.	
h	0.19		0.30
z	0		8



1. All dimensioning and tolerancing per ASME. Y14.5-1994
2. Controlling dimension: millimeter
3. This outline conforms to JEDEC Publication 95 Registration MS-026

Figure 6. Package Drawing for TSSOP-16 (YD)



DIMENSIONS				
REF.	MIN	TYP	MAX	NOTE
A		0.85	1.00	
A1	0.00	0.01	0.05	11
A2		0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2		2.5		
E2		2.5		

NOTES:
1. Die thickness allowable is 0.305mm maximum (0.012 inches maximum).
2. Dimensioning and tolerances conform to ASME Y14.5M.-1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction.
4. Dimension "b" applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
5. Pin 1 is indicated on the top surface of package by indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. All dimensions are in millimeters.
8. The shape shown on four corners are not actual I/O.
9. Package maximum warpage is 0.05mm.
10. Applies to exposed pad and terminals only; excludes embedded part of exposed pad.
11. Applies only to terminals.

Figure 7. Package Drawing for 24-Pin QFP-N (YF)

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC7959 CML Limiting Amplifier with LOS Detect

Part Number	Description
VSC7959YD-1	TSSOP-16, 4.4mm x 5mm body
VSC7959YF-1	24-pin QFP-N, 4mm x 4mm leadless body
VSC7959-W	Bare die in waffle pack

CORPORATE HEADQUARTERS
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