

SN54ABT16244, SN74ABT16244A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS073E - SEPTEMBER 1991 - REVISED JULY 1994

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II*™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The SN54ABT16244 and SN74ABT16244A are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16244A is characterized for operation from -40°C to 85°C .

SN54ABT16244...WD PACKAGE
SN74ABT16244A...DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OE}$	1	48	$2\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$4\overline{OE}$	24	25	$3\overline{OE}$

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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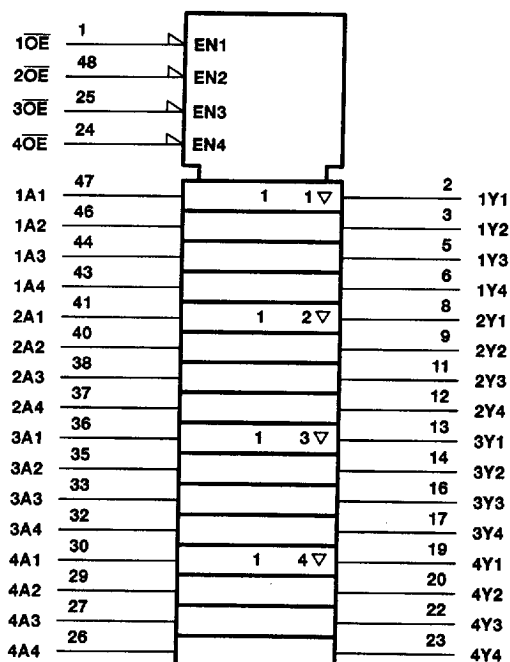
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16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

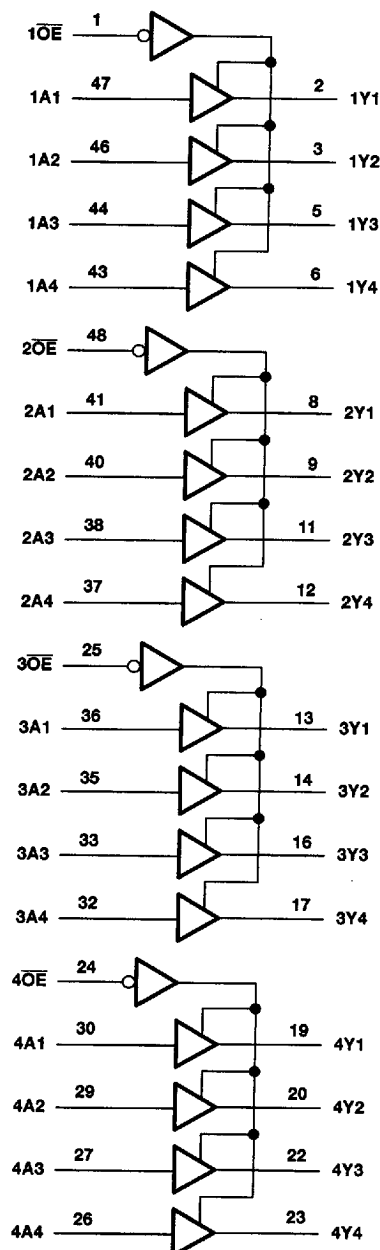
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16244	96 mA
SN74ABT16244A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT16244		SN74ABT16244A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.



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SN54ABT16244, SN74ABT16244A
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
		MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2		2				
		I _{OH} = -32 mA	2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55	0.55				V
		I _{OL} = 64 mA		0.55*			0.55		
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1	±1		±1		µA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10§	10		10§		µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10§	-10		-10§		µA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100			±100		µA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50	50		50		µA
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V			-50 -100 -180	-50 -180		-50 -180		mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		3	2		3		mA
		Outputs low		32	32		32		
		Outputs disabled		3	2		3		
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Data inputs	Outputs enabled	0.05	1.5		0.05		mA
			Outputs disabled	0.05	1		0.05		
		Control inputs		0.05	1.5		0.05		
C _i	V _I = 2.5 V or 0.5 V		3						pF
C _o	V _O = 2.5 V or 0.5 V		8						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 † Characteristics for T_A = 25°C apply to the SN74ABT16244A only.

 ‡ All typical values are at V_{CC} = 5 V.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 # This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1	2.3	3.2	0.7	3.7	1	3.5	ns
t _{PHL}			1	2.6	3.7	0.5	4.3	1	4.1	
t _{PZH}	OE	Y	1	3	3.8	0.7	5	1	4.8	ns
t _{PZL}			1	3.2	4	0.9	5	1	4.8	
t _{PHZ}	OE	Y	1	3.6	4.4	1	5	1	4.8	ns
t _{PLZ}			1	2.9	3.7	1	4.3	1	4.1	

 † Characteristics for T_A = 25°C apply to the SN74ABT16244A only.

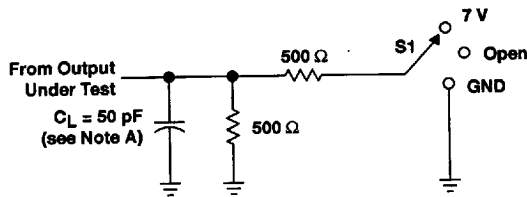
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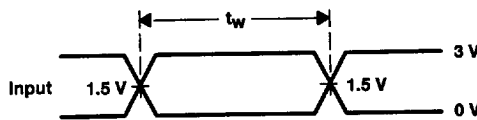
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PARAMETER MEASUREMENT INFORMATION

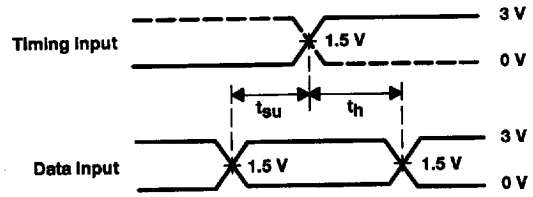


LOAD CIRCUIT FOR OUTPUTS

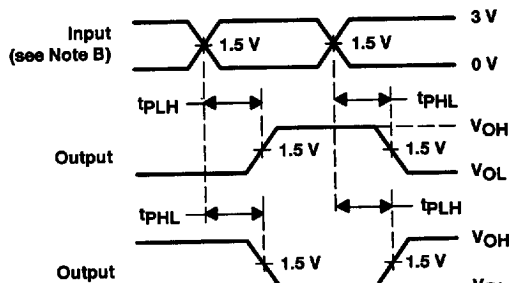
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



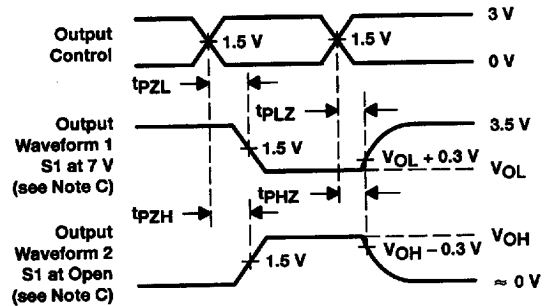
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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