

DIVIDE-BY-SIXTEEN COUNTER

MC939F · MC839F, P

This monolithic ripple counter is designed to operate at $\pm 20\%$ of the nominal 5.0 volt power supply voltage and is guaranteed to 15 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 binary code with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin in 1.0 volt. Typical input fall time required to toggle is $5 \mu s$ measured from 2.5 volts to 0.50 volts.

Input Loading Factor:

$$S_D = 1.5$$

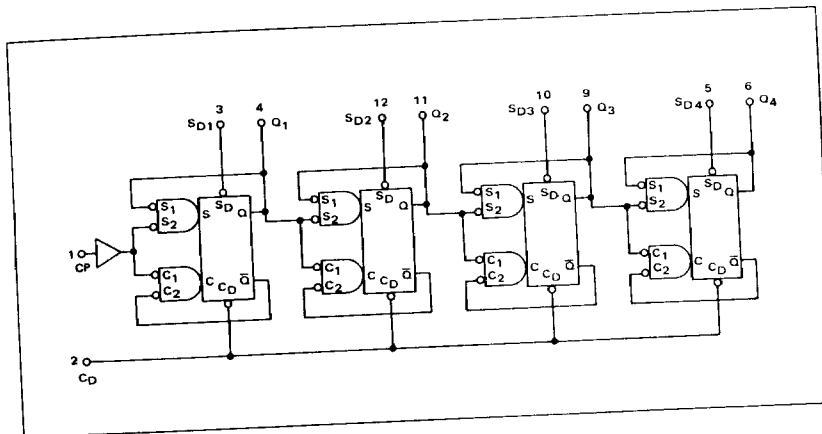
$$C_D = 5$$

$$CP = 1$$

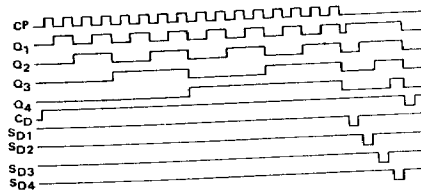
Output Loading Factor = 8

Total Power Dissipation = 150 mW typ/pkg

Maximum Counting Frequency = 30 MHz typ



COUNTER SEQUENCE

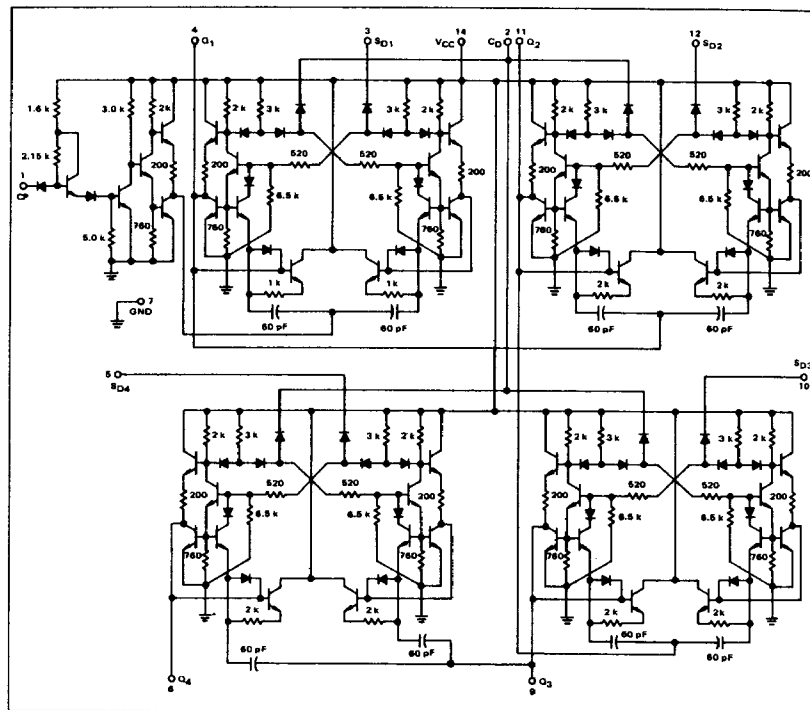


DECODING LOGIC

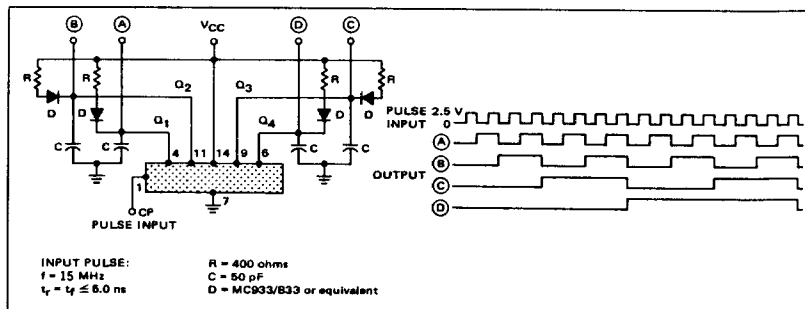
0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
3	Q_1	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
5	Q_1	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
6	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
7	Q_1	Q_2	Q_3	$\bar{Q}_4$
8	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
9	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
10	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	Q_4
11	Q_1	Q_2	$\bar{Q}_3$	Q_4
12	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	Q_4
13	Q_1	$\bar{Q}_2$	Q_3	Q_4
14	$\bar{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

MC939F/MC839F, P (continued)

CIRCUIT SCHEMATIC



COUNTING FREQUENCY TEST CIRCUIT AND WAVEFORMS



The diagram shows a four-stage shift register. Each stage consists of a D flip-flop. The output of each flip-flop is connected to the D input of the next flip-flop in the sequence. The output of the final flip-flop is connected back to the D input of the first flip-flop, forming a feedback loop. The flip-flops are labeled with their respective inputs and outputs: s_0, a_1 for the first stage, s_1, a_2 for the second, s_2, a_3 for the third, and s_3, a_4 for the fourth. The outputs are labeled a_1, a_2, a_3, a_4 and the inputs are labeled s_0, s_1, s_2, s_3 . The diagram is titled 'CENTRAL CHARACTERISTICS'.

(continued)

Pins not listed are left open.

† Momentarily ground. This terminal before applying test condition.

†† Momentary ground. Release ground on pin 2 before taking measurement.

* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:

The diagram shows two waveforms, V_{IN} and S_D , over time. The time axis is divided into three sections: C_D , S_D , and MEASUREMENT INTERVAL. In the C_D section, both V_{IN} and S_D are at a low level. In the S_D section, V_{IN} remains at a low level while S_D transitions to a high level. In the MEASUREMENT INTERVAL section, both V_{IN} and S_D return to a low level.

Pins not listed are left open.

† Momentarily ground this terminal before applying test condition.

at Momentary ground. Release ground on pin 2 before

1 Momentary ground. Release ground on pin 2 before taking measurement.

- * Inputs to C_{∞} (pin 2) and appropriate S_{∞} (pins 3, 5, 10, or 12) as shown; (taking measurements).

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

