

# 74AHC2G125; 74AHCT2G125

Dual buffer/line driver; 3-state

Rev. 3 — 6 May 2013

Product data sheet

## 1. General description

The 74AHC2G125 and 74AHCT2G125 are high-speed Si-gate CMOS devices. They provide a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ( $nOE$ ). A HIGH at  $nOE$  causes the output to assume a high-impedance OFF-state.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

## 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
  - ◆ HBM JESD22-A114E: exceeds 2000 V
  - ◆ MM JESD22-A115-A: exceeds 200 V
  - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74AHC2G125DP	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74AHCT2G125DP					
74AHC2G125DC	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74AHCT2G125DC					
74AHC2G125GD	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm		SOT996-2
74AHCT2G125GD					



## 4. Marking

Table 2. Marking codes

Type number	Marking
74AHC2G125DP	A25
74AHCT2G125DP	C25
74AHC2G125DC	A25
74AHCT2G125DC	C25
74AHC2G125GD	A25
74AHCT2G125GD	C25

## 5. Functional diagram

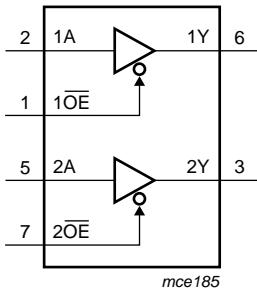


Fig 1. Logic symbol

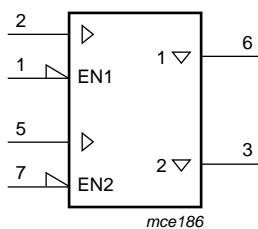


Fig 2. IEC logic symbol

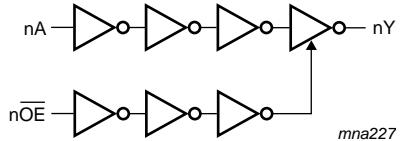


Fig 3. Logic diagram (one buffer)

## 6. Pinning information

### 6.1 Pinning

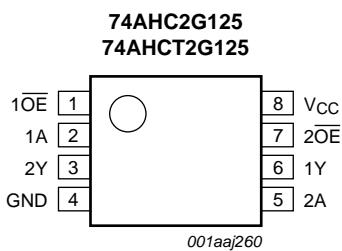


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

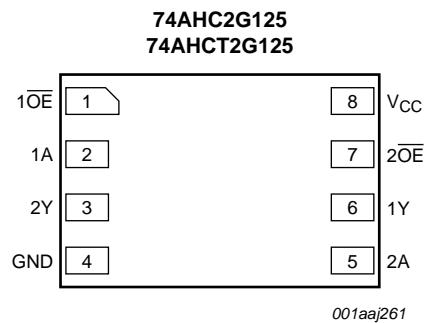


Fig 5. Pin configuration SOT996-2 (XSON8)

## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1 $\overline{OE}$ , 2 $\overline{OE}$	1, 7	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

For XSON8 package: above 45 °C the value of P<sub>tot</sub> derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G125			74AHCT2G125			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC2G125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = −50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = −50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = −50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = −8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.25	-	2.5	-	10	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	μA

**Table 7. Static characteristics ...continued**  
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_I$	input capacitance		-	1.5	10	-	10	-	10	pF
<b>74AHCT2G125</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
$V_{OL}$	LOW-level output voltage	$I_O = -8.0 \text{ mA}$	3.94	-	-	3.8	-	3.70	-	V
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_{OZ}$	OFF-state output current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	0.25	-	2.5	-	10	$\mu\text{A}$
$I_I$	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = 3.4 \text{ V};$ other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

GND = 0 V; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC2G125</b>										
$t_{pd}$	propagation delay	$n\text{A to } n\text{Y}; \text{ see } \text{Figure 6}$	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50 \text{ pF}$	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	9.5	ns

**Table 8. Dynamic characteristics ...continued**  
GND = 0 V; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{en}$	enable time	$n\overline{OE}$ to $nY$ ; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50 \text{ pF}$	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
$t_{dis}$	disable time	$n\overline{OE}$ to $nY$ ; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		$C_L = 50 \text{ pF}$	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50 \text{ pF}$	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	[4]	-	9	-	-	-	-	pF

**74AHCT2G125**

$t_{pd}$	propagation delay	$nA$ to $nY$ ; see <a href="#">Figure 6</a>	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	8.5	ns
$t_{en}$	enable time	$n\overline{OE}$ to $nY$ ; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.9	5.1	1.0	6.0	1.0	6.0	ns
		$C_L = 50 \text{ pF}$	-	5.1	7.5	1.0	8.5	1.0	8.5	ns
$t_{dis}$	disable time	$n\overline{OE}$ to $nY$ ; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	4.5	6.8	1.0	8.0	1.0	8.0	ns
		$C_L = 50 \text{ pF}$	-	6.1	8.8	1.0	10.0	1.0	10.0	ns

**Table 8. Dynamic characteristics ...continued**  
 GND = 0 V; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation per buffer; capacitance	$C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	[4]	-	11	-	-	-	-	pF

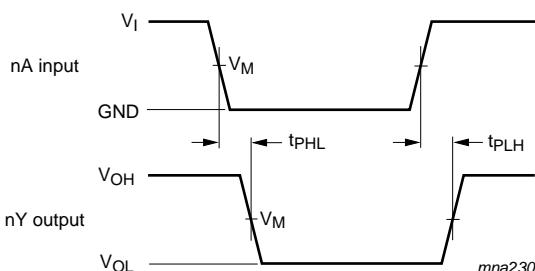
[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] Typical values are measured at  $V_{CC} = 3.3 \text{ V}$ .

[3] Typical values are measured at  $V_{CC} = 5.0 \text{ V}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts.

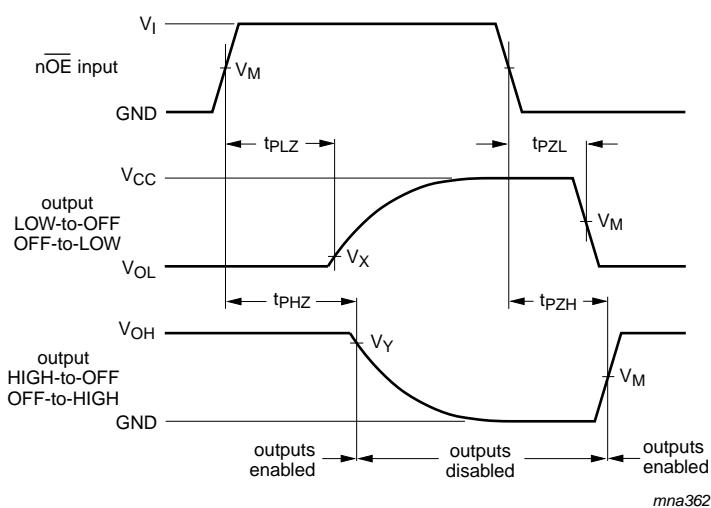
## 12. Waveforms



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. Input (nA) to output (nY) propagation delays**



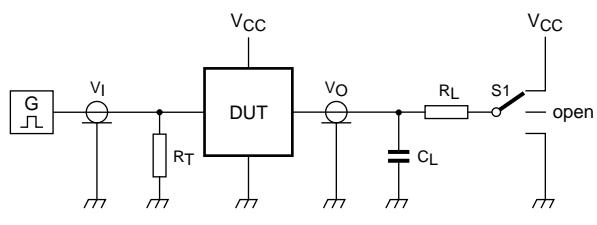
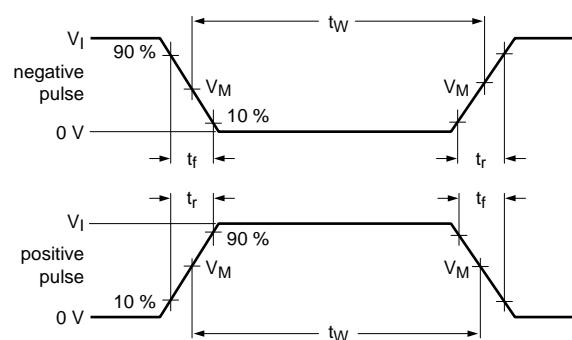
Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 9. Measurement points**

Type	Input	Output		
		$V_M$	$V_M$	$V_X$
74AHC2G125	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
74AHCT2G125	1.5 V	0.5V <sub>CC</sub>	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



001aad983

Test data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$S1$  = Test selection switch.

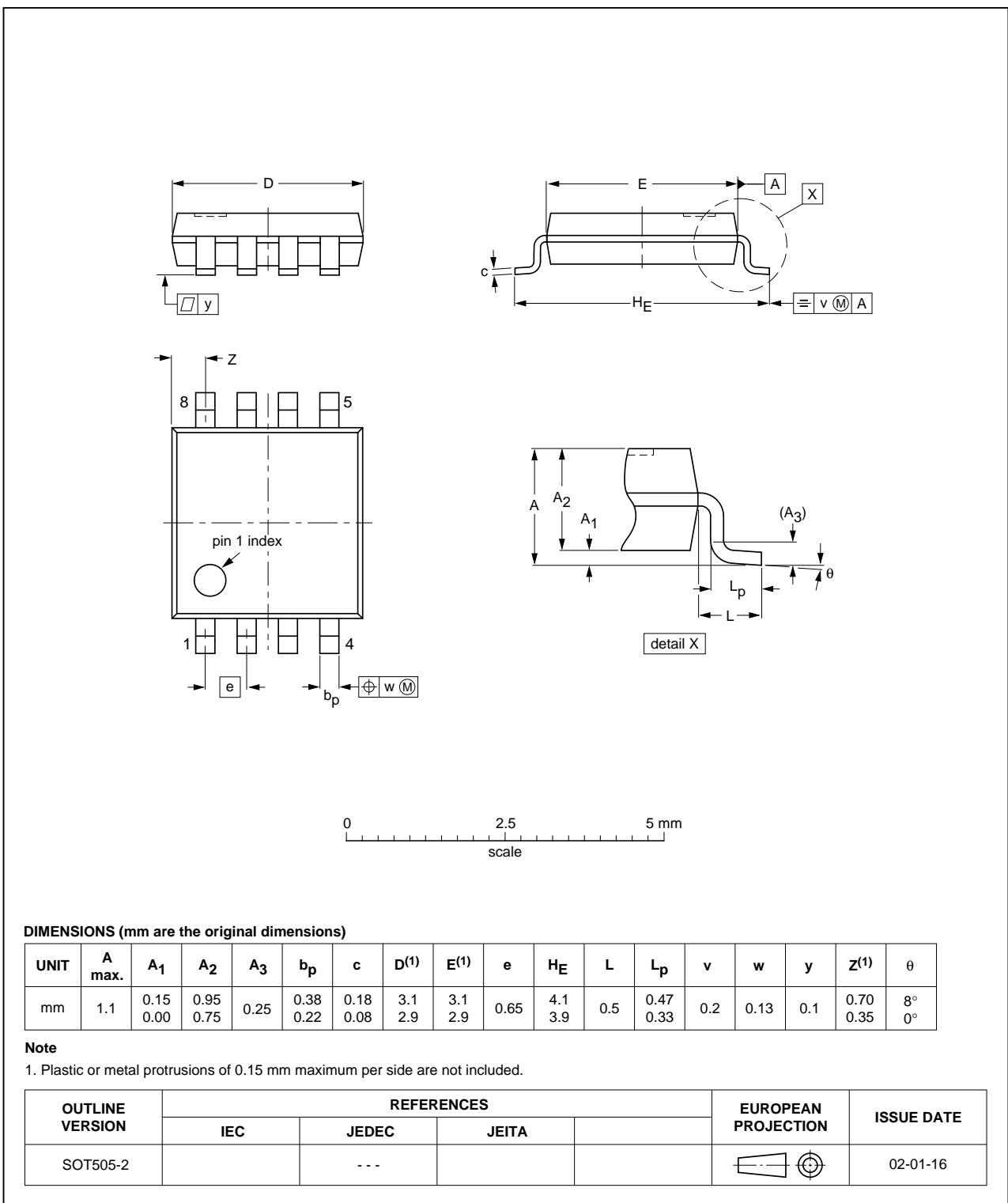
**Fig 8. Test circuit for measuring switching times**

**Table 10. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC2G125	$V_{CC}$	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT2G125	3 V	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



### DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	z <sup>(1)</sup>	θ
mm	1.1 0.00	0.15 0.75	0.95	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

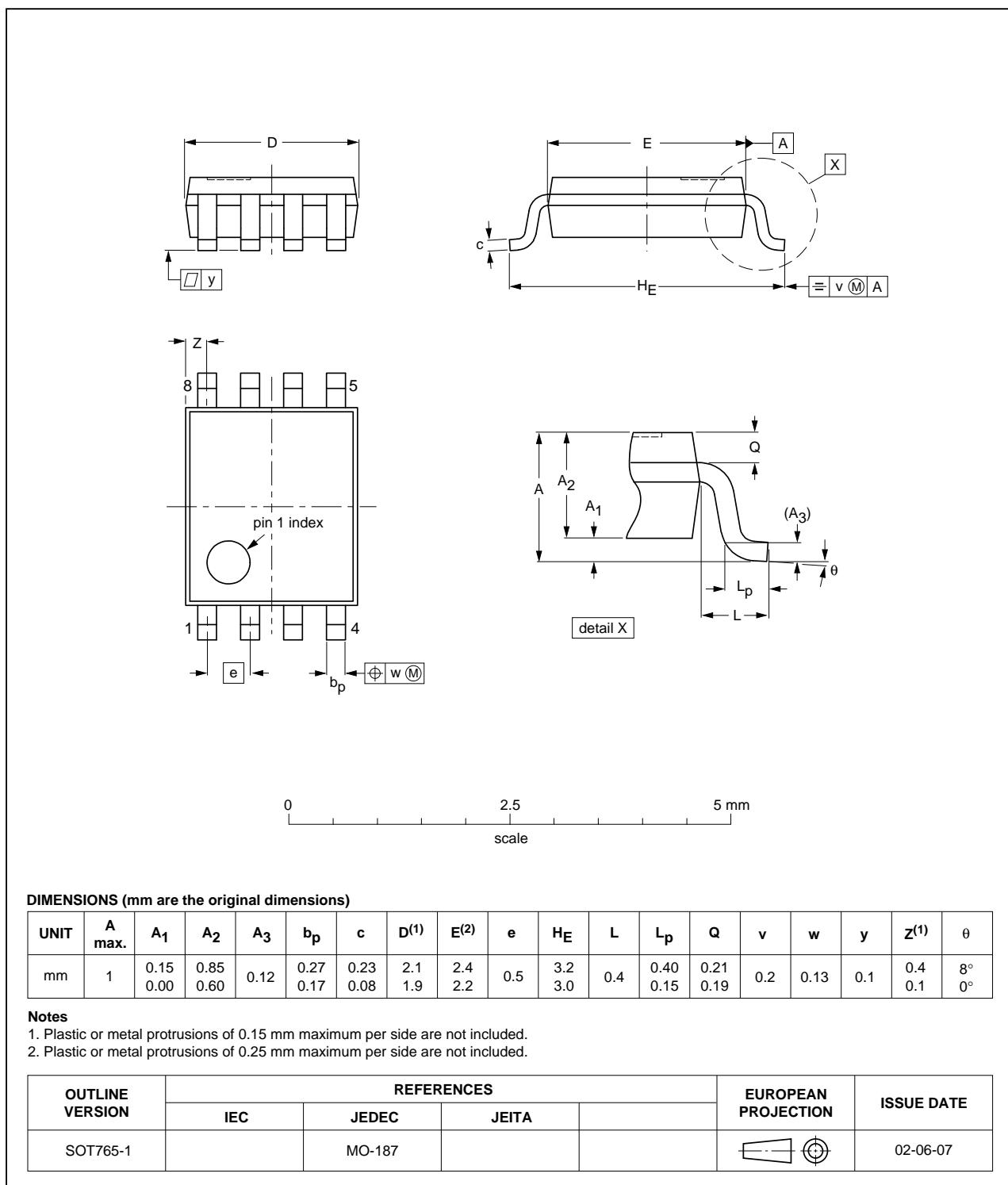


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;  
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

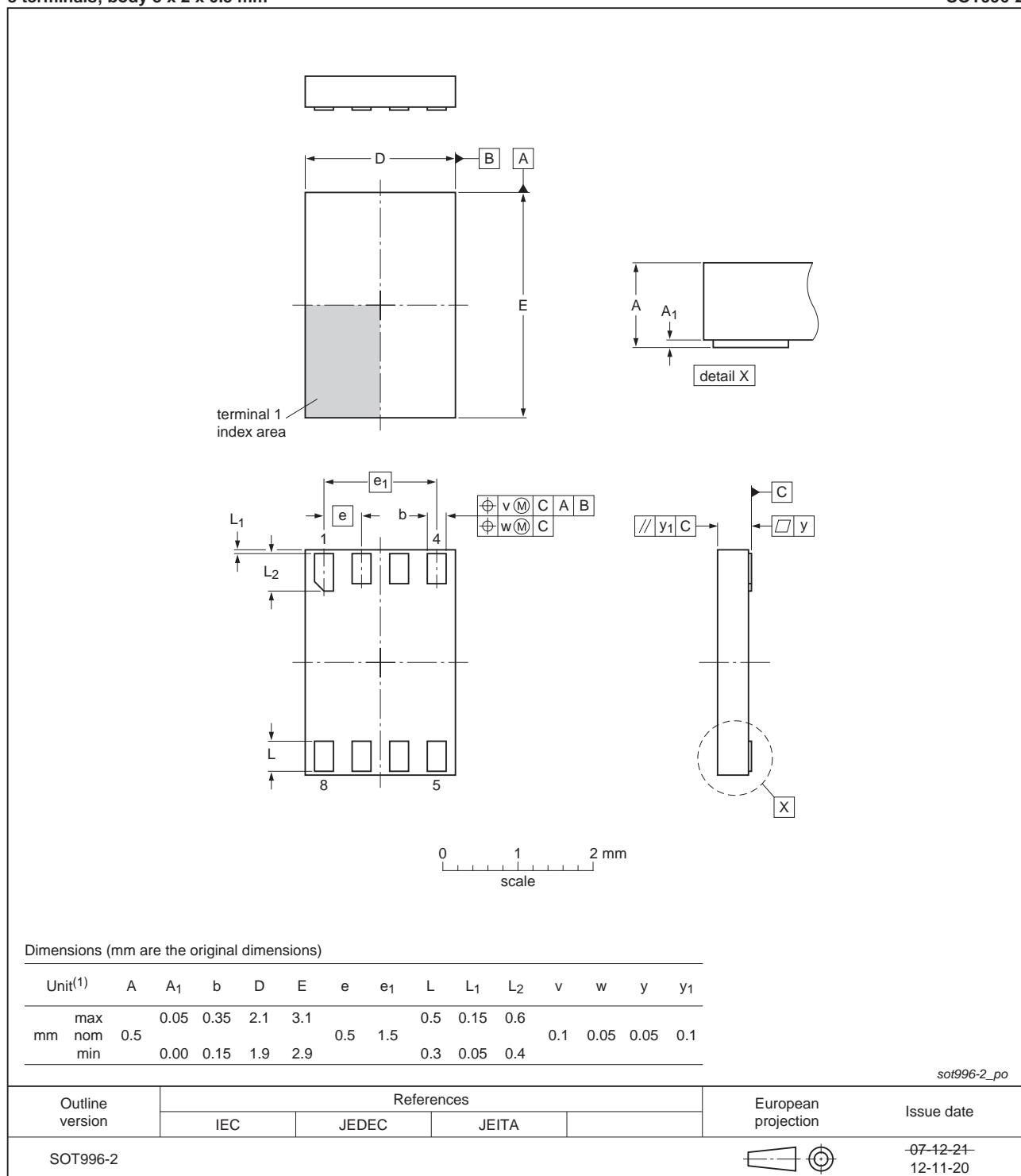


Fig 11. Package outline SOT996-2 (XSON8)

## 14. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G125 v.3	20130506	Product data sheet	-	74AHC_AHCT2G125 v.2
Modifications:				• For type number 74AHC2G125GD and 74AHCT2G125GD XSON8U has changed to XSON8.
74AHC_AHCT2G125 v.2	20081222	Product data sheet	-	74AHC_AHCT2G125 v.1
Modifications:				• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74AHC2G125GD and 74AHCT2G125GD (XSON8U package).
74AHC_AHCT2G125 v.1	20040113	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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