NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

Dual Ultra Low N… …Amplifiers

EL5236, EL5237

The EL5236 is a dual, low noise, 300MHz Gain Bandwidth product Voltage Feedback Op Amp (VFA). The minimum operating gain of 2 comes with a very low input noise voltage of 1.5nV/√ Hz and 1.8pA/√Hz current noise. This makes this dual device ideal for low noise differential active filters, dual channel photodiode detectors, differential receivers with equalization, and any other wideband, high dynamic range application.

Each channel requires only 5.8mA on a ±6V supply. Minimal performance change over a supply range of ±2.5V to ±6V is provided (or single +5V ->+12V). Where system power is paramount, the EL5237 dual with disable allows the amplifiers to be separately powered down to less than 20µA/Ch.

The 8 Ld dual EL5236 is available in the industry standard pinout SO-8 or space saving MSOP-8. The 10 Ld EL5237 is available in an MSOP-10.

Features

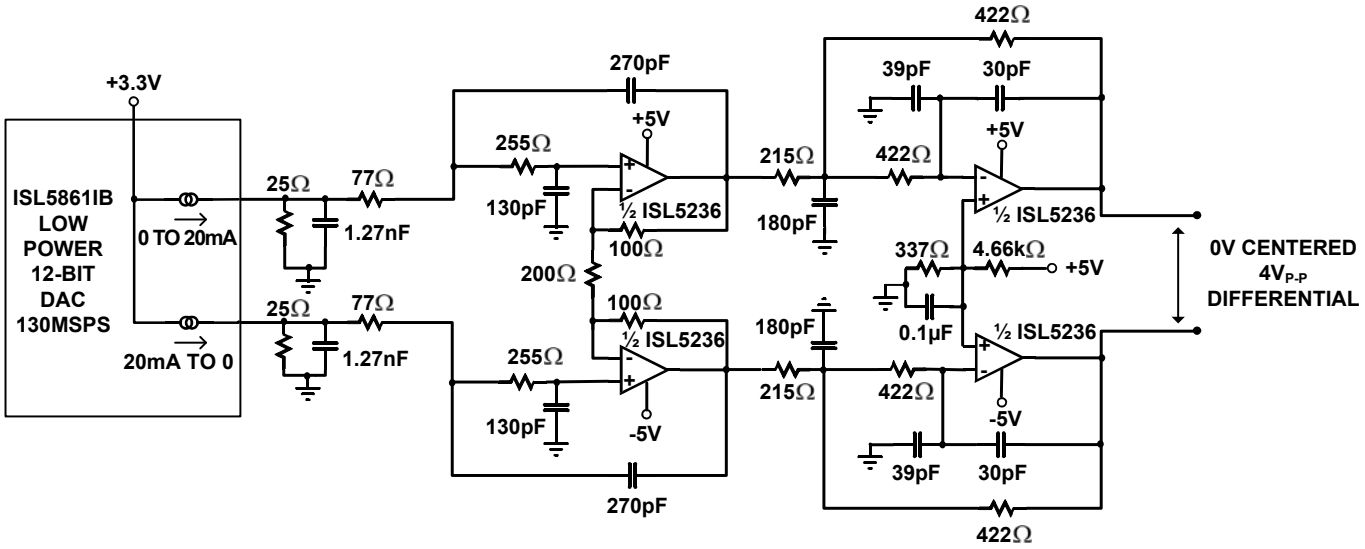
- Bandwidth (-3dB) of 250MHz @ A_V = +2
- Gain Bandwidth Product: 300MHz
- Voltage Noise: 1.5nV/√Hz
- Current Noise: 1.8pA/√Hz
- I_S: 5.8mA/Channel
- 100mA I_{OUT}
- Fast Enable/Disable (EL5237 only)
- ±2.5V to ±6V Supply Range Operation

Applications

- Differential ADC Driver
- Complementary DAC Output Driver
- Ultrasound Input Amplifiers
- AGC and PLL Active Filters
- Transimpedance Designs

Related Products

- ISL28290, Dual, 80MHz, 1nV/√Hz
- ISL55290, Dual, 700MHz, 1.1nV/√Hz

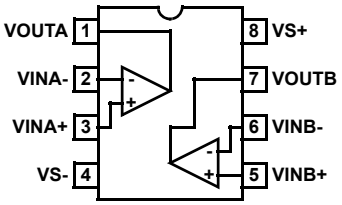


LOW POWER, LOW NOISE, DIFFERENTIAL DAC OUTPUT TRANSIMPEDANCE WITH A 5TH ORDER, 5MHz, BUTTERWORTH FILTER

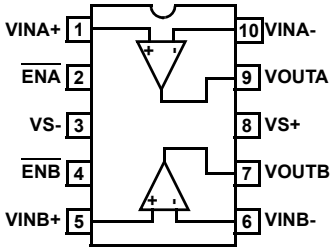
FIGURE 1. TYPICAL APPLICATION

Pin Configurations

EL5236
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



EL5237
(10 LD MSOP)
TOP VIEW



Pin Descriptions

EL5236 (8 Ld SOIC AND 8 Ld MSOP)	EL5237 (10 Ld MSOP)	PIN NAME	DESCRIPTION
1	9	VOUTA	Output of Op Amp A
2	10	VINA-	Inverting Input of Op Amp A
3	1	VINA+	Non-Inverting Input of Op Amp A
4	3	VS-	Negative Supply Voltage
5	5	VINB+	Non-Inverting Input of Op Amp B
6	6	VINB-	Inverting Input of Op Amp B
7	7	VOUTB	Output of Op Amp B
8	8	VS+	Positive Supply Voltage
-	2	$\overline{\text{ENA}}$	Low Enable Op Amp A
-	4	$\overline{\text{ENB}}$	Low Enable Op Amp B

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
EL5236IYZ	BBBSA	-40 to +85	8 Ld MSOP (3.0mm)	M8.118A
EL5236ISZ	5236ISZ	-40 to +85	8 Ld SOIC (150 mil)	M8.15E
EL5237IYZ	BBBTA	-40 to +85	10 Ld MSOP (3.0mm)	M10.118A

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5236, EL5237. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S 14V
Input Voltage . . . . . V_S- -0.3V, V_S +0.3V
Maximum Continuous Output Current 40mA
Maximum Die Temperature . . . . . +150°C
ESD Rating
  Human Body Model 3000V
  Machine Model 300V
  Charged Device Model 2000V
Latch Up (Class 2, Level A) . . . . . Passed at +85°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP Package	160	60
10 Ld MSOP Package	160	60
8 Ld SOIC Package	125	90

Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +6V, V_S- = -6V, R_L = 500Ω, $R_F = R_G$ = 620Ω, V_{CM} = 0V, and T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP			300		MHz
-3dB Bandwidth	BW1	A_V = -1		175		MHz
-3dB Bandwidth	BW2	A_V = +2		250		MHz
2nd Harmonic Distortion	HD2	f = 1MHz, $V_O = 2V_{P-P}$, R_L = 500Ω		-110		dBc
		R_L = 100Ω		-105		dBc
3rd Harmonic Distortion	HD3	f = 1MHz, $V_O = 2V_{P-P}$, R_L = 500Ω		-110		dBc
		R_L = 100Ω		-108		dBc
Slew Rate	SR	V_O = ±2.5V square wave, measured 25% to 75%	90	128		V/µs
Settling to 0.1% (A_V = +2)	t_S	A_V = +2, V_O = ±1V		20		ns
Voltage Noise	e_n	f = 100kHz		1.5		nV/√Hz
Current Noise	i_n	f = 100kHz		1.8		pA/√Hz
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_{CM} = 0V	-3	0.1	3	mV
Average Offset Voltage Drift	TCV_{OS}			-0.3		µV/°C
Input Bias Current	I_B	V_{CM} = 0V		6.5	9	µA
Input Offset Current	I_{OS}		-500	50	500	nA
Input Impedance	R_{IN}			12		MΩ
Input Capacitance	C_{IN}			1.6		pF
Common-Mode Input Range	CMIR		-4.5		+5.5	V
Common-Mode Rejection Ratio	CMRR	For V_{IN} from -4.4V to 5.4V	90	110		dB
Open-Loop Gain	A_{VOL}	V_O = ±2.5V	75	80		dB

Electrical Specifications

V_S+ = +6V, V_S- = -6V, R_L = 500Ω, R_F = R_G = 620Ω, V_{CM} = 0V, and T_A = +25°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
OUTPUT CHARACTERISTICS						
Output Swing High	V_{OH}	R_L = 500Ω	4.8	4.9		V
		R_L = 150Ω	4.5	4.7		V
Output Swing Low	V_{OL}	R_L = 500Ω		-4.8	-4.7	V
		R_L = 150Ω		-4.6	-4.5	V
Short Circuit Current	I_{SC}	R_L = 10Ω (Sourcing and Sinking)	110	160		mA
POWER SUPPLY PERFORMANCE						
Power Supply Rejection Ratio	PSRR	V_S is moved from ±5.4V to ±6.6V	75	85		dB
Supply Current Enable (Per Amplifier)	$I_{S\ ON}$	No load		5.8	7	mA
Supply Current Disable (Per Amplifier) (EL5237)	$I_{S\ OFF}$	$+V_S$		2	20	µA
		$-V_S$	-26	-16		µA
Operating Range	V_S	Single Supply	5		12	V
ENABLE (EL5237)						
Enable Time	t_{EN}			125		ns
Disable Time	t_{DIS}			336		ns
$\overline{EN}$ Pin Input High Current	I_{IHEN}	$\overline{EN}$ = V_S+		17	20	µA
$\overline{EN}$ Pin Input Low Current	I_{ILEN}	$\overline{EN}$ = V_S-	-1	0.1		µA
$\overline{EN}$ Pin Input High Voltage for Power-down	V_{IHEN}			V_S+ -1		V
$\overline{EN}$ Pin Input Low Voltage for Power-up	V_{IHEN}			V_S- +3		V

Electrical Specifications

V_S+ = +2.5V, V_S- = -2.5V, R_L = 500Ω, R_F = R_G = 620Ω, V_{CM} = 0V, and T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP			300		MHz
Slew Rate	SR	V_O = ±1.25V square wave, measured 25% to 75%	80	110		V/µs
Settling to 0.1% (A_V = +2)	t_S	A_V = +2, V_O = ±1V		25		ns
-3dB Bandwidth	BW1	A_V = -1		175		MHz
-3dB Bandwidth	BW2	A_V = +2		250		MHz
2nd Harmonic Distortion	HD2	f = 1MHz, V_O = $2V_{P-P}$, R_L = 500Ω		-94		dBc
3rd Harmonic Distortion	HD3	f = 1MHz, V_O = $2V_{P-P}$, R_L = 500Ω		-100		dBc
Voltage Noise	e_n	f = 100kHz		1.5		nV/√Hz
Current Noise	i_n	f = 100kHz		1.7		pA/√Hz
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_{CM} = 0V	-3	-0.2	+3	mV
Average Offset Voltage Drift	TCV_{OS}			-0.3		µV/°C
Input Bias Current	I_B	V_{CM} = 0V		6.5	9	µA
Input Offset Current	I_{OS}		-500	50	500	nA

Electrical Specifications

V_S+ = +2.5V, V_S- = -2.5V, R_L = 500Ω, R_F = R_G = 620Ω, V_{CM} = 0V, and T_A = +25°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Input Impedance	R_{IN}			2		MΩ
Input Capacitance	C_{IN}			1.6		pF
Common-Mode Input Range	CMIR		-1.3		+1.7	V
Common-Mode Rejection Ratio	CMRR	For V_{IN} from -1.3V to +1.7V	85	105		dB
Open-Loop Gain	A_{VOL}	V_O = ±1.25V	70	75		dB
OUTPUT CHARACTERISTICS						
Output Swing High	V_{OH}	R_L = 500Ω	1.5	1.6		V
		R_L = 150Ω	1.4	1.5		V
Output Swing Low	V_{OL}	R_L = 500Ω		-1.45	-1.35	V
		R_L = 150Ω		-1.37	-1.25	V
Short Circuit Current	I_{SC}	R_L = 10Ω (Sourcing and Sinking)	60	75		mA
POWER SUPPLY PERFORMANCE						
Power Supply Rejection Ratio	PSRR	V_S is moved from ±2.25V to ±2.75V	75	80		dB
Supply Current Enable (Per Amplifier)	$I_{S\ ON}$	No load		5.7	7	mA
Supply Current Disable (Per Amplifier) (EL5237)	$I_{S\ OFF}$	$+V_S$		2	20	µA
		$-V_S$	-21	-16		µA
Operating Range	V_S	Single Supply	5		12	V
ENABLE (EL5237)						
Enable Time	t_{EN}			125		ns
Disable Time	t_{DIS}			336		ns
$\overline{EN}$ Pin Input High Current	I_{IHEN}	$\overline{EN}$ = V_S+		16	20	µA
$\overline{EN}$ Pin Input Low Current	I_{ILEN}	$\overline{EN}$ = V_S-	-1	0.1		µA
$\overline{EN}$ Pin Input High Voltage for Power-down	V_{IHEN}			V_S+ -1		V
$\overline{EN}$ Pin Input Low Voltage for Power-up	V_{IHEN}			V_S- +3		V

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

V_S = ±6V, T_A ≈ +25°C, A_V = +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified.

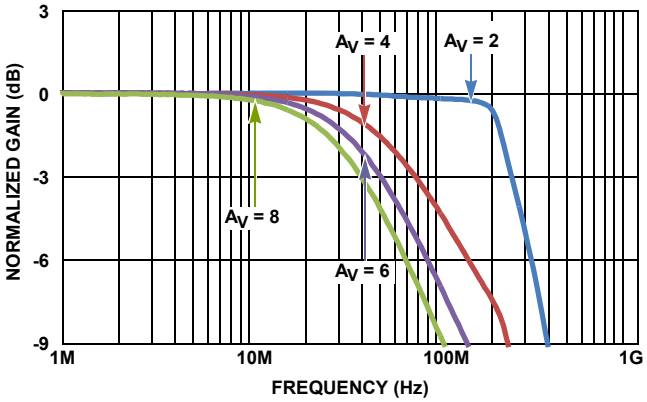


FIGURE 2. NON-INVERTING SMALL SIGNAL FREQUENCY REPONSE vs GAIN

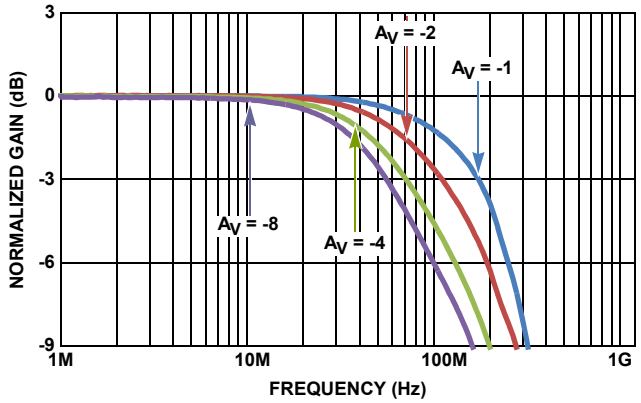


FIGURE 3. INVERTING SMALL SIGNAL FREQUENCY RESPONSE

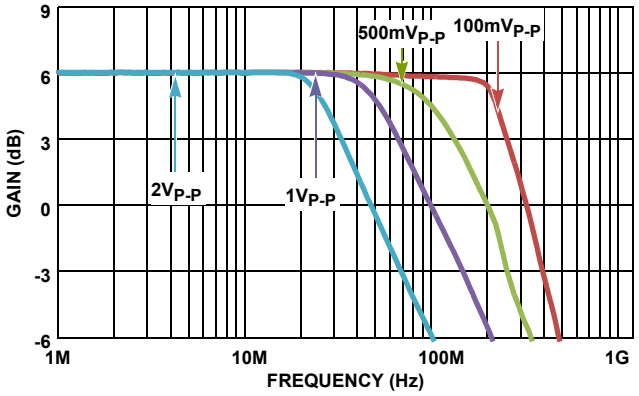


FIGURE 4. NON-INVERTING LARGE SIGNAL RESPONSE

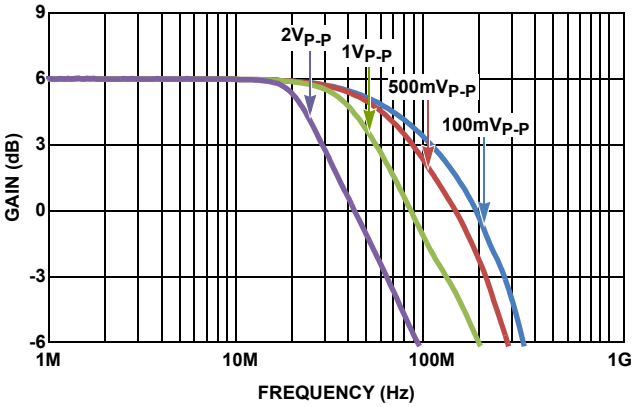


FIGURE 5. INVERTING LARGE SIGNAL RESPONSE

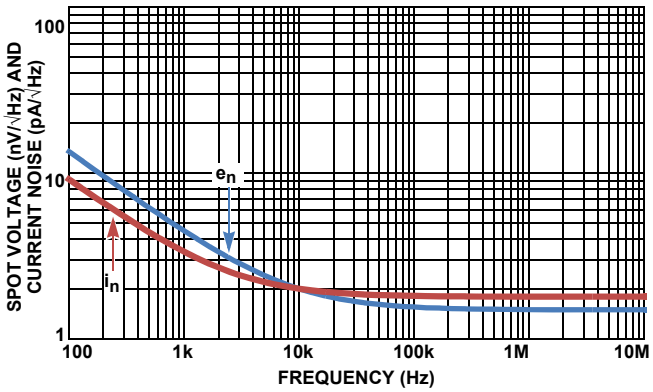


FIGURE 6. INPUT SPOT NOISE

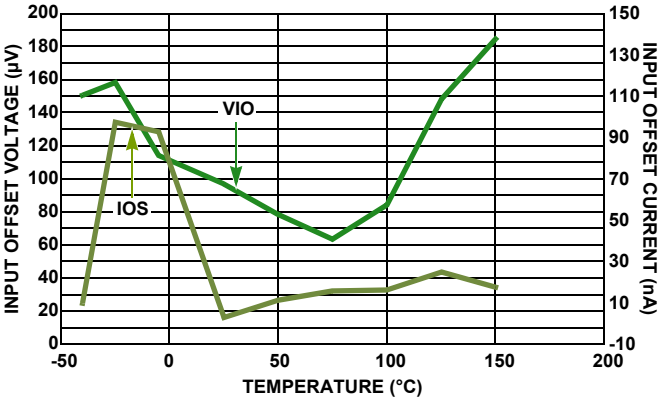


FIGURE 7. INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

Typical Performance Curves

V_S = ±6V, T_A ≈ +25°C, A_V = +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified. **(Continued)**

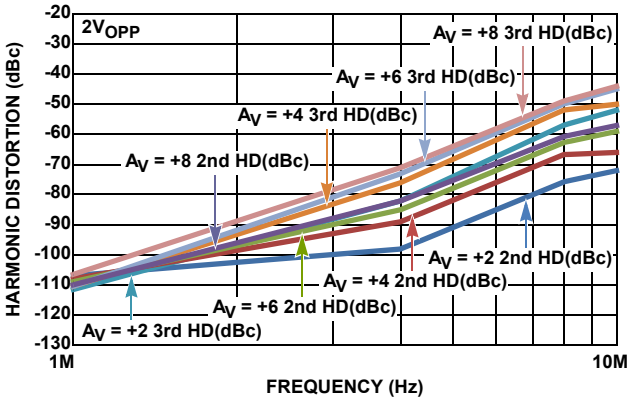


FIGURE 8. NON-INVERTING HD2 AND HD3 vs GAIN

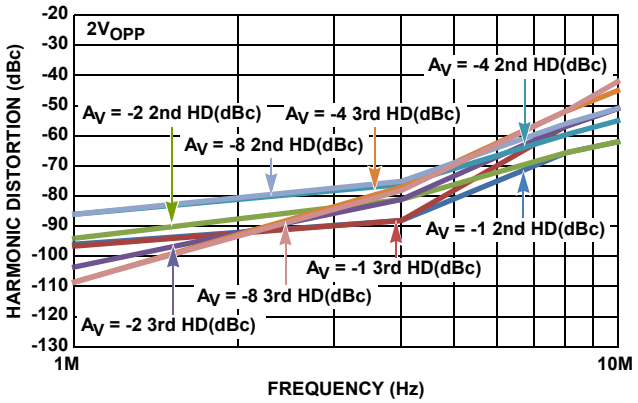


FIGURE 9. INVERTING HD2 AND HD3 vs GAIN

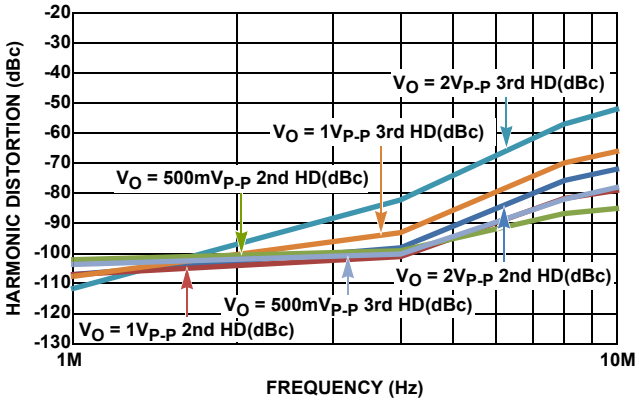


FIGURE 10. NON-INVERTING HD2 AND HD3 vs OUTPUT V_{P-P}

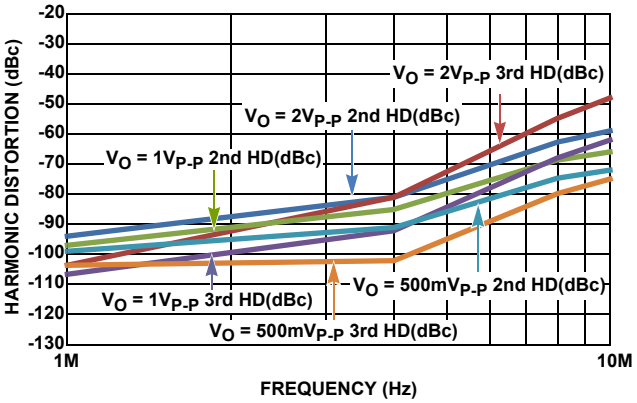


FIGURE 11. INVERTING HD2 AND HD3 vs OUTPUT V_{P-P}

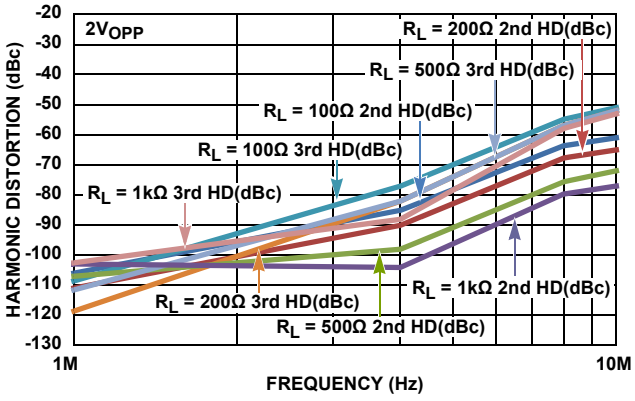


FIGURE 12. NON-INVERTING HD2 AND HD3 vs R_{LOAD}

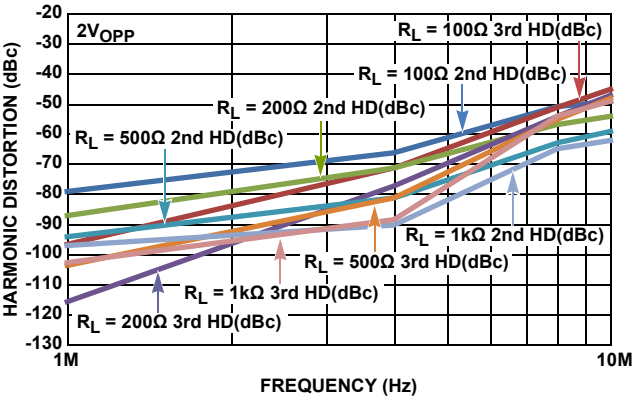


FIGURE 13. INVERTING HD2 AND HD3 vs R_{LOAD}

Typical Performance Curves

V_S = ±6V, T_A ≈ +25°C, A_V = +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified. **(Continued)**

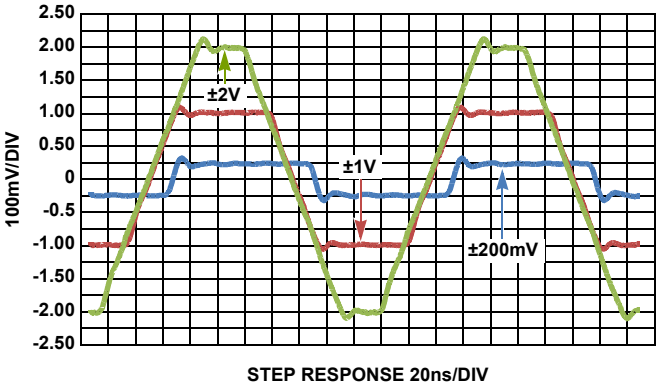


FIGURE 14. NON-INVERTING LARGE AND SMALL SIGNAL STEP RESPONSE

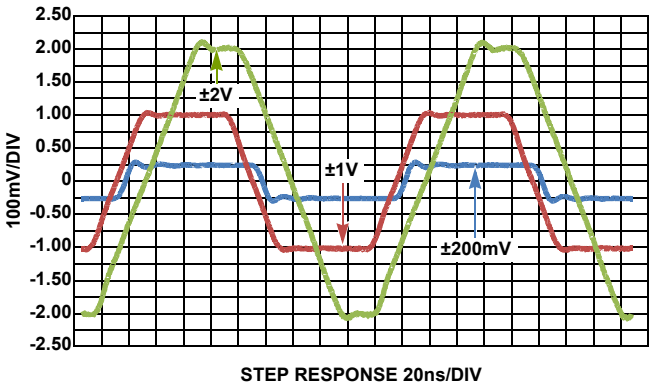


FIGURE 15. INVERTING LARGE AND SMALL SIGNAL STEP RESPONSE

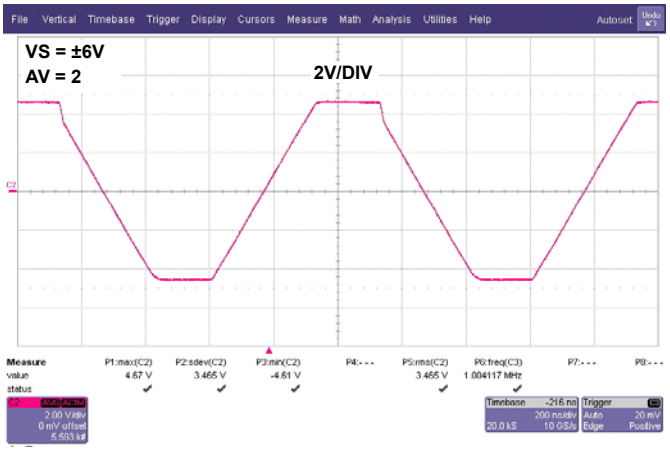


FIGURE 16. NON-INVERTING OVERDRIVE RECOVERY

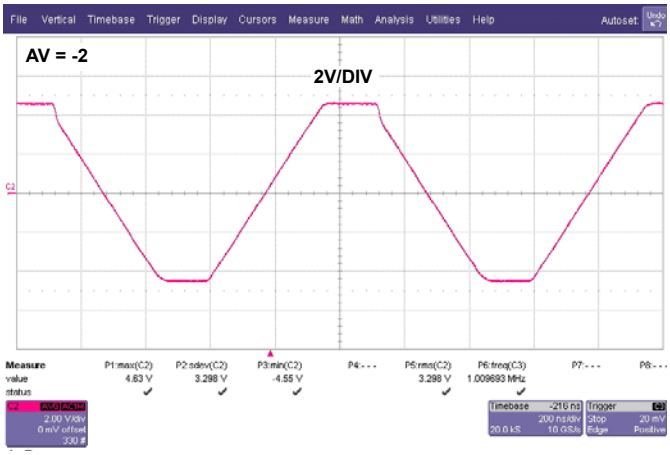


FIGURE 17. INVERTING OVERDRIVE RECOVERY

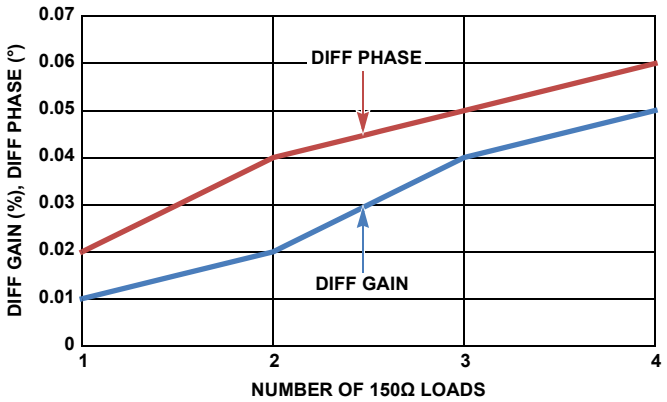


FIGURE 18. DIFFERENTIAL GAIN AND PHASE vs VIDEO LOADS

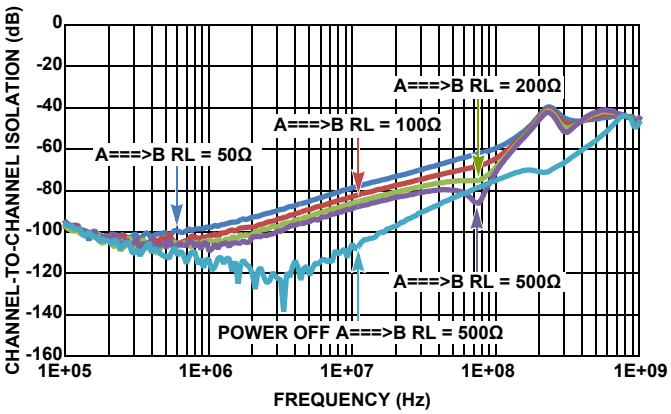


FIGURE 19. CHANNEL-TO-CHANNEL ISOLATION

Typical Performance Curves

V_S = ±6V, T_A ≈ +25°C, A_V = +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified. **(Continued)**

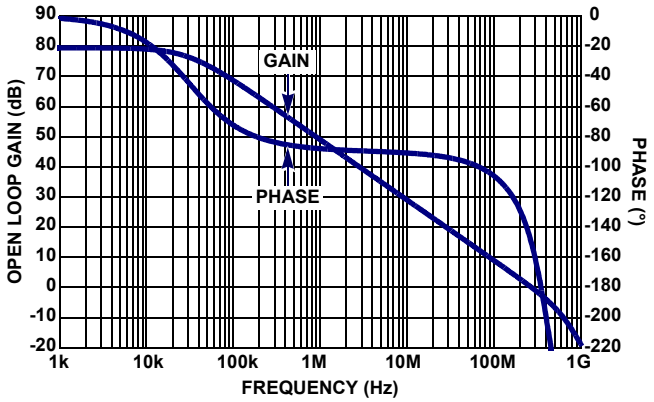


FIGURE 20. OPEN LOOP GAIN

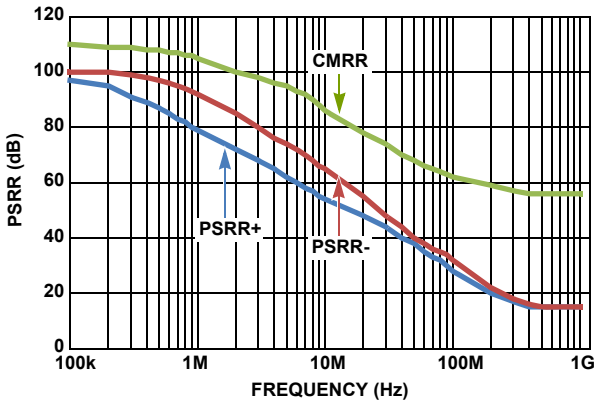


FIGURE 21. CMRR AND PSRR

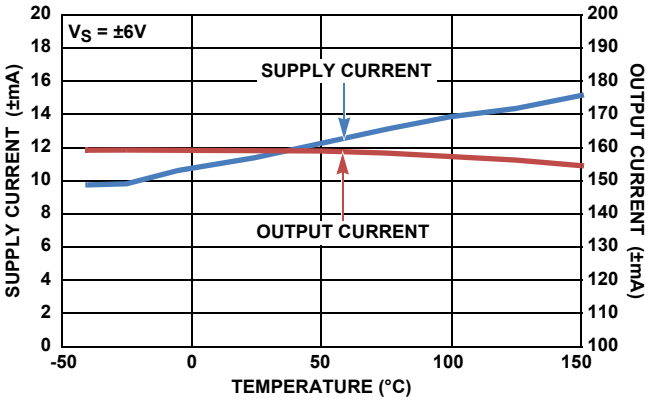


FIGURE 22. SUPPLY CURRENT AND OUTPUT CURRENT OVER-TEMPERATURE

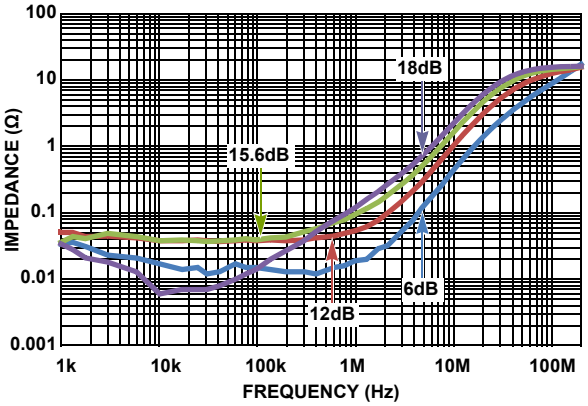


FIGURE 23. CLOSED LOOP OUTPUT IMPEDANCE vs GAIN

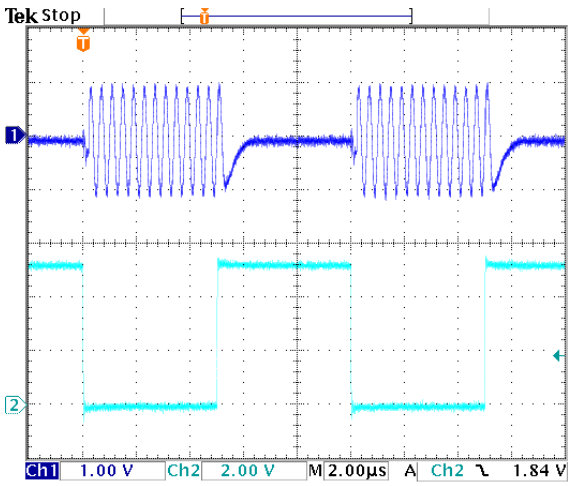


FIGURE 24. NON-INVERTING TURN ON AND TURN OFF DELAY

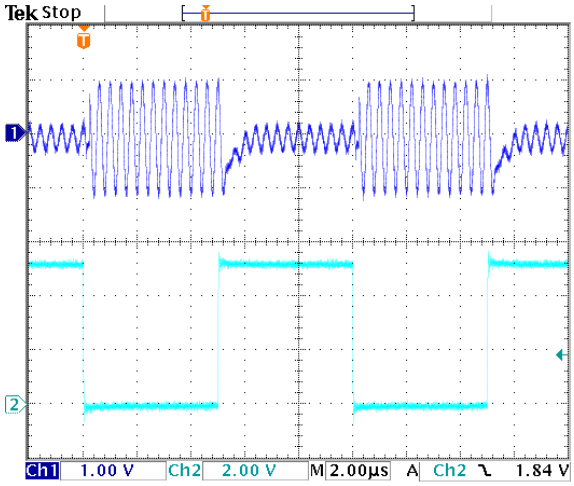


FIGURE 25. INVERTING TURN ON AND TURN OFF DELAY

Typical Performance Curves

V_S = ±6V, T_A ≈ +25°C, A_V = +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified. **(Continued)**

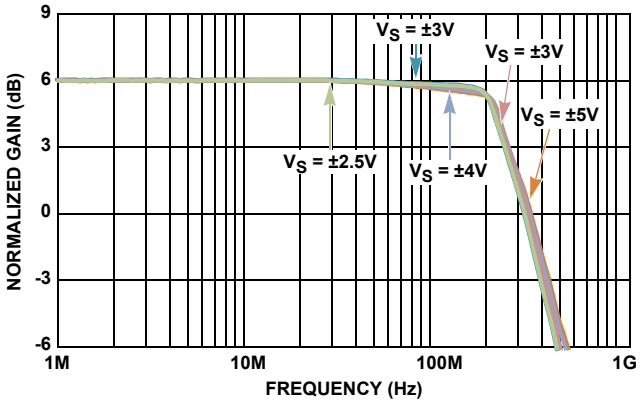


FIGURE 26. NON-INVERTING SMALL SIGNAL RESPONSE vs SUPPLY VOLTAGE

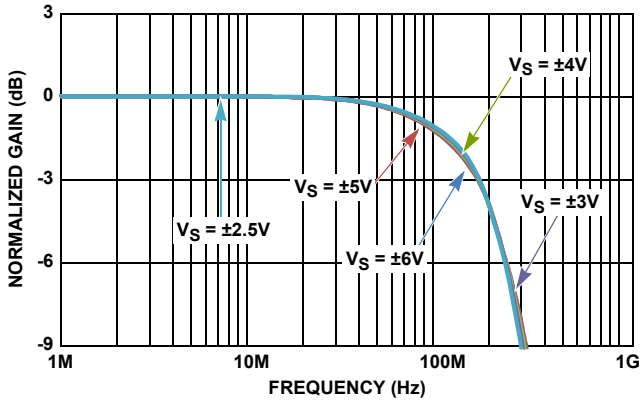


FIGURE 27. INVERTING SMALL SIGNAL RESPONSE VS SUPPLY VOLTAGE

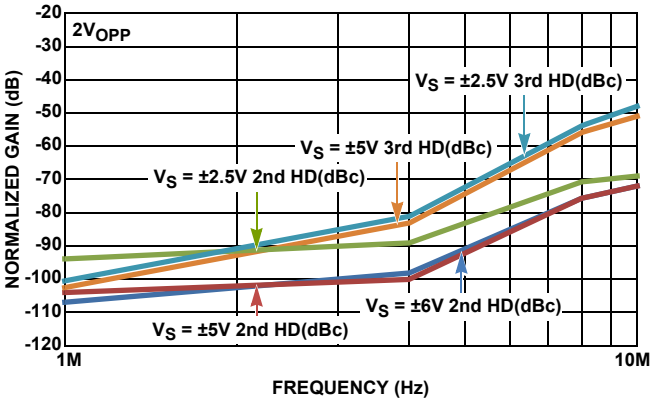


FIGURE 28. NON-INVERTING HD2 AND HD3 vs SUPPLY VOLTAGE

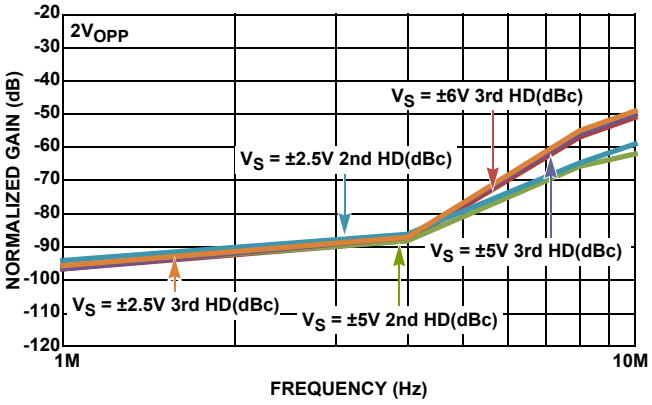


FIGURE 29. INVERTING HD2 AND HD3 vs SUPPLY VOLTAGE

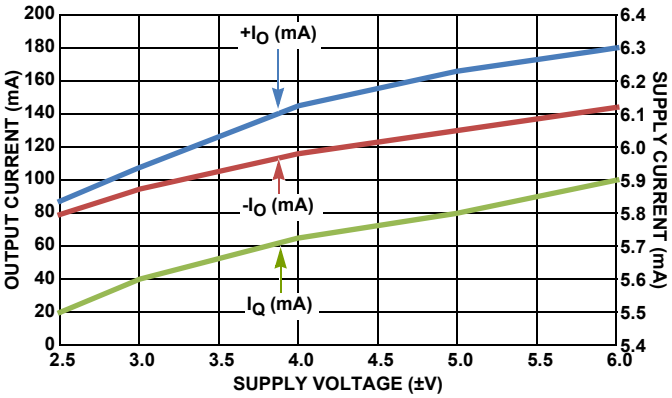


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

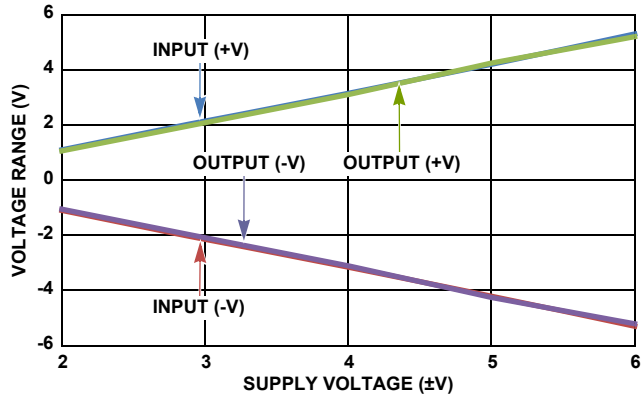


FIGURE 31. COMMON MODE INPUT RANGE AND OUTPUT SWING VS SUPPLY VOLTAGE

Typical Performance Curves

V_S = ±2.5V, T_A ≈ +25°C, A_V= +2V/V, R_F = 402Ω, R_{LOAD} = 500Ω, unless otherwise specified.

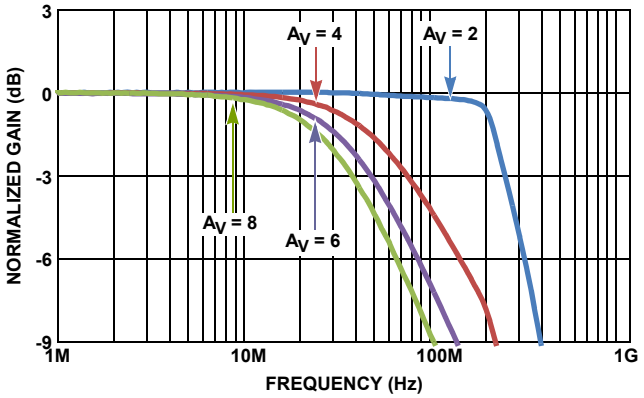


FIGURE 32. NON-INVERTING SMALL SIGNAL RESPONSE vs GAIN

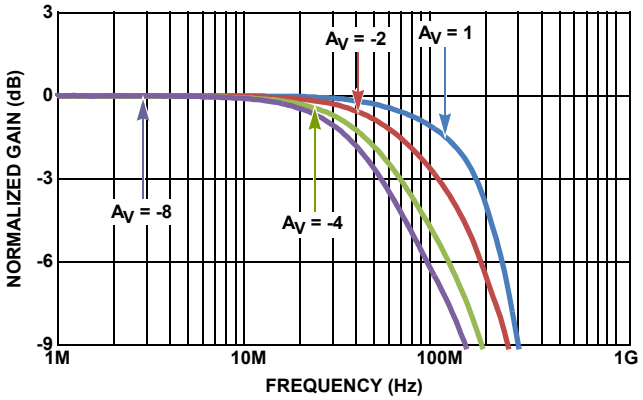


FIGURE 33. INVERTING SMALL SIGNAL RESPONSE vs GAIN

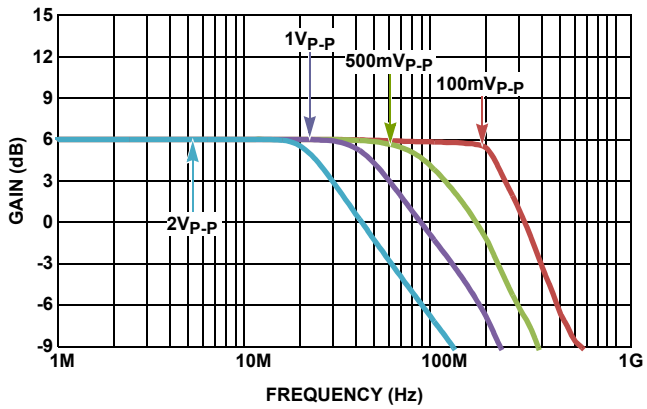


FIGURE 34. NON-INVERTING LARGE SIGNAL RESPONSE

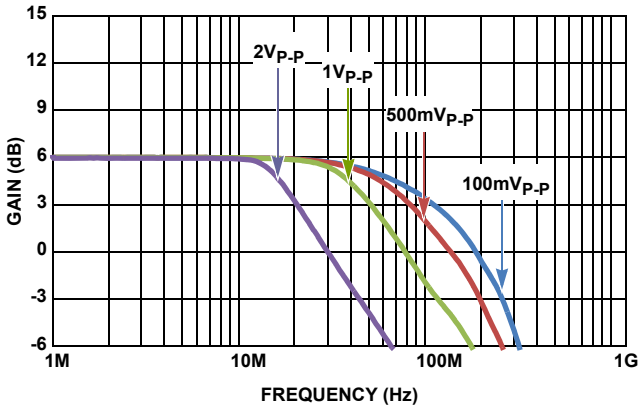


FIGURE 35. INVERTING LARGE SIGNAL RESPONSE

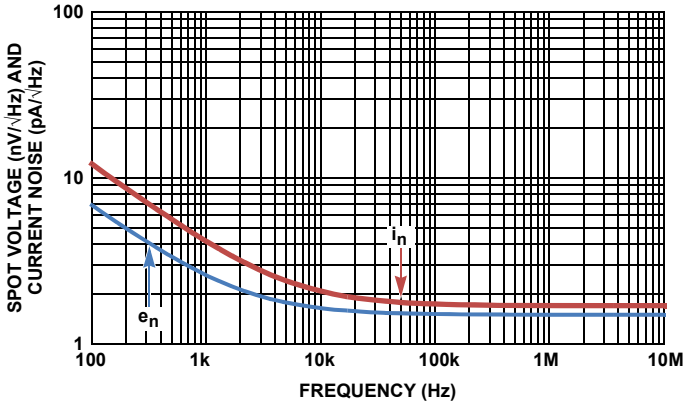


FIGURE 36. INPUT SPOT NOISE VOLTAGE AND CURRENT

Applications Information

Non-inverting Operation

The dual wideband EL5236 (and EL5237 with disable) provides a very power efficient low gain optimized amplifier solution using a slightly decompensated VFA design. This gives a lower input referred voltage noise and higher slew rate at the very low 5.6mA/ch nominal supply current. Unity gain operation is possible with external compensation but most high speed designs are at a gain > 1.

Figure 37 shows the gain of +2V/V configuration used for most of the characterization curves. As most lab equipment is expecting a 50Ω termination at the source, the non-inverting input and output show a 50Ω termination. The 402Ω feedback and gain resistors give a good compromise between several parasitic factors. These include the added noise of those resistors, loading effects, and to minimize the loss of phase margin back to the inverting node. A wide range of values can be used, where lower values will reduce noise with more output loading and higher values will start to dominate the output noise and introduce more phase margin loss into the loop. The EL5236 macromodel is a very good tool to predict the impact of these different values.

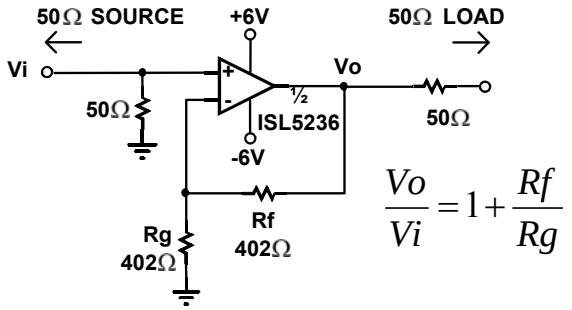


FIGURE 37. G = +2V/V CHARACTERIZATION CIRCUIT

Tests over gain (Figures 2, 8) held the Feedback R = 402Ω and varied the Rg element to achieve different gain settings.

Inverting Operation

Figure 38 shows the inverting gain configuration used for the inverting mode characterization curves. In this case, the feedback resistor is held at 402Ω while both the Rg and Rt elements are adjusted. Rg is adjusted to get different gains while Rt is adjusted to retain the input impedance at 50Ω. This does give a different loop gain (and hence bandwidth vs. gain) profile over gain as reflected in Figure 39. In a system application, Rm can be used to match the source impedance to get bias current cancellation. For the lowest noise, include a de-coupling capacitor across that resistor (0.1µF in Figure 38).

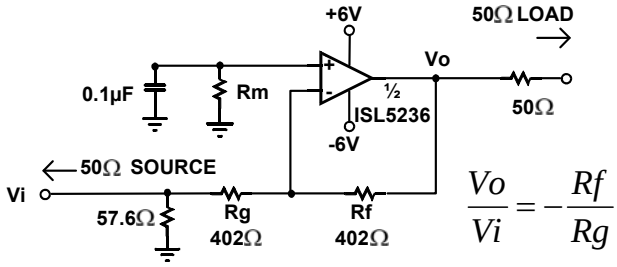
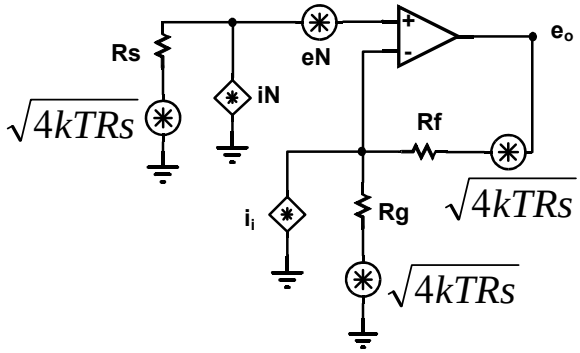


FIGURE 38. G = -1V/V CHARACTERIZATION CIRCUIT

Getting the Lowest Noise

A very low noise op amp like the EL5236 will only deliver a low output noise if the resistor values used to implement the design add a noise contribution that is also low. Figure 39 shows the full noise model for a non-inverting configuration.



$$NoiseGain = 1 + \frac{Rf}{Rg}$$

FIGURE 39. OP AMP NON-INVERTING NOISE ANALYSIS CIRCUIT

Each of these voltage and current noise terms will contribute to an output noise power. Getting the gains for each, then squaring, summing, and then taking the square root will give the combined output spot noise using the model of Figure 39 as shown in Equation 1:

$$e_o = \sqrt{\left(e_n^2 + \left(i_n R_s\right)^2 + 4kTR_s\right) * \left(NG\right)^2 + \left(i_i R_f\right)^2 + 4kTR_f\left(NG\right)} \quad \text{(EQ. 1)}$$

The source resistor shows up combining with the op amps non-inverting input voltage noise to give a total non-inverting input noise that then gets the full noise gain to the output. As a point of reference, solve for where those noise terms equal the contribution from just the op amp voltage noise. This is given in Equation 2 and evaluating this for the 1.5nV and 1.8pA input noise terms gives Rs = 136Ω.

$$R_s = \frac{2kT}{i_n^2}\left(\sqrt{1 + \left(\frac{e_n i_n}{2kT}\right)^2} - 1\right) \quad \text{(EQ. 2)}$$

Similarly, compare the output noise due to just the non-inverting input noise voltage to the terms on the inverting node in Equation 1. Solving for equality there (to get a maximum Rf value to limit the inverting side noise contributions at the output), gives Equation 3. Evaluating this for 1.5nV and 1.8pA input noise terms at a NG = 2 gives an Rf = 272Ω.

$$R_f = \frac{2kT}{i_n^2} NG\left(\sqrt{1 + \left(\frac{e_n i_n}{2kT}\right)^2} - 1\right) \quad \text{(EQ. 3)}$$

This simplified analysis indicates the 402Ω used for the non-inverting characterization is already starting to dominate the output noise at a gain of 2. Going up in gain, with a fixed Rf = 402Ω, will quickly make those input side terms dominant.

This approximate analysis is intended to show the importance of working with relatively low resistor values if the low noise of the EL5236 is to be retained. It also shows why, with an inverting configuration, it is important to either keep a low impedance on the non-inverting input and/or add a noise shunting capacitor across it.

DC Precision

The EL5236 offers extremely low input offset voltage and input offset current. To take full advantage of the very low offset current (<±500nA), the source resistance looking out of the two inputs must be matched. Figure 40 shows the output DC offset analysis circuit.

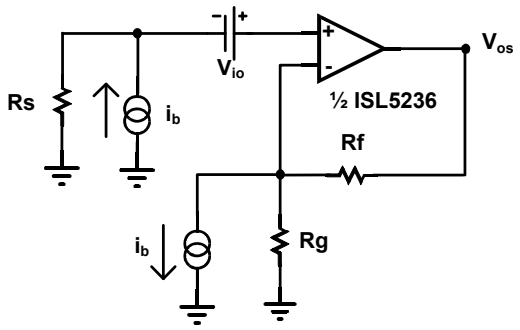


FIGURE 40. OUTPUT DC OFFSET ANALYSIS CIRCUIT

If Rs = Rf||Rg is imposed on the design, the total output offset will be given by Equation 4:

$$V_{os} = \pm V_{io} * NG \pm I_{os} * R_f \quad \text{(EQ. 4)}$$

Putting in the specified worst case limits of ±3mV for the offset voltage and ±500nA for the offset current into a NG = 2 and Rf = 402Ω condition would give an output DC error envelope of ±6.2mV. This is assuming the Rs is set to 201Ω. To change Figure 37 to a 201Ω Rs, add a 175Ω in series with the V+ node from the 50Ω termination. This will reduce the output offset induced from the Ib terms to the ±0.2mV part of the ±6.0mV computed above – at the cost of a bit higher input noise.

A second issue would be the tempco of the output offset voltage. To the extent that the output is dominated by the offset voltage term, its drift will dominate. The specified typical input Vos drift is -300nV/°C. Continuing this example, that would give a typical output drift of -0.6µV/°C. Over a +50°C ambient range, this would map to only a 30µV shift in the output offset voltage.

Active Filter Designs

Being a low gain stable wideband VFA op amp, the EL5236 is particularly suited to differential I/O active filters, as shown in Figure 1. That relatively complex example gives a 5th order Butterworth filter as part of an output stage interface to a complementary DAC output current. These DAC output stages generate both a common mode voltage and a differential signal at the termination resistors to ground. The design of Figure 1 gets the real pole as part of that termination then implements the two complex pole pairs as an SKF stage followed by an MFB stage. This gives much better stop band rejection using the 2nd MFB stage and allows an easy place to introduce a common mode level shift to remove the DAC output common mode. This was used to return the final output to be a ground centered differential signal. The MFB design of the output stage uses a feedback capacitor inside the filter that normally expects a unity gain stable op amp for implementation. Adding the two capacitors to ground on the inverting inputs of this stage shapes the noise gain up at higher frequencies holding this stage stable.

Simpler designs are possible as shown in Figure 41. This is a single stage gain of 2 Butterworth filter with a 20MHz cutoff. Even with the 300MHz gain bandwidth product of the EL5236, this is a fairly high frequency filter to attempt with this relatively limited amplifier bandwidth margin. In this case, the Rf = Rg = 649Ω is also being set to get bias current cancellation for improved output DC precision along with the necessary gain of 2 setting for the design.

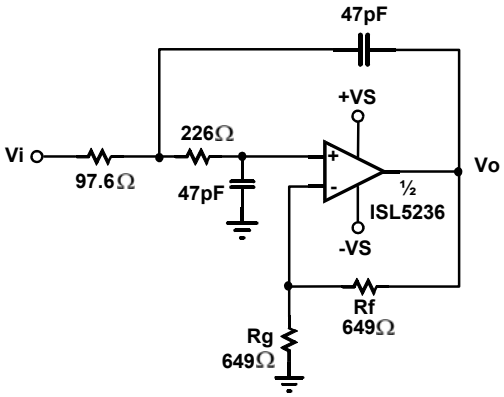


FIGURE 41. GAIN = +2V/V, 20MHZ 2nd ORDER BUTTERWORTH LOW PASS ACTIVE FILTER

This design was produced using the Intersil online active filter designer which includes an amplifier bandwidth adjustment in the R1 and R2 values. It is a general active filter tool tailored to the available precision and high speed op amps from Intersil. It is available at the following link:

http://web.transim.com/iSimFilter/Pages/DesignReq.aspx

As shown in the simulated vs. ideal curves of Figure 42, the design is doing a very good job of matching the ideal response through 80MHz. All SKF filters deviate from the ideal roll-off at higher frequencies due to the increase in output impedance as the amplifier bandwidth is approached.

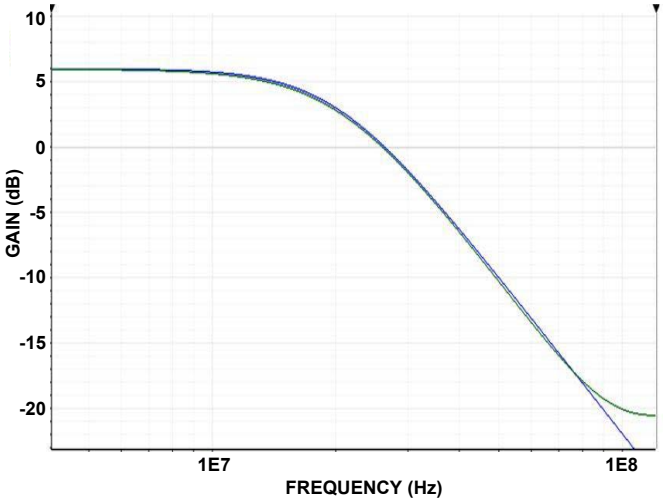


FIGURE 42. SIMULATED vs IDEAL FILTER RESPONSE COMPARISON

Shutdown Operation (EL5237 only)

EL5237 has the feature to enable or disable each amplifier to save power when not in use. Pulling low will enable the amplifier and pulling high will disable the amplifier. Refer to the “Electrical Specifications” tables for appropriate values to use.

Power Supply De-coupling and Layout

Short feedback loop is essential in the layout of the op amp board as well as minimizing the capacitance around the inverting/non-inverting input pins and output pins. A 0.1µF ceramic capacitor placed close to the supply pins allows for proper supply de-coupling.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 31, 2011	FN7833.0	Initial release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: EL5236, EL5237

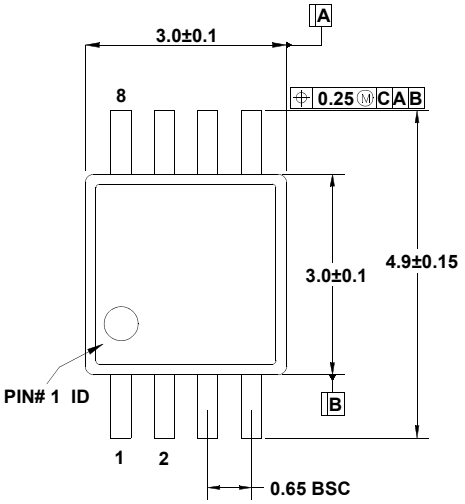
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

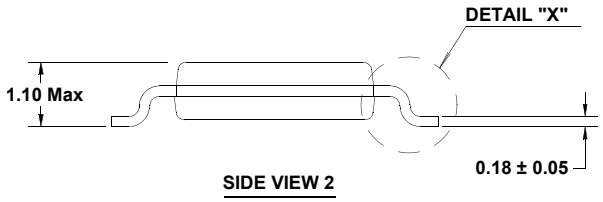
Package Outline Drawing

M8.118A

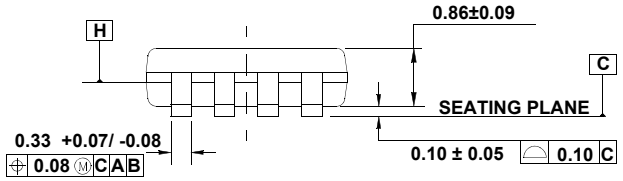
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



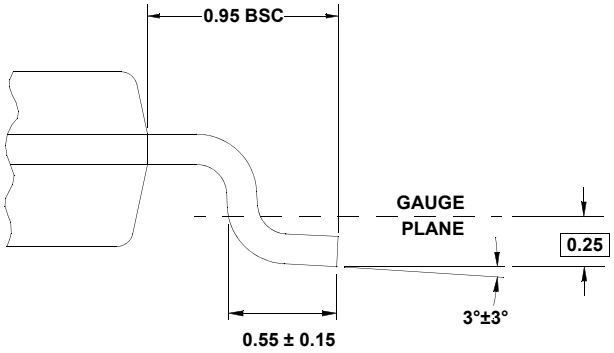
TOP VIEW



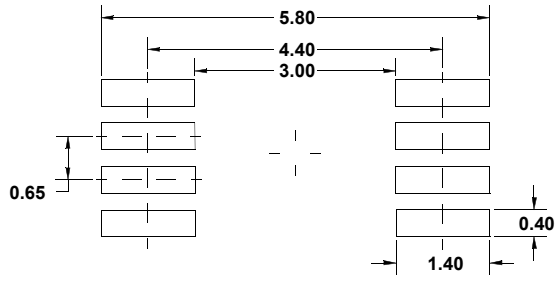
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

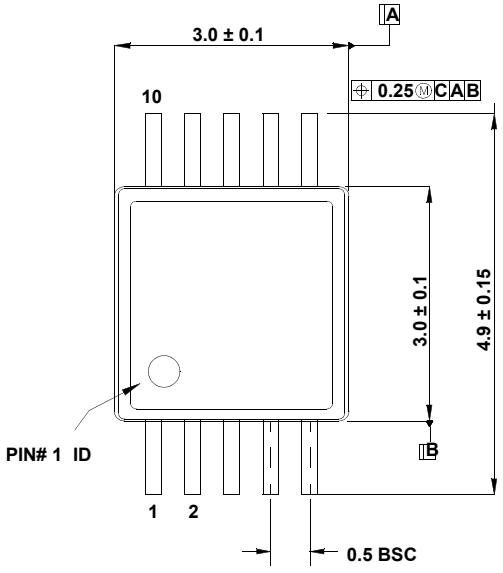
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

Package Outline Drawing

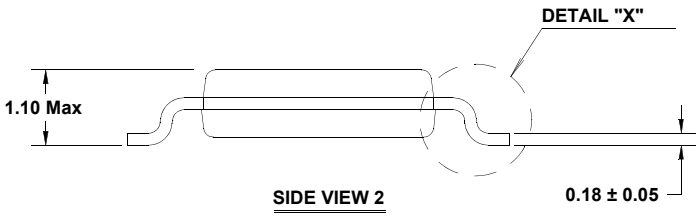
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

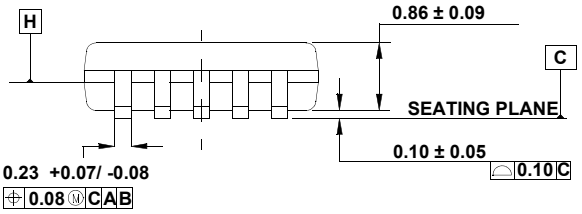
Rev 0, 9/09



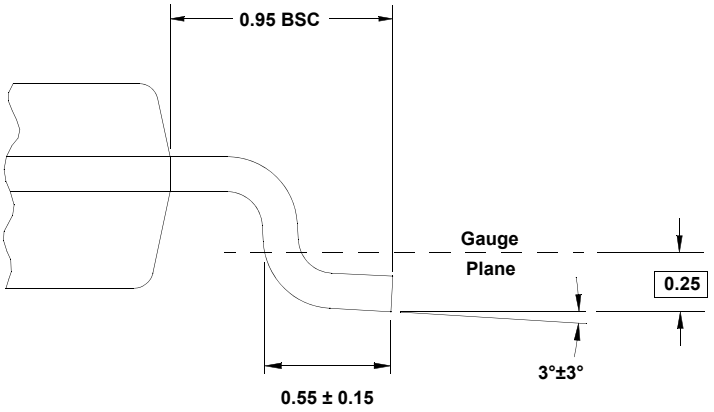
TOP VIEW



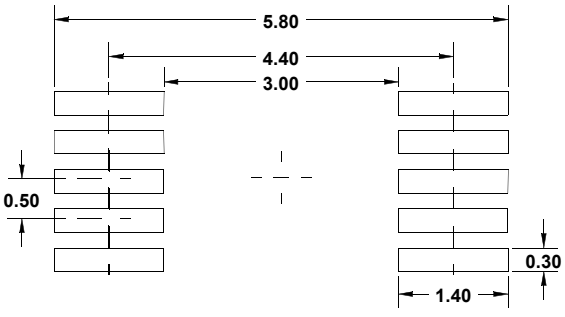
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

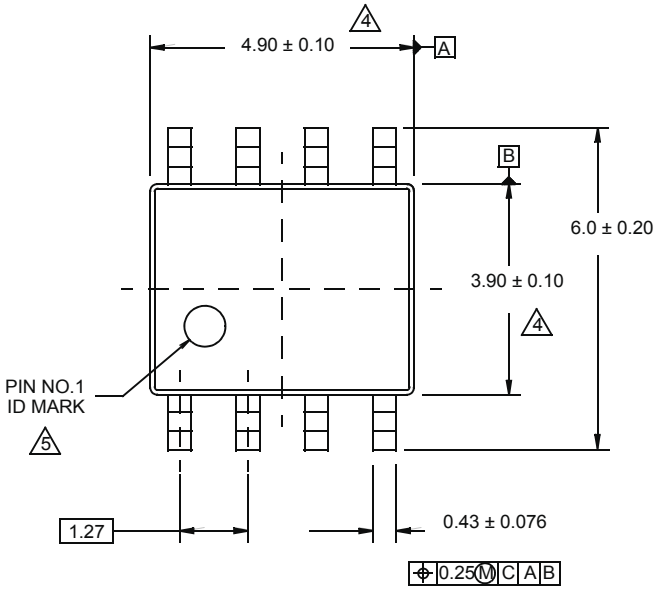
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

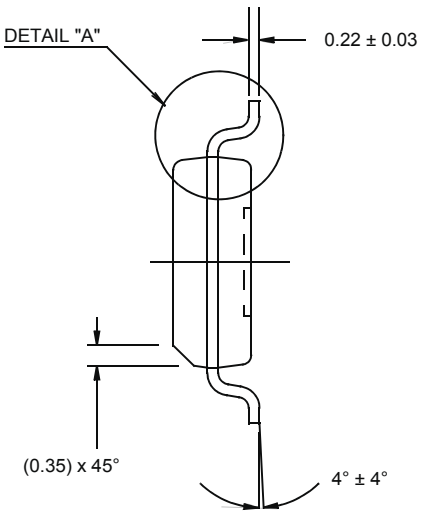
Package Outline Drawing

M8.15E

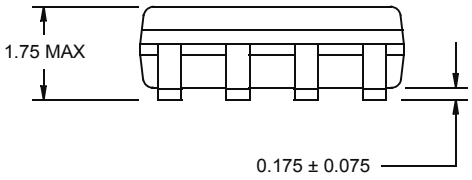
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



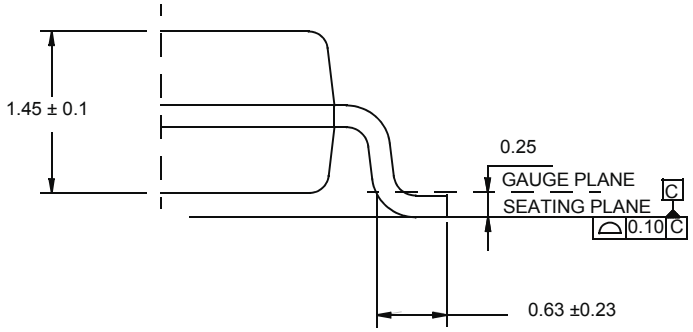
TOP VIEW



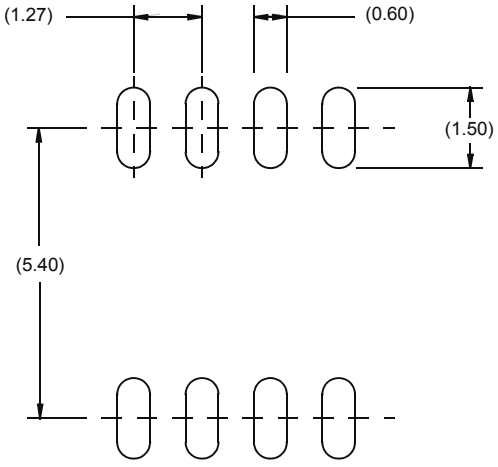
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.