

TOSHIBA Bipolar Linear IC Silicon Monolithic

# TA2152FLG

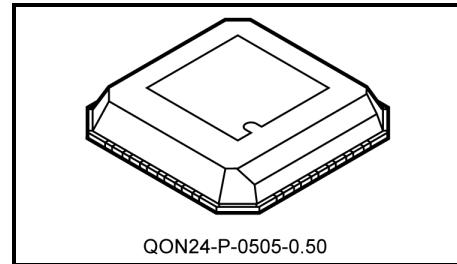
## Low Current Consumption Headphone Amplifier (for 1.5-V/3-V Use)

The TA2152FLG is a headphone amplifier of low current consumption type developed for portable digital audio.

It is especially suitable for portable CD players, portable MD players etc.

### Features

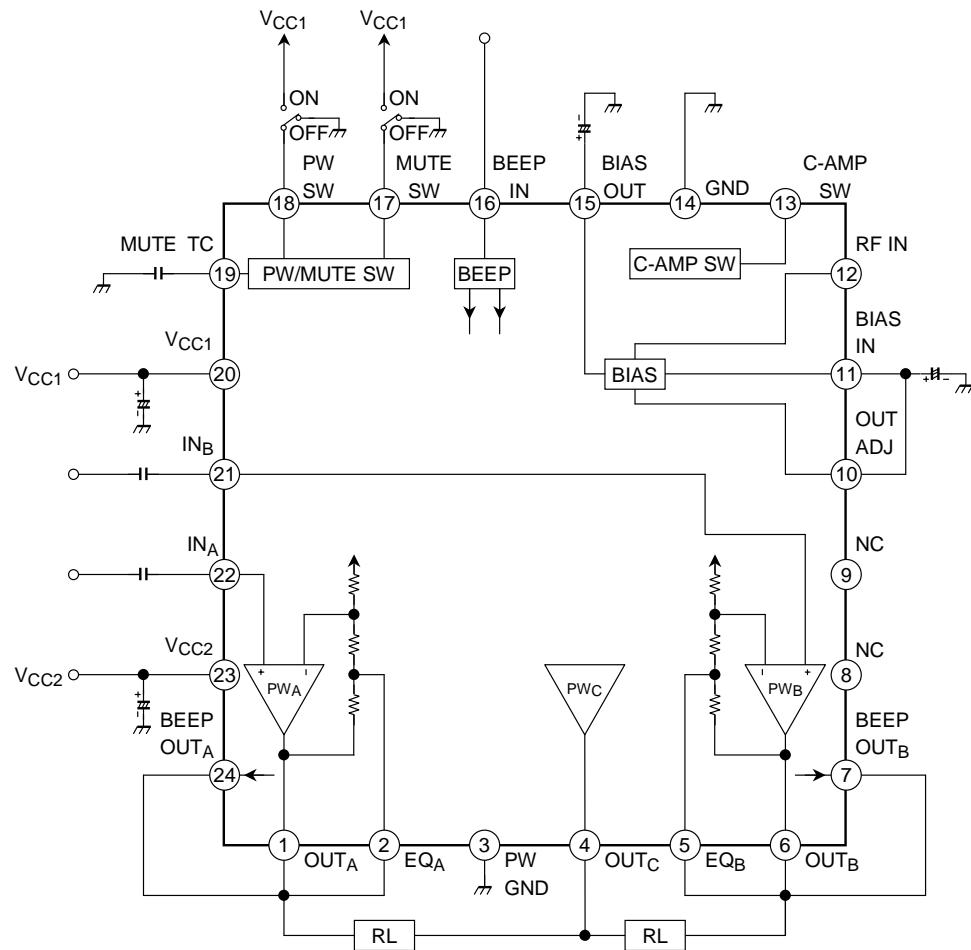
- Low current consumption
  - The power amplifier output stage can be driven using a single battery.  
As a result, overall current consumption is low.
  - Built-in center amplifier switch  
For the output-coupling type, the consumption current has been decreased still further.
  - Current value (VCC1 = 2.4 V, VCC2 = 1.2 V, f = 1 kHz, RL = 16 Ω, Ta = 25°C, typ.)
    - Output-coupling type
      - No Signal: ICC (VCC1) = 0.4 mA, ICC (VCC2) = 0.3 mA
      - 0.1 mW × 2 ch: ICC (VCC1) = 0.5 mA, ICC (VCC2) = 2.2 mA
      - 0.5 mW × 2 ch: ICC (VCC1) = 0.5 mA, ICC (VCC2) = 5.0 mA
    - OCL type
      - No Signal: ICC (VCC1) = 0.7 mA, ICC (VCC2) = 0.7 mA
      - 0.1 mW × 2 ch: ICC (VCC1) = 0.7 mA, ICC (VCC2) = 4.5 mA
      - 0.5 mW × 2 ch: ICC (VCC1) = 0.8 mA, ICC (VCC2) = 10.0 mA
  - Output power: Po = 8 mW (typ.)  
(VCC1 = 2.4 V, VCC2 = 1.2 V, f = 1 kHz, RL = 16 Ω, THD = 10%, Ta = 25°C)
  - Voltage gain: GV = 11.5dB (typ.)
  - Built-in beep function
  - Built-in low-pass compensation (output-coupling type)
  - Built-in mute switch
  - Built-in power switch
  - Operating supply voltage range (Ta = 25°C)  
VCC1 (opr) = 1.8 V~4.5 V  
VCC2 (opr) = 0.9 V~4.5 V



Weight: 0.05 g (typ.)

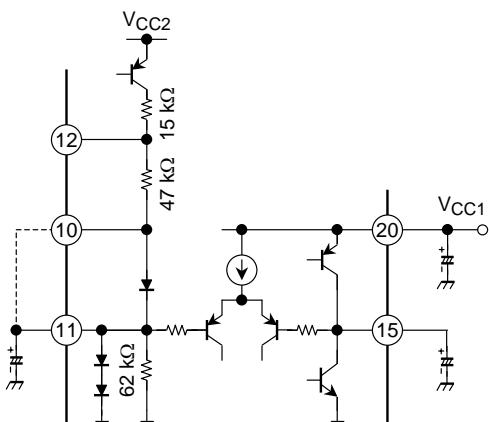
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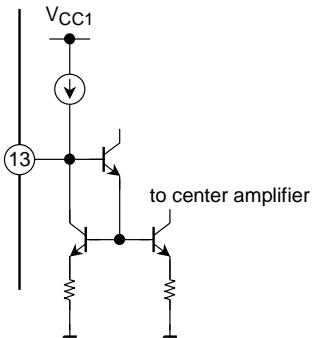
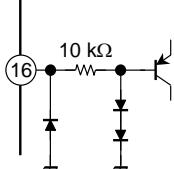
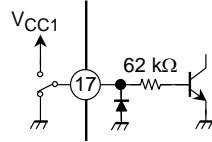
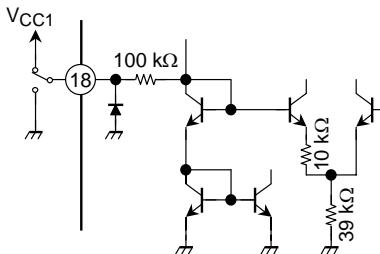
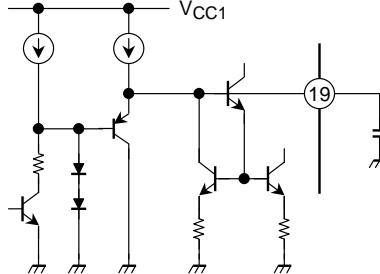
## Block Diagram (of OCL Application)



## Pin Descriptions

**Pin Voltage: Typical pin voltage for test circuit when no input signal is applied**  
 $(V_{CC1} = 2.4 \text{ V}, V_{CC2} = 1.2 \text{ V}, T_a = 25^\circ\text{C})$

Pin	Function	Internal Circuit	Pin Voltage (V)	
No.	Name			
1	OUT <sub>A</sub>	<p>Outputs from power amplifier</p> <p>3 PW GND GND for power drive stage</p> <p>23 V<sub>CC2</sub> V<sub>CC</sub> for power drive stage</p>	0.6	
4	OUT <sub>C</sub>			
6	OUT <sub>B</sub>			
21	IN <sub>B</sub>			
22	IN <sub>A</sub>			
7	BEEP OUT <sub>B</sub>	<p>Outputs for beep signal</p>	—	
24	BEEP OUT <sub>A</sub>			
14	GND	GND for everything other than power drive stage	0	
8	NC	Not connected	—	
9	NC		—	
10	OUT ADJ	DC output voltage adjustment Either connect this pin or leave it open depending on the level of V <sub>CC2</sub> . If the power supply of a 1.5 V system is applied to V <sub>CC2</sub> , connect this pin to BIAS IN (pin11). If the power supply of a 3 V system is applied to V <sub>CC2</sub> , leave this pin open.		0.6
11	BIAS IN	Bias circuit input		
12	RF IN	Ripple filter input		
15	BIAS OUT	Bias circuit output		
20	V <sub>CC1</sub>	V <sub>CC</sub> for everything other than power drive stage		

Pin		Function	Internal Circuit	Pin Voltage (V)
No.	Name			
13	C-AMP SW	Center amplifier switch (C-Cup type: GND (OCL type: Open		—
16	BEEP IN	Beep signal input If the beep function is not used, this pin is connected to GND.		—
17	MUTE SW	Mute switch (Mute OFF: L level (Mute ON: H level Refer to application note (6)		—
18	PW SW	Power switch (IC ON: H level (IC OFF: L level Refer to application note (6)		—
19	MUTE TC	Mute smoothing Reduces pop noises during switching.		—

## Application Notes

### (1) Beep function

In Power Mute Mode, the beep signal from the microcomputer or other controlling device is input on the BEEP IN pin (pin 16). This signal is output as a current which flows to the load via the BEEP output pin (pin 7/24). The beep level is set to  $V_0 = -50\text{dBV}$  ( $R_L = 16\Omega$  (typ.)). For the beep signal timing, please refer to Figure 1.

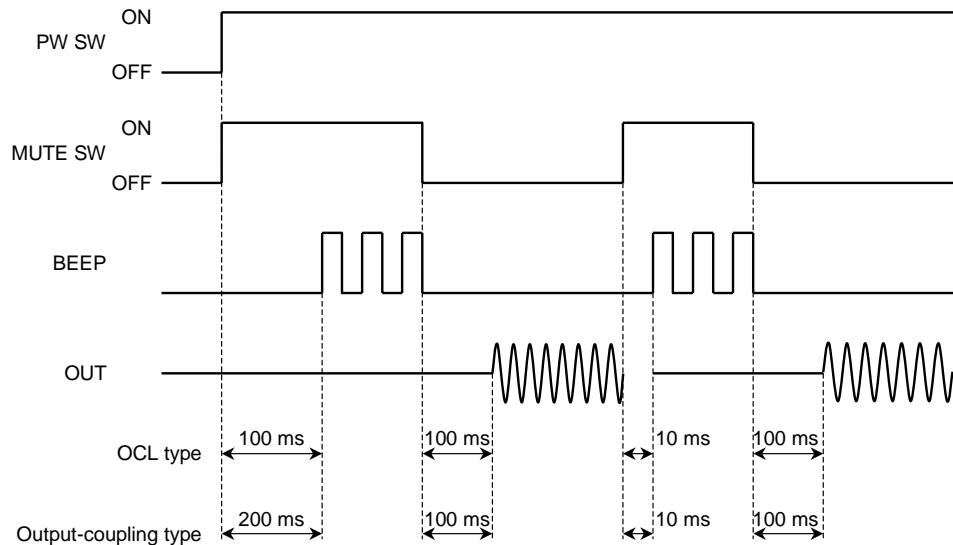


Figure 1 Timing chart for beep and output signals

### (2) Low-cut compensation

For output-coupling type, the low-frequency range can be decreased using an output-coupling capacitor and a load ( $f_c = 45\text{ Hz}$  at  $C = 220\text{ }\mu\text{F}$ ,  $R = 16\Omega$ ). However, since the capacitor is connected between the IC's output pin (pin 1/6) and EQ pin (pin 2/5), the low-frequency gain of the power amplifier increases, enabling low-cut compensation to be performed. For the response of capacitors of different values, please refer to Figure 2.

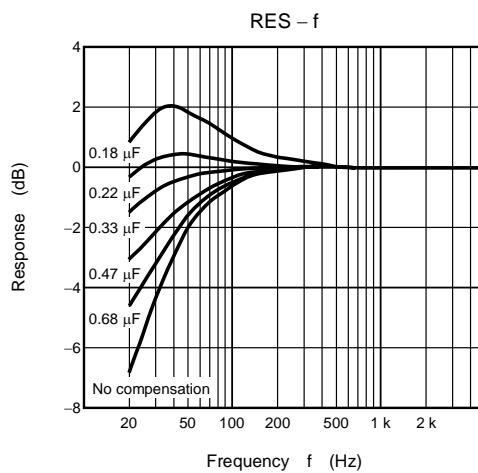


Figure 2 Capacitor response

### (3) Adjustment of DC output voltage

Please perform the OUT ADJ pin (pin 10) as follows by the power supply of VCC1 and VCC2.

- If a boost voltage is applied to VCC1, VCC2 is connected to a battery and the difference between VCC1 and VCC2 is greater than or equal to 0.7 V, short pins 10 and 11 together. In this case the DC output voltage

will be  $\frac{V_{CC2}}{2}$ .

- If the difference between VCC1 and VCC2 is less than 0.7 V, or if VCC1 and VCC2 are connected to the same power supply, leave pin 10 open.

In these cases the DC output voltage will be  $\frac{V_{CC2} - 0.7 \text{ V}}{2}$ .

However, when the voltage level of VCC2 is high, the DC output voltage is will be set to approximately 1.4 V.

### (4) RF IN pin

The ripple rejection ratio can be improved by connecting a capacitor to this pin. Connection of a capacitor is recommended, particularly for output-coupling type.

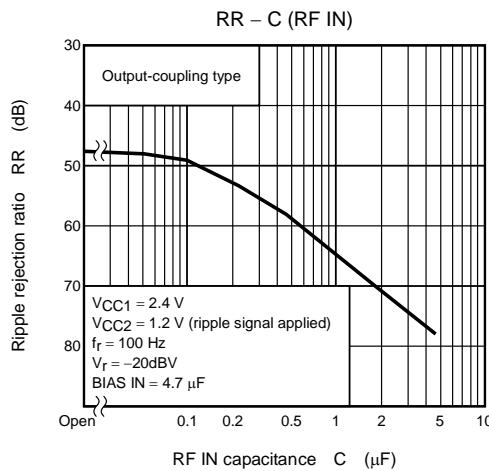


Figure 3 Improvement of ripple rejection ratio

### (5) Output application of power amplifier

For output-coupling type the center amplifier is not used with the result that current consumption is low.

Please set the C-AMP SW pin (pin 13) accordingly.

- Output-coupling type: Pin 13 is connected to GND.
- OCL type: Pin 13 is open.

## (6) Switching pins

### (a) PW SW

The device is ON when this pin is set to High. To prevent the IC being turned ON by external noise, it is necessary to connect an external pull-down resistor to the PW SW pin. The pin is highly sensitive.

### (b) MUTE SW

If the MUTE SW pin is fixed to High, current will flow through the pin, even when the PW SW pin is in OFF Mode. To prevent the IC being turned ON by external noise, it is necessary to connect an external pull-down resistor.

The pop noise heard when the MUTE SW switch is turned ON or OFF can be reduced by connecting an external capacitor to the MUTE TC pin.

### (c) Switch sensitivity ( $T_a = 25^\circ\text{C}$ )

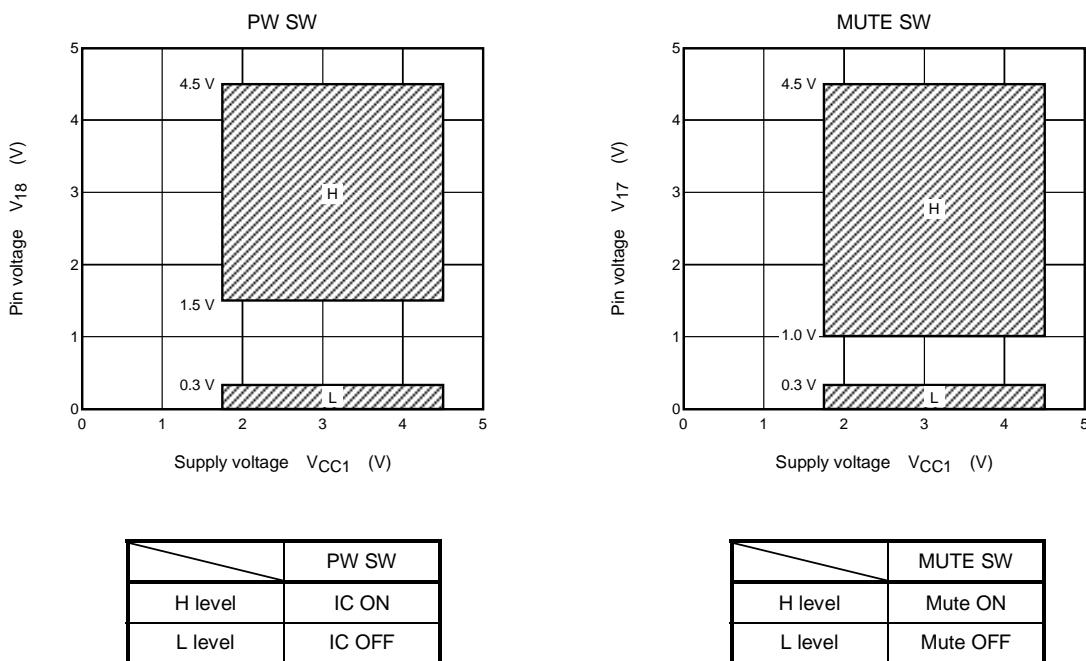


Figure 4 Switch sensitivity

## (7) Miscellaneous

The following capacitors must have excellent temperature and frequency characteristics.

- Capacitor between VCC1 (pin 20) and GND (pin 14)
- Capacitor between VCC2 (pin 23) and PW GND (pin 3)
- Capacitor between BIAS IN (pin 11) and GND (pin 14)
- Capacitor between BIAS OUT (pin 15) and GND (pin 14)
- Capacitor between RF IN (pin 12) and GND (pin 14)

**Absolute Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Supply voltage 1	V <sub>CC1</sub>	4.5	V
Supply voltage 2	V <sub>CC2</sub>	4.5	
Output current	I <sub>o</sub> (peak)	100	mA
Power dissipation	P <sub>D</sub> (Note)	350	mW
Operating temperature	T <sub>opr</sub>	-25~75	°C
Storage temperature	T <sub>stg</sub>	-55~150	°C

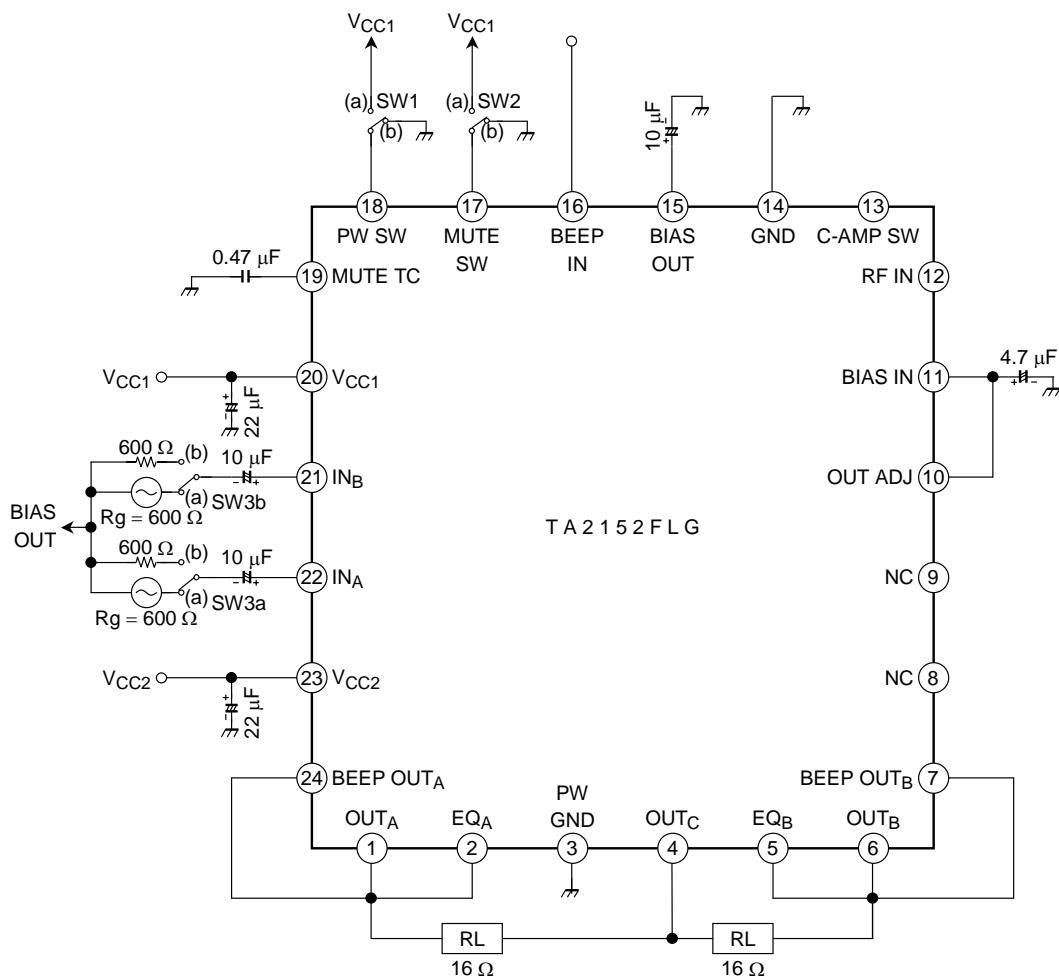
Note: Derated by 2.8 mW/°C above Ta = 25°C

**Electrical Characteristics**

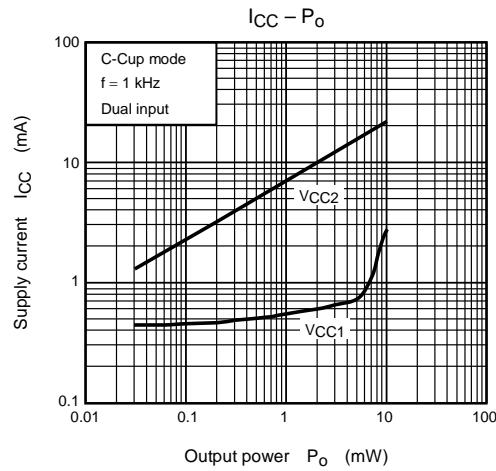
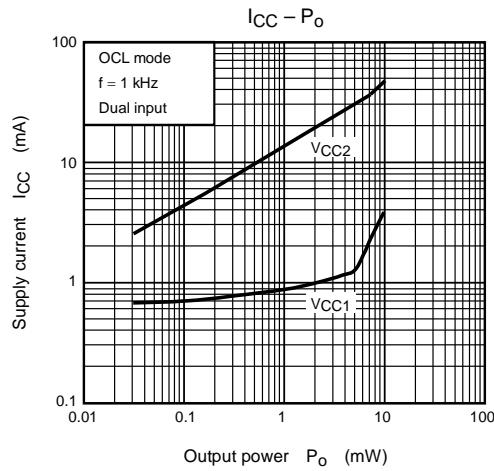
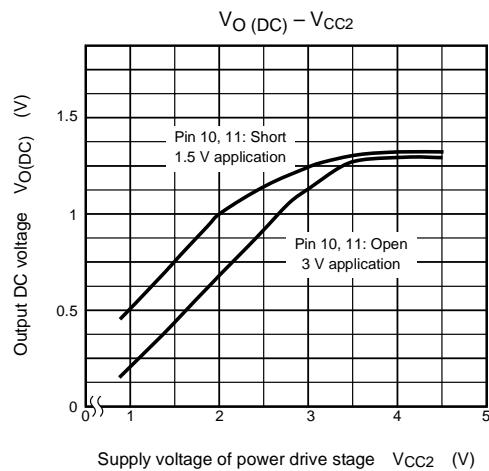
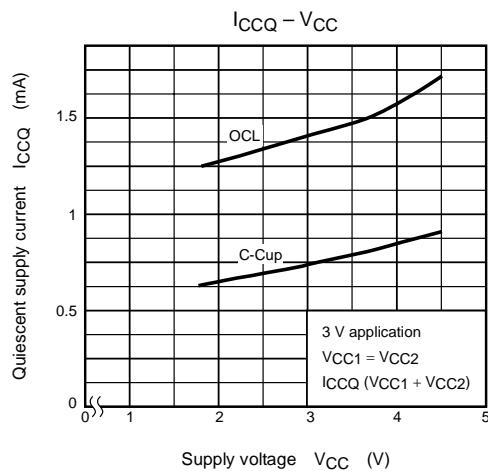
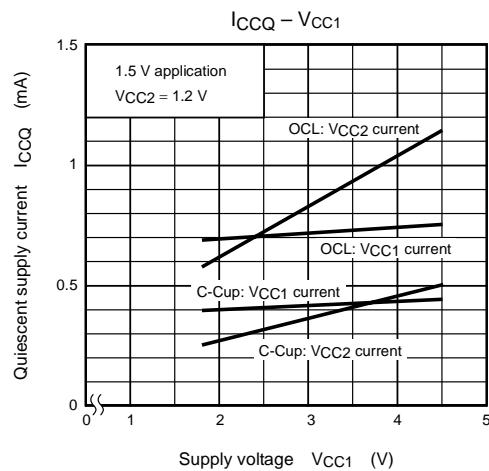
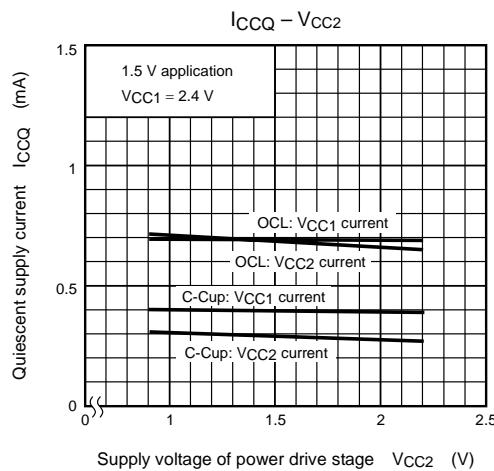
**(Unless otherwise specified V<sub>CC1</sub> = 2.4 V, V<sub>CC2</sub> = 1.2 V, R<sub>g</sub> = 600 Ω, R<sub>L</sub> = 16 Ω, f = 1 kHz, Ta = 25°C, SW1: a, SW2: b, SW3: a)**

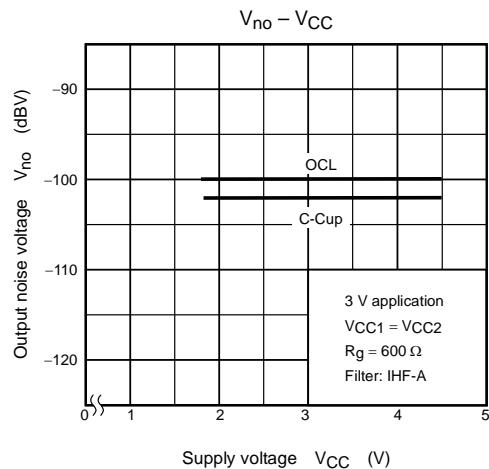
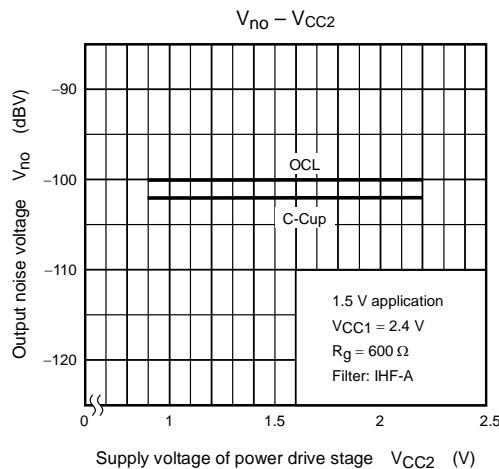
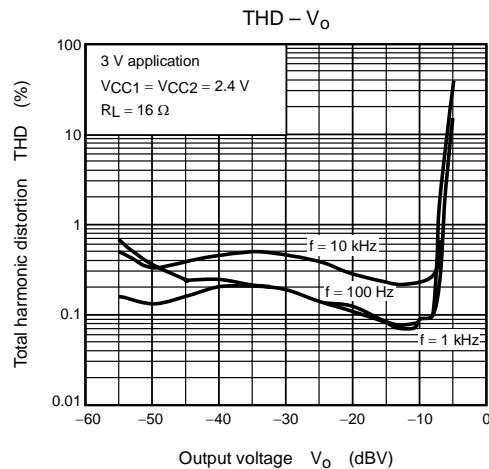
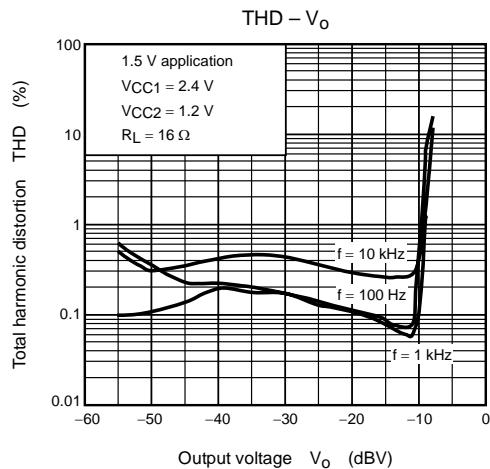
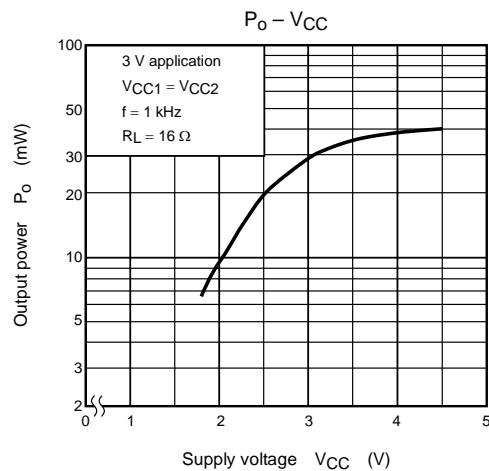
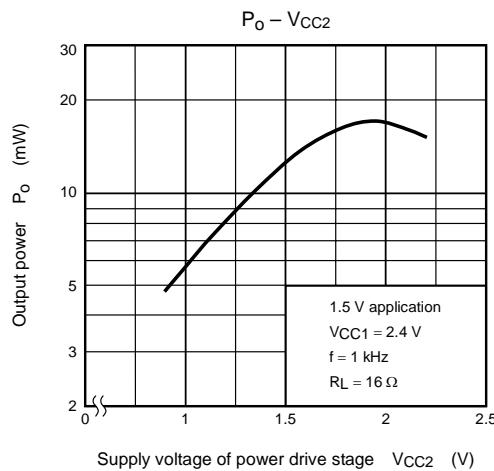
Characteristic	Symbol	Test conditions	Min	Typ.	Max	Unit
Quiescent supply current	I <sub>CCQ1</sub>	IC OFF (V <sub>CC1</sub> ), SW1: b	—	0.1	5	μA
	I <sub>CCQ2</sub>	IC OFF (V <sub>CC2</sub> ), SW1: b	—	0.1	5	
	I <sub>CCQ3</sub>	OCL, Mute ON (V <sub>CC1</sub> ), SW2: a	—	400	600	
	I <sub>CCQ4</sub>	OCL, Mute ON (V <sub>CC2</sub> ), SW2: a	—	650	1400	
	I <sub>CCQ5</sub>	C-Cup, Mute ON (V <sub>CC1</sub> ), SW2: a	—	170	250	
	I <sub>CCQ6</sub>	C-Cup, Mute ON (V <sub>CC2</sub> ), SW2: a	—	85	170	
	I <sub>CCQ7</sub>	OCL, no signal (V <sub>CC1</sub> )	—	0.7	1.1	
	I <sub>CCQ8</sub>	OCL, no signal (V <sub>CC2</sub> )	—	0.7	1.5	
	I <sub>CCQ9</sub>	C-Cup, no signal (V <sub>CC1</sub> )	—	0.4	0.6	
	I <sub>CCQ10</sub>	C-Cup, no signal (V <sub>CC2</sub> )	—	0.3	0.6	
Power supply current during drive	I <sub>CC1</sub>	OCL, 0.5 mW × 2 ch (V <sub>CC1</sub> )	—	0.8	—	mA
	I <sub>CC2</sub>	OCL, 0.5 mW × 2 ch (V <sub>CC2</sub> )	—	10.0	—	
	I <sub>CC3</sub>	C-Cup, 0.5 mW × 2 ch (V <sub>CC1</sub> )	—	0.5	—	
	I <sub>CC4</sub>	C-Cup, 0.5 mW × 2 ch (V <sub>CC2</sub> )	—	5.0	—	
Voltage gain	G <sub>V</sub>	V <sub>o</sub> = -22 dBV	9.5	11.5	13.5	dB
Channel balance	CB	V <sub>o</sub> = -22 dBV	-1.5	0	+1.5	
Output power	P <sub>o</sub>	THD = 10%	5	8	—	mW
Total harmonic distortion	THD	P <sub>o</sub> = 1 mW	—	0.1	1.0	%
Output noise voltage	V <sub>no</sub>	R <sub>g</sub> = 600 Ω, Filter: IHF-A, SW3: b	—	-100	-96	dBV
Cross talk	CT	V <sub>o</sub> = -22 dBV	-25	-35	—	dB
Ripple rejection ratio 1	RR1	Inflow to V <sub>CC1</sub> , SW3: b f <sub>r</sub> = 100 Hz, V <sub>r</sub> = -20 dBV	-65	-85	—	
Ripple rejection ratio 2	RR2	Inflow to V <sub>CC2</sub> , SW3: b f <sub>r</sub> = 100 Hz, V <sub>r</sub> = -20 dBV	-85	-100	—	
Muting attenuation	ATT	V <sub>o</sub> = -12 dBV	-100	-115	—	
Beep sound output voltage	V <sub>BEEP</sub> (OUT)	V <sub>BEEP</sub> (IN) = 2 V <sub>p-p</sub>	-55	-50	-45	dBV
PW SW ON current	I <sub>18</sub>	V <sub>CC1</sub> = 1.8 V, V <sub>CC2</sub> = 0.9 V	5	—	—	μA
PW SW OFF voltage	V <sub>18</sub>	V <sub>CC1</sub> = 1.8 V, V <sub>CC2</sub> = 0.9 V	0	—	0.3	V
Mute SW ON current	I <sub>17</sub>	V <sub>CC1</sub> = 1.8 V, V <sub>CC2</sub> = 0.9 V	5	—	—	μA
Mute SW OFF voltage	V <sub>17</sub>	V <sub>CC1</sub> = 1.8 V, V <sub>CC2</sub> = 0.9 V	0	—	0.3	V

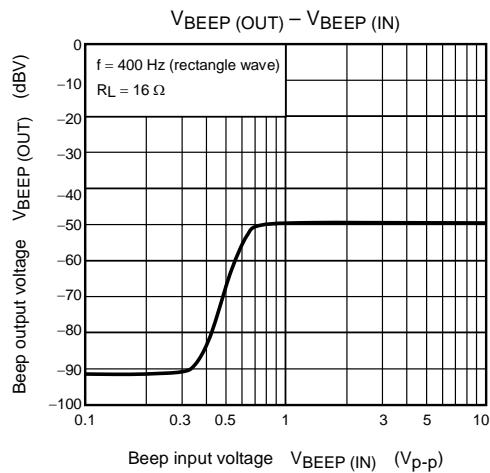
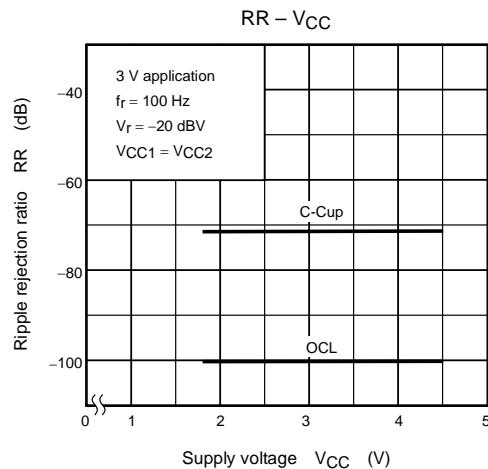
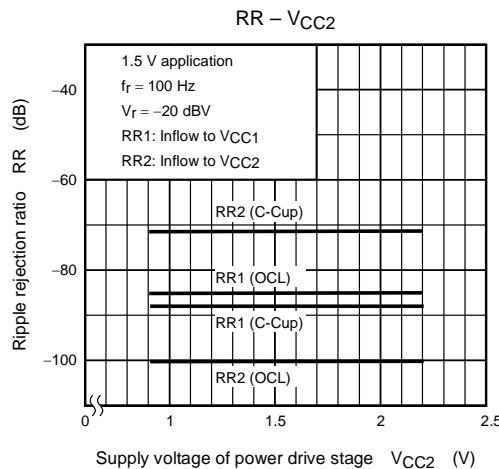
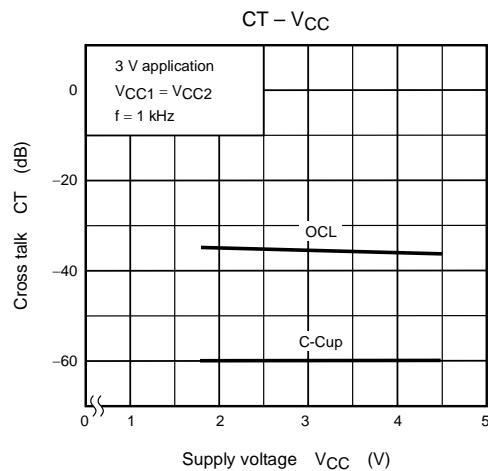
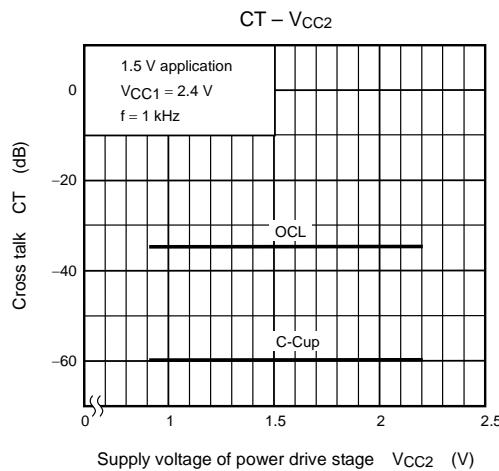
## Test Circuit

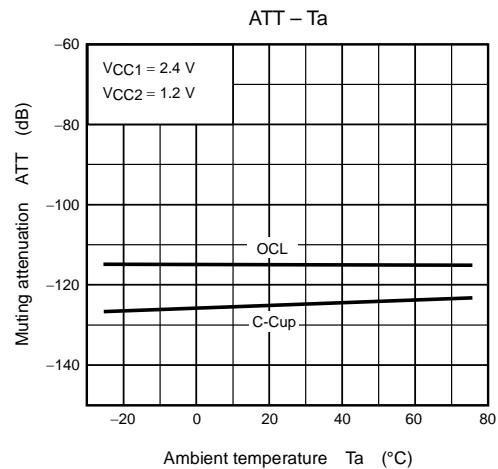
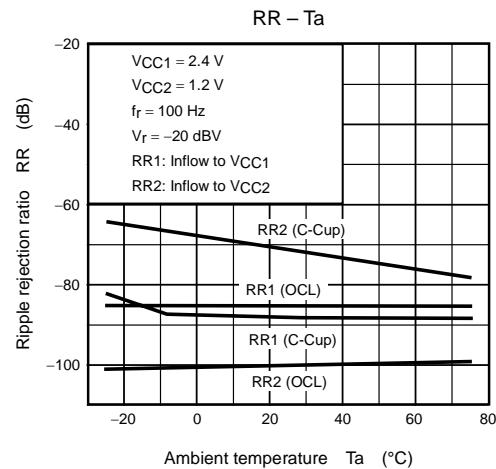
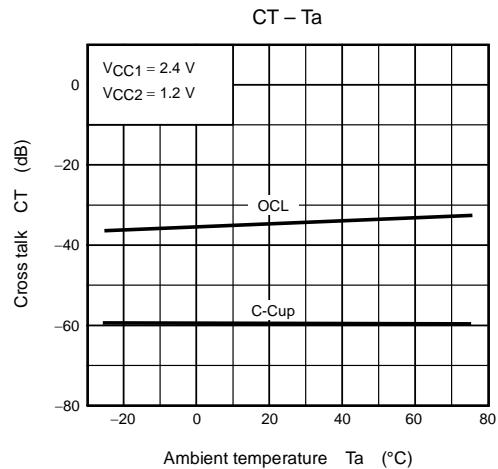
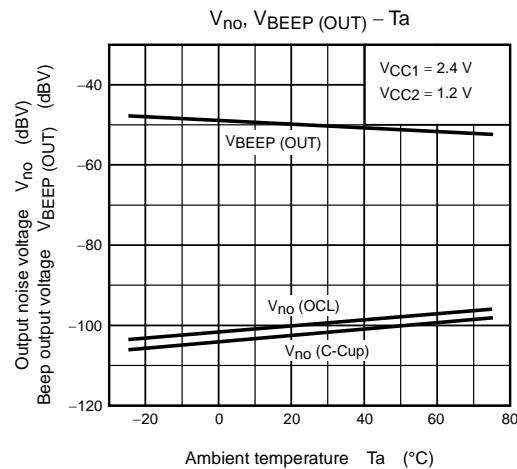
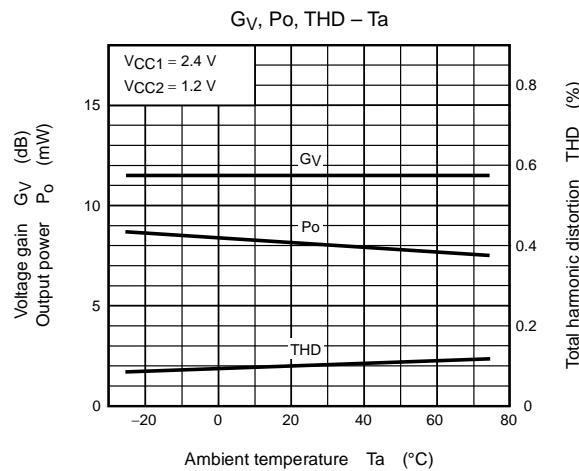
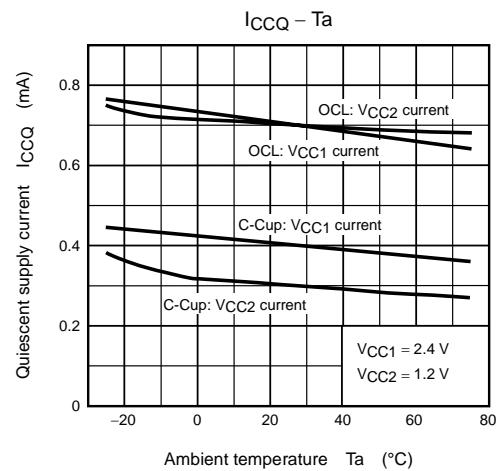


**Characteristic Curves (unless otherwise specified,  $V_{CC1} = 2.4$  V,  $V_{CC2} = 1.2$  V,  $R_g = 600 \Omega$ ,  $R_L = 16 \Omega$ ,  $f = 1$  kHz,  $T_a = 25^\circ\text{C}$ )**

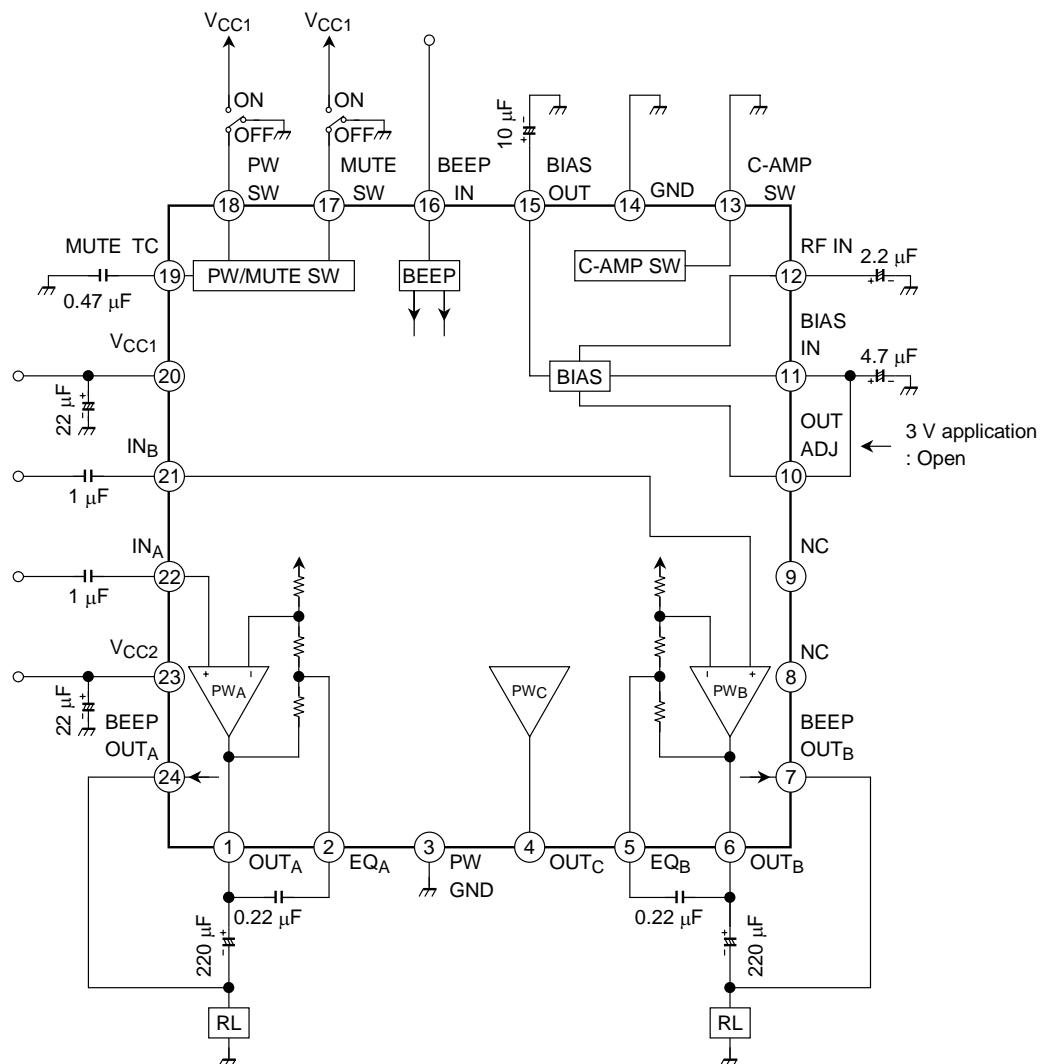




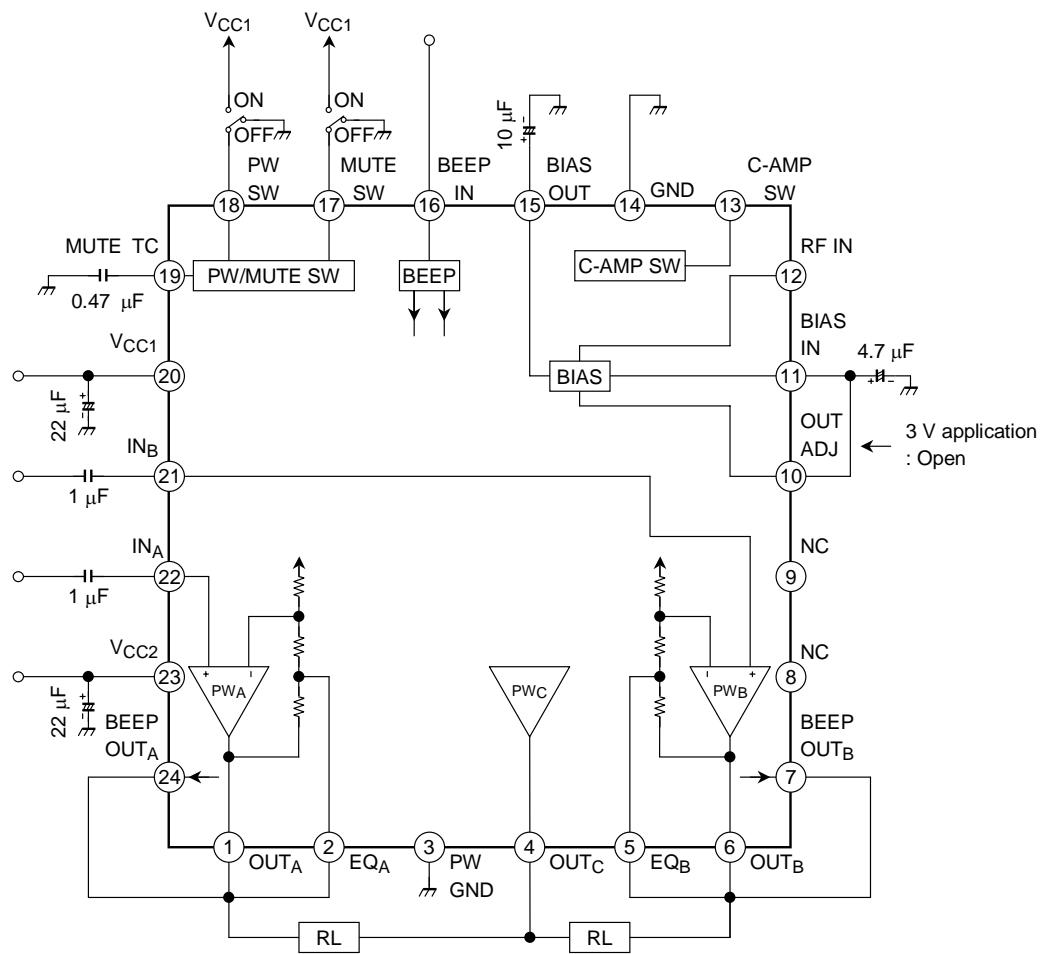




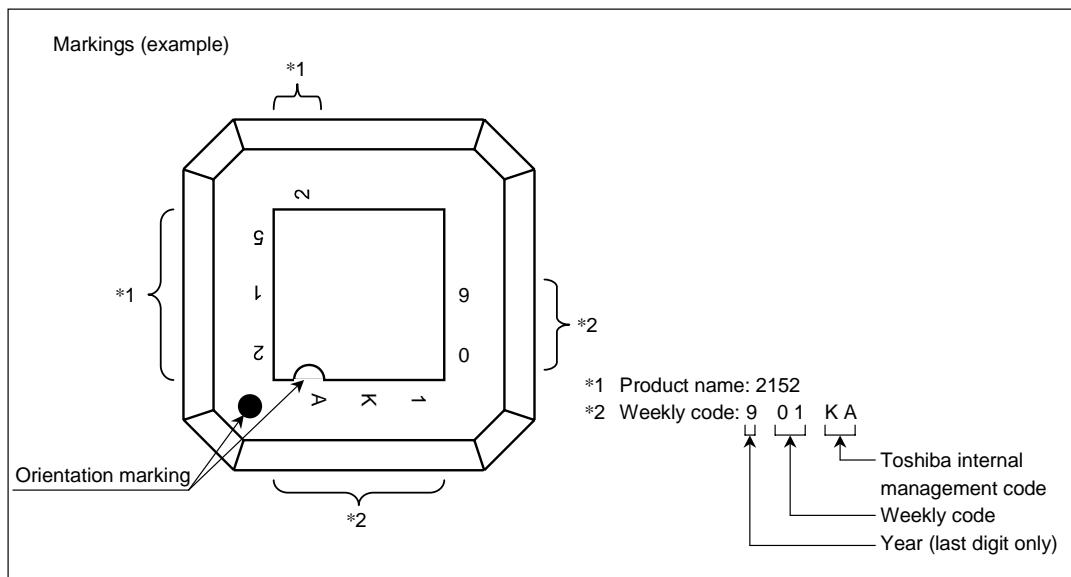
## Application Circuit1 (1.5 V Output Coupling Type)



## Application Circuit2 (1.5 V OCL Type)

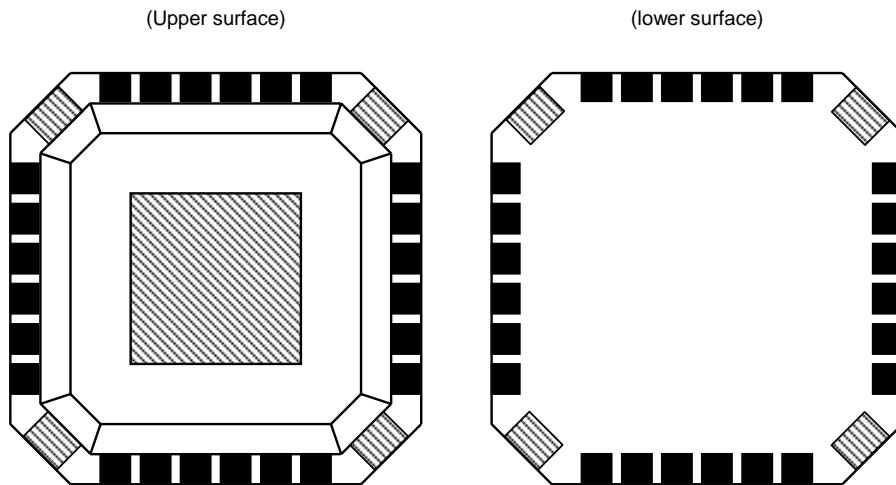


## Markings



## Precautions when using QON

### Package outline



Please take into account the following points regarding the QON package

- (1) Do not attempt to strengthen the device mechanically by performing soldering on the island sections at the four corners of the package (the sections illustrated by diagonal lines) on the diagram of the lower surface.
- (2) This island sections on the package surfaces (the sections illustrated by diagonal lines on the upper and lower surface diagrams) must be electrically insulated.

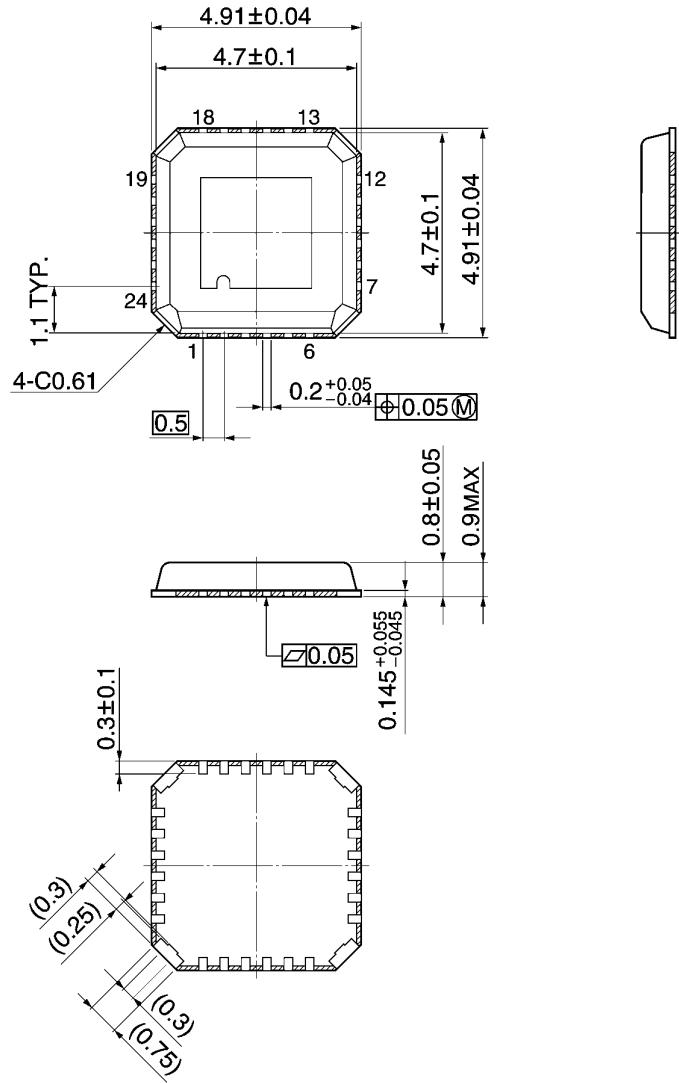
\*1: Ensure that the island sections on the lower surface (as indicated by the diagonal lines on the diagram) do not come into contact with solder from via holes in the board.

- When mounting or soldering, take care to ensure that neither static electricity nor electrical overstress is applied to the IC (by taking measures to prevent antistatic, leaks etc.).
- When incorporating the device into an item of equipment employ a set design which does not result in voltage being applied directly to the island section.

## Package Dimensions

QON24-P-0505-0.50

Unit: mm



Weight: 0.05 g (typ.)

**RESTRICTIONS ON PRODUCT USE**

060116EBA

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- The products described in this document are subject to the foreign exchange and foreign trade laws. 021023\_E

About solderability, following conditions were confirmed

- Solderability
  - (1) Use of Sn-37Pb solder Bath
    - solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux
  - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
    - solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux