Ultralow Noise and Spurious 0.37GHz to 6.39GHz Integer-N Synthesizer with Integrated VCO

FEATURES

- **Low Noise Integer-N PLL with Integrated VCO**
- **–226dBc/Hz Normalized In-Band Phase Noise Floor**
- **–274dBc/Hz Normalized In-Band 1/f Noise**
- **–157dBc/Hz Wideband Output Phase Noise Floor**
- **Excellent Spurious Performance**
- **Output Divider (1 to 6, 50% Duty Cycle)**
- **Output Buffer Muting**
- **Low Noise Reference Buffer**
- Charge Pump Current Adjustable from 250µA to 11.2mA
- Configurable Status Output
- SPI Compatible Serial Port Control
- PLLWizard™ Software Design Tool Support

APPLICATIONS

- Wireless Base Stations (LTE, WiMAX, W-CDMA, PCS)
- Broadband Wireless Access
- Military and Secure Radio
- Test and Measurement

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DESCRIPTION

The LTC®6946 is a high performance, low noise, 6.39GHz phase-locked loop (PLL) with a fully integrated VCO, including a reference divider, phase-frequency detector (PFD) with phase-lock indicator, ultralow noise charge pump, integer feedback divider, and VCO output divider. The charge pump contains selectable high and low voltage clamps useful for VCO monitoring.

The integrated low noise VCO uses no external components. It is internally calibrated to the correct output frequency with no external system support.

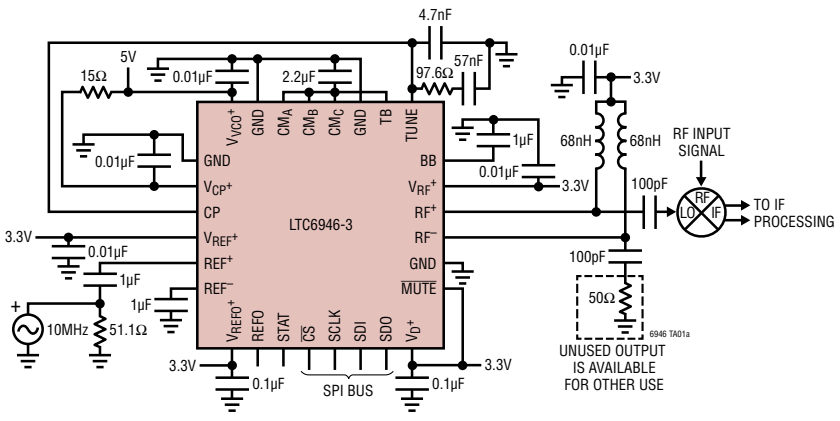
The part features a buffered, programmable VCO output divider with a range of 1 through 6, providing a wide frequency range.

Frequency Coverage Options

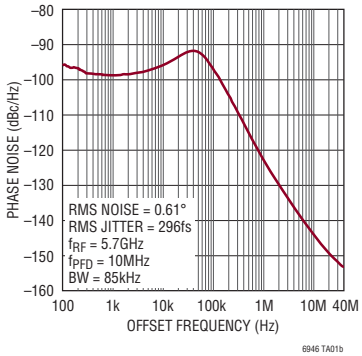
	LTC6946-1	LTC6946-2	LTC6946-3	LTC6946-4
0 DIV=1	2.240 to 3.740	3.080 to 4.910	3.840 to 5.790	4.200 to 6.390
0 DIV=2	1.120 to 1.870	1.540 to 2.455	1.920 to 2.895	2.100 to 3.195
0 DIV=3	0.747 to 1.247	1.027 to 1.637	1.280 to 1.930	1.400 to 2.130
0 DIV=4	0.560 to 0.935	0.770 to 1.228	0.960 to 1.448	1.050 to 1.598
0 DIV=5	0.448 to 0.748	0.616 to 0.982	0.768 to 1.158	0.840 to 1.278
0 DIV=6	0.373 to 0.623	0.513 to 0.818	0.640 to 0.965	0.700 to 1.065

TYPICAL APPLICATION

5.7GHz Wideband Receiver



LTC6946-3 PLL Phase Noise



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V^+ (V_{REF}^+, V_{REFO}^+, V_{RF}^+, V_D^+) to GND 3.6V

V_{CP}^+, V_{VCO}^+ to GND 5.5V

Voltage on CP Pin ..... GND – 0.3V to V_{CP}^+ + 0.3V

Voltage on All Other Pins ..... GND – 0.3V to V^+ + 0.3V

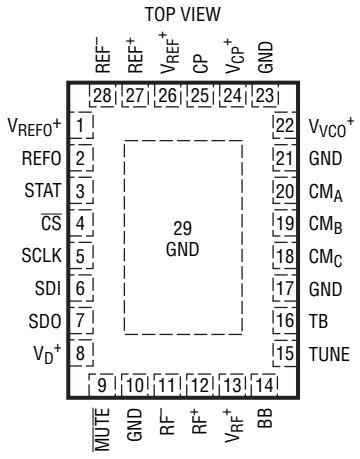
Operating Junction Temperature Range, T_J (Note 2)

LTC6946I ..... –40°C to 105°C

Junction Temperature, T_{JMAX} ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 3°C/W, θ_{JCtop} = 26°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6946IUFD-1#PBF	LTC6946IUFD-1#TRPBF	69461	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C
LTC6946IUFD-2#PBF	LTC6946IUFD-2#TRPBF	69462	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C
LTC6946IUFD-3#PBF	LTC6946IUFD-3#TRPBF	69463	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C
LTC6946IUFD-4#PBF	LTC6946IUFD-4#TRPBF	69464	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AVAILABLE OPTIONS

VCO FREQUENCY RANGE (GHz)	PACKAGE STYLE	OUTPUT FREQUENCY RANGE vs OUTPUT DIVIDER SETTING (GHz)					
	QFN-28 (UFD28)	0 DIV = 6	0 DIV = 5	0 DIV = 4	0 DIV = 3	0 DIV = 2	0 DIV = 1
2.240 to 3.740	LTC6946IUFD-1	0.373 to 0.623	0.448 to 0.748	0.560 to 0.935	0.747 to 1.247	1.120 to 1.870	2.240 to 3.740
3.080 to 4.910	LTC6946IUFD-2	0.513 to 0.818	0.616 to 0.982	0.770 to 1.228	1.027 to 1.637	1.540 to 2.455	3.080 to 4.910
3.840 to 5.790	LTC6946IUFD-3	0.640 to 0.965	0.768 to 1.158	0.960 to 1.448	1.280 to 1.930	1.920 to 2.895	3.840 to 5.790
4.200 to 6.390	LTC6946IUFD-4	0.700 to 1.065	0.840 to 1.278	1.050 to 1.598	1.400 to 2.130	2.100 to 3.195	4.200 to 6.390
		Overlapping Frequency Bands					

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF⁺, REF⁻)							
f_{REF}	Input Frequency		●	10		250	MHz
V_{REF}	Input Signal Level	Single Ended, 1µF AC-Coupling Capacitors	●	0.5	2	2.7	V_{P-P}
	Input Slew Rate		●	20			V/µs
	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.65	1.85	2.25	V
	Input Resistance	Differential	●	6.2	8.4	11.6	kΩ
	Input Capacitance	Differential			3		pF
Reference Output (REFO)							
f_{REFO}	Output Frequency		●	10		250	MHz
P_{REFO}	Output Power	f_{REFO} = 10MHz, R_{LOAD} = 50Ω	●	–0.2		3.2	dBm
	Output Impedance, Disabled				800		Ω
VCO							
f_{VCO}	Frequency Range	LTC6946-1 (Note 3) LTC6946-2 (Note 3) LTC6946-3 (Note 3) LTC6946-4 (Note 3)	● ● ● ●	2.24 3.08 3.84 4.20		3.74 4.91 5.79 6.39	GHz GHz GHz GHz
K_{VCO}	Tuning Sensitivity	LTC6946-1 (Notes 3, 4) LTC6946-2 (Notes 3, 4) LTC6946-3 (Notes 3, 4) LTC6946-4 (Notes 3, 4)			4.7 to 7.2 4.7 to 7.0 4.0 to 6.0 4.5 to 6.5		%Hz/V %Hz/V %Hz/V %Hz/V
RF Output (RF⁺, RF⁻)							
f_{RF}	Output Frequency		●	0.373		6.39	GHz
O	Output Divider Range	All Integers Included	●	1		6	
	Output Duty Cycle				50		%
	Output Resistance	Single Ended, Each Output to V_{RF}^+	●	111	136	159	Ω
	Output Common Mode Voltage		●	2.4		V_{RF}^+	V
$P_{RF(SE)}$	Output Power, Single Ended, f_{RF} = 900MHz	RFO[1:0] = 0, R_Z = 50Ω, LC Match RFO[1:0] = 1, R_Z = 50Ω, LC Match RFO[1:0] = 2, R_Z = 50Ω, LC Match RFO[1:0] = 3, R_Z = 50Ω, LC Match	● ● ● ●	–9.7 –6.8 –3.9 –1.2		–6.0 –3.6 –0.4 2.3	dBm dBm dBm dBm
	Output Power, Muted	R_Z = 50Ω, Single Ended, f_{RF} = 900MHz, O = 2 to 6	●			–60	dBm
	Mute Enable Time		●			110	ns
	Mute Disable Time		●			170	ns
Phase/Frequency Detector							
f_{PFD}	Input Frequency		●			100	MHz
Lock Indicator, Available on the STAT Pin and via the SPI-Accessible Status Register							
t_{LWW}	Lock Window Width	LKWIN[1:0] = 0 LKWIN[1:0] = 1 LKWIN[1:0] = 2 LKWIN[1:0] = 3			3.0 10.0 30.0 90.0		ns ns ns ns
t_{LWHYS}	Lock Window Hysteresis	Increase in t_{LWW} Moving from Locked State to Unlocked State			22		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Pump							
I_{CP}	Output Current Range	12 Settings (See Table 5)		0.25		11.2	mA
	Output Current Source/Sink Accuracy	All Settings $V_{CP} = V_{CP}^+/2$				±6	%
	Output Current Source/Sink Matching	I_{CP} = 250µA to 1.4mA, $V_{CP} = V_{CP}^+/2$ I_{CP} = 2.0mA to 11.2mA, $V_{CP} = V_{CP}^+/2$				±3.5 ±2	% %
	Output Current vs Output Voltage Sensitivity	(Note 5)	●		0.1	1.0	%/V
	Output Current vs Temperature	$V_{CP} = V_{CP}^+/2$	●		170		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 700µA, CPCLO = CPCHI = 0 (Note 5) I_{CP} = 11.2mA, CPCLO = CPCHI = 0 (Note 5)			0.5 5		nA nA
$V_{CLMP(LO)}$	Low Clamp Voltage	CPCLO = 1			0.84		V
$V_{CLMP(HI)}$	High Clamp Voltage	CPCHI = 1, Referred to V_{CP}^+			–0.96		V
V_{MID}	Mid-Supply Output Bias Ratio	Referred to (V_{CP}^+ – GND)			0.48		V/V
Reference (R) Divider							
R	Divide Range	All Integers Included	●	1		1023	counts
VCO (N) Divider							
N	Divide Range	All Integers Included	●	32		65535	counts
Digital Pin Specifications							
V_{IH}	High Level Input Voltage	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●	1.55			V
V_{IL}	Low Level Input Voltage	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK			250		mV
	Input Current	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●			±1	µA
I_{OH}	High Level Output Current	SDO and STAT, $V_{OH} = V_D^+$ – 400mV	●		–2.3	– 1.4	mA
I_{OL}	Low Level Output Current	SDO and STAT, V_{OL} = 400mV	●	1.8	2.6		mA
	SDO Hi-Z Current		●			±1	µA
Digital Timing Specifications (See Figures 7 and 8)							
t_{CKH}	SCLK High Time		●	25			ns
t_{CKL}	SCLK Low Time		●	25			ns
t_{CSS}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Time		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SCLK to SDO Time	To V_{IH}/V_{IL}/Hi-Z with 30pF Load	●			16	ns
Power Supply Voltages							
	V_{REF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{REFO}^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{RF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{VCO}^+ Supply Range		●	4.75	5.0	5.25	V
	V_{CP}^+ Supply Range		●	4.0		5.25	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Currents							
I_{DD}	V_D^+ Supply Current	Digital Inputs at Supply Levels	●			500	µA
$I_{CC(5V)}$	Sum V_{CP}^+, V_{VCO}^+ Supply Currents	I_{CP} = 11.2mA	●		50	63	mA
		I_{CP} = 1.0mA	●		28	39	mA
		PDALL = 1	●		405	660	µA
$I_{CC(REFO)}$	V_{REFO}^+ Supply Currents	REFO Enabled, $R_Z = \infty$	●		7.8	9.0	mA
$I_{CC\ (3.3V)}$	Sum V_{REF}^+, V_{RF}^+ Supply Currents	RF Muted, OD[2:0] = 1	●		65	76	mA
		RF Enabled, RFO[1:0] =0, OD[2:0] = 1	●		76	86	mA
		RF Enabled, RFO[1:0] = 3, OD[2:0] = 1	●		85	97	mA
		RF Enabled, RFO[1:0] =3, OD[2:0] = 2	●		103	117	mA
		RF Enabled, RFO[1:0] =3, OD[2:0] = 3	●		108	123	mA
		RF Enabled, RFO[1:0] =3, OD[2:0] = 4 to 6	●		113	128	mA
		PDALL = 1	●		195	340	µA
Phase Noise and Spurious							
L_M	Phase Noise (LTC6946-1, f_{VCO} = 3.0GHz, f_{RF} = 3.0GHz, OD[2 :0] = 1 (Note 6))	10kHz Offset			–80		dBc/Hz
		1MHz Offset			–130		dBc/Hz
		40MHz Offset			–157		dBc/Hz
	Phase Noise (LTC6946-2, f_{VCO} = 4.0GHz, f_{RF} = 4.0GHz, OD[2 :0] = 1 (Note 6))	10kHz Offset			–77		dBc/Hz
		1MHz Offset			–127		dBc/Hz
		40MHz Offset			–156		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 5.0GHz, OD[2 :0] = 1 (Note 6))	10kHz Offset			–75		dBc/Hz
		1MHz Offset			–126		dBc/Hz
		40MHz Offset			–155		dBc/Hz
	VCO Phase Noise (LTC6946-4, f_{VCO} = 6.0GHz, f_{RF} = 6.0GHz, OD[2 :0] = 1 (Note 6))	10kHz Offset			–73		dBc/Hz
		1MHz Offset			–132		dBc/Hz
		40MHz Offset			–154		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 2.50GHz, OD[2 :0] = 2 (Note 6))	10kHz Offset			–81		dBc/Hz
		1MHz Offset			–132		dBc/Hz
		40MHz Offset			–155		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 1.667GHz, OD[2 :0] = 3 (Note 6))	10kHz Offset			–84		dBc/Hz
		1MHz Offset			–135		dBc/Hz
		40MHz Offset			–156		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 1.25GHz, OD[2 :0] = 4 (Note 6))	10kHz Offset			–87		dBc/Hz
		1MHz Offset			–138		dBc/Hz
		40MHz Offset			–156		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 1.00GHz, OD[2 :0] = 5 (Note 6))	10kHz Offset			–89		dBc/Hz
		1MHz Offset			–140		dBc/Hz
		40MHz Offset			–157		dBc/Hz
	Phase Noise (LTC6946-3, f_{VCO} = 5.0GHz, f_{RF} = 0.833GHz, OD[2 :0] = 6 (Note 6))	10kHz Offset			–90		dBc/Hz
		1MHz Offset			–141		dBc/Hz
		40MHz Offset			–158		dBc/Hz
$L_{M(NORM)}$	Normalized In-Band Phase Noise Floor	I_{CP} = 11.2mA (Notes 7, 8, 9)			–226		dBc/Hz
$L_{M(NORM\ –\ 1/f)}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 7, 10)			–274		dBc/Hz
$L_{M(IB)}$	In-Band Phase Noise Floor	(Notes 7, 8, 9, 11)			–99		dBc/Hz
	Integrated Phase Noise from 100Hz to 40MHz	(Notes 8, 12)			0.17		°RMS
	Spurious	$f_{OFFSET} = f_{PFD}$, PLL Locked (Notes 8, 12, 13)			–103		dBc

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6946I is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the exposed pad (Pin 29) be soldered directly to the ground plane with an array of thermal vias as described in the Applications Information section.

Note 3: Valid for 1.60V ≤ TUNE ≤ 2.85V with part calibrated after a power cycle or software power-on-reset (POR).

Note 4: Based on characterization.

Note 5: For 0.9V ≤ V_{CP} ≤ (V_{CP}^+ – 0.9V).

Note 6: Measured outside the loop bandwidth, using a narrowband loop, RFO[1:0] = 3.

Note 7: Measured inside the loop bandwidth with the loop locked.

Note 8: Reference frequency supplied by Wenzel 501-04608A, f_{REF} = 10MHz, P_{REF} = 13dBm.

Note 9: Output phase noise floor is calculated from normalized phase noise floor by $L_{M(OUT)} = –226 + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{RF}/f_{PFD})$.

Note 10: Output 1/f phase noise is calculated from normalized 1/f phase noise by $L_{M(OUT-1/f)} = –274 + 20\log_{10}(f_{RF}) – 10\log_{10}(f_{OFFSET})$.

Note 11: I_{CP} = 11.2mA, f_{PFD} = 250kHz, FILT[1:0] = 3, Loop BW = 25kHz; f_{RF} = 900MHz, f_{VCO} = 2.7GHz (LTC6946-1), f_{VCO} = 3.6GHz (LTC6946-2), f_{VCO} = 4.5GHz (LTC6946-3, LTC6946-4).

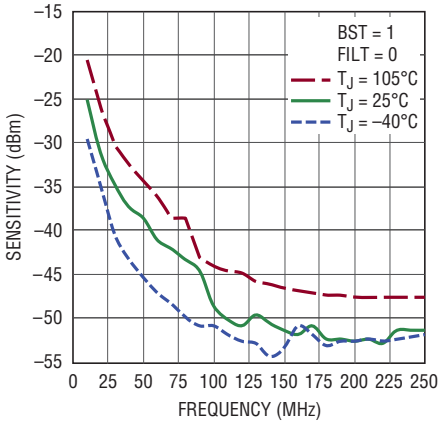
Note 12: I_{CP} = 11.2mA, f_{PFD} = 1MHz, FILT[1:0] = 3, Loop BW = 40kHz; f_{RF} = 900MHz, f_{VCO} = 2.7GHz (LTC6946-1), f_{VCO} = 3.6GHz (LTC6946-2), f_{VCO} = 4.5GHz (LTC6946-3, LTC6946-4).

Note 13: Measured using DC1705.

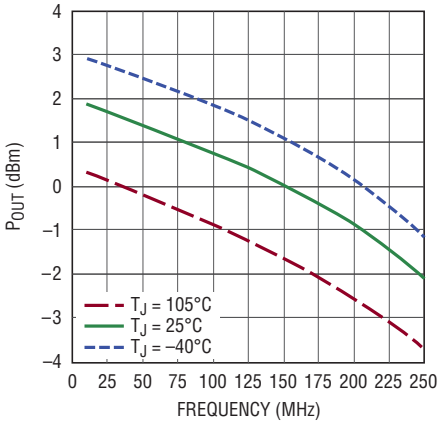
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, RFO[1:0] = 3, unless otherwise noted.

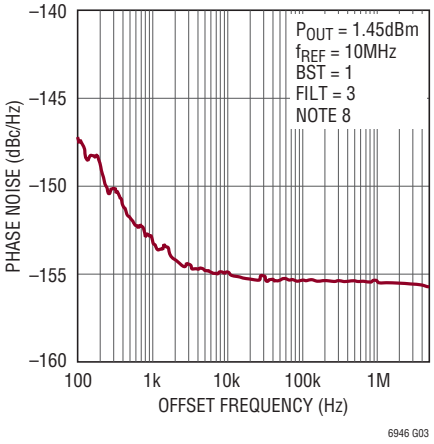
REF Input Sensitivity vs Frequency



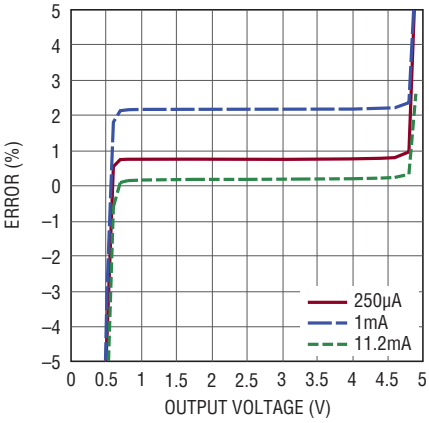
REFO Output Power vs Frequency



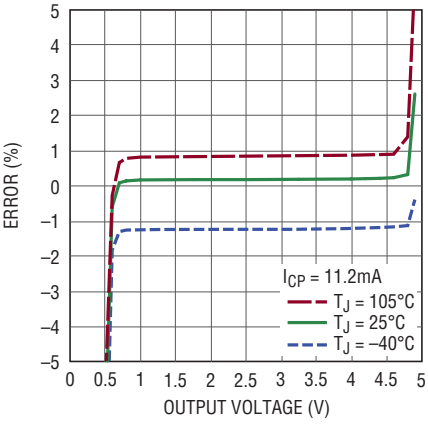
REFO Phase Noise



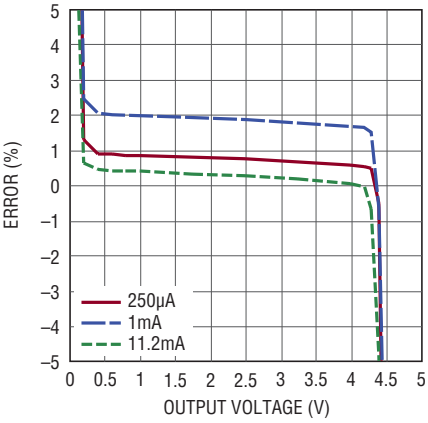
Charge Pump Sink Current Error vs Voltage, Output Current



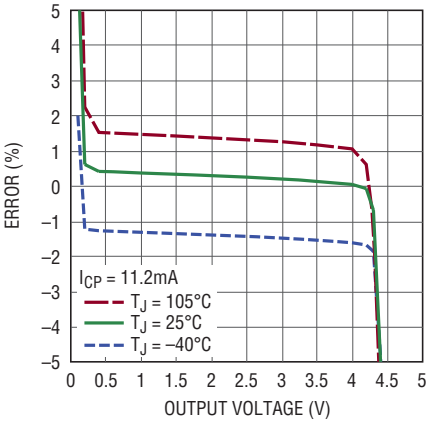
Charge Pump Sink Current Error vs Voltage, Temperature



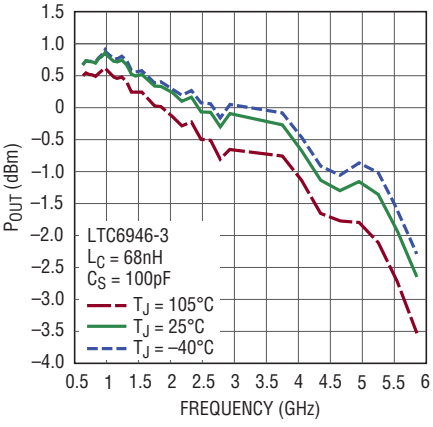
Charge Pump Source Current Error vs Voltage, Output Current



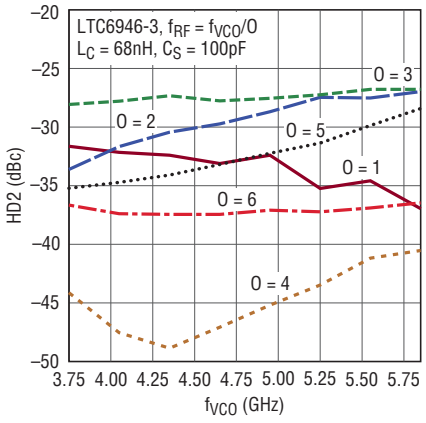
Charge Pump Source Current Error vs Voltage, Temperature



RF Output Power vs Frequency (Single Ended on RF⁻)



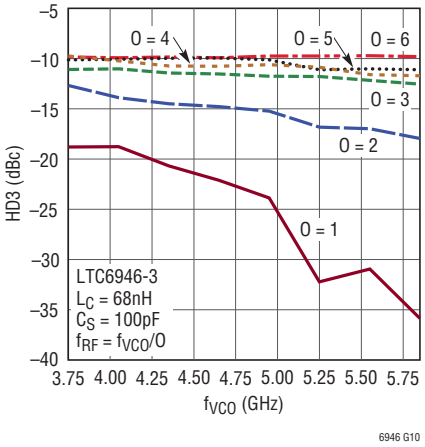
RF Output HD2 vs Output Divide (Single Ended on RF⁻)



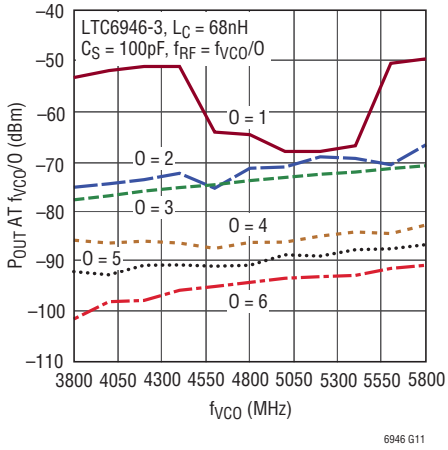
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, RFO[1:0] = 3, unless otherwise noted.

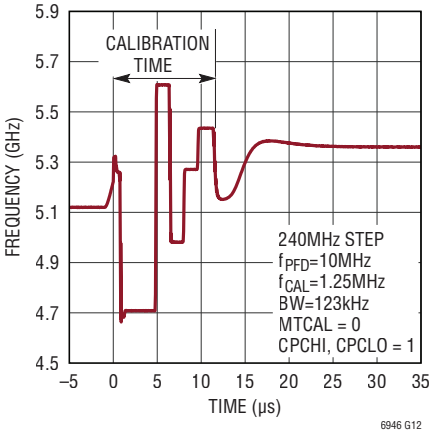
RF Output HD3 vs Output Divide (Single Ended on RF⁻)



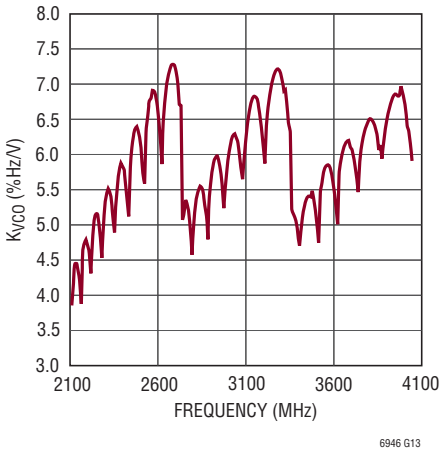
MUTE Output Power vs f_{VCO} and Output Divide (Single Ended on RF⁻)



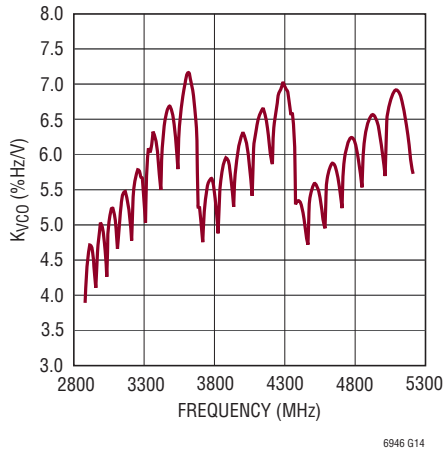
LTC6946-4 Frequency Step Transient



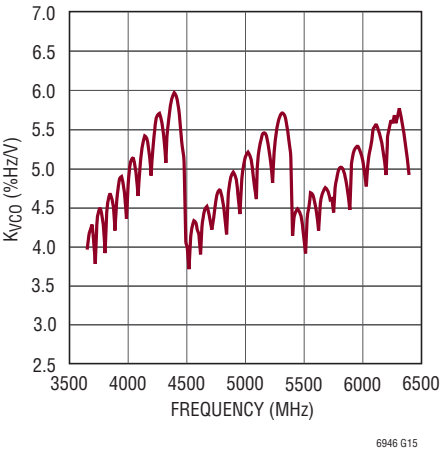
LTC6946-1 VCO Tuning Sensitivity



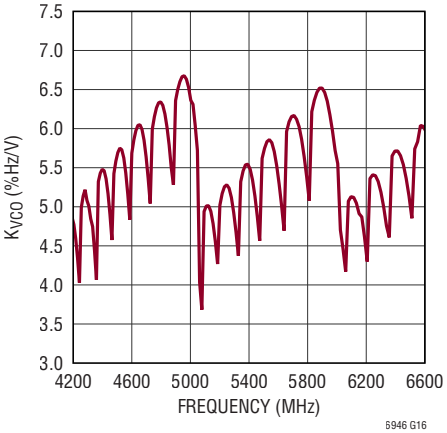
LTC6946-2 VCO Tuning Sensitivity



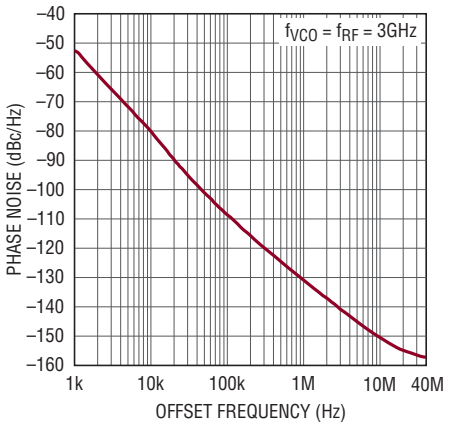
LTC6946-3 VCO Tuning Sensitivity



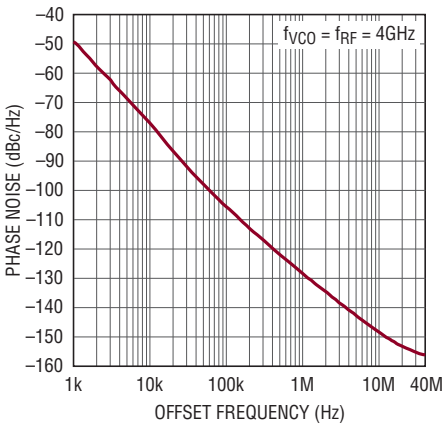
LTC6946-4 VCO Tuning Sensitivity



LTC6946-1 VCO Phase Noise



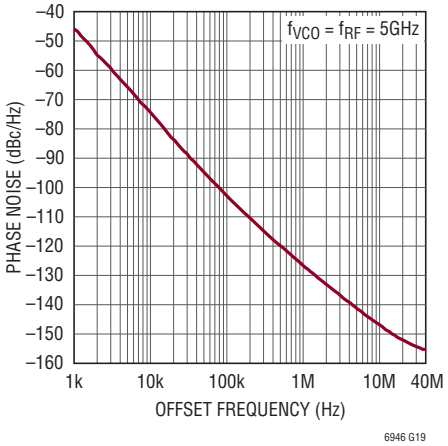
LTC6946-2 VCO Phase Noise



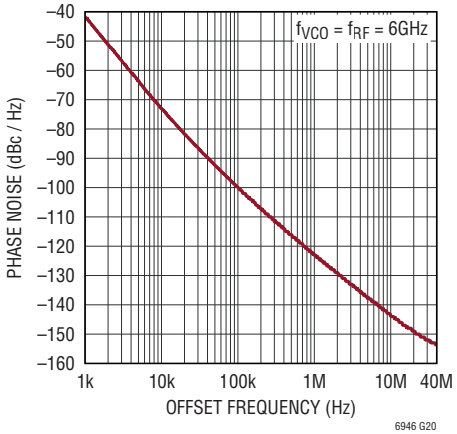
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, RFO[1:0] = 3, unless otherwise noted.

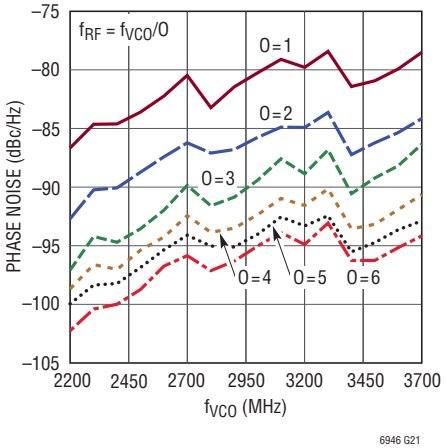
LTC6946-3 VCO Phase Noise



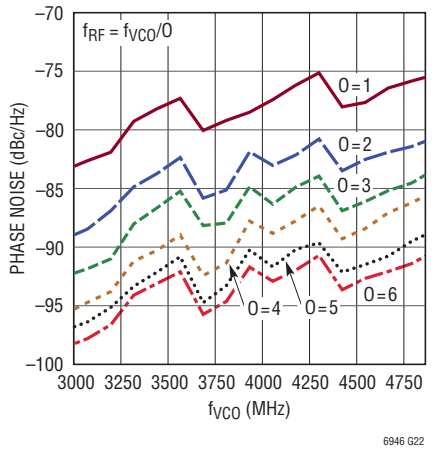
LTC6946-4 VCO Phase Noise



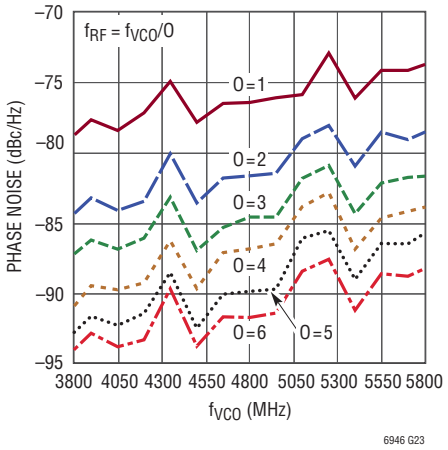
LTC6946-1 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 10kHz)



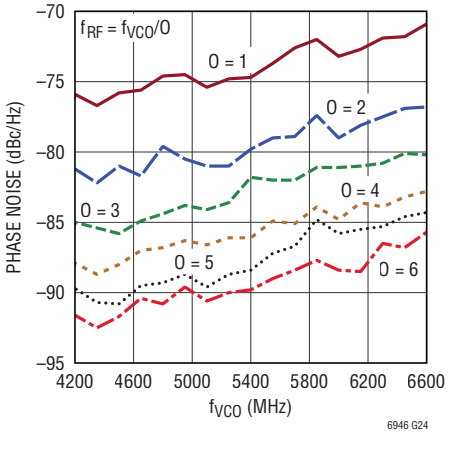
LTC6946-2 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 10kHz)



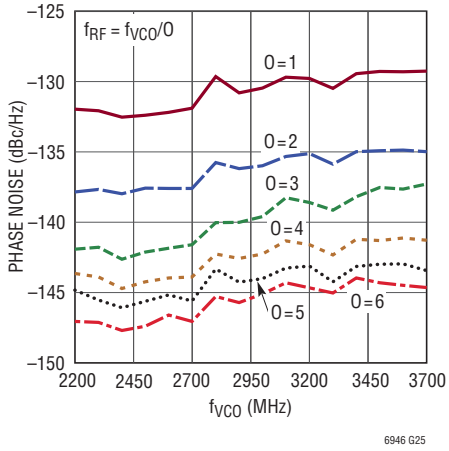
LTC6946-3 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 10kHz)



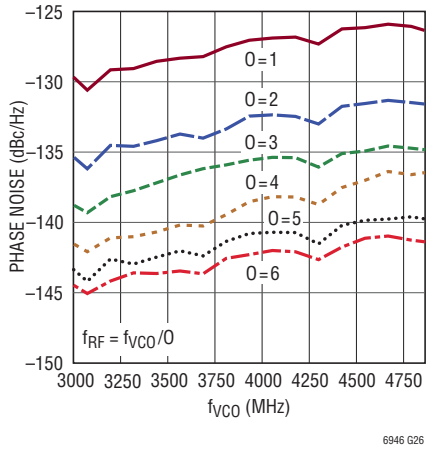
LTC6946-4 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 10kHz)



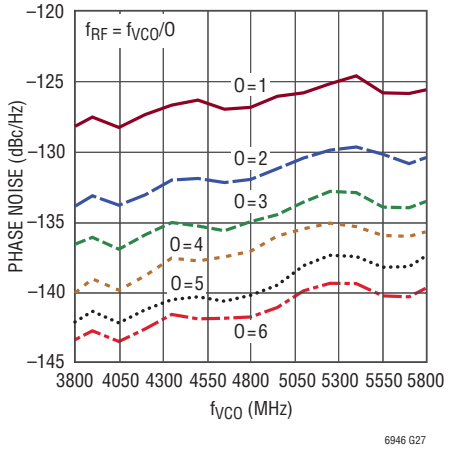
LTC6946-1 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 1MHz)



LTC6946-2 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 1MHz)



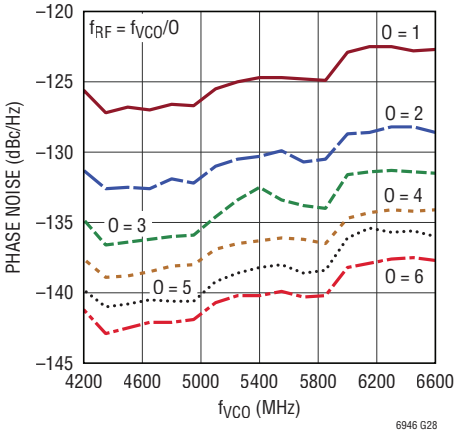
LTC6946-3 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 1MHz)



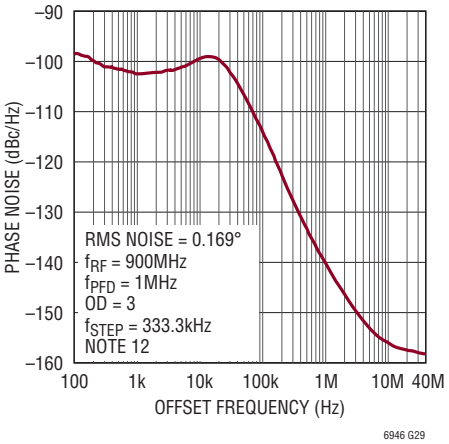
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $V_{REF}^+ = V_{REFO}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, RFO[1:0] = 3, unless otherwise noted.

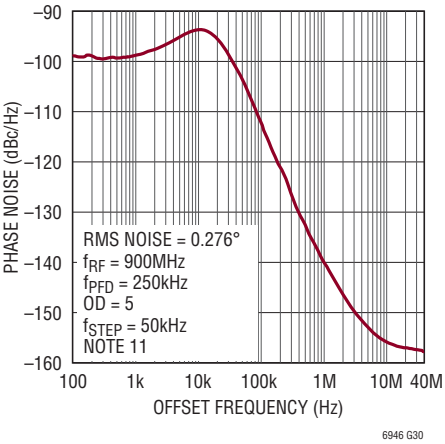
LTC6946-4 VCO Phase Noise vs f_{VCO}, Output Divide (f_{OFFSET} = 1MHz)



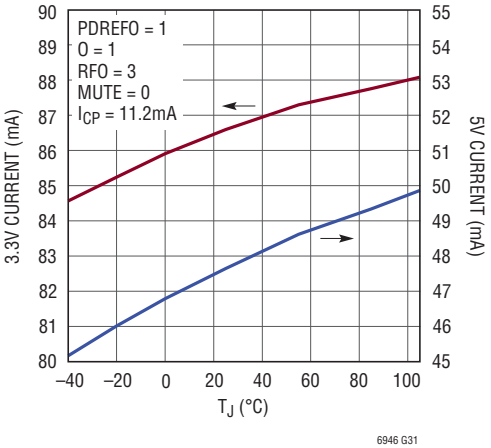
Closed-Loop Phase Noise, Loop Bandwidth = 40kHz, LTC6946-1



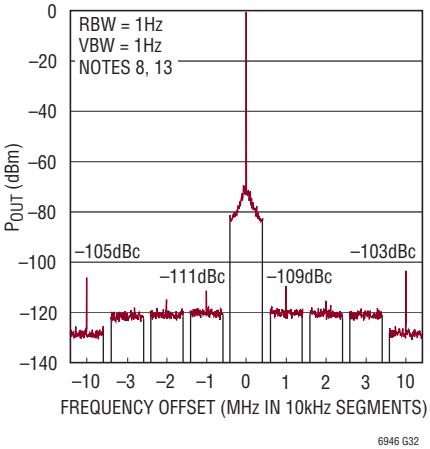
Closed-Loop Phase Noise, Loop Bandwidth = 25kHz, LTC6946-3



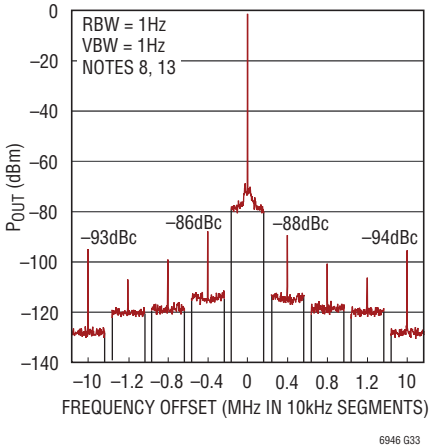
LTC6946-2 Supply Current vs Temperature



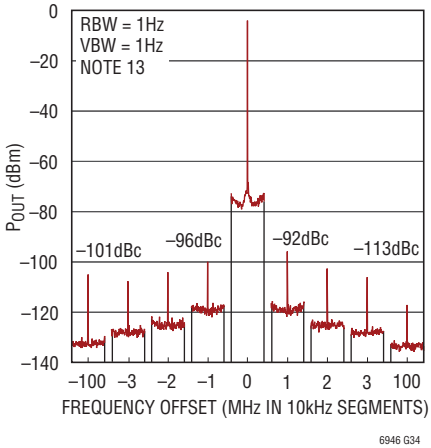
LTC6946-3 Spurious Response f_{RF} = 900MHz, f_{REF} = 10MHz, f_{PFD} = 1MHz, Loop BW = 40kHz



LTC6946-3 Spurious Response f_{RF} = 2200MHz, f_{REF} = 10MHz, f_{PFD} = 0.4MHz, Loop BW = 28kHz



LTC6946-3 Spurious Response f_{RF} = 5700MHz, f_{REF} = 100MHz, f_{PFD} = 1MHz, Loop BW = 33kHz



PIN FUNCTIONS

V_{REFO}^+ (Pin 1): 3.15V to 3.45V Positive Supply Pin for REFO Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

REFO (Pin 2): Reference Frequency Output. This produces a low noise square wave, buffered from the REF± differential inputs. The output is self-biased and must be AC-coupled with a 22nF capacitor.

STAT (Pin 3): Status Output. This signal is a configurable logical OR combination of the UNLOCK, LOCK, ALCHI, ALCLO, THI and TLO status bits, programmable via the STATUS register. See the Operation section for more details.

$\overline{CS}$ (Pin 4): Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high. See the Operation section for more details.

SCLK (Pin 5): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Operation section for more details.

SDI (Pin 6): Serial Port Data Input. The serial port uses this CMOS input for data. See the Operation section for more details.

SDO (Pin 7): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a read communication burst. Optionally attach a resistor of >200k to GND to prevent a floating output. See the Operation section for more details.

V_D^+ (Pin 8): 3.15V to 3.45V Positive Supply Pin for Serial Port Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

$\overline{MUTE}$ (Pin 9): RF Mute. The CMOS active-low input mutes the RF± differential outputs while maintaining internal bias levels for quick response to de-assertion.

GND (Pins 10, 17, 21): Negative Power Supply (Ground). These pins should be tied directly to the ground plane with multiple vias for each pin.

RF^-, RF^+ (Pins 11, 12): RF Output Signals. The VCO output divider is buffered and presented differentially on these pins. The outputs are open collector, with 136Ω (typical) pull-up resistors tied to V_{RF}^+ to aid impedance matching. If used single ended, the unused output should be terminated to 50Ω. See the Applications Information section for more details on impedance matching.

V_{RF}^+ (Pin 13): 3.15V to 3.45V Positive Supply Pin for RF Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

BB (Pin 14): RF Reference Bypass. This output must be bypassed with a 1.0µF ceramic capacitor to GND. Do not couple this pin to any other signal.

TUNE (Pin 15): VCO Tuning Input. This frequency control pin is normally connected to the external loop filter. See the Applications Information section for more details.

TB (Pin 16): VCO Bypass. This output must be bypassed with a 2.2µF ceramic capacitor to GND, and is normally connected to CM_A, CM_B and CM_C with a short trace. Do not couple this pin to any other signal.

CM_C, CM_B, CM_A (Pins 18, 19, 20): VCO Bias Inputs. These inputs are normally connected to TB with a short trace and bypassed with a 2.2µF ceramic capacitor to GND. Do not couple these pins to any other signal. **For best phase noise performance, do not place a trace between these pads underneath the package.**

V_{VCO}^+ (Pin 22): 4.75V to 5.25V Positive Supply Pin for VCO Circuitry. This pin should be bypassed directly to the ground plane using both 0.01µF and 1µF ceramic capacitors as close to the pin as possible.

PIN FUNCTIONS

GND (23): Negative Power Supply (Ground). This pin is attached directly to the die attach paddle (DAP) and should be tied directly to the ground plane.

V_{CP}^+ (Pin 24): 4.0V to 5.25V Positive Supply Pin for Charge Pump Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

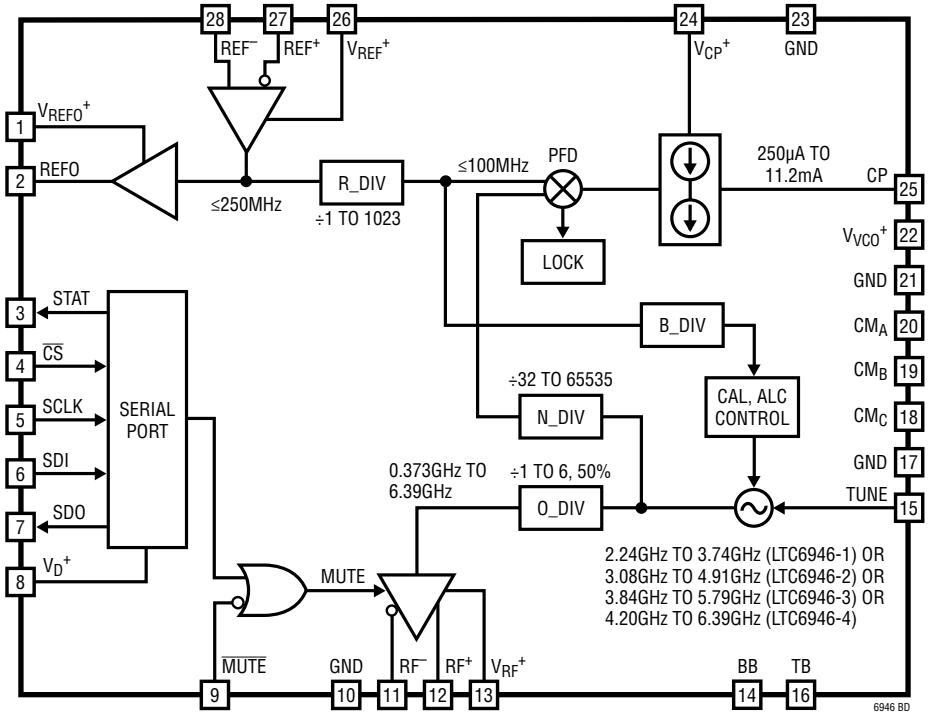
CP (Pin 25): Charge Pump Output. This bi-directional current output is normally connected to the external loop filter. See the Applications Information section for more details.

V_{REF}^+ (Pin 26): 3.15V to 3.45V Positive Supply Pin for Reference Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

REF^+, REF^- (Pins 27, 28): Reference Input Signals. This differential input is buffered with a low noise amplifier, which feeds the reference divider and reference buffer. They are self-biased and must be AC-coupled with 1µF capacitors. If used single ended, bypass REF^- to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, bypass REF^- to GND with a 47pF capacitor.

GND (Exposed Pad Pin 29): Negative Power Supply (Ground). The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

BLOCK DIAGRAM



OPERATION

The LTC6946 is a high performance PLL complete with a low noise VCO available in three different frequency range options. The output frequency range may be further extended by utilizing the output divider (see Available Options table, for more details). The device is able to achieve superior integrated phase noise by the combination of its extremely low in-band phase noise performance and excellent VCO noise characteristics.

REFERENCE INPUT BUFFER

The PLL's reference frequency is applied differentially on pins REF^+ and REF^-. These high impedance inputs are self-biased and must be AC-coupled with 1µF capacitors (see Figure 1 for a simplified schematic). Alternatively, the inputs may be used single ended by applying the reference frequency at REF^+ and bypassing REF^- to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, then use a 47pF capacitor for the GND bypass.

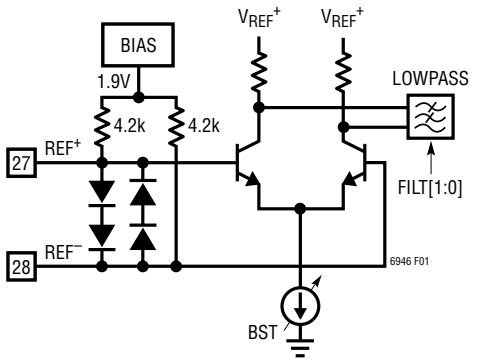


Figure 1. Simplified REF Interface Schematic

A high quality signal must be applied to the $REF^{\pm}$ inputs as they provide the frequency reference to the entire PLL. To achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

Additional options are available through serial port register h08 to further refine the application. Bits FILT[1:0] control the reference input buffer's lowpass filter, and should be set based upon f_{REF} to limit the reference's wideband noise. The FILT[1:0] bits must be set correctly to reach the $L_{M(NORM)}$ normalized in-band phase noise floor. See Table 1 for recommended settings.

The BST bit should be set based upon the input signal level to prevent the reference input buffer from saturating. See Table 2 for recommended settings and the Applications Information section for programming examples.

Table 1. FILT[1:0] Programming

FILT[1:0]	f_{REF}
3	<20MHz
2	NA
1	20MHz to 50MHz
0	>50MHz

Table 2. BST Programming

BST	V_{REF}
1	$<2.0V_{P-P}$
0	$\geq 2.0V_{P-P}$

REFERENCE OUTPUT BUFFER

The reference output buffer produces a low noise square wave with a noise floor of –155dBc/Hz (typical) at 10MHz. Its output is low impedance, and produces 0dBm typical output power into a 50Ω load at 10MHz. Larger output swings will result if driving larger impedances. The output is self-biased, and must be AC-coupled with a 22nF capacitor (see Figure 2 for a simplified schematic). The buffer may be powered down by using bit PDREFO found in the serial port Power register h02.

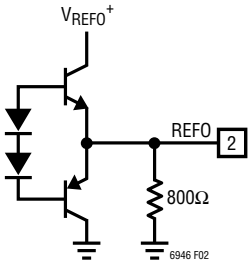


Figure 2. Simplified REFO Interface Schematic

OPERATION

REFERENCE (R) DIVIDER

A 10-bit divider, R_DIV, is used to reduce the frequency seen at the PFD. Its divide ratio R may be set to any integer from 1 to 1023, inclusive. Use the RD[9:0] bits found in registers h03 and h04 to directly program the R divide ratio. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD}, f_{VCO} and f_{RF} frequencies.

PHASE/FREQUENCY DETECTOR (PFD)

The phase/frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase-lock the loop, forcing a phase alignment at the PFD's inputs. The PFD may be disabled with the CPRST bit which prevents UP and DOWN pulses from being produced. See Figure 3 for a simplified schematic of the PFD.

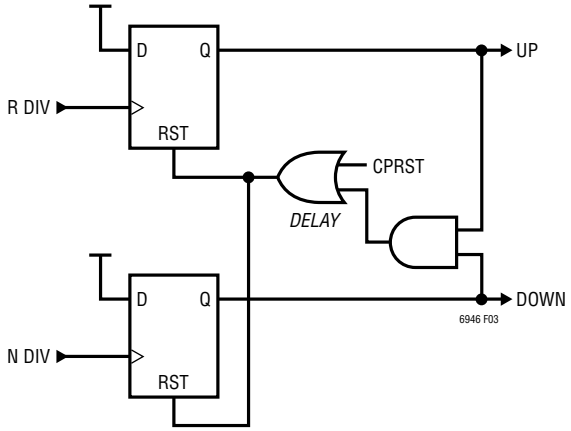


Figure 3. Simplified PFD Schematic

LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by setting the LKEN bit in the serial port register h07, and produces both LOCK and UNLOCK status flags, available through both the STAT output and serial port register h00.

The user sets the phase difference lock window time, t_{LWW}, for a valid LOCK condition with the LKWIN[1:0] bits. See Table 3 for recommended settings for different FPFD frequencies and the Applications Information section for examples.

Table 3. LKWIN[1:0] Programming

LKWIN[1:0]	t_{LWW}	f_{PFD}
0	3ns	>5MHz
1	10ns	≤5MHz
2	30ns	≤1.7MHz
3	90ns	≤550kHz

The PFD phase difference must be less than t_{LWW} for the LOKCNT number of successive counts before the lock indicator asserts the LOCK flag. The LKCNT[1:0] bits found in register h09 are used to set LOKCNT depending upon the application. See Table 4 for LKCNT[1:0] programming and the Applications Information section for examples.

Table 4. LKCNT[1:0] Programming

LKCNT[1:0]	COUNTS
0	32
1	128
2	512
3	2048

When the PFD phase difference is greater than t_{LWW}, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than t_{LWW}. See Figure 4 for more details.

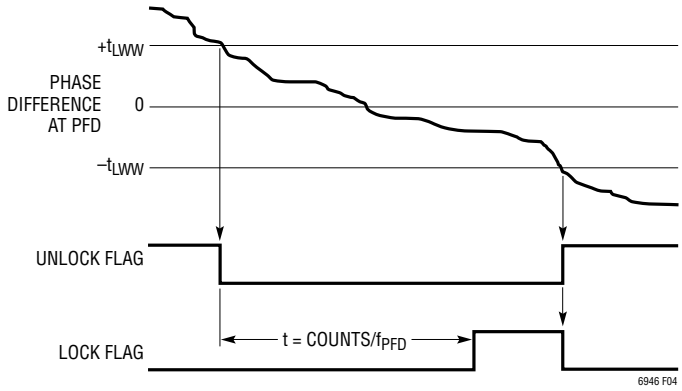


Figure 4. UNLOCK and LOCK Timing

OPERATION

CHARGE PUMP

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin, which should be connected to an appropriate loop filter. See Figure 5 for a simplified schematic of the charge pump.

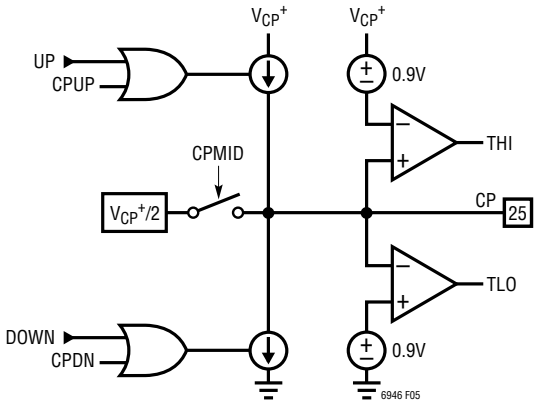


Figure 5. Simplified Charge Pump Schematic

The output current magnitude I_{CP} may be set from 250µA to 11.2mA using the CP[3:0] bits found in serial port register h09. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components. See Table 5 for programming specifics and the Applications Information section for loop filter examples.

Table 5. CP[3:0] Programming

CP[3:0]	I_{CP}
0	250µA
1	350µA
2	500µA
3	700µA
4	1.0mA
5	1.4mA
6	2.0mA
7	2.8mA
8	4.0mA
9	5.6mA
10	8.0mA
11	11.2mA
12 to 15	Invalid

The CPINV bit found in register h0A should be set for applications requiring signal inversion from the PFD, such as for complex external loops using an inverting op amp. A passive loop filter as shown in Figure 14 requires CPINV = 0.

CHARGE PUMP FUNCTIONS

The charge pump contains additional features to aid in system start-up and monitoring. See Table 6 for a summary.

Table 6. Charge Pump Function Bit Descriptions

BIT	DESCRIPTION
CPCHI	Enable High Voltage Output Clamp
CPCLO	Enable Low Voltage Output Clamp
CPDN	Force Sink Current
CPINV	Invert PFD Phase
CPMID	Enable Mid-Voltage Bias
CPRST	Reset PFD
CPUP	Force Source Current
CPWIDE	Extend Current Pulse Width
THI	High Voltage Clamp Flag
TLO	Low Voltage Clamp Flag

The CPCHI and CPCLO bits found in register h0A enable the high and low voltage clamps, respectively. When CPCHI is enabled and the CP pin voltage exceeds approximately V_{CP}^+ – 0.9V, the THI status flag is set, and the charge pump sourcing current is disabled. Alternately, when CPCLO is enabled and the CP pin voltage is less than approximately 0.9V, the TLO status flag is set, and the charge pump sinking current is disabled. See Figure 5 for a simplified schematic.

The CPMID bit also found in register h0A enables a resistive $V_{CP}^+/2$ output bias which may be used to pre-bias troublesome loop filters into a valid voltage range. When using CPMID, it is recommended to also assert the CPRST bit, forcing a PFD reset. Both CPMID and CPRST must be set to "0" for normal operation.

OPERATION

The CPUP and CPDN bits force a constant I_{CP} source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with the CPUP and CPDN bits, allowing a pre-charge of the loop to a known state, if required. CPUP, CPDN, and CPRST must be set to "0" to allow the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value (see Figure 3). CPWIDE is normally set to 0.

VCO

The integrated VCO is available in one of three frequency ranges. The output frequency range may be further extended by utilizing the output divider (see Available Options table, for more details). The wide frequency range of the VCO, coupled with the output divider capability, allows the LTC6946 to cover an extremely wide range of continuously selectable frequencies.

VCO Calibration

The VCO must be calibrated each time its frequency is changed by either f_{REF}, the R divider, or N divider, but not the O divider (see the Applications Information section for the relationship between R, N, O, and the f_{REF}, f_{PFD}, f_{VCO} and f_{RF} frequencies). *The output frequency is then stable over the LTC6946's entire temperature range, regardless of the temperature at which it was calibrated, until the part is reset due to a power cycle or software power-on reset (POR).*

The output of the B divider is used to clock digital calibration circuitry as shown in the Block Diagram. The B value, programmed with bits BD[3:0], is determined according to Equation 1.

$$B \geq \frac{f_{PFD}}{f_{CAL\text{-}MAX}} \qquad (1)$$

The maximum calibration frequency $f_{CAL\text{-}MAX}$ for each part option is shown in Table 7.

Table 7. Maximum Calibration Frequency

PART	$f_{CAL\text{-}MAX}$ (MHz)
LTC6946-1	1.0
LTC6946-2	1.33
LTC6946-3	1.7
LTC6946-4	1.8

The relationship between bits BD[3:0] and the B value is shown in Table 8.

Table 8. BD[3:0] Programming

BD[3:0]	B DIVIDE VALUE
0	8
1	12
2	16
3	24
4	32
5	48
6	64
7	96
8	128
9	192
10	256
11	384
12 to 15	Invalid

The VCO may be calibrated once the RD[9:0], ND[15:0], and BD[3:0] bits are written. The reference frequency f_{REF} must also be present and stable at the REF± inputs.

A calibration cycle is initiated each time the CAL bit is written to "1" (the bit is self-clearing). The calibration cycle takes between 12 and 14 cycles of the B divider output.

OPERATION

VCO Automatic Level Control (ALC)

The VCO uses an internal automatic level control (ALC) algorithm to maintain an optimal amplitude on the VCO resonator, and thus optimal phase noise performance. The user has several ALC configuration and status reporting options as seen in Table 9.

Table 9. ALC Bit Descriptions

BIT	DESCRIPTION
ALCCAL	Auto Enable ALC During CAL Operation
ALCEN	Always Enable ALC (Overrides ALCCAL, ALCMON and ALCULOK)
ALCHI	ALC Too High Flag (Resonator Amplitude Too High)
ALCLO	ALC Too Low Flag (Resonator Amplitude Too Low)
ALCMON	Enable ALC Monitoring for Status Flags Only; Does NOT Enable Amplitude Control
ALCULOK	Auto Enable ALC when PLL Unlocked

Changes in the internal ALC output can cause extremely small jumps in the VCO frequency. These jumps may be acceptable in some applications but not in others. Use the above table to choose when the ALC is active. The ALCHI and ALCLO flags, valid only when the ALC is active or the ALCMON bit is set, may be used to monitor the resonator amplitude.

The ALC must be allowed to operate during or after a calibration cycle. At least one of the ALCCAL, ALCEN or ALCULOK bits must be set.

VCO (N) DIVIDER

The 16-bit N divider provides the feedback from the VCO to the PFD. Its divide ratio N may be set to any integer from 32 to 65535, inclusive. Use the ND[15:0] bits found in registers h05 and h06 to directly program the N divide ratio. See the Applications Information section for the relationship between N and the f_{REF}, f_{PFD}, f_{VCO} and f_{RF} frequencies.

OUTPUT (O) DIVIDER

The 3-bit O divider can reduce the frequency from the VCO to extend the output frequency range. Its divide ratio O may be set to any integer from 1 to 6, inclusive, outputting a 50% duty cycle even with odd divide values. Use the OD[2:0] bits found in register h08 to directly program the O divide ratio. See the Applications Information section for the relationship between O and the f_{REF}, f_{PFD}, f_{VCO} and f_{RF} frequencies.

RF OUTPUT BUFFER

The low noise, differential output buffer produces a differential output power of –6dBm to 3dBm, settable with bits RFO[1:0] according to Table 10. The outputs may be combined externally, or used individually. Terminate any unused output with a 50Ω resistor to V_{RF}^+.

Table 10. RFO[1:0] Programming

RFO[1:0}	P_{RF} (Differential)	P_{RF} (Single Ended)
0	–6dBm	–9dBm
1	–3dBm	–6dBm
2	0dBm	–3dBm
3	3dBm	0dBm

Each output is open collector with 136Ω pull-up resistors to V_{RF}^+, easing impedance matching at high frequencies. See Figure 6 for circuit details and the Applications Information section for matching guidelines. The buffer may be muted with either the OMUTE bit, found in register h02, or by forcing the $\overline{\text{MUTE}}$ input low.

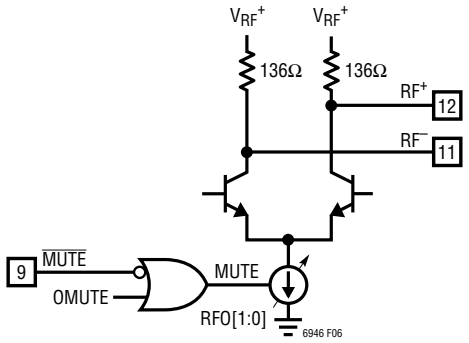


Figure 6. Simplified RF Interface Schematic

OPERATION

SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality. A configurable status output, STAT, gives additional instant monitoring.

Communication Sequence

The serial bus is comprised of $\overline{CS}$, SCLK, SDI and SDO. Data transfers to the part are accomplished by the serial bus master device first taking $\overline{CS}$ low to enable the LTC6946's port. Input data applied on SDI is clocked on the rising edge of SCLK, with all transfers MSB first. The communication burst is terminated by the serial bus master returning $\overline{CS}$ high. See Figure 7 for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC6946 connected in parallel on the serial bus), as SDO is three-stated (Hi-Z) when $\overline{CS}$ = 1, or when data is not being read from the part. *If the LTC6946 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a high value resistor of greater than 200k between SDO and GND to ensure the line returns to a known level during Hi-Z states. See Figure 8 for details.*

Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 12, byte-wide registers. All data bursts are comprised of at least two bytes. The 7 most significant bits of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 9 for an example of a detailed write sequence, and Figure 10 for a read sequence.

Figure 11 shows an example of two write communication bursts. The first byte of the first burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of "0" indicating a write. The next byte is the data intended for the register at address Addr0. $\overline{CS}$ is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (Addr1) and an LSB indicating a write. The next byte on SDI is the data intended for the register at address Addr1. $\overline{CS}$ is then taken high to terminate the transfer.

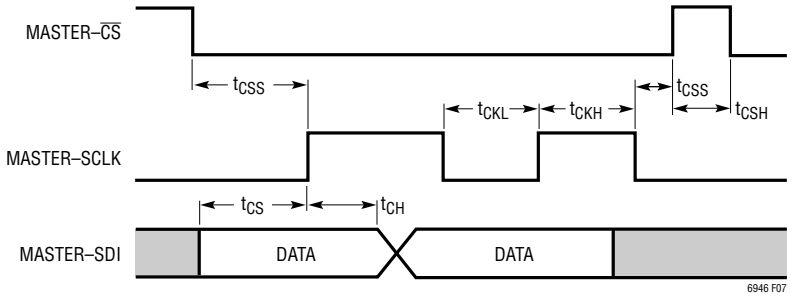


Figure 7. Serial Port Write Timing Diagram

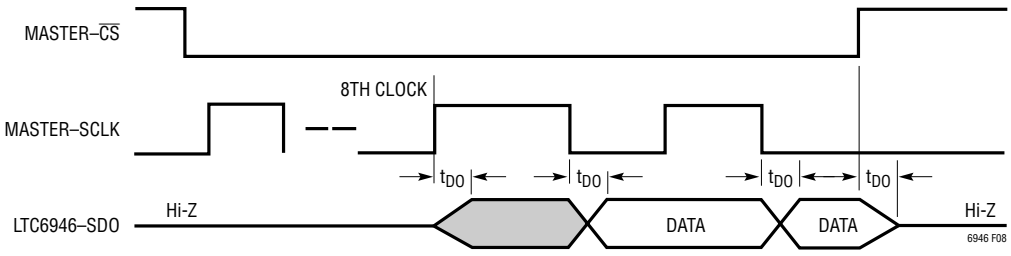


Figure 8. Serial Port Read Timing Diagram

OPERATION

Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC6946's register address auto-increment feature as shown in Figure 12. The serial port master sends the destination register address in the first byte and its data in the second byte as before, but continues sending bytes destined for subsequent registers. Byte 1's address is Addr0+1, Byte 2's address is Addr0+2, and so on. If the resister address pointer attempts to increment past 11 (h0B), it is automatically reset to 0.

An example of an auto-increment read from the part is shown in Figure 13. The first byte of the burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of "1" indicating a read. Once the LTC6946 detects a read burst, it takes SDO out of the Hi-Z condition and sends data bytes sequentially,

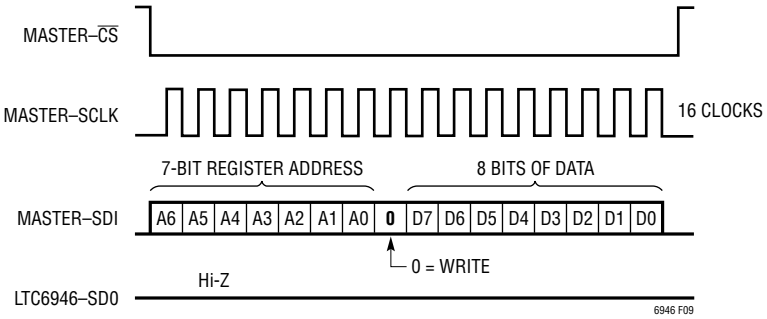


Figure 9. Serial Port Write Sequence

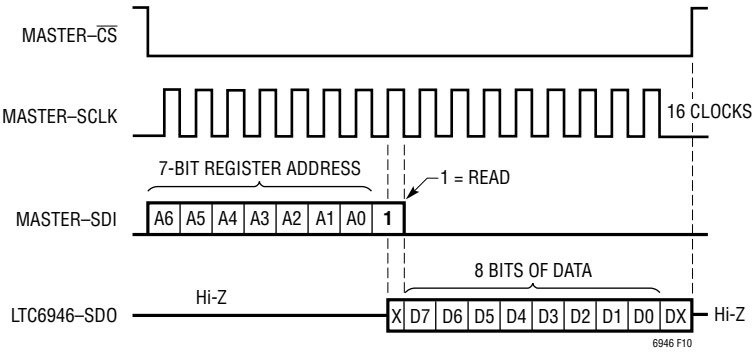


Figure 10. Serial Port Read Sequence

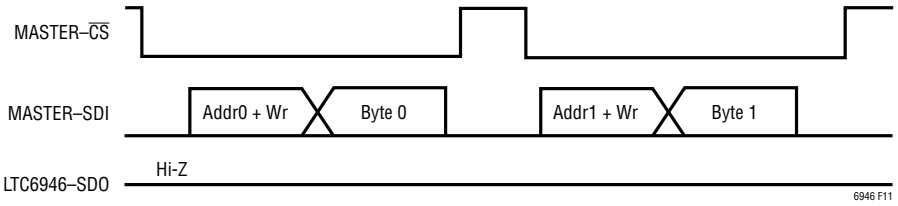


Figure 11. Serial Port Single Byte Write

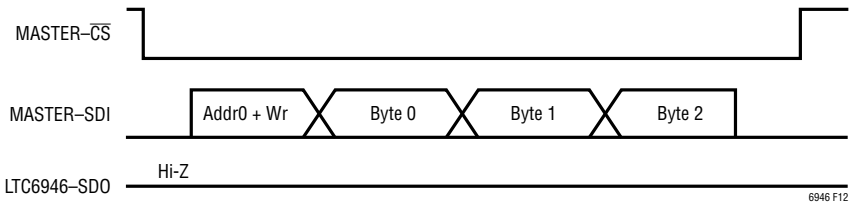


Figure 12. Serial Port Auto-Increment Write

OPERATION

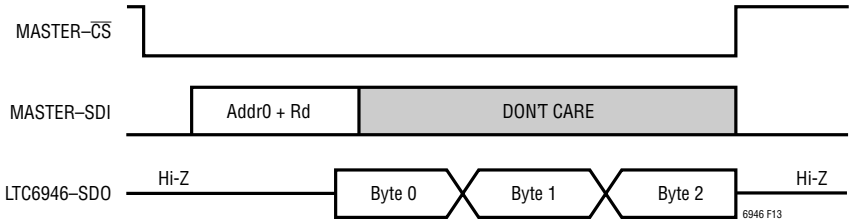


Figure 13. Serial Port Auto-Increment Read

beginning with data from register Addr0. The part ignores all other data on SDI until the end of the burst.

Multidrop Configuration

Several LTC6946s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate $\overline{CS}$ for each LTC6946 and ensure that only one device has $\overline{CS}$ asserted at any time. It is recommended to attach a high value resistor to SDO to ensure the line returns to a known level during Hi-Z states.

Serial Port Registers

The memory map of the LTC6946 may be found in Table 11, with detailed bit descriptions found in Table 12. The register address shown in hexadecimal format under the ADDR column is used to specify each register. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset is shown at the right.

The read-only register at address h00 is used to determine different status flags. These flags may be instantly output on the STAT pin by configuring register h01. See the STAT Output section for more information.

The read-only register at address h0B is a ROM byte for device identification.

Table 11. Serial Port Register Contents

ADDR	MSB	[6]	[5]	[4]	[3]	[2]	[1]	LSB	R/W	DEFAULT
h00	*	*	UNLOCK	ALCHI	ALCLO	LOCK	THI	TLO	R	
h01	*	*	x[5]	x[4]	x[3]	x[2]	x[1]	x[0]	R/W	h04
h02	PDALL	PDPLL	PDVCO	PDOUT	PDREFO	MTCAL	OMUTE	POR	R/W	h0E
h03	BD[3]	BD[2]	BD[1]	BD[0]	*	*	RD[9]	RD[8]	R/W	h30
h04	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	R/W	h01
h05	ND[15]	ND[14]	ND[13]	ND[12]	ND[11]	ND[10]	ND[9]	ND[8]	R/W	h00
h06	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]	R/W	hFA
h07	ALCEN	ALCMON	ALCCAL	ALCULOK	*	*	CAL	LKEN	R/W	h21
h08	BST	FILT[1]	FILT[0]	RFO[1]	RFO[0]	OD[2]	OD[1]	OD[0]	R/W	hF9
h09	LKWIN[1]	LKWIN[0]	LKCT[1]	LKCT[0]	CP[3]	CP[2]	CP[1]	CP[0]	R/W	h9B
h0A	CPCHI	CPCLO	CPMID	CPINV	CPWIDE	CPRST	CPUP	CPDN	R/W	hE4
h0B	REV[2]	REV[1]	REV[0]	PART[4]	PART[3]	PART[2]	PART[1]	PART[0]	R	hxx†

*unused †varies depending on version

OPERATION

Table 12. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT
ALCCAL	Auto Enable ALC During CAL Operation	1
ALCEN	Always Enable ALC (Override)	1
ALCHI	ALC Too Hi Flag	
ALCLO	ALC Too Low Flag	
ALCMON	Enable ALC Monitor for Status Flags Only	0
ALCULOK	Enable ALC When PLL Unlocked	0
BD[3:0]	Calibration B Divider Value	h3
BST	REF Buffer Boost Current	1
CAL	Start VCO Calibration (auto clears)	0
CP[3:0]	CP Output Current	hB
CPCHI	CP Enable Hi Voltage Output Clamp	1
CPCLO	CP Enable Low Voltage Output Clamp	1
CPDN	CP Pump Down Only	0
CPINV	CP Invert Phase	0
CPMID	CP Bias to Mid-Rail	1
CPRST	CP Three-State	1
CPUP	CP Pump Up Only	0
CPWIDE	CP Extend Pulse Width	0
FILT[1:0]	REF Input Buffer Filter	h3
LKCT[1:0]	PLL Lock Cycle Count	h1
LKEN	PLL Lock Indicator Enable	1
LKWIN[1:0]	PLL Lock Indicator Window	h2
LOCK	PLL Lock Indicator Flag	
MTCAL	Mutes Output During Calibration	1
ND[15:0]	N Divider Value (ND[15:0] > 31)	h00FA
OD[2:0]	Output Divider Value (0 < OD[2:0] < 7)	h1
OMUTE	Mutes RF Output	1
PART[4:0]	Part code (h01 for LTC6946-1, h02 for LTC6946-2, h03 for LTC6946-3, h04 for LTC6946-4 Version)	h01, h02, h03, h04
PDALL	Full Chip Power Down	0
PDOUT	Powers Down O_DIV, RF Output Buffer	0
PDPLL	Powers Down REF, REFO, R_DIV, PFD, CPUMP, N_DIV	0
PDREFO	Powers Down REFO	1
PDVCO	Powers Down VCO, N_DIV	0
POR	Force Power-On Reset	0
RD[9:0]	R Divider Value (RD[9:0] > 0)	h001
REV[2:0]	Rev Code	
RFO[1:0]	RF Output Power	h3
THI	CP Clamp High Flag	
TLO	CP Clamp Low Flag	
UNLOCK	PLL Unlock Flag	
x[5:0]	STAT Output OR Mask	h04

STAT Output

The STAT output pin is configured with the x[5:0] bits of register h01. These bits are used to bit-wise mask, or enable, the corresponding status flags of status register h00, according to Equation 2. The result of this bit-wise Boolean operation is then output on the STAT pin:

STAT = OR (Reg00[5:0] AND Reg01[5:0]) (2)

or expanded:

STAT = (UNLOCK AND x[5]) OR
(ALCHI AND x[4]) OR
(ALCLO AND x[3]) OR
(LOCK AND x[2]) OR
(THI AND x[1]) OR
(TLO AND x[0])

For example, if the application requires STAT to go high whenever the ALCHI, ALCLO, or THI flags are set, then x[4], x[3], and x[1] should be set to “1”, giving a register value of h1A.

Block Power-Down Control

The LTC6946’s power-down control bits are located in register h02, described in Table 12. Different portions of the device may be powered down independently. *Care must be taken with the LSB of the register, the POR (power-on reset) bit. When written to a “1”, this bit forces a full reset of the part’s digital circuitry to its power-up default state.*

APPLICATIONS INFORMATION

INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the frequency input at REF± and outputs a higher frequency at RF±. The PFD, charge pump, N divider, and external VCO and loop filter form a feedback loop to accurately control the output frequency (see Figure 14). The R and O divider are used to set the output frequency resolution.

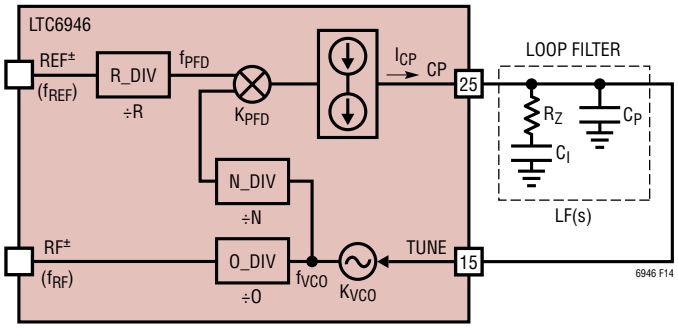


Figure 14. PLL Loop Diagram

OUTPUT FREQUENCY

When the loop is locked, the frequency f_{VCO} (in Hz) produced at the output of the VCO is determined by the reference frequency, f_{REF}, and the R and N divider values, given by Equation 3:

$$f_{VCO} = \frac{f_{REF} \bullet N}{R} \quad (3)$$

Here, the PFD frequency f_{PFD} produced is given by the following equation:

$$f_{PFD} = \frac{f_{REF}}{R} \quad (4)$$

and f_{VCO} may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet N$$

The output frequency f_{RF} produced at the output of the O divider is given by Equation 5:

$$f_{RF} = \frac{f_{VCO}}{O} \quad (5)$$

Using the above equations, the output frequency resolution f_{STEP} produced by a unit change in N is given by Equation 6:

$$f_{STEP} = \frac{f_{REF}}{R \bullet O} \quad (6)$$

LOOP FILTER DESIGN

A stable PLL system requires care in selecting the external loop filter values. The Linear Technology PLLWizard application, available from www.linear.com, aids in design and simulation of the complete system.

The loop design should use the following algorithm:

1. *Determine the output frequency, f_{RF}, and frequency step size, f_{STEP}, based on application requirements.* Using Equations 3, 4, 5 and 6, change f_{REF}, N, R, and O until the application frequency constraints are met. Use the minimum R value that still satisfies the constraints. Then calculate B using Equation 1 and Table 7.
2. *Select the open-loop bandwidth, BW, constrained by f_{PFD}.* A stable loop requires that BW is less than f_{PFD} by at least a factor of 10.
3. *Select loop filter component R_Z and charge pump current I_{CP} based on BW and the VCO gain factor, K_{VCO}.* BW (in Hz) is approximated by the following equation:

$$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N} \quad (7)$$

or

$$R_Z = \frac{2 \bullet \pi \bullet BW \bullet N}{I_{CP} \bullet K_{VCO}}$$

where K_{VCO} is in Hz/V, I_{CP} is in Amps, and R_Z is in Ohms.

K_{VCO} is obtained from the VCO tuning sensitivity in the Electrical Characteristics. Use I_{CP} = 11.2mA to lower in-band noise unless component values force a lower setting.

APPLICATIONS INFORMATION

4. *Select loop filter components C_I and C_P based on BW and R_Z.* A reliable loop can be achieved by using the following equations for the loop capacitors (in Farads):

$$C_I = \frac{3.5}{2 \bullet \pi \bullet BW \bullet R_Z} \quad (8)$$

$$C_P = \frac{1}{7 \bullet \pi \bullet BW \bullet R_Z} \quad (9)$$

DESIGN AND PROGRAMMING EXAMPLE

This programming example uses the DC1705A with the LTC6946-3. Assume the following parameters of interest:

f_{REF} = 20MHz at 7dBm into 50Ω

f_{STEP} = 125kHz

f_{RF} = 2.4GHz

From the Electrical Characteristics table:

f_{VCO} = 3.840GHz to 5.790GHz

$K_{VCO\%}$ = 4.0%Hz/V to 6.0%Hz/V

Determining Divider Values

Following the Loop Filter Design algorithm, first determine all the divider values. Using Equations 2, 3, 4 and 5 calculate the following values:

O = 2

R = 20MHz/(125kHz • 2) = 80

f_{PFD} = 250kHz

N = 2 • 2.4GHz/250kHz = 19200

f_{VCO} = 4.8GHz

Also, from Equation 1 or Table 7 determine B:

B = 8 and BD[3:0] = 0

The next step in the algorithm is to determine the open-loop bandwidth. BW should be at least 10× smaller than f_{PFD}. Wider loop bandwidths could have lower integrated phase noise, depending on the VCO phase noise signature, while narrower bandwidths will likely have lower spurious power. Use a factor of 15 for this design example:

$$BW = \frac{250kHz}{15} = 16.7kHz$$

Loop Filter Component Selection

Now set loop filter resistor, R_Z, and charge pump current, I_{CP}. Because the K_{VCO} varies over the VCO's frequency range, using the K_{VCO} geometric mean gives good results. Using an I_{CP} of 11.2mA, R_Z is determined:

$$K_{VCO} = 4.8 \bullet 10^9 \bullet \sqrt{0.04 \bullet 0.06} = 235MHz / V$$

$$R_Z = \frac{2 \bullet \pi \bullet 16.7k \bullet 19200}{11.2m \bullet 235M}$$

$$R_Z = 765\Omega$$

Now calculate C_I and C_P from Equations 7 and 8:

$$C_I = \frac{3.5}{2 \bullet \pi \bullet 16.7k \bullet 765} = 44nF$$

$$C_P = \frac{1}{7 \bullet \pi \bullet 16.7k \bullet 765} = 3.6nF$$

Status Output Programming

This example will use the STAT pin to alert the system whenever the LTC6946 generates a fault condition. Program x[5], x[4], x[3], x[1], x[0] = 1 to force the STAT pin high whenever any of the UNLOCK, ALCHI, ALCLO, THI or TLO flags asserts:

Reg01 = h3B

Power Register Programming

For correct PLL operation all internal blocks should be enabled, but PDREFO should be set if the REFO pin is not being used. OMUTE may remain asserted (or the MUTE pin held low) until programming is complete. For PDREFO = 1 and OMUTE = 1:

Reg02 = h0A

APPLICATIONS INFORMATION

Divider Programming

Program registers Reg03 to Reg06 with the previously determined B, R and N divider values.

Reg03 = h00

Reg04 = h50

Reg05 = h4B

Reg06 = h00

VCO ALC and Calibration Programming

Now that all the divider registers are programmed, and assuming that the reference frequency is stable at REF±, calibrate the VCO. Set the ALC options (ALCMON = 1, ALCCAL = 1) and the lock enable bit (LKEN = 1) at the same time:

Reg07 = h63

The LTC6946 will now calibrate its VCO. The ALC will only be active during the calibration cycle, but the ALCHI and ALCLO status conditions will be monitored.

Reference Input Settings and Output Divider Programming

From Table 1, FILT = 1 for a 20MHz reference frequency.

Next, convert 7dBm into V_{P-P}. For a CW tone, use the following equation with R = 50:

$$V_{P-P} \cong \sqrt{R} \bullet 10^{(dBm-21)/20} \quad (10)$$

This gives V_{P-P} = 1.41V, and, according to Table 2, set BST = 1.

Now program Reg08, assuming maximum RF± output power (RFO[1:0] = 3 according to Table 9) and OD[2:0] = 2:

Reg08 = hBA

Lock Detect and Charge Pump Current Programming

Next, determine the lock indicator window from f_{PFD}. From Table 3, LKWIN[1:0] = 3 for a t_{LWW} of 90ns. The LTC6946 will consider the loop "locked" as long as the phase coincidence at the PFD is within 8°, as calculated:

phase = 360° • t_{LWW} • f_{PFD} = 360 • 90n • 250k ≅ 8°

LKWIN[1:0] may be set to a smaller value to be more conservative. However, the inherent phase noise of the loop could cause false "unlocks" for too small a value.

Choosing the correct LOKCNT depends upon the ratio of the bandwidth of the loop to the PFD frequency (BW/f_{PFD}). Smaller ratios dictate larger LOKCNT values. A LOKCNT value of 128 will work for our ratio of 1/15. From Table 4, LKCNT[1:0] = 1 for 128 counts.

Using Table 5 with the previously selected I_{CP} of 11.2mA, gives CP[3:0] = 11 (hB). This is enough information to program Reg09:

Reg09 = hDB

Charge Pump Function Programming

This example uses the additional voltage clamp features to allow us to monitor fault conditions by setting CPCHI = 1 and CPCLO = 1. If something occurs and the system can no longer lock to its intended frequency, the charge pump output will move toward either GND or V_{CP}^+, thereby setting either the TLO or THI status flags, respectively. Disable all the other charge pump functions (CPMID, CPINV, CPRST, CPUP and CPDN) to allow the loop to lock:

Reg0A = hC0

The loop should now lock. Now unmute the output by setting OMUTE = 0 (assumes the MUTE pin is high):

Reg02 = h08

REFERENCE SOURCE CONSIDERATIONS

A high quality signal must be applied to the REF± inputs as they provide the frequency reference to the entire PLL. As mentioned previously, to achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

The LTC6946 may be driven single ended to CMOS levels (greater than $2.7V_{P-P}$). Apply the reference signal directly without a DC-blocking capacitor at REF+, and bypass REF– to GND with a 47pF capacitor. The BST bit must also be set to "0", according to guidelines given in Table 2.

APPLICATIONS INFORMATION

The LTC6946 achieves an in-band normalized phase noise floor of –226dBc/Hz (typical). To calculate its equivalent input phase noise floor $L_{M(IN)}$, use the following Equation 11:

$$L_{M(IN)} = -226 + 10 \bullet \log_{10}(f_{REF}) \quad (11)$$

For example, using a 10MHz reference frequency gives an input phase noise floor of –156dBc/Hz. The reference frequency source's phase noise must be at least 3dB better than this to prevent limiting the overall system performance.

IN-BAND OUTPUT PHASE NOISE

The in-band phase noise produced at f_{RF} may be calculated by using Equation 12.

$$L_{M(OUT)} = -226 + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{f_{RF}}{f_{PFD}}\right) \quad (12)$$

or

$$L_{M(OUT)} = -226 + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{N}{O}\right)$$

As can be seen, for a given PFD frequency f_{PFD}, the output in-band phase noise increases at a 20dB-per-decade rate with the N divider count. So, for a given output frequency f_{RF}, f_{PFD} should be as large as possible (or N should be as small as possible) while still satisfying the application's frequency step size requirements.

OUTPUT PHASE NOISE DUE TO 1/f NOISE

In-band phase noise at very low offset frequencies may be influenced by the LTC6946's 1/f noise, depending upon f_{PFD}. Use the normalized in-band 1/f noise of –274dBc/Hz with Equation 13 to approximate the output 1/f phase noise at a given frequency offset f_{OFFSET}.

$$L_{M(OUT\text{-}1/f)}(f_{OFFSET}) = -274 + 20 \bullet \log_{10}(f_{RF}) - 10 \bullet \log_{10}(f_{OFFSET}) \quad (13)$$

Unlike the in-band noise floor $L_{M(OUT)}$, the 1/f noise $L_{M(OUT\ 1/f)}$ does not change with f_{PFD}, and is not constant over offset frequency. See Figure 15 for an example of in-band phase noise for f_{PFD} equal to 3MHz and 100MHz. The total phase noise will be the summation of $L_{M(OUT)}$ and $L_{M(OUT\ 1/f)}$.

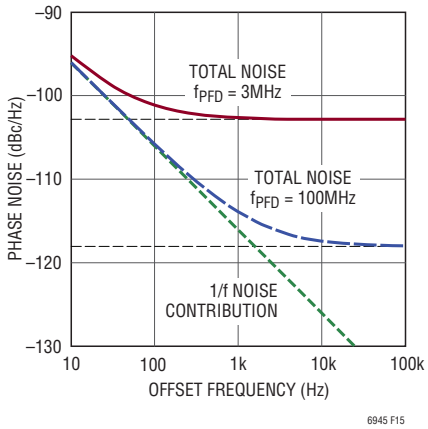


Figure 15. Theoretical In-Band Phase Noise, f_{RF} = 2500MHz

RF OUTPUT MATCHING

The RF± outputs may be used in either single-ended or differential configurations. Using both RF outputs differentially will result in approximately 3dB more output power than single ended. Impedance matching to an external load in both cases requires external chokes tied to V_{RF}^+. Measured RF± s-parameters are shown below in Table 13 to aid in the design of impedance matching networks.

Table 13. Single-Ended RF Output Impedance

FREQUENCY (MHZ)	IMPEDANCE (Ohms)	S11 (dB)
500	102.8 – j49.7	–6.90
1000	70.2 – j60.1	–6.53
1500	52.4 – j56.2	–6.35
2000	43.6 – j49.2	–6.58
2500	37.9 – j39.6	–7.34
3000	32.7 – j28.2	–8.44
3500	27.9 – j17.8	–8.99
4000	24.3 – j9.4	–8.72
4500	22.2 – j3.3	–8.26
5000	21.6 + j1.9	–8.02
5500	21.8 + j6.6	–7.91
6000	23.1 + j11.4	–8.09
6500	25.7 + j16.9	–8.38
7000	29.3 + j23.0	–8.53
7500	33.5 + j28.4	–8.56
8000	37.9 + j32.6	–8.64

APPLICATIONS INFORMATION

Single-ended impedance matching is accomplished using the circuit of Figure 16, with component values found in Table 14. *Using smaller inductances than recommended can cause phase noise degradation, especially at lower center frequencies.*

Table 14. Suggested Single-Ended Matching Component Values

f_{RF} (MHz)	L_C (nH)	C_S (pF)
350 to 1500	180	270
1000 to 5800	68	100

Return loss measured on the DC1705 using the above component values is shown in Figure 17. A broadband match is achieved using an (L_C, C_S) of either (68nH, 100pF) or (180nH, 270pF). However, for maximum output power and best phase noise performance, use the recommended component values of Table 13. L_C should be a wirewound inductor selected for maximum Q factor and SRF, such as the Coilcraft HP series of chip inductors.

The LTC6946's differential RF± outputs may be combined using an external balun to drive a single-ended load. The advantages are approximately 3dB more output power than each output individually and better 2nd order harmonic performance.

For lower frequencies, transmission line (TL) baluns such as the M/A-COM MABACT0065 and the TOKO #617DB-1673 provide good results. At higher frequencies, surface mount (SMT) baluns such as those produced by TDK, Anaren, and Johanson Technology, can be attractive alternatives. See Table 15 for recommended balun part numbers versus frequency range.

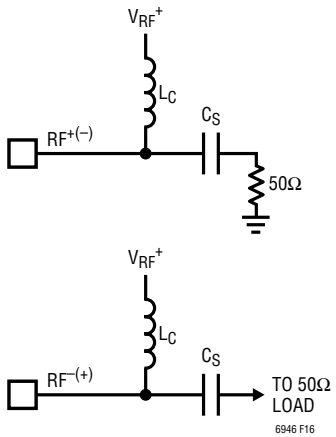


Figure 16. Single-Ended Output Matching Schematic

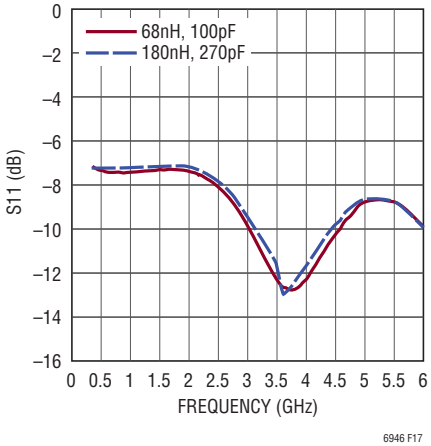


Figure 17. Single-Ended Return Loss

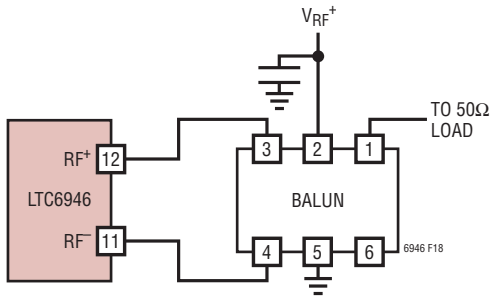
The listed SMT baluns contain internal chokes to bias RF± and also provide input-to-output DC isolation. The pin denoted as GND or DC FEED should be connected to the V_{RF}^+ voltage. Figure 18 shows a surface mount balun's connections with a DC FEED pin.

Table 15. Suggested Baluns

f_{RF} (MHz)	PART NUMBER	MANUFACTURER	TYPE
350 to 900	#617DB-1673	TOKO	TL
400 to 600	HHM1589B1	TDK	SMT
600 to 1400	BD0810J50200	Anaren	SMT
600 to 3000	MABACT0065	M/A-COM	TL
1000 to 2000	HHM1518A3	TDK	SMT
1400 to 2000	HHM1541E1	TDK	SMT
1900 to 2300	2450BL15B100E	Johanson	SMT
2000 to 2700	HHM1526	TDK	SMT
3700 to 5100	HHM1583B1	TDK	SMT
4000 to 6000	HHM1570B1	TDK	SMT

The listed TL baluns do not provide input-to-output DC isolation and must be AC coupled at the output. Figure 18 displays RF± connections using these baluns.

APPLICATIONS INFORMATION



BALUN PIN CONFIGURATION

1	UNBALANCED PORT
2	GND OR DC FEED
3	BALANCED PORT
4	BALANCED PORT
5	GND
6	NC

Figure 18. Example SMT Balun Connection

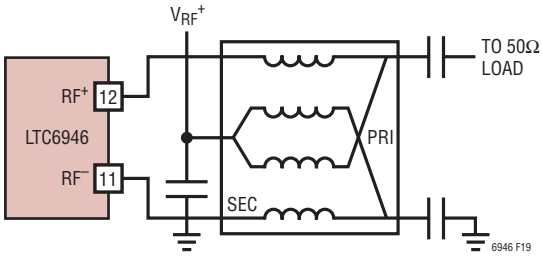


Figure 19. Example TL Balun Connection

SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

Care must be taken when creating a PCB layout to minimize power supply decoupling and ground inductances. All power supply V^+ pins should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible. Multiple vias to the ground plane should be used for all ground connections, including to the power supply decoupling capacitors.

The package's exposed pad is a ground connection, and must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance (see Figure 20 for an example). See QFN Package Users Guide, page 8, on Linear Technology website's Packaging Information page for specific recommendations concerning land patterns and land via solder masks. A link is provided below.

http://www.linear.com/designtools/packaging

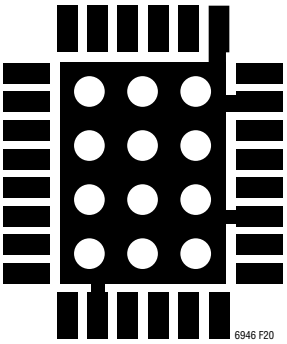


Figure 20. Example Exposed Pad Land Pattern

REFERENCE SIGNAL ROUTING, SPURIOUS AND PHASE NOISE

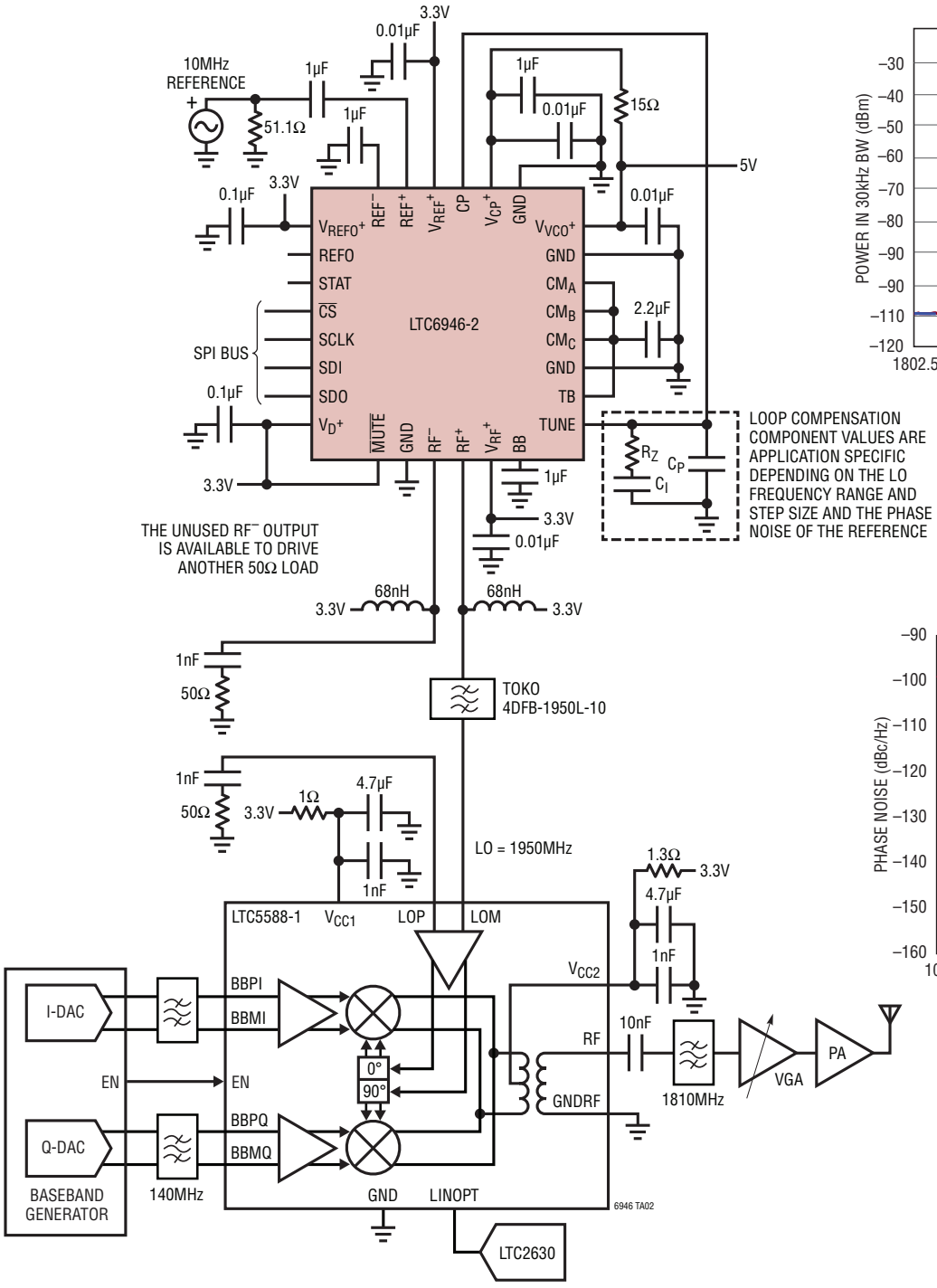
The charge pump operates at the PFD's comparison frequency f_{PFD}. The resultant output spurious energy is small and is further reduced by the loop filter before it modulates the VCO frequency.

However, improper PCB layout can degrade the LTC6946's inherent spurious performance. Care must be taken to prevent the reference signal f_{REF} from coupling onto the VCO's tune line, or into other loop filter signals. Example suggestions are the following.

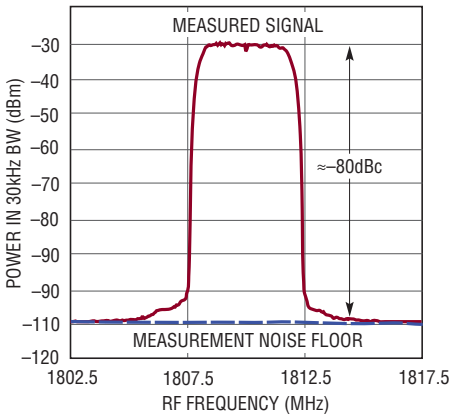
1. Do not share power supply decoupling capacitors between same voltage power supply pins.
2. Use separate ground vias for each power supply decoupling capacitor, especially those connected to V_{REF}^+, V_{CP}^+, and V_{VCO}^+.
3. Physically separate the reference frequency signal from the loop filter and VCO.
4. Do not place a trace between the CM_A, CM_B and CM_C pads underneath the package as worse phase noise could result.

APPLICATIONS INFORMATION

LTC6946-2 Driving a Modulator

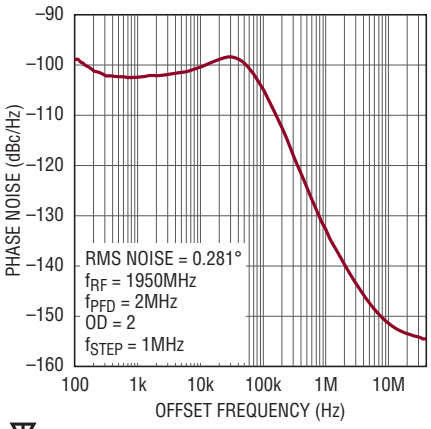


Measured W-CDMA ACPR (3.84MHz Bandwidth)



6946 TA02b

LTC6946-2 Modulator Application Phase Noise

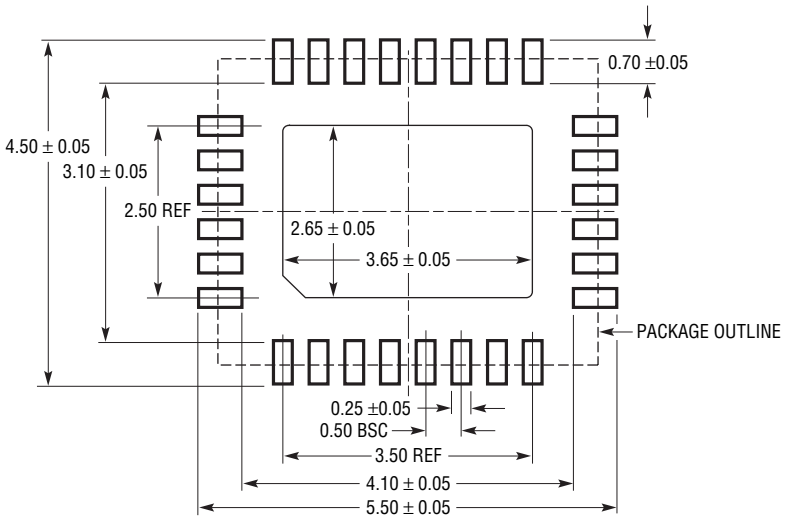


6946 TA02c

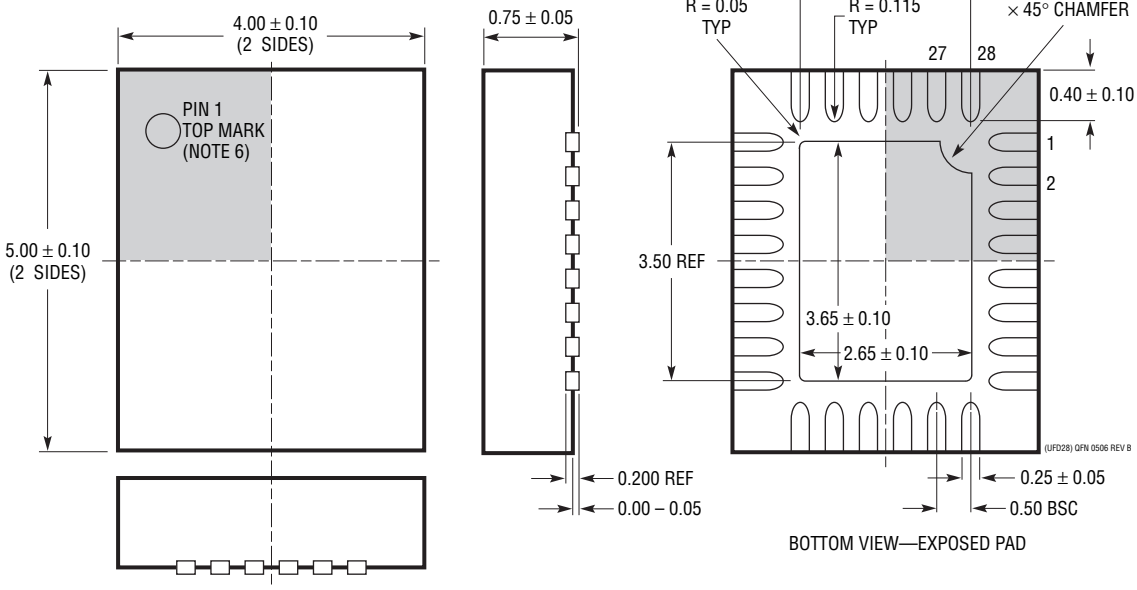
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

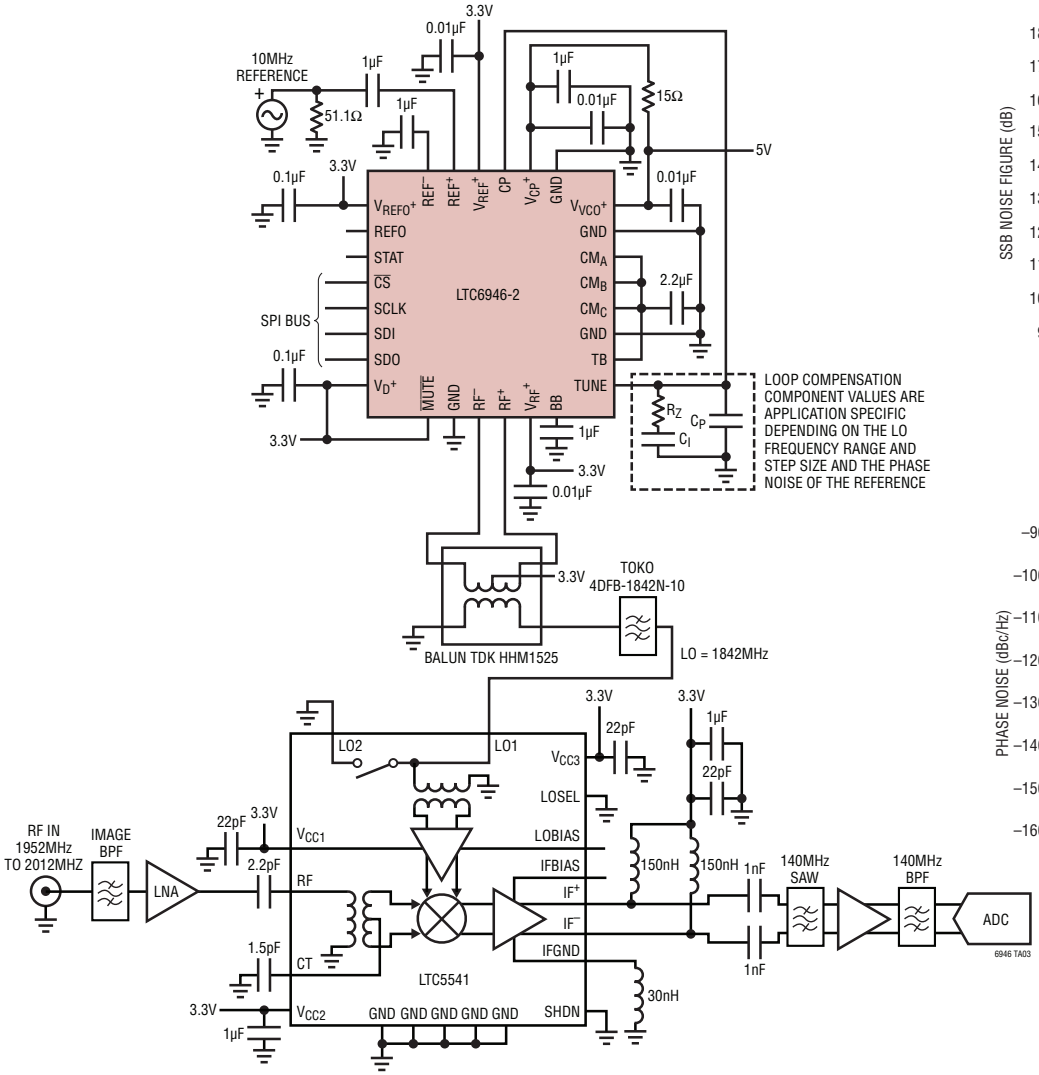
REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/11	Add I_{OL} and remove Max value, remove Max value for I_{OH} Revise values on Block Diagram	4 11
B	03/15	Added LTC6946-4.	All pages
		Changed operating core temperature to operating junction temperature.	2
		Updated power supply currents.	5
		Updated VCO calibration.	8, 17

LINEAR TECHNOLOGY

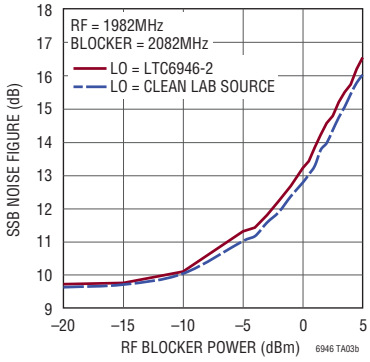
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

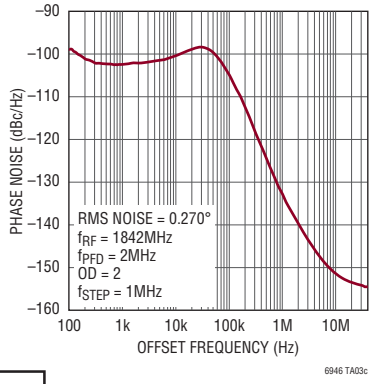
LTC6946-2 Driving a Passive Downconverting Mixer



LTC5541 Noise Figure vs Blocker Power and LO Signal Source



LTC6946-2 Mixer Application Phase Noise



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6945	Ultralow Noise and Spurious Integer-N Synthesizer	350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor
LTC6947	Ultralow Noise and Spurious Fractional-N Synthesizer	350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor
LTC6948	Ultralow Noise and Spurious Frac-N Synthesizer with VCO	370MHz to 6.39GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor
LTC6950	Low Phase Noise and Spurious Integer-N PLL Core with Five Output Clock Distribution and EZSync	1.4GHz Max VCO Frequency, Additive Jitter <20fsRMS, –226dBc/Hz Normalized In-Band Phase Noise Floor
LTC6957	Low Phase Noise, Dual Output Buffer/Driver/Logic Converter	Optimized Conversion of Sine Waves to Logic Levels, LVPECL/LVDS/CMOS
LTC2000	16-/14-/11-Bit 2.5Gsps DAC	Superior 80dBc SFDR at 70MHz Output, 40mA Nominal Drive and High Linearity
LTC5569	Broadband Dual Mixer	300MHz to 4GHz, 26.8dBm IIP3, 2dB Gain, 11.7dB NF, 600mW Power
LTC5588-1	Ultrahigh OIP3 I/Q Modulator	200MHz to 6GHz, 31dBm OIP3, –160.6dBm/Hz Noise Floor
LT®5575	Direct Conversion I/Q Demodulator	800MHz to 2.7GHz, 22.6dBm IIP3, 60dBm IIP2, 12.7dB NF

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