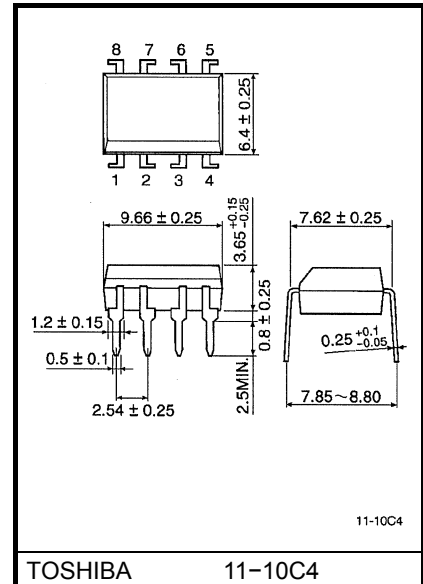


TLP559(IGM)

Transistor Inverters
Air Conditioner Inverters
Line Receivers
Intelligent Power Modules (IPMs) Interfaces

Unit: mm



Weight: 0.54 g (typ.)

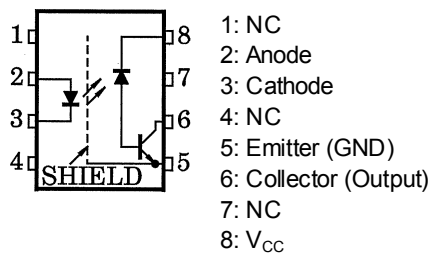
The TOSHIBA TLP559(IGM) consists of a high-output GaAlAs light emitting diode optically coupled to a high-speed photodiode with a transistor amplifier.

The TLP559(IGM) has no internal base connection. The Faraday shield in the photodetector chip provides an effective common-mode noise transient immunity.

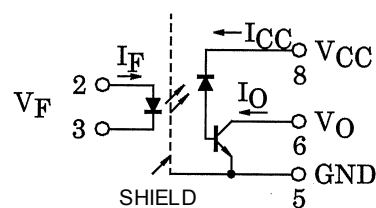
The TLP559(IGM) guarantees minimum and maximum propagation delay time, a relative time difference between the rise and fall time, and common-mode transient immunity. Therefore, the TLP559(IGM) is suitable for an isolation interface between an Intelligent Power Module (IPM) and a control IC in motor control applications.

- Isolation Voltage: 2500 Vrms (min)
- Common-Mode Transient Immunity: ± 10 kV/ μ s (min) @ $V_{CM} = 1500$ V
- Switching Time: $t_{pHL}, t_{pLH} = 0.1 \mu$ s (min), $= 0.8 \mu$ s (max) @ $I_F = 10$ mA, $V_{CC} = 15$ V, $R_L = 20$ k Ω , $T_a = 25^\circ$ C
- Switching Time Dispersion: 0.7μ s (max)
 (| $t_{pLH} - t_{pHL}$ |)
- TTL Compatible
- UL Recognized: UL1577, File No. E67349

Pin Configuration (Top view)



Schematic



Start of commercial production
 1995/01

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Note 1)	I _F	25	mA
	Pulse Forward Current (Note 2)	I _{FP}	50	mA
	Peak Transient Forward Current (Note 3)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
	Diode Power Dissipation (Note 4)	P _D	45	mW
DETECTOR	Output Current	I _O	8	mA
	Peak Output Current	I _{OP}	16	mA
	Output Voltage	V _O	-0.5 to 20	V
	Supply Voltage	V _{CC}	-0.5 to 30	V
	Output Power Dissipation (Note 5)	P _O	100	mW
Operating Temperature Range		T _{opr}	-55 to 100	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature(10s) (Note 6)		T _{sol}	260	°C
Isolation Voltage(AC, 1 minute, R.H.≤60%, Ta=25°C) (Note 7)		BV _S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8 mA above 70°C.

(Note 2) 50% duty cycle, 1 ms pulse width.

Derate 1.6 mA/°C above 70°C.

(Note 3) Pulse width PW ≤ 1μs, 300 pps.

(Note 4) Derate 0.9 mW/°C above 70°C.

(Note 5) Derate 2 mW/°C above 70°C.

(Note 6) Soldering portion of lead : up to 2mm from the body of the device.

(Note 7) Device considers a two-terminal device : pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
LED	Forward Voltage	V_F	$I_F = 16 \text{ mA}$	—	1.65	1.85	V
	Forward Voltage Temperature Coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16 \text{ mA}$	—	-2	—	mV / °C
	Reverse Current	I_R	$V_R = 5 \text{ V}$	—	—	10	μA
	Capacitance between Terminal	C_T	$V = 0, f = 1 \text{ MHz}$	—	45	—	pF
DETECTOR	High Level Output Current	$I_{OH(1)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$	—	3	500	nA
		$I_{OH(2)}$	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$ $V_O = 20 \text{ V}$	—	—	5	μA
		I_{OH}	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$ $V_O = 20 \text{ V}, T_a = 70^\circ\text{C}$	—	—	50	
	High Level Supply Voltage	I_{CCH}	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$	—	0.01	1	μA
	Supply Voltage	V_{CC}	$I_{CC} = 0.01 \text{ mA}$	30	—	—	V
	Output Voltage	V_O	$I_O = 0.5 \text{ mA}$	20	—	—	V

Coupled Electrical Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Current Transfer Ratio	I_O / I_F	$I_F = 10 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $V_O = 0.4 \text{ V}$	25	35	75	%
		$I_F = 10 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $V_O = 0.4 \text{ V}, T_a = -25 \text{ to } 100^\circ\text{C}$	15	—	—	
Low Level Output Voltage	V_{OL}	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $I_O = 2.4 \text{ mA}$	—	—	0.4	V

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance Input to Output	C_S	$V = 0, f = 1 \text{ MHz}$ (Note 7)	—	0.8	—	pF
Isolation Resistance	R_S	R.H. $\leq 60\%$, $V_S = 500 \text{ V}$ (Note 7)	5×10^{10}	10^{14}	—	Ω
Isolation Voltage	BV_S	AC, 1 minute	2500	—	—	V_{rms}
		AC, 1 second, in oil	—	5000	—	
		DC, 1 minute, in oil	—	5000	—	Vdc

Switching Characteristics (Ta = 25°C, VCC = 15 V)

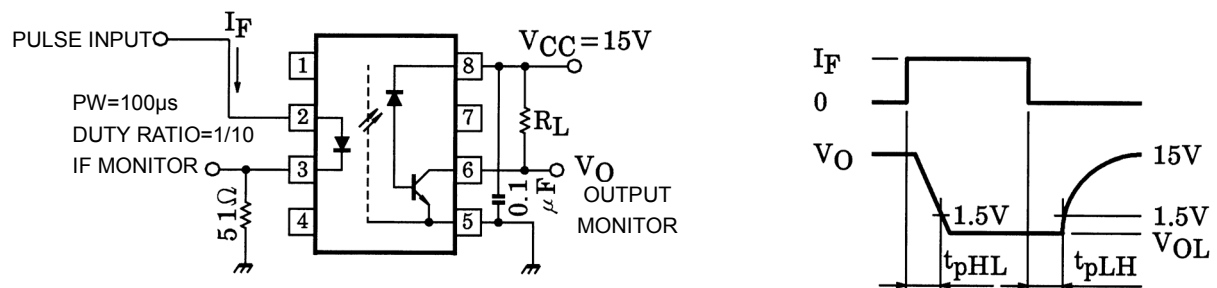
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time (H→L)	t_{pHL}	1	$I_F = 10 \text{ mA}$, $R_L = 20 \text{ k}\Omega$	0.1	0.45	0.8	μs
Propagation Delay Time (L→H)	t_{pLH}		$I_F = 10 \text{ mA}$, $R_L = 20 \text{ k}\Omega$ $T_a = 0 \sim 85^\circ\text{C}$	0.1	0.45	0.9	
			$I_F = 10 \text{ mA}$, $R_L = 20 \text{ k}\Omega$ $T_a = -25 \sim 100^\circ\text{C}$	0.1	0.45	1.0	
Switching Time Dispersion between ON and OFF	$ t_{pLH} - t_{pHL} $	1	$I_F = 10 \text{ mA}$, $R_L = 20 \text{ k}\Omega$	—	0.25	0.7	μs
			$I_F = 10 \text{ mA}$, $R_L = 20 \text{ k}\Omega$ $T_a = 0 \sim 85^\circ\text{C}$	—	0.25	0.8	
			$I_F = 20 \text{ mA}$, $R_L = 20 \text{ k}\Omega$ $T_a = -25 \sim 100^\circ\text{C}$	—	0.25	0.9	
Common Mode Transient Immunity at Logic High Output (Note 8)	CM_H	2	$I_F = 0 \text{ mA}$, $V_{CM} = 1500 \text{ V}_{p-p}$, $R_L = 20 \text{ k}\Omega$	10000	15000	—	$\text{V}/\mu\text{s}$
Common Mode Transient Immunity at Logic Low Output (Note 8)	CM_L		$I_F = 10 \text{ mA}$, $V_{CM} = 1500 \text{ V}_{p-p}$, $R_L = 20 \text{ k}\Omega$	-10000	-15000	—	$\text{V}/\mu\text{s}$

(Note 8) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1\text{V}$).

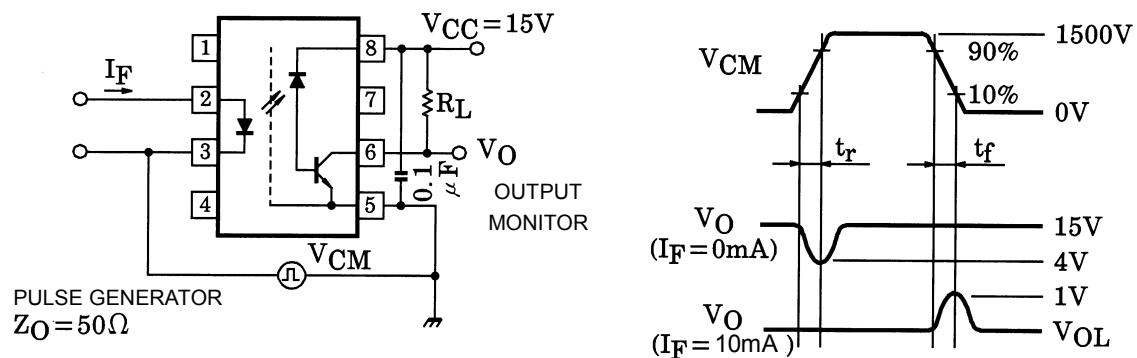
CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 4\text{V}$).

(Note 9) Maximum electrostatic discharge voltage for any pins: 100V ($C \leq 200\text{pF}$, $R=0$)

Test Circuit 1: Switching time test circuit



Test Circuit 2: Common mode noise immunity test circuit



$$CM_H = \frac{1200(\text{V})}{t_r(\mu\text{s})}, \quad CM_L = \frac{1200(\text{V})}{t_f(\mu\text{s})}$$

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