CMOS 4-BIT MICROCONTROLLER

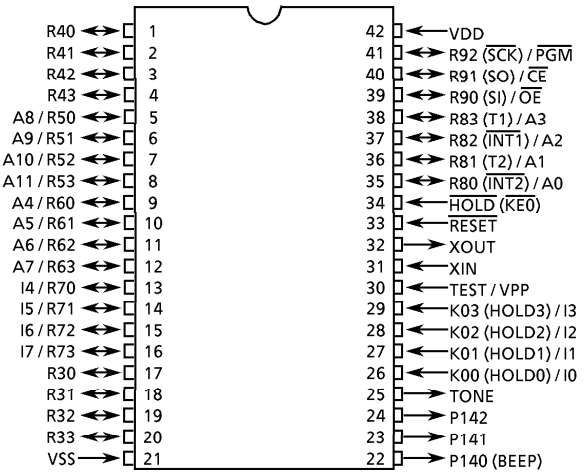
TMP47P453VN
TMP47P453VF

The 47P453V is the OTP microcontroller with 32kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket (BM1120, BM1121). A.C./D.C characteristics are equivalent to Mask-programed ROM device.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P453VN	OTP 4096 × 8-bit	768 × 4-bit	SDIP42-P-600-1.78	BM1120
TMP47P453VF			QFP44-P-1414-0.80D	BM1121

PIN ASSIGNMENT (TOP VIEW)

SDIP42-P-600-1.78



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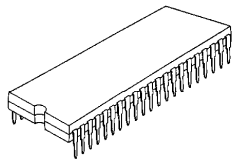

TMP47P453VN

980901EBP1

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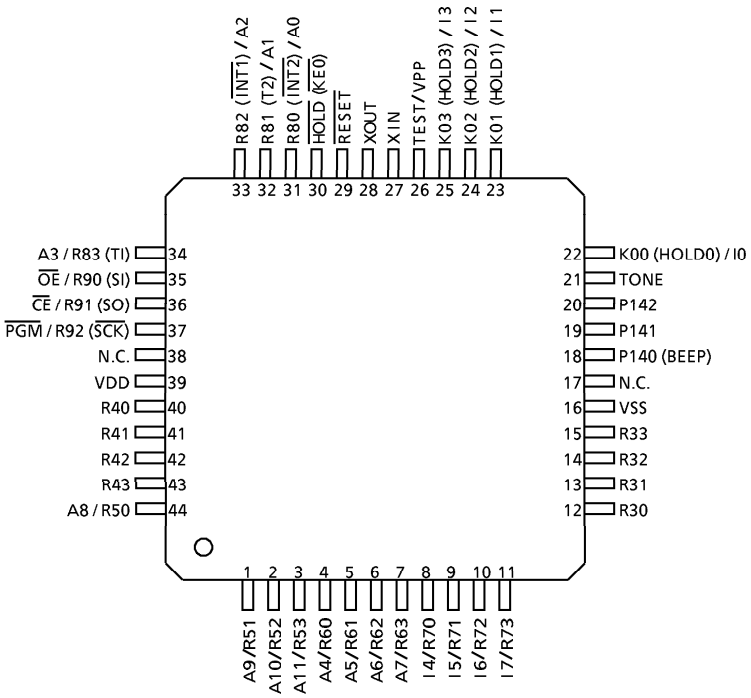
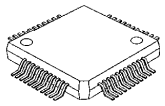
PIN ASSIGNMENT (TOP VIEW)

QFP44-P-1414-0.80D



QFP44-P-1414-0.80D



TMP47P453VF

PIN FUNCTION

The 47P453A has MCU mode and PROM mode.

(1) MCU mode

The 47C453A and the 47P453V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A11 to A8	Input	Address inputs	R53 to R50
A7 to A4			R63 to R60
A3 to A0			R83 to R80
I7 to I4	I/O	Data inputs / outputs	R73 to R70
I3 to I0			K03 to K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
TONE	Output	Open	
R33 to R30	I/O	Be fixed to low level	
R43 to R40			
P142 to P140	Output	Open	
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	External clock input (to keep the internal state stable)	
XOUT	Output	Open	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P453V.
The 47P453V is the same as the 47C453A except that an OTP is used instead of a Mask ROM.

1. OPERATION MODE

The 47P453V has an MCU mode and a PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C453A, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C453A.

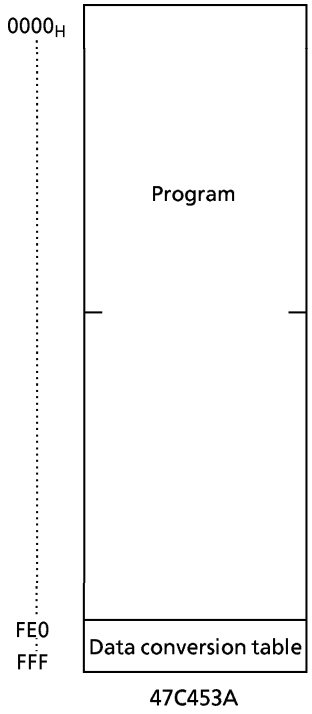


Figure 1-1. Program area

1.1.2 Data Memory

The 47P453V has 768 × 4-bit data memory.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C453A except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P453V is the same as I/O code WB of the 47C453A.
External resistance, for example, is required when using as evaluator of other I/O codes (WE, WH) (Refer to Figure 1-2).

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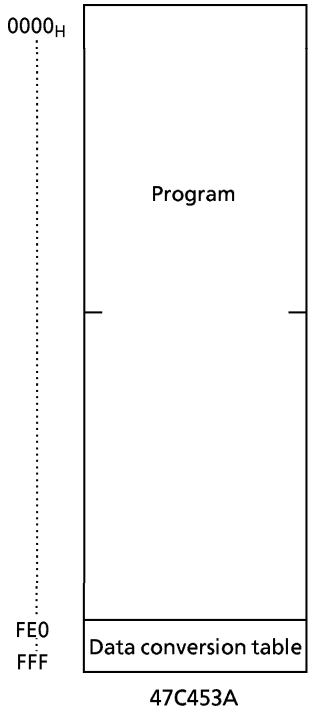

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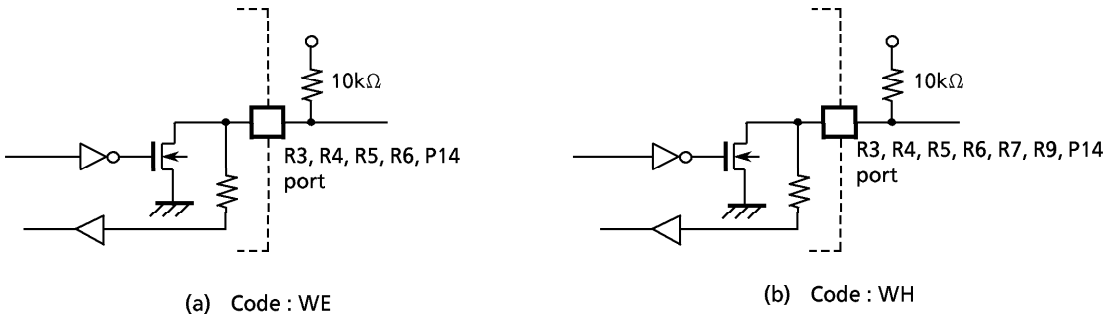


Figure 1-2. I/O code and external circuitry

1.2 PROM Mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).

An adapter socket (part No. BM1120 / BM1121) is available for connecting a PROM writer.

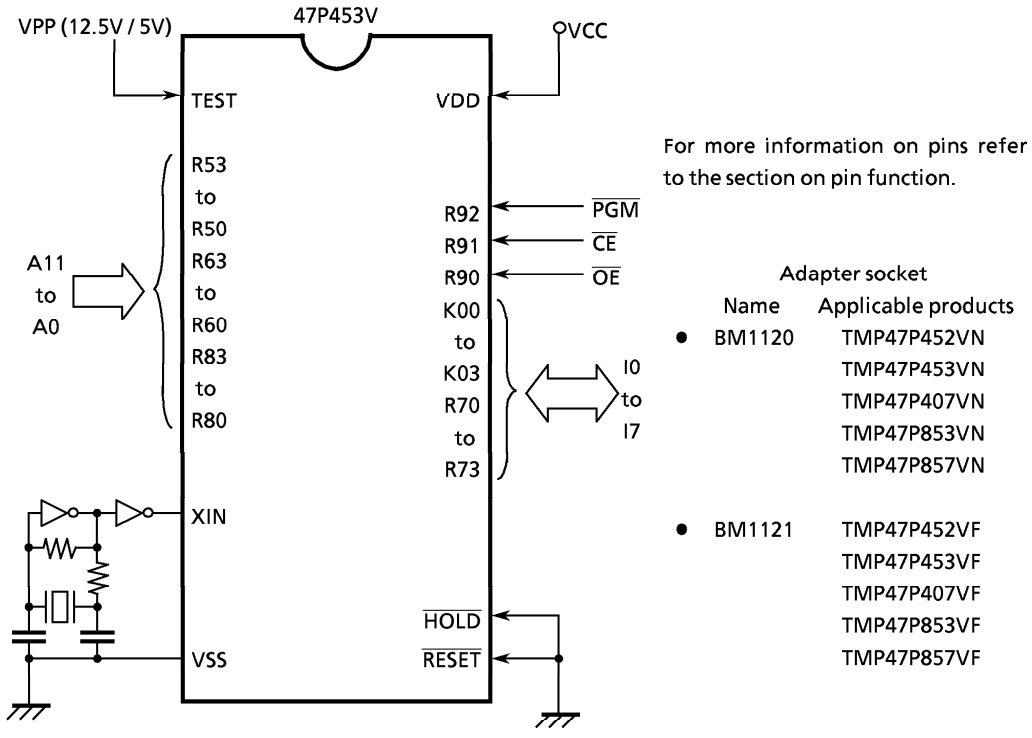
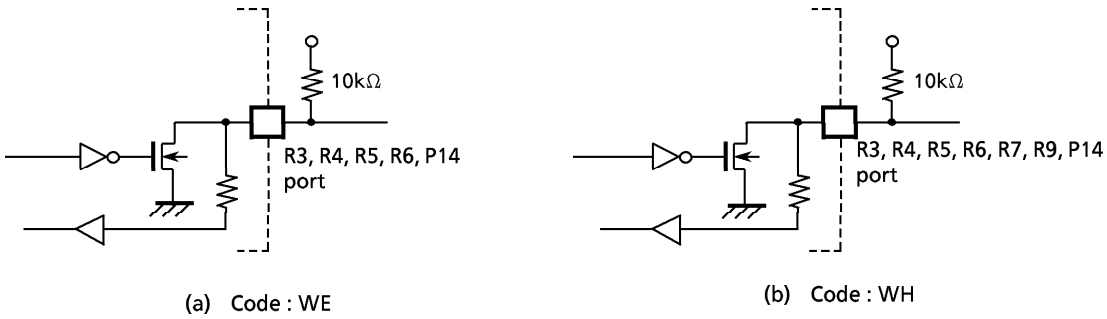


Figure 1-3. Setting for PROM mode

1.2.1 Writing

Set the PROM writer ROM to TMM2764AD (64k-bit), or equivalent. Before writing to a 47P453V (32k-bit), set the data area for writing to 32k-bits (start address: 0000_H, ending address: $0FFF_H$), or else load the same data to the first 32k bits (0000_H-$0FFF_H$) and the second 32k bits (1000_H-$1FFF_H$).



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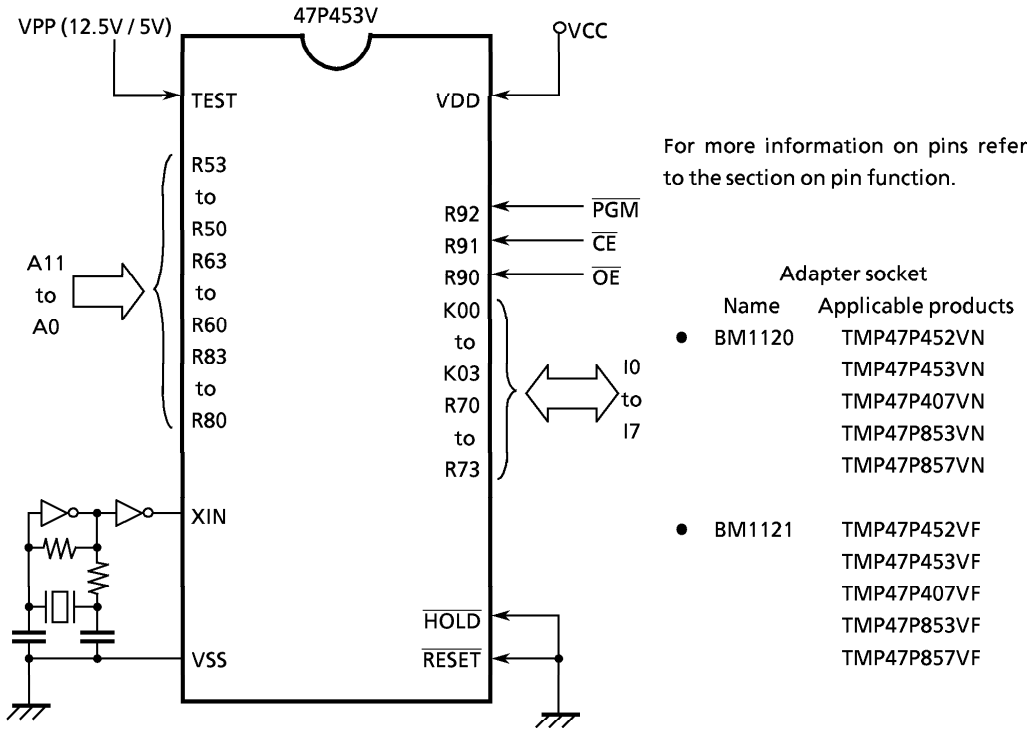

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1.2.2 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp terminal with Vcc = 6V and $\overline{PGM} = V_{IH4}$. The programming is achieved by applying a Single TTL low level 1 ms, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

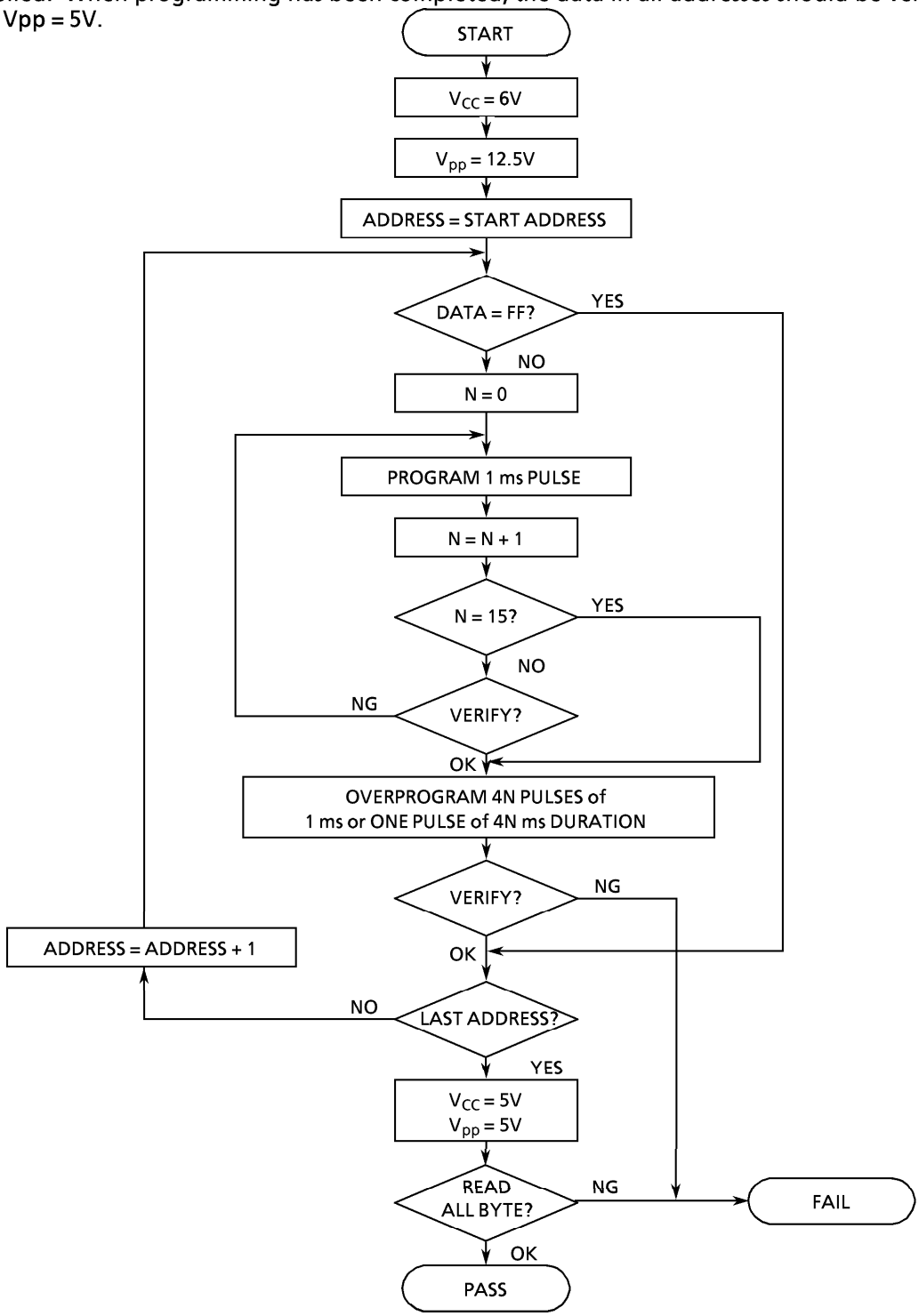


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST/VPP pin	– 0.3 to 14.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R7	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 60°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 60	°C

Note. Characteristic of R7 is different from 47C453A

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.2	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			960		kHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports P, R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Supply Current (in the Normal mode)	I_{DD}		Except TONE generating V_{DD} = 2.2V fc = 960kHz	—	0.3	0.5	mA
	I_{DDT}		TONE generating V_{DD} = 2.2 V fc = 960kHz	—	0.6	1.2	
Supply Current (in the HOLD mode)	I_{DDT}		V_{DD} = 5.5V	—	0.5	10	μA
			V_{DD} = 2.2V, Topr = 25°C	—	—	0.5	

Note 1. Typ.values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up / pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 2.0V / 0.2V
The K0 port is opened when the pull-up/pull-down resistor is contained.
The Voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

TONE OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10kΩ, V_{DD} = 2.2V	125	185	250	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL /ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

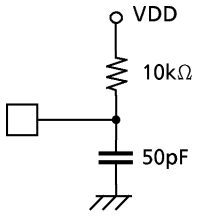
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

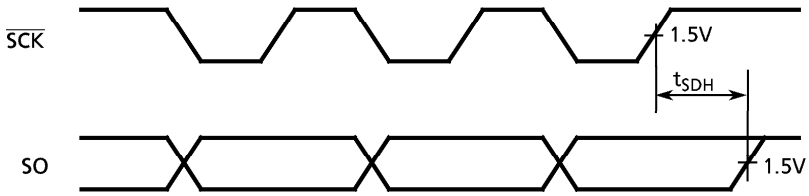
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		8.3			μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$-300	—	—	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmisson)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

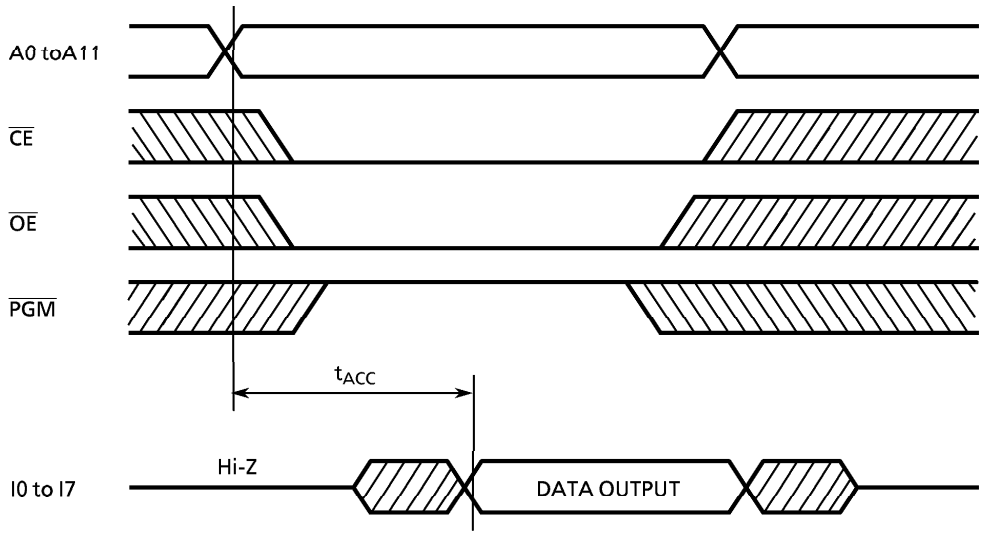
Recommended oscillating conditions of the 47P453V are equal to the 47C453A's.

D.C./A.C. CHARACTERISTICS

(V_{SS} = 0V)

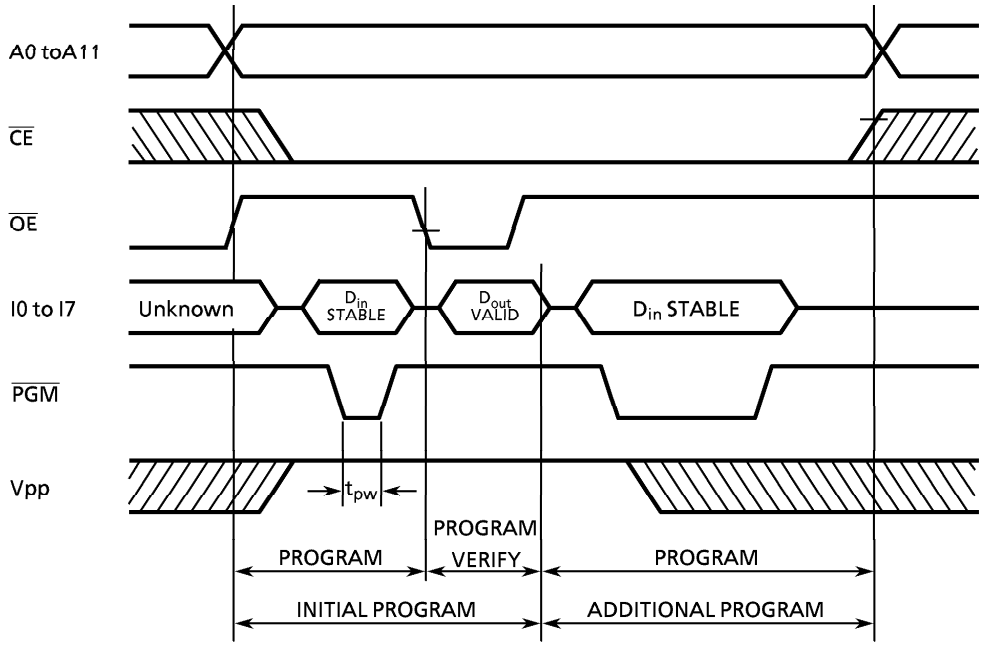
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.3	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	–	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms



TYPICAL CHARACTERISTICS