WM8608

5 to 7.1 Channel PWM Controller

DESCRIPTION

The WM8608 comprises a high performance multi-channel PWM digital power amplifier controller. Simply by adding appropriate power output stages a multi-channel power amplifier may be built. Six identical full audio bandwidth channels, plus a reduced bandwidth sub channel are provided as PWM outputs, to drive 6 speakers plus Sub.

The PCM to PWM converter supports up to 7.1 channels of audio, in PCM input formats. These may be mixed down to 6.1 or 5.1 outputs, by mixing rear channel data into centre rear or surround speakers if required. If 5.1 channel data is input, the surround data may be processed internally to create a pseudo 6.1 signal with rear channel output.

A Graphic Equaliser function is provided, plus selectable high frequency equalisation to suit different speaker types. Independent volume control for each channel is provided.

The WM8608 PWM controller is compatible with integrated switching output stages available from a number of vendors or alternatively may be used with a discrete output stage configuration and achieve similar levels of performance.

A Dynamic Peak Compressor with programmable attack and decay times is included, which allows headroom for tone control, bass management and extra digital gain to be provided, without clipping occurring.

A Synchroniser allows slaving to LRCLK, thus making the WM8608 independent of source MCLK frequency and jitter.

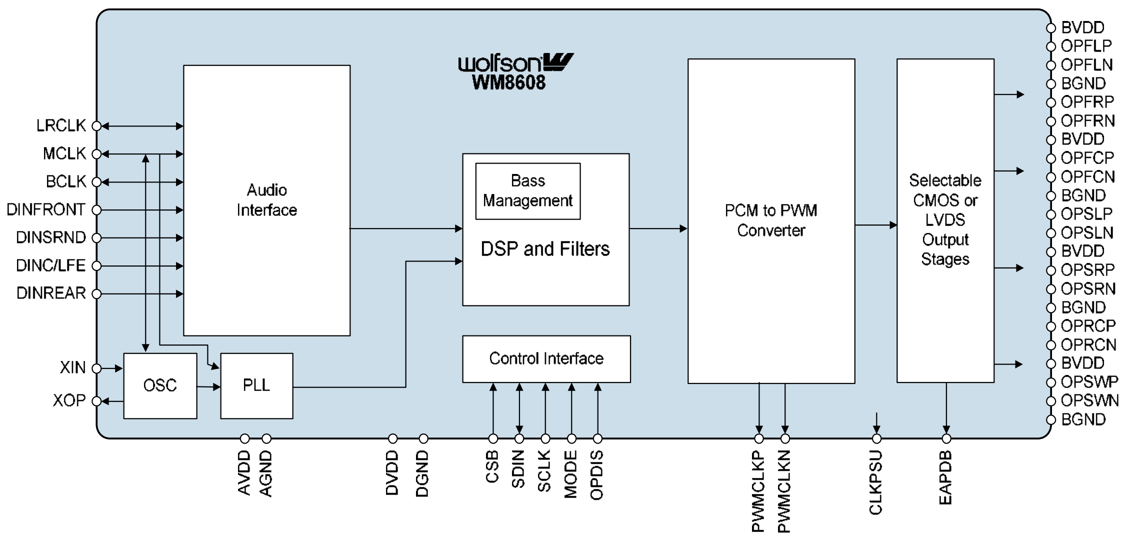
The device is controlled via a 2/3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mutes, de-emphasis and power management facilities. The device is supplied in a 48-pin TQFP package.

FEATURES

- Multi-channel PWM audio amplifier controller
- Supports Stereo, 5.1, 6.1 or 7.1 inputs
- Supports 2.1, 5.1 or 6.1 outputs with optional rear centre channel generation
- PWM Audio Performance with typical output stage
  - 100dB SNR ('A' weighted @ 48kHz)
  - 0.01% THD @ 1Watt
  - 0.1% THD @ 30Watt
- Integrated Bass Management support with adjustable filter
- Integrated 4-band Graphic Equaliser for 3 front channels
- Adjustable output stage filter compensation for different speakers
- Volume control on each 6.1 channel +24dB to -103.5dB in 0.5dB steps, with volume ramping and auto-mute functions
- Programmable Dynamic Peak Compressor avoids clipping even at high volume settings
- Internal PLL and optional crystal oscillator, supporting Audio and MPEG standards
- 2/3-Wire MPU Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- De-emphasis support for stereo
- Selectable CMOS or LVDS digital outputs

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio
- DVD receivers



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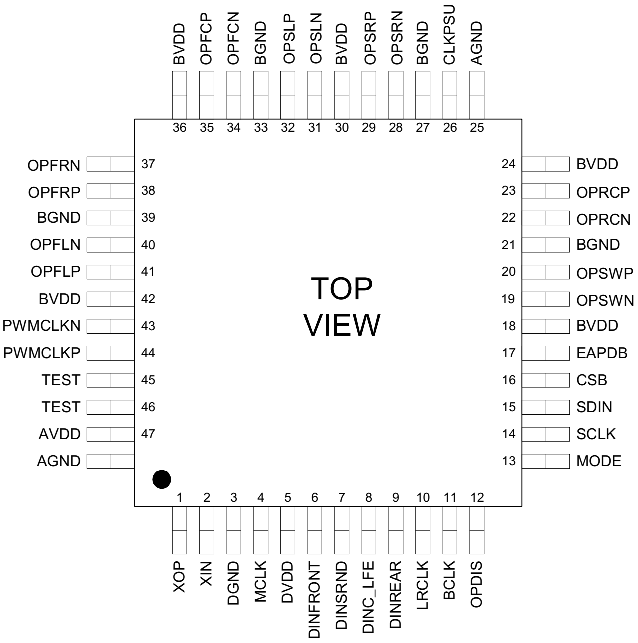
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP RANGE	PACKAGE	MOISTURE LEVEL SENSITIVITY
WM8608EFT/V	-25 to + 85°C	TQFP 48 7x7mm	MSL2
WM8608SEFT/V	-25 to + 85°C	TQFP 48 7x7mm (lead free)	MSL2
WM8608EFT/RV	-25 to + 85°C	TQFP 48 7x7mm (tape and reel)	MSL2
WM8608SEFT/RV	-25 to + 85°C	TQFP 48 7x7mm (lead free, tape and reel)	MSL2

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	XOP	Digital Output	Crystal oscillator output connection
2	XIN	Digital Input	Crystal oscillator input connection (may be left unconnected in slave mode)
3	DGND	Supply	Digital negative supply
4	MCLK	Digital Input/Output	Master clock; 256, 384, 512 fs (fs = word clock frequency) or 27MHz
5	DVDD	Supply	Digital positive supply
6	DINFRONT	Digital Input	Front channel data input
7	DINSRND	Digital Input	Surround channel data input
8	DINC_LFE	Digital Input	Centre and surround channel data input
9	DINREAR	Digital Input	Rear channel data for 6.1 and 7.1 inputs
10	LRCLK	Digital Input/Output	Left/right word clock
11	BCLK	Digital IO	Audio interface bit clock
12	OPDIS	Digital Input p.d.	Output disable
13	MODE	Digital Input p.d.	2/3 Wire control interface mode
14	SCLK	Digital Input	Serial interface clock
15	SDIN	Digital Input/Output	Serial interface data
16	CSB	Digital Input	Serial interface load signal
17	EAPDB	Digital Output	External output stage power down
18	BVDD	Supply	PWM output buffer positive supply
19	OPSWN	Digital Output	PWM output negative Subwoofer channel
20	OPSWP	Digital Output	PWM output positive Subwoofer channel
21	BGND	Supply	PWM output buffer ground supply
22	OPRCN	Digital Output	PWM output negative Rear centre (left) channel
23	OPRCP	Digital Output	PWM output positive Rear centre (left) channel
24	BVDD	Supply	PWM output buffer positive supply
25	AGND	Supply	Analogue negative supply
26	CLKPSU	Digital Output	Clock for external PSU
27	BGND	Supply	PWM output buffer ground supply
28	OPSRN	Digital Output	PWM output negative Surround right channel
29	OPSRP	Digital Output	PWM output positive Surround right channel
30	BVDD	Supply	PWM output buffer positive supply
31	OPSLN	Digital Output	PWM output negative Surround left channel
32	OPSLP	Digital Output	PWM output positive Surround left channel
33	BGND	Supply	PWM output buffer ground supply
34	OPFCN	Digital Output	PWM output negative Front centre channel
35	OPFCP	Digital Output	PWM output positive Front centre channel
36	BVDD	Supply	PWM output buffer positive supply
37	OPFRN	Digital Output	PWM output negative Front right channel
38	OPFRP	Digital Output	PWM output positive Front right channel
39	BGND	Supply	PWM output buffer ground supply
40	OPFLN	Digital Output	PWM output negative Front left channel
41	OPFLP	Digital Output	PWM output positive Front left channel
42	BVDD	Supply	PWM output buffer positive supply
43	PWMCLKN	Digital Output	PWM Clock negative
44	PWMCLKP	Digital Output	PWM Clock positive
45	NC	Not Connected	Do Not Connect
46	NC	Not Connected	Do Not Connect
47	AVDD	Analogue Supply	Analogue positive supply
48	AGND	Analogue Supply	Analogue negative supply

Notes: Digital input pins have Schmitt trigger input buffers. Pins marked ‘p.u.’ or ‘p.d.’ have internal pull-up or pull down.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage (AVDD)	-0.3V	+5V
Digital supply voltage (DVDD)	-0.3V	+5V
PWM output buffer supply voltage (BVDD)	-0.3V	+5V
Voltage range inputs	DGND -0.3V	DVDD +0.3V
Master Clock Frequency	10MHz	50MHz
Operating temperature range, T_A	-20°C	+85°C
Storage temperature	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 seconds)		+183°C

Notes:

1. GND power supplies (i.e. AGND, DGND, and BGND) must always be within 0.3V of each other.
2. VDD power supplies (i.e. AVDD, DVDD, and BVDD) must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue supply range	AVDD		2.7		3.6	V
Digital supply range	DVDD		2.7		3.6	V
PWM output buffer supply	BVDD		2.7		3.6	V
Ground	AGND, DGND, BGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, BVDD, DVDD = 2.7 to 3.3V, AGND, DGND, BGND = 0V, T_A = -20 to +85^oC, fs = 44.1kHz/48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capacitance	C_i			3	4	pF
Input leakage	I_{leak}			±0.1	±0.5	µA
Oscillator						
Input XIN LOW level	VX_{IL}		0		0.44	V
Input XIN HIGH level	VX_{IH}		0.77		AVDD	V
Input XIN capacitance	C_{XI}			4	5	pF
Input XIN leakage	IX_{leak}		0.10	0.11	0.13	mA
Output XOP LOW	VX_{OL}	15pF load capacitors	0.1	0.4	0.5	V
Output XOP HIGH	VX_{OH}	15pF load capacitors	1.2	1.3	1.4	V
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Pull-up/pull-down resistance			100	200	400	kΩ
Output LOW	V_{OL}	I_{OL}=+1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OL}=-1mA	0.9 x DVDD			V
Digital Logic Levels (LVDS Levels)						
Output differential voltage	V_{OD}		200	350	500	mV
Offset voltage	V_{OS}		0.95	1.25	1.4	V
Termination load	R_T	20pF load		100		Ω
PCM to PWM converter						
Digital SNR				105		dB
Typical SNR with output stage (A-weighted)				100		dB
Typical Dynamic Range with output stage				100		dB
Digital THD+N at 0dBfs				0.001		%
Typical THD+N at 30Watt with output stage				0.1		%
Typical THD+N at 1Watt with typical output stage				0.01		%
Typical IMD (CCIF – 19/20kHz)				-70		dBFS
Typical IMD (SMPTE – 60Hz/7kHz)				-70		dBFS
PWM buffer drive strength	I_{source}	CMOS	25			mA
	I_{sink}	20pF load	25			mA
	I_{source}	LVDS	2.1	3.4	5.4	mA
	I_{sink}	20pF,100Ω load	2.1	3.4	5.4	mA
PWM pulse repetition rate	f_{PWM}	fs = 44.1kHz		352.8		kHz
		fs = 48kHz		384		kHz

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz AES17 low pass filter, except where noted an A-weight filter is used. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. The XIN input supports both a clock as well as a crystal input.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied.
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the RMS values, of (Noise + Distortion)/Signal.

POWER CONSUMPTION

MODE DESCRIPTION	TYPICAL SUPPLY CURRENTS [mA]				TOTAL POWER [mW]
	I_{AVDD}	I_{DVDD}	I_{BVDD}		
			CMOS	LVDS	
AVDD, DVDD, BVDD = 3.3V					
OFF	<0.01	<0.01	<0.01	<0.01	0.01
Standby (STDBY = 1 or OPDIS = 1)	TBD	TBD	TBD	TBD	
Mute	TBD	<0.01	<0.01	<0.01	<1
Stereo	TBD	TBD	TBD	TBD	
5.1	TBD	TBD	TBD	TBD	
6.1	TBD	TBD	TBD	TBD	
7.1	TBD	TBD	TBD	TBD	

Table 1 Supply Current Consumption

Notes:

1. T_A = +25^{o}C, Slave Mode, fs = 48kHz, MCLK = 12.288MHz (256fs), 24-bit data
2. All figures are quiescent, with no signal.

SIGNAL TIMING REQUIREMENTS

POWER SUPPLY

Test Conditions

AGND, DGND, BGDN = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Timing Information					
AVDD: rise time 10% to 90% AVDD	t_{AR}	0.2		50	ms
DVDD: rise time 10% to 90% DVDD	t_{DR}	0.2		50	ms
BVDD: rise time 10% to 90% BVDD	t_{BR}	0.2		50	ms

Table 2 Power Supply Timing Requirements

MASTER CLOCK TIMING

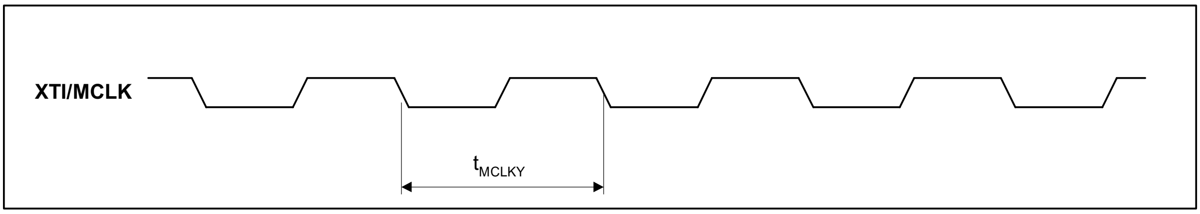


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGDN = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
XTI/MCLK System clock cycle time	t_{MCLKY}	20		100	ns
XTI/MCLK Duty cycle		40:60		60:40	%
XTI/MCLK Period Jitter				200	ps
XTI/MCLK Rise/Fall times				1	ns

Table 3 Master Clock Timing Requirements

AUDIO INTERFACE TIMING – MASTER MODE

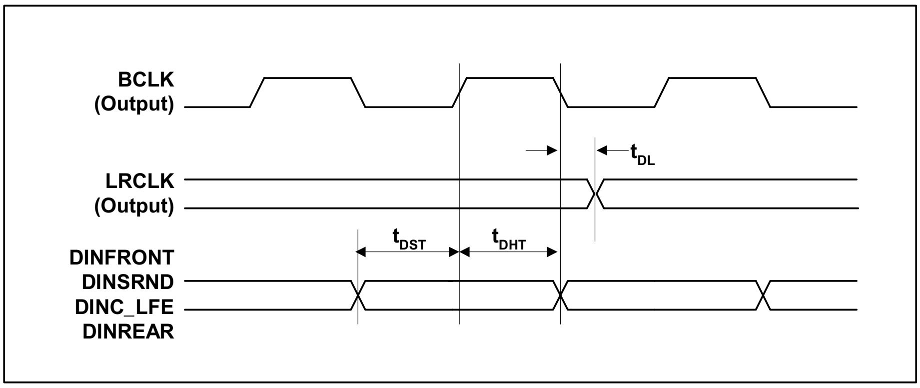


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGDN = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRCLK propagation delay from BCLK falling edge	t_{DL}			10	ns
DINFRONT, DINSRND, DINC_LFE and DINREAR setup time to BCLK rising edge	t_{DST}	10			ns
DINFRONT, DINSRND, DINC_LFE and DINREAR hold time from BCLK rising edge	t_{DHT}	10			ns

Table 4 Audio Interface Timing – Master Mode

AUDIO INTERFACE TIMING – SLAVE MODE

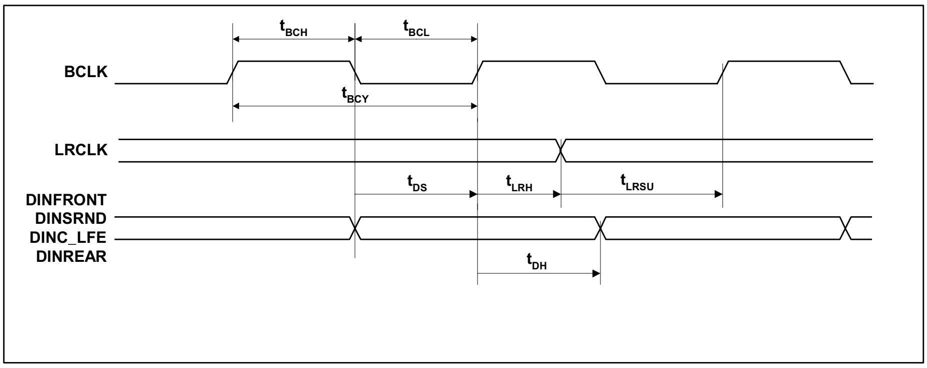


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGND = 0V, T_A = +25^{o}C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
BCLK rise/fall times				5	ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
LRCLK rise/fall times				5	ns
DINFRONT, DINSRND, DINC_LFE and DINREAR hold time from BCLK rising edge	t_{DH}	10			ns

Table 5 Audio Interface Timing – Slave Mode

Note: BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

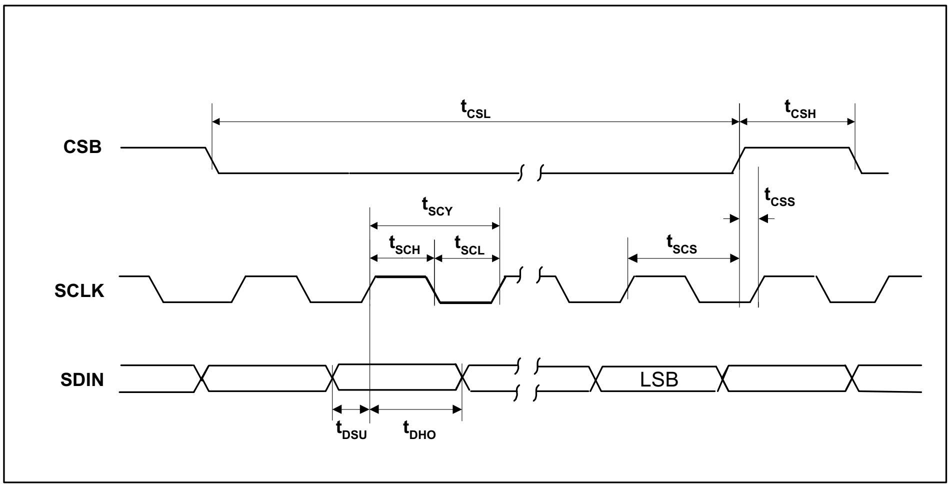


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	60			ns
SCLK pulse cycle time	t_{SCY}	80			ns
SCLK pulse width low	t_{SCL}	30			ns
SCLK pulse width high	t_{SCH}	30			ns
SDIN to SCLK set-up time	t_{DSU}	20			ns
SCLK to SDIN hold time	t_{DHO}	20			ns
CSB pulse width low	t_{CSL}	20			ns
CSB pulse width high	t_{CSH}	20			ns
CSB rising to SCLK rising	t_{CSS}	20			ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 6 Control Interface Timing – 3-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 2-WIRE MODE

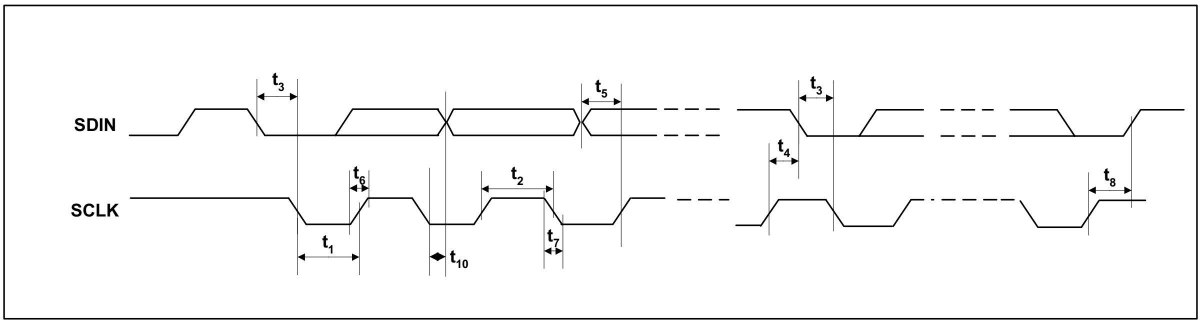


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	600			ns
SCLK High Pulse-Width	t_2	1.3			us
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 7 Control Interface Timing – 2-Wire Serial Control Mode

PWM OUTPUT TIMING

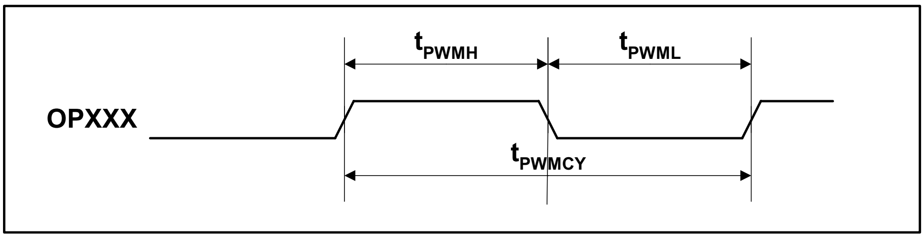


Figure 6 PWM Output Timing

Test Conditions

AVDD, DVDD, BVDD = 2.7 to 3.3V, AGND, DGND, BGND = 0V, T_A = -20 to +85°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL/NOTE	MIN	TYP	MAX	UNIT
Program Register Input Information					
PWM Frequency	t_{PWMCY}		384		kHz
PWM Low Pulse-Width	t_{PWML}	122			ns
PWM High Pulse-Width	t_{PWMH}	122			ns
LVDS Mode					
PWM Rise Time	20pF load	1.5	1.8	2.0	ns
PWM Fall Time	20pF load	1.7	2.0	2.2	ns
CMOS Mode					
PWM Rise Time	20pF load		1.5	2.3	ns
PWM Fall Time	20pF load		1.5	2.3	ns

Table 8 PWM Interface Timing

DEVICE DESCRIPTION

INTRODUCTION

The WM8608 is a high-performance multi-channel Pulse-Width Modulation (PWM) digital power amplifier controller. The device accepts up to 7.1 channels of audio in PCM input format, and outputs six PWM full-bandwidth channels, plus a PWM sub-woofer channel. The outputs are suitable for directly driving integrated switching output stages available from a number of vendors. The device is also compatible with discrete MOSFET output stages. In both cases, Wolfson Microelectronics offer Reference Designs for complete PWM digital power amplifiers, providing high-performance low-cost solutions ideal for Surround Sound AV Processors and DVD Receivers.

The WM8608 has a configurable input processor which accepts either Stereo, 5.1, 6.1 or 7.1 channels of PCM audio and outputs Stereo, 2.1, 5.1 or 6.1 outputs. This is done by mixing rear channel data into centre rear or surround output channels, as required. If 5.1 channel data is input, the surround data may be processed to create the rear-centre output.

The device has a Bass Management function, which has low-pass and high-pass filters for feeding the sub channel and main output channels. It also provides selectable boost for the LFE channel. Each channel can be configured to drive either “large” full-range speakers or “small” satellite speakers with limited bass capability.

A Tone Control function is provided, plus selectable high frequency equalisation to compensate for different loudspeaker characteristics. Independent volume control is provided for all channels, with comprehensive mute features.

A Dynamic Peak Compressor with programmable attack and decay times is included, which allows headroom for tone control, bass management and extra digital gain to be provided, without clipping occurring.

The device is controlled via a 2/3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mute, de-emphasis and power management facilities.

SIGNAL PATH

The WM8606 receives digital input data via an 8-channel digital audio interface. The data is processed in turn by the Input Processor, Bass Management and Equalisation, Volume Control and Dynamic Peak Compressors, Interpolation Filters, and PCM-PWM Converters, as shown in Figure 7. The PWM signals are output via selectable LVDS/CMOS drivers.

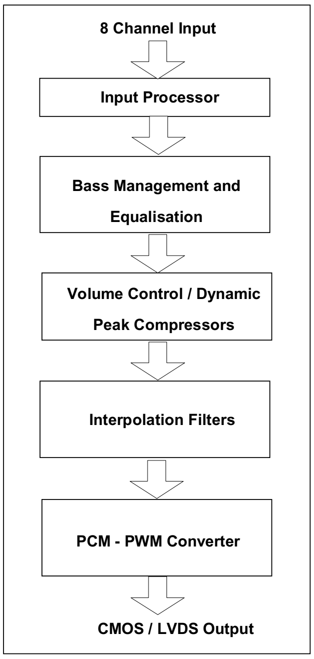


Figure 7 Signal Processing Block Diagram

Parameter	Group Delay	Unit	fs=48kHz	Unit
FL/FR/FC/SL/SR/RC channel	47	samples	1.0	ms
SUB channel	22	samples	0.5	ms

Table 9 Signal Path Group Delay

Key: FL = Front-Left, FR = Front-Right, FC = Front-Centre, SL = Surround-Left, SR = Surround-Right, RL = Surround-Left, RR = Surround-Right, RC = Surround-Centre, SUB = Subwoofer

Note: The shorter delay on the SUB channel will not significantly affect audio performance. (It is equivalent to moving the subwoofer forwards by about 15cm.)

DIGITAL AUDIO INTERFACE

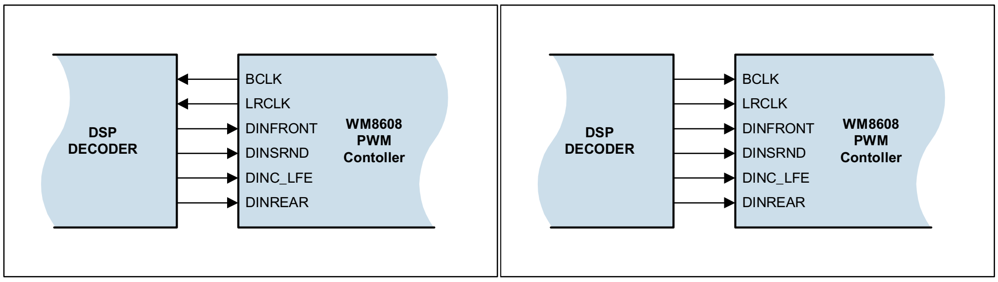
The digital audio interface is used for inputting audio data into the WM8608. It uses five pins:

- DINFRONT: Front L+R channel data input
- DINSRND: Surround L+R channel data input
- DINC_LFE: Front Centre (L) and LFE (R) channel data input
- DINREAR: Rear L+R channel data input
- LRCLK: Data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and LRCLK can be outputs when the WM8608 operates as a master, or inputs when it is a slave (see Master and Salve Mode Operation, below).

MASTER AND SLAVE MODE OPERATION

The WM8608 can be configured as either a master or slave mode device. As a master device the WM8608 generates BCLK and LRCLK and thus controls sequencing of the data transfer on the data channels. In slave mode, the WM8608 receives data and clock signals over the digital audio interface. The mode can be selected by writing to the MS bit (see Table 23). Master and slave modes are illustrated below.



Master Mode **Slave Mode**

Figure 8 Operation Mode

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK Audio data is applied to the internal filters via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP mode A
- DSP mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits. Except that 32 bit data is not supported in right justified mode. DINFRONT, DINSRND, DINC_LFE, DINREAR and LRCLK are sampled on the rising, or falling edge of BCLK.

In left justified, right justified and I^2S modes the digital audio interface receives data on the DINFRONT, DINSRND, DINC_LFE and DINREAR inputs. Audio Data for each stereo channel is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes, the minimum number of BCLKs per DACLRC period is 2 times the selected word length. LRCLK must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRCLK is acceptable provided the above requirements are met.

In DSP mode A or B, all channels are time multiplexed onto DINFRONT. LRCLK is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is 8 times the selected word length. Any mark to space ratio is acceptable on LRCLK provided the rising edge is correctly positioned (see Figure 9, Figure 10 and Figure 11).

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCLK following a LRCLK transition. LRCLK is high during the left samples and low during the right samples.

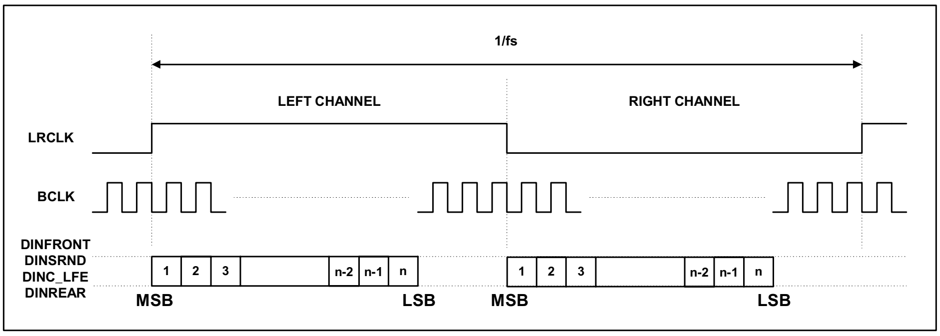


Figure 9 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCLK preceding a LRCLK transition. LRCLK is high during the left samples and low during the right samples.

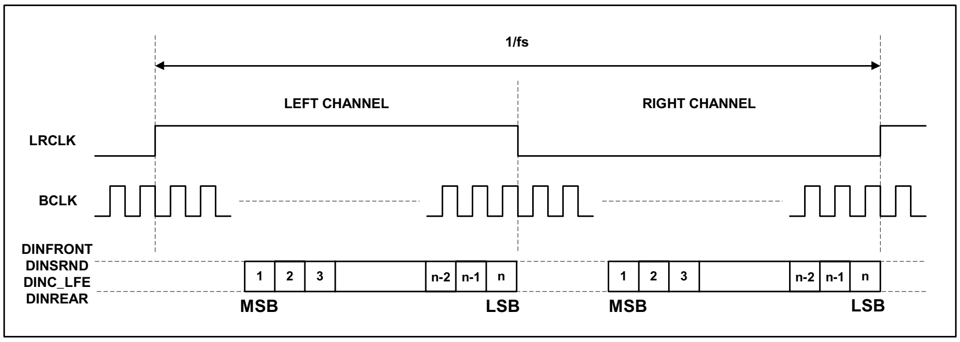


Figure 10 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCLK following a LRCLK transition. LRCLK is low during the left samples and high during the right samples.

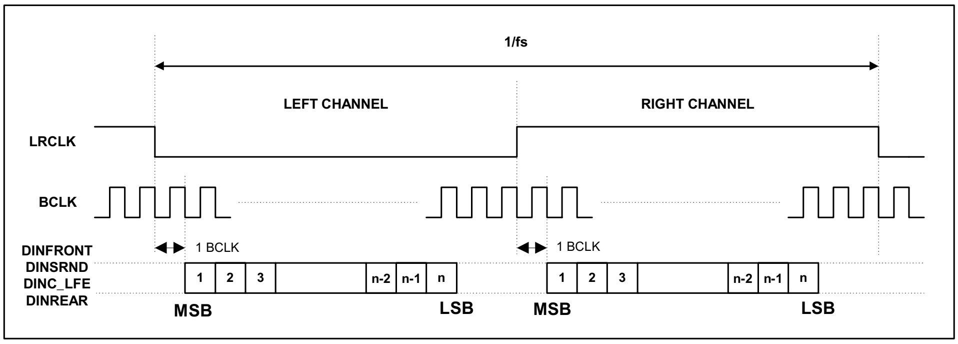


Figure 11 I²S Mode TIming Diagram

DSP MODE A AND B

In DSP mode, the Front Left (FL) channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

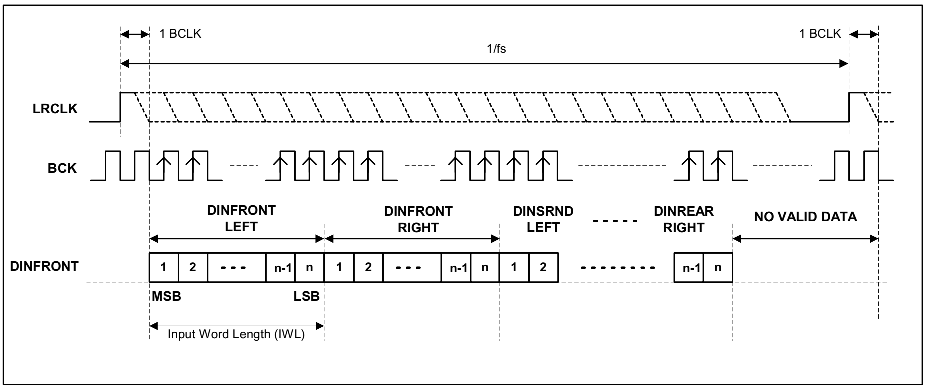


Figure 12 DSP Mode A Timing Diagram

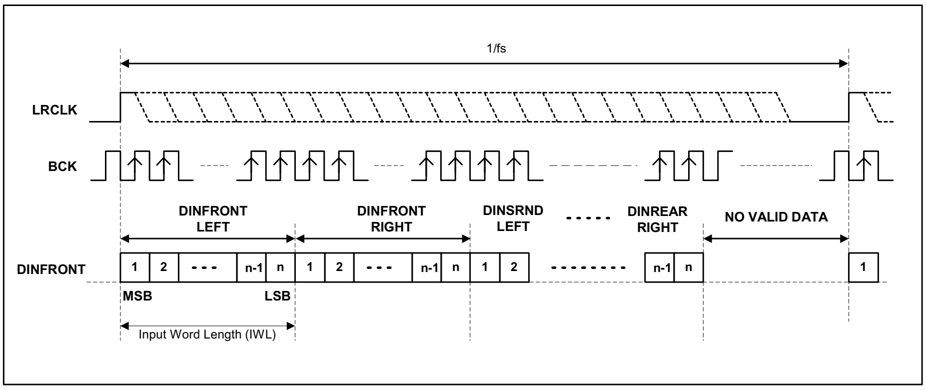


Figure 13 DSP Mode B Timing Diagram

In both DSP modes A and B, DINFRONT left is always sent first, followed immediately by data words for the other channels. No BCLK edges are allowed between the data words.

MODE	INPUT FORMAT (ORDER)	SUPPORTED MODES
Stereo	FL, FR	Restrictions apply for audio sample rates (fs) of 176.4 and 192kHz, e.g. fs = MCLK/192; maximal input word length = 24 bits, or fs = 192kHz, MCLK = 27 MHz; maximal input word length = 16 bits (see also Table 14).
5.1	FL, FR, SL, SR, FC, LFE	
6.1	FL, FR, SL, SR, FC, LFE, RC	
7.1	FL, FR, SL, SR, FC, LFE, RL, RR	

Table 10 DSP Mode Input Format

Key: FL = Front-Left, FR = Front-Right, FC = Front-Centre, SL = Surround-Left, SR = Surround-Right, RL = Surround-Left, RR = Surround-Right, RC = Surround-Centre, LFE = Low Frequency Effects

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master/slave mode are summarised below. MS selects audio interface operation in master or slave mode. In Master mode BCLK and LRCLK are outputs and the frequency of LRCLK is set by the sample rate control bits SR[3:0]. In Slave mode BCLK and LRCLK are inputs (refer to Table 12 for sample rate control in this case).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Audio IF Format	8	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	7	MS	0	Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	6	LRSWAP	0	Left/Right channel swap 1 = swap left and right data in audio interface 0 = output left and right data as normal
	5	SUBSWP	0	Front Centre – LFE channel swap 1 = Front Centre right and LFE left 0 = Front Centre left and LFE right
	4	LRP	0	Right, left & I^2S modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity (as show in e.g. Figure 12)
				DSP Mode – A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)
	3:2	WL[1:0]	10	Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 11 Audio Data Format Control

Notes:

1. Right Justified mode does not support 32-bit data.
2. LRSWAP does not affect the polarity of SUBSWP, the left-right controlling of DINC_LFE is separate from the other channels.

MASTER CLOCK AND AUDIO SAMPLE RATES

The WM8608 supports a wide range of master clock frequencies on the MCLK pin, and can generate many commonly used audio sample rates directly from the master clock. (See Table 14 for details.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Clocking	0	CMAST	1	Master Clock Mode 0 = MCLK input 1 = XIN input
	1	MPEG	1	MPEG Mode 0 = see Table 14 1 = MCLK is 27MHz
	2	MEDGE	0	Master Clock Active Edge 0 = positive edge 1 = negative edge
	3	CLKDIV2	0	Master Clock Divide by 2 1 = MCLK is divided by 2 0 = MCLK is not divided

Table 12 Clocking and Sample Rate Control (1)

If the WM8608 is running in MPEG mode (i.e. f_{XIN} = 27MHz) the sample can be detected automatically if the SRDET bit is set. In this case, the SR bits do not need programming.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Sample Rate	3:0	SR [3:0]	0000	Sample Rate Control. Refer to Table 14.
	4	SRDET	1	Sample rate detect 1 = Enabled (in MPEG mode only) 0 = Disabled

Table 13 Clocking and Sample Rate Control (2)

The clocking of the WM8608 is controlled using the CLKDIV2 and SR control bits. Setting the CLKDIV2 bit divides MCLK by two internally. Each value of SR[3:0] selects one combination of MCLK division ratios and hence one combination of sample rates (see next page). Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes the sample rates change proportionally.

MCLK / XIN		AUDIO SAMPLE RATE		SR [3:0]
(MPEG = 0)				
CLKDIV2=0	CLKDIV2=1			
[MHz]	[MHz]	[kHz]		
12.288	24.576	32	(MCLK/384)	0001
		48	(MCLK/256)	0000
24.576	49.152	96	(MCLK/256)	0011
		192	(MCLK/128)	0010
11.2896	22.5792	44.1	(MCLK/256)	0100
22.5792	45.1584	88.2	(MCLK/256)	0111
		176.4	(MCLK/128)	0110
18.432	36.864	32	(MCLK/512)	1001
		48	(MCLK/384)	1000
36.864	not supported	96	(MCLK/384)	1011
		192	(MCLK/192)	1010
16.9344	33.8688	44.1	(MCLK/384)	1100
33.8688	not supported	88.2	(MCLK/384)	1111
		176.4	(MCLK/192)	1110
(MPEG = 1)				
27.000	not supported	32		0001
		44.1		0100
		48		0000
		88.2		0111
		96		0011
		176.4		0110
		192		0010

Table 14 Master Clock and Sample Rates

The following Figure 14, Figure 15, Figure 16 and Figure 17 illustrate the different Clocking and Audio IF modes.

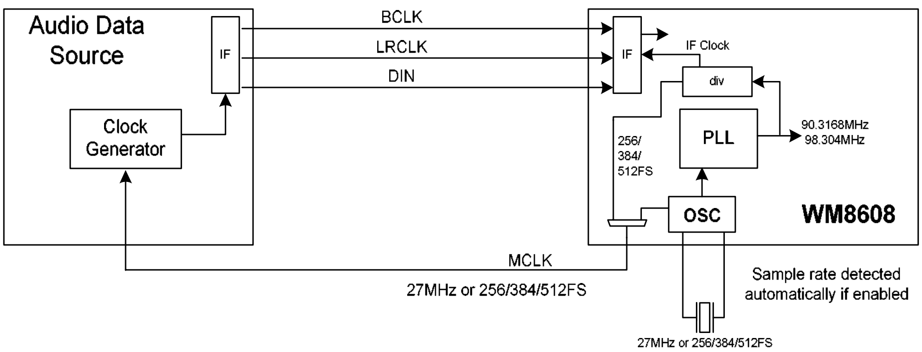


Figure 14 Clock and Audio IF: Clock Master / Audio IF Slave (default)

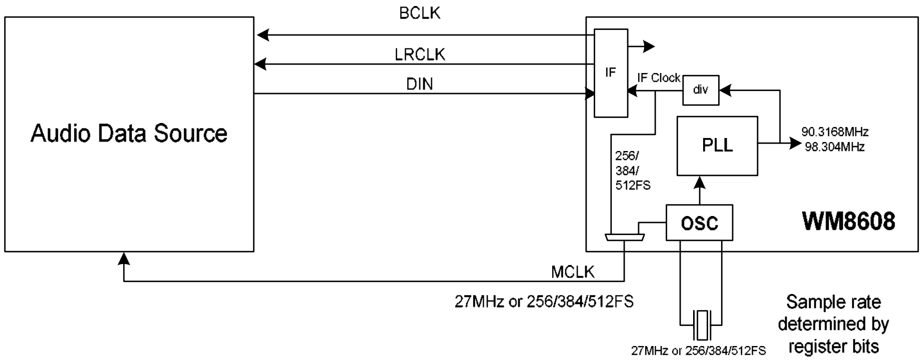


Figure 15 Clock and Audio IF: Clock Master / Audio IF Master

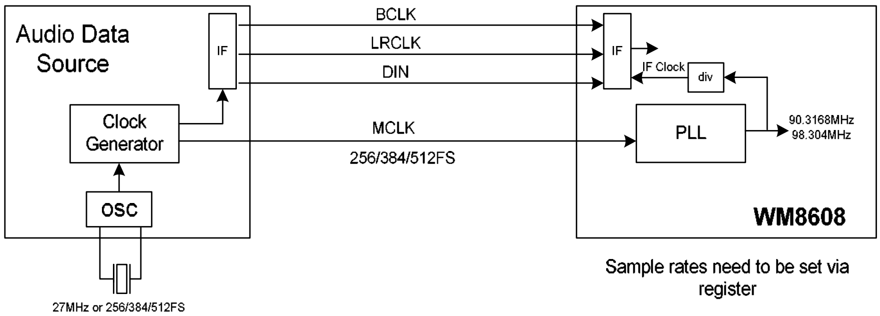


Figure 16 Clock and Audio IF: Clock Slave / Audio IF Slave

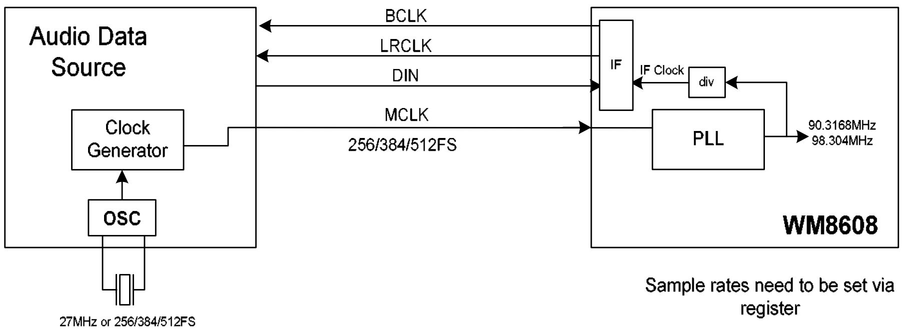


Figure 17 Clock and Audio IF: Clock Slave / Audio IF Master

SYNCHRONISER

The WM8608 contains a synchroniser circuit to support the synchronisation of an external LRCLK to the local LRCLK. This mode is only supported in MPEG mode.

The specification of the synchroniser circuit is:

Test Conditions

AVDD, DVDD, BVDD = 3.3V, AGND, DGND, BGND = 0V, T_A = +25°C, f_{XIN} = 27MHz, Slave Mode, fs = 48kHz, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Lock time	t_{lock}		<1	2	s
LRCLK frequency offset	$f_{offLRCLK}$		±1000	±10'000	ppm f_s
LRCLK drift in Lock	$drift_{LRCLK}$			0.2	ppm/s
				6	Hz

Table 15 Synchroniser Specification

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) Synchroniser (1)	0	SYNCEN	1	Synchroniser Enable 0: Disable 1: Enable (in MPEG mode only)
	2:1	GMIN[1:0]	10	Minimum Synchroniser Gain 00: minimum gain = 2^0 01: minimum gain = 2^1 10: minimum gain = 2^2 11: minimum gain = 2^3
	4:3	GMAX[1:0]	10	Maximum Synchroniser Gain 00: maximum gain = 2^8 01: maximum gain = 2^{10} 10: maximum gain = 2^{12} 11: maximum gain = 2^{14}
	5	HOLD	0	Hold Synchroniser (and SR detect) 1 : Synchroniser in hold mode

Table 16 Synchroniser (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 (21h) Synchroniser (2)	2:0	SYNTO[2:0]	100	Synchroniser Gain time-out 000: 0.2 ms 001: 0.5 ms 010: 1 ms 011: 2 ms 100: 5 ms (default) 101: 10 ms 110: 20 ms 111: 50 ms

Table 17 Synchroniser (2)

The next table illustrates recommendation for the Synchroniser loop gain G (see also Table 16) and time-out time (Table 17) with respect to the LRCLK frequency and the resulting Synchroniser lock time.

$F_{OFFLRCLK}$ [ppm]	G max	G min	GAIN TIME-OUT [ms]
±100	2^8	2^0	~1
±1000	2^{10}	2^0	~4
±10’000	2^{10}	2^0	~20

Table 18 Synchroniser Setup and Locking

Note: The Synchroniser requires a continuously running LRCLK. If that is not the case the HOLD signal has to be applied to avoid the synchronizer drifting.

CONTROL INTERFACE OPERATION

SELECTION OF CONTROL MODE

The WM8608 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are register bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin selects the interface format. An internal pull-down resistor configures the Control Interface to a default 2 wire format.

MODE	INTERFACE FORMAT
Low	2 wire (default)
High	3 wire

Table 19 Control Interface Mode Selection

The WM8606 Control Interface operates as a slave device only.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The WM8608 is controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is use to latch in the program data. The 3-wire interface protocol is shown in Figure 13.

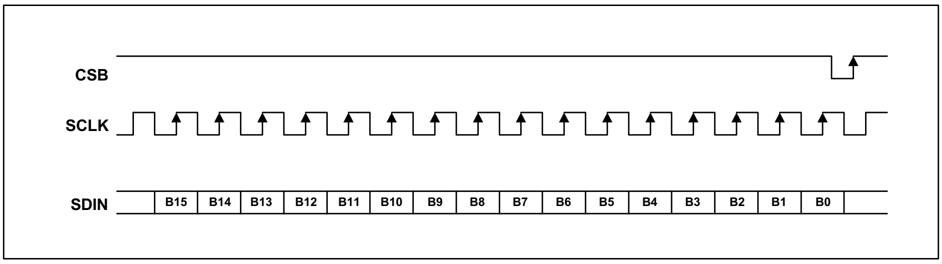


Figure 18 3-wire Serial Interface

The bits B[15:9] are Control Address Bits and the bits B[8:0] are Control Data Bits

2-WIRE SERIAL CONTROL MODE

The WM8608 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8608).

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8608 and the R/W bit is ‘0’, indicating a write, then the WM8608 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is ‘1’, the WM8608 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8608 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8608 register address plus the first bit of register data). The WM8608 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8608 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8608 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

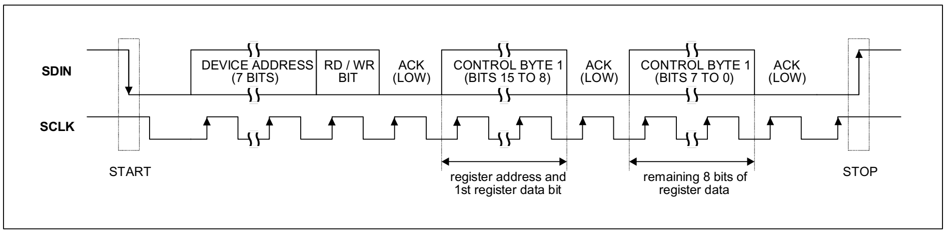


Figure 18 2-Wire Serial Control Interface

The WM8608 has two possible device addresses, which can be selected using the CSB pin.

CSB STATE	DEVICE ADDRESS
Low	0011010
High	0011011

Table 20 2-Wire MPU Interface Address Selection

INPUT PROCESSOR

The WM8608 supports the production of 2.1, 5.1 and 6.1 outputs from stereo, 5.1, 6.1 and 7.1 inputs according to Table 21 and Table 22.

INPUT CONFIGURATIONS								
CONFIG	**FL IN**	**FR IN**	**SL IN**	**SR IN**	**RL/RC IN**	**RR/RC IN**	**FC IN**	**LFE IN**
Stereo	●	●						
5.1	●	●	●	●			●	●
6.1	●	●	●	●	● or	●	●	●
7.1	●	●	●	●	●	●	●	●

Table 21 Input Configuration

The RC channel is accepted either in the RL or RR input, or alternatively in both RL and RR inputs. Register control bit RCCFG (Table 23) determines which option is used.

OUTPUT CONFIGURATIONS							
CONFIG	**FL OUT**	**FR OUT**	**SL OUT**	**SR OUT**	**FC OUT**	**RC OUT**	**SUB OUT**
Stereo	●	●					
2.1	●	●					●
5.1	●	●	●	●	●		●
6.1	●	●	●	●	●	●	●

Table 22 Output Configuration

By default the Subwoofer channel is directed to the SUB output, which is a lower bandwidth channel operating at half the PWM frequency of the other channels. Optionally, the subwoofer channel can be redirected to the RC channel at the full bandwidth.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Input/Output Configuration	1:0	IPCFG[1:0]	01	Input Configuration 00 = Stereo 01 = 5.1 10 = 6.1 11 = 7.1
	2	RCCFG	0	Rear-Centre Input Channel Configuration 0 = Rear-Centre input in Left channel 1 = Rear-Centre input in Right Channel (Only applicable when operating in 6.1 input mode.)
	4:3	OPCFG[1:0]	11	Output Configuration 00 = Stereo 01 = 2.1 10 = 5.1 11 = 6.1
	5	SUBCFG	0	Subwoofer Channel Configuration 0 = Subwoofer Output on SUB 1 = Subwoofer Output on RC (Only applicable when operating in 2.1 or 5.1 output mode.)

Table 23 Input and Output Configuration Register

A typical speaker configuration is illustrated in Figure 19.

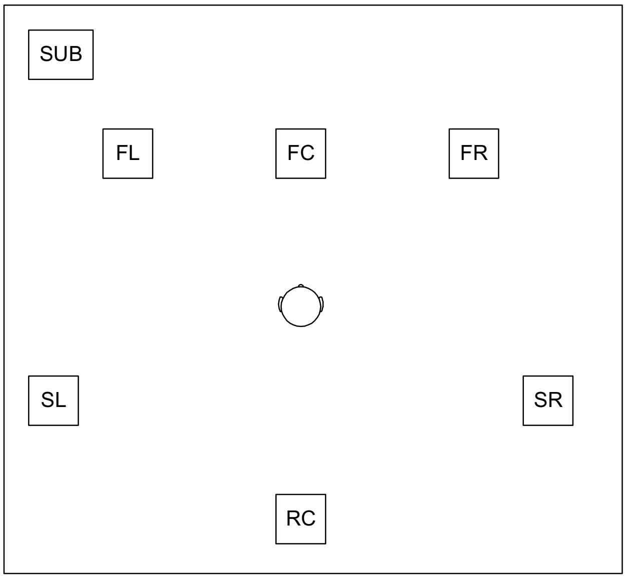


Figure 19 Loudspeaker Configuration for 6.1 Output

The WM8608 also supports Stereo input – Stereo output via the Bass Management filtering options, as discussed in **Bass Management** (page 28). In this case, the output configuration is set to 2.1.

Where there are a different number of input and output channels, the data is processed as follows. Refer to the section on **Bass Management** (page 28) for details on how the sub-channel is created.

STEREO INPUT – STEREO OUTPUT

The Front-Left and Front-Right inputs are passed to the Front-Left and Front-Right Outputs. All other channels are muted.

STEREO INPUT – 2.1 OUTPUT

The Front-Left and Front-Right inputs are passed to the Front-Left and Front-Right Outputs. The low-frequency contents of the Front inputs, may be optionally mixed and passed to the SUB output. The Surround, Front Centre and Rear Centre channel outputs are muted.

5.1 INPUT – 2.1 OUTPUT

Stereo mix-down is not supported. In this mode, the Front-Left and Front-Right inputs are passed to the Front-Left and Front-Right Outputs. The LFE and the low-frequency contents of the Front and Surround inputs, may be optionally mixed and passed to the SUB output. The Surround, Front Centre and Rear Centre channel outputs are muted.

5.1 INPUT – 6.1 OUTPUT

The Front and Surround channel inputs are passed to the Front and Surround channel outputs. The LFE and the low-frequency contents of the Front and Surround inputs optionally, may be mixed and passed to the SUB output. The RC OUT channel is obtained from the surround channels according to the equation:

RC OUT = (SL IN + SR IN)/2

5.1 INPUT – 5.1 OUTPUT

The Front and Surround channel inputs are passed to the Front and Surround channel outputs.

The LFE and the low-frequency contents of the Front and Surround inputs, may be optionally mixed and passed to the SUB output. The Rear-Centre channel is muted.

6.1 INPUT – 2.1 OUTPUT

Stereo mix-down is not supported. The Front-Left and Front-Right inputs are passed to the Front-Left and Front-Right Outputs. The LFE and the low-frequency contents of the Front, Surround and Rear-centre inputs are optionally mixed and passed to the SUB output. The Surround, Front Centre and Rear Centre channel outputs are muted.

6.1 INPUT – 5.1 OUTPUT

The Front channel inputs are passed to the Front channel outputs. The LFE and the low-frequency contents of the Front, Surround and Rear-centre inputs, may be optionally mixed and passed to the SUB output. The RC IN channel is mixed into the SL OUT and SR OUT output channels according to the equations:

SL OUT = (SL IN + RC IN)/2, SR OUT = (SR IN + RC IN)/2

The Rear-Centre output channel is muted.

6.1 INPUT –6.1 OUTPUT

The Front and Surround channel inputs are passed to the Front and Surround channel outputs. The LFE and the low-frequency contents of the Front, Surround and Rear-centre inputs, may be optionally mixed and passed to the SUB output. The RC OUT channel is obtained from either *RL IN* or *RR IN* (dependent on setting of register bit RCFG).

7.1 INPUT – 2.1 OUTPUT

Stereo mix-down is not supported. The Front-Left and Front-Right inputs are passed to the Front-Left and Front-Right outputs. The LFE and the low-frequency contents of the Front, Surround and Rear inputs, may be optionally mixed and passed to the SUB output. The Surround, Front Centre and Rear Centre channels are muted.

7.1 INPUT – 5.1 OUTPUT

The Front channel inputs are passed to the Front channel outputs. The LFE and the low-frequency contents of the Front, Surround and Rear inputs, may be optionally mixed and passed to the SUB output. The RL IN and RL OUT channels are mixed into the SL OUT and SR OUT channels according to the equations:

SL OUT = (SL IN + RL IN)/2, SR OUT = (SR IN + RR IN)/2

The Rear-Centre output channel is muted.

7.1 INPUT –6.1 OUTPUT

The Front and Surround channel inputs are passed to the Front and Surround channel outputs. The LFE and the low-frequency contents of the Front, Surround and Rear inputs, may be optionally mixed and passed to the SUB output. The RC OUT channel is obtained from:

(RL IN + RR IN)/2

BASS MANAGEMENT

The Bass-Management function filters and combines the input signals to produce a low-pass filtered output for the sub-woofer channel and high-pass filtered outputs for the remaining channels. The filters have selectable cut-off frequencies to match different types of sub-woofer and satellite speakers. The filters are designed so that the cut-off frequencies for the high-pass and low-pass filters remain constant irrespective of the sampling frequency used. 1st order filters are used for the low-pass and high-pass filters.

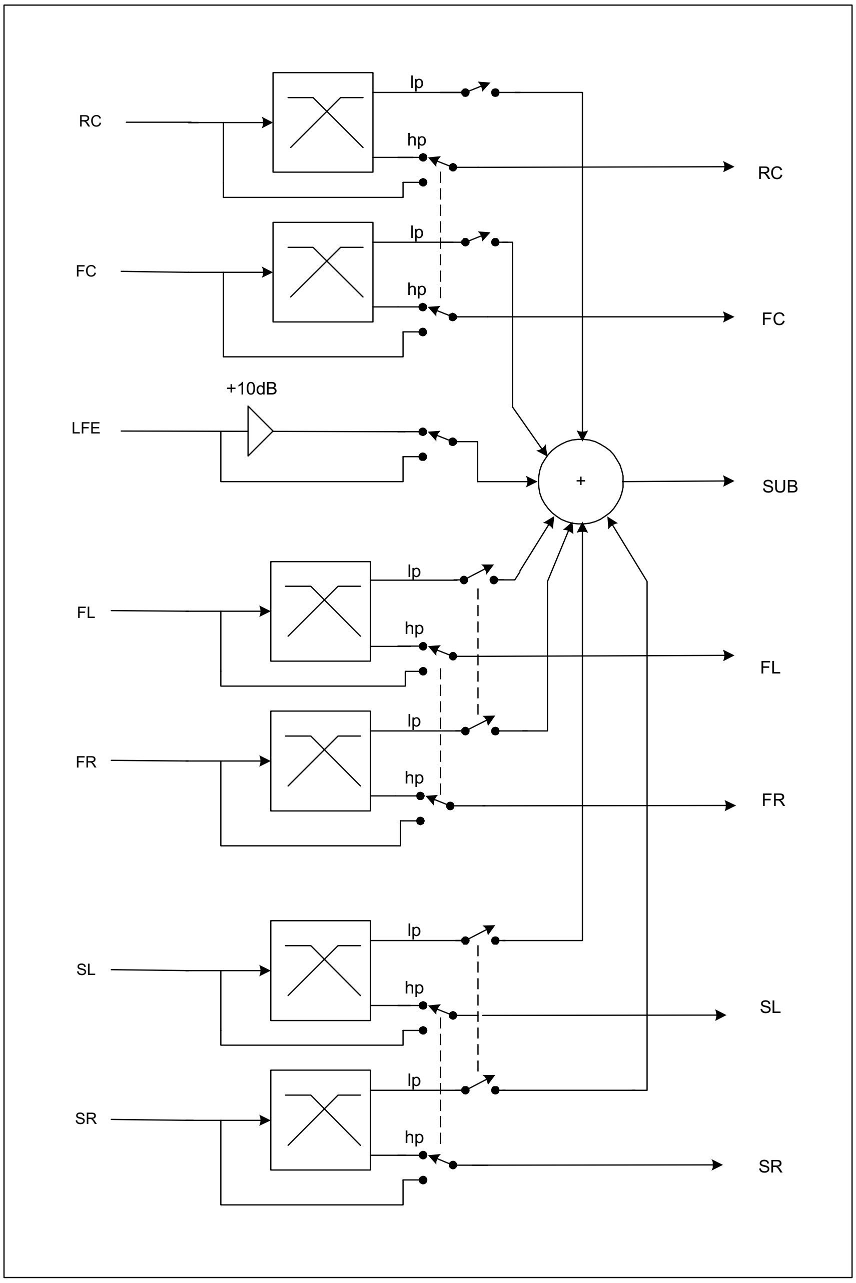


Figure 20 Bass Management

The high-pass filters pairs can be bypassed to allow full-range speakers to be used on any of the 3 main output channel pairs. The low-pass outputs from the Front channels can also be disabled to provide Stereo In – Stereo Out capability when full range front speakers are used.

The Bass-Management also provides a selectable LFE boost of 10dB via the LFEBOOST control bit. This is to compensate for the standard practise of recording the LFE channel 10dB down in the mix.

Additional gain-adjust is provided after this block (refer to page 32).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh) Bass Management Filter	1:0	LPHPCO[1:0]	01	Low-/High-Pass Cutoff Frequency (-3dB) 00 = 75Hz 01 = 100Hz 10 = 133Hz 11 = 178Hz
	2	LFEBOOST	0	LFE Boost Enable 0 = Boost Disabled 1 = 10dB Boost Enabled

Table 24 Bass Management Filter

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) Bass Management Filter Bypass	0	HPENF	1	Front High-Pass Filter 0 = High-Pass Filter bypassed 1 = High-Pass Filter enabled
	1	HPENS	1	Surround High-Pass Filter 0 = High-Pass Filter bypassed 1 = High-Pass Filter enabled
	2	HPENC	1	Front Centre and Rear Centre High-Pass Filter 0 = High-Pass Filter bypassed 1 = High-Pass Filter enabled
	3	LPENF	1	Front Low-Pass Filter Enable 0 = Low-Pass Filter output disabled 1 = Low-Pass Filter output enabled
	4	LPENS	1	Surround Low-Pass Filter Enable 0 = Low-Pass Filter output disabled 1 = Low-Pass Filter output enabled
	5	LPENC	1	Front Centre and Rear Centre Low-Pass Filter Enable 0 = Low-Pass Filter output disabled 1 = Low-Pass Filter output enabled

Table 25 Bass Management Filter Bypass

GRAPHIC EQUALISER

The WM8608 has a 4-band Graphic Equaliser on the front three channels. The three upper bands are controlled via registers (see Table 26, Table 27, Table 28 and Table 29). The lowest band is controlled via the subwoofer volume control (see VOLS in Table 32). The function has selectable cut-off frequencies which are independent of sample rate. The boost/cut for the upper three bands is controllable in 1.5dB steps from -6dB to +9dB via the EQB control bits.

The front-left and front-right controls are tied together, whilst the front-centre controls can be independently adjusted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh) EQ Band 1 Gain Control	3:0	EQ1GF [3:0]	1111 (Disabled)	Band 1 Front-Left/Front-Right Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable
	7:4	EQ1GFC [7:4]	1111 (Disabled)	Band 1 Front-Centre Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable

Table 26 EQ Band 1 Gain Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) EQ Band 2 Gain Control	3:0	EQ2GF [3:0]	1111 (Disabled)	Band 2 Front-Left/Front-Right Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable
	7:4	EQ2GFC [7:4]	1111 (Disabled)	Band 2 Front-Centre Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable

Table 27 EQ Band 2 Gain Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) EQ Band 3 Gain Control	3:0	EQ3GF [3:0]	1111 (Disabled)	Band 3 Front-Left/Front-Right Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable
	7:4	EQ3GFC [7:4]	1111 (Disabled)	Band 3 Front-Centre Gain 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable

Table 28 EQ Band 3 Gain Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) EQ Centre-Frequency Control	0	EQ1CF	1	Band 1 Front-Left/Front Right Centre-Frequency 0 = High Cutoff (500Hz) 1 = Low Cutoff (250Hz)
	1	EQ1CFC	1	Band 1 Front-Centre Centre-Frequency 0 = High Cutoff (500Hz) 1 = Low Cutoff (250Hz)
	2	EQ2CF	1	Band 2 Front-Left/Front Right Centre-Frequency 0 = High Cutoff (2kHz) 1 = Low Cutoff (1kHz)
	3	EQ2CFC	1	Band 2 Front-Centre Centre-Frequency 0 = High Cutoff (2kHz) 1 = Low Cutoff (1kHz)
	4	EQ3CF	1	Band 3 Front-Left/Front Right Cutoff Frequency 0 = High Cutoff (8kHz) 1 = Low Cutoff (4kHz)
	5	EQ3CFC	1	Band 3 Front-Centre Cutoff Frequency 0 = High Cutoff (8kHz) 1 = Low Cutoff (4kHz)

Table 29 EQ Frequency Control

Band 0 is controlled via the sub-woofer volume control register R11 as described in Table 32. The functionality to add/subtract the boost/cut setting to the sub-woofer volume must be written into the software controller for the chip.

The Band 0 Cutoff frequency can be changed using the corner frequency of the low-pass/high-pass filters as described in Table 24.

DIGITAL LOUDSPEAKER EQUALISER

A loudspeaker equaliser is provided for the front three channels to compensate for high-frequency variations that can occur when loudspeakers of different impedances are used with different output filters in typical output stages. The equaliser has selectable cut-off frequencies which are independent of sample rate. The gain at 20kHz is controllable in 0.5dB steps from -1.5dB to +2dB via the LSEQ control bit. The settings are applied to all three front channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 (13h) Loudspeaker Equaliser	0	LSCO	0	LSEQ Filter Characteristic 0 = High Cutoff (15kHz) 1 = Low Cutoff (10kHz)
	3:1	LSEQ [2:0]	100 (Disabled)	High Frequency Equalisation 000 = +2dB 001 = +1.5dB 010 = +1dB 011 = +0.5dB 100 = Disable 101 = -0.5dB 110 = -1dB 111 = -1.5dB

Table 30 Loudspeaker Equaliser

DIGITAL DEEMPHASIS

The digital 'de-emphasis' is used to equalize pre-emphasised digital CD recordings. De-emphasis filtering is available on the Front-Left and Front-Right channels only, for sample rates of 32kHz, 44.1kHz and 48kHz. The settings are applied to the two channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) De-emphasis	0	DEEMP	0	De-emphasis Control 0 = No De-emphasis 1 = De-emphasis enabled

Table 31 De-emphasis

Refer to Figure 31, Figure 32, Figure 33, Figure 34, Figure 35 and Figure 36 for details of the De-Emphasis modes at different sample rates.

Note: Using the De-emphasis filters for other sample rates as defined above will result in a frequency response error as shown in Figure 32, Figure 34 and Figure 36.

DIGITAL VOLUME CONTROL

The volume control allows the gain of each channel to be independently adjusted in 0.5dB steps from -103.5dB to +24dB. When the Dynamic Peak Compressor (see below) is enabled, gains of greater than 0dB can be applied without digital clipping occurring. The volume control has a digital zero-cross circuit which minimises clicks during changing the volume.

An update control bit is provided which allows the volume setting on each channel to be first stored in an intermediate latch, then afterwards applied simultaneously to all channels. If UPDATE=0, the Volume value will be written to the pre-latch but not applied to the relevant channel. If UPDATE=1, all pre-latched values will be applied from the next input sample. The value of UPDATE itself is not latched.

To prevent audible clicks, the volume control includes a ramp function which automatically ramps the volume in small steps between register updates. The ramp rate is 256dB/s ±5%.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Front-Left Volume	7:0	VOLFL[7:0]	10110001 (-15dB)	Front-Left Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	Volume Update 0 = Store FLVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains
R5 (05h) Front-Right Volume	7:0	VOLFR [7:0]	10110001 (-15dB)	Front-Right Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	Volume Update 0 = Store FRVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains
R6 (06h) Surround-Left Volume	7:0	VOLSL [7:0]	10110001 (-15dB)	Surround-Left Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	Volume Update 0 = Store SLVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Surround-Right Volume	7:0	VOLSR [7:0]	10110001 (-15dB)	Surround-Right Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	Volume Update 0 = Store SRVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains
R8 (08h) Front-Centre Volume	7:0	VOLFC [7:0]	10110001 (-15dB)	Front-Centre Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	UPDATE 0 = Store FCVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains
R9 (09h) Rear-Centre Volume	7:0	VOLRC [7:0]	10110001 (-15dB)	Rear-Centre Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	UPDATE 0 = Store RCVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains
R10 (0Ah) Subwoofer Volume	7:0	VOLS [7:0]	10110001 (-15dB)	Sub Volume in 0.5dB steps. Refer to Table 14
	8	UPDATE	0	UPDATE 0 = Store SVOL in intermediate latch (no gain change) 1 = Store and Update all channel gains

Table 32 Volume Control

VOLXX[7:0]	VOLUME LEVEL
00(hex)	-∞dB (mute)
01(hex)	-103dB
:	:
:	:
CF(hex)	0dB
:	:
:	:
FE(hex)	+23.5dB
FF(hex)	+24dB

Table 33 Volume Control Levels

DUAL VOLUME CONTROL

Setting the DVC register bit causes the volume settings to be applied in pairs. For example, the DVCF causes the Front-Left channel volume settings to be applied to both the Front-Left and Front-Right channels from the next audio input sample. No update to the VOL registers is required for DVC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Dual Volume Control	0	DVCF	0	Dual Volume Control – Front Channels: 0 : Use VOLFR setting for Front-Right channel 1: Apply VOLFL setting to Front-Right channel
	1	DVCS	0	Dual Volume Control – Surround Channels: 0 : Use VOLSR setting for Surround-Right channel 1: Apply VOLSL setting to Surround-Right channel
	2	DVCC	0	Dual Volume Control – Front Centre and Rear Centre Channels: 0 : Use VOLRC setting for Rear-Centre channel 1: Apply VOLFC setting to Rear-Centre channel

Table 34 Dual Volume Control

SOFT MUTE AND AUTO-MUTE

The WM8608 has a Soft Mute function set by the SMUTE control bit. Figure 21 shows the application and release of SMUTE while a full amplitude sinusoid is being played at 48kHz sampling rate. When SMUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards zero with a time constant of approximately 64 input samples. When SMUTE is turned off, the output will restart almost immediately from the current input sample.

This function is disabled by default.

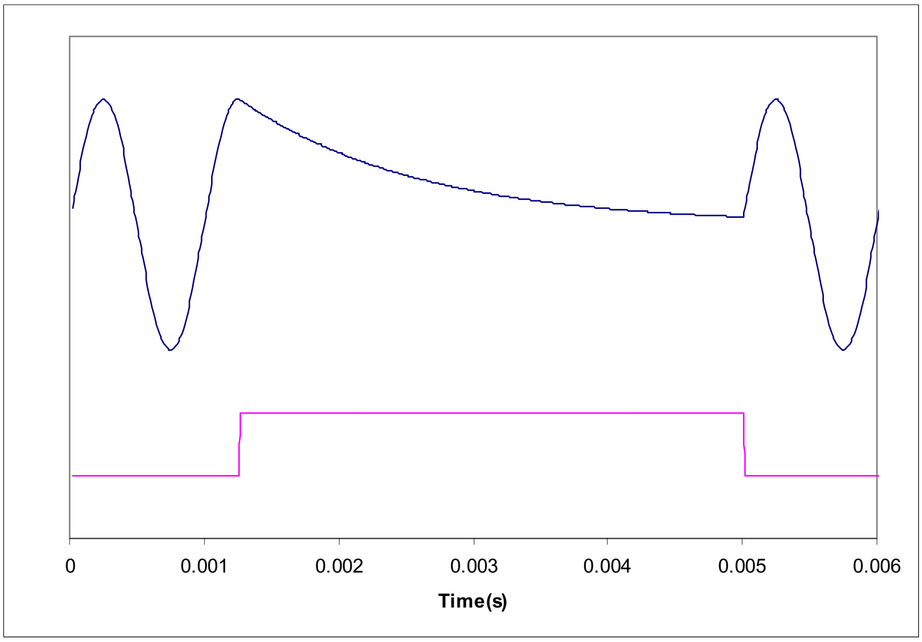


Figure 21 Application and Release of Soft Mute

An auto-mute function is provided which automatically mutes the output stage when a digital silence period is detected. Digital silence is defined as a consecutive period of 1024 zero input samples at the output of the volume control. Auto-mute will be removed as soon as the channel receives any non-zero input.

The auto-mute operates independently across all channel pairs, and can be enabled or disabled on individual channel pairs.

The mute features maximize the SNR of the PWM amplifier system. Soft-mute will only maximize the SNR of channel pairs that have auto-mute enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) Mute	0	SMUTE	0	Digital Soft Mute 0 = disable (signal active) 1= enable
	1	AMUTEF	1	Front Auto-mute 0 = disable 1 = enable
	2	AMUTES	1	Surround Auto-mute 0 = disable 1 = enable
	3	AMUTEC	1	Front Centre and Rear Centre Auto-mute 0 = disable 1 = enable
	4	AMUTESB	1	Subwoofer Auto-mute 0 = disable 1 = enable

Table 35 Mute

DYNAMIC PEAK COMPRESSOR

The WM8608 includes a Dynamic Peak Compressor for each channel, which prevents the occurrence of digital clipping when gains in excess of 0dB are applied. The compressor automatically adjusts the signal amplitude to allow headroom for the LFE boost, sub-woofer mixing, tone controls, loudspeaker equalisation and digital volume control. The compressor has a programmable limit threshold, programmable attack and decay time-constants, a frequency-dependent decay mode, and built-in zero-cross detect. The compressor can be configured either to operate independently on all channels (DUAL MONO), or on linked channel-pairs (STEREO), e.g. Table 36. The following channels are paired together: Front-Left and Front-Right, Surround-Left and Surround-Right, Front-Centre and Rear-Centre.

COMPRESSOR THRESHOLD

The compressor has a digital peak detector which tracks the maximum input signal level at the output of the volume control. With reference to Figure 22, if this signal is below the threshold set by control bit THRESH, the compressor operates transparently with no change to the signal level. However, if peak signal rises above the threshold, the gain through the compressor is modified so that the upper part of the curve is followed. This ensures that the output signal does not exceed 0dB.

ATTACK AND DECAY TIMES

The **attack time-constant** ATK controls how fast the gain is reduced when the signal goes above the threshold. It is defined as the time taken for the gain to reduce by 6dB. Normally a short attack time-constant is used to prevent the signal clipping when a high-amplitude transient occurs.

The **decay time-constant** DCY controls how fast the gain is increased when the signal begins to fall again. It is defined as the time taken for the gain to increase by 6dB. Normally, the decay time-constant is much longer than the attack time-constant, to prevent the input signal from entering repeated limiting cycles.

The **frequency-dependent decay** feature automatically detects the input frequency and sets the decay time to decay slower for low frequency signals. This reduces low-frequency signal distortion by preserving the waveform of each input cycle, whilst allowing the compressor to respond quickly to high frequency transients. This feature is enabled via the FDEP control bit.

ZERO-CROSS

The Dynamic Peak Compressor has a zero cross detector to prevent gain changes introducing clicks in the signal. The ZC is controlled by the same register RXX used in the volume control.

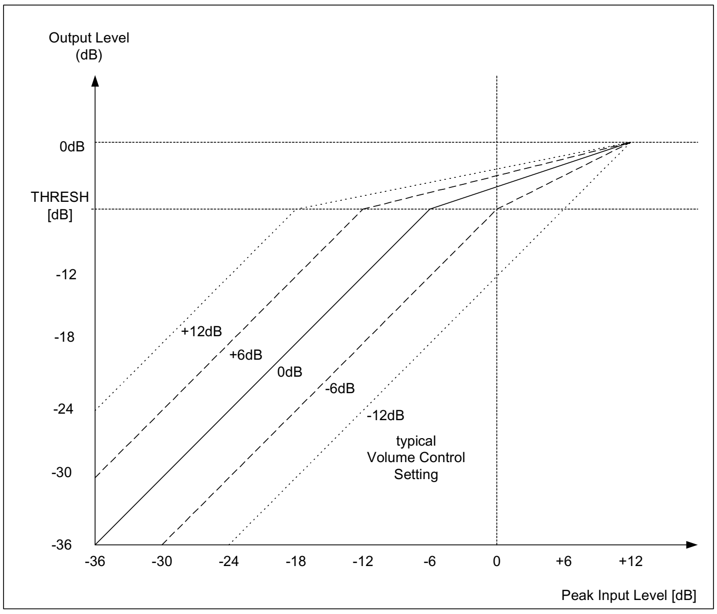


Figure 22 Dynamic Peak Compressor Characteristics

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Front, Surround, Front Centre and Rear Centre Channel Dynamic Peak Compressor	0	PLENF	1	Front Channel Compressor Enable 0 = disable 1 = enable
	1	PLENS	1	Surround Channel Compressor Enable 0 = disable 1 = enable
	2	PLENC	1	Front Centre and Rear Centre Channel Compressor Enable 0 = disable 1 = enable
	3	DUALF	0	Front Channel Peak Compressor Operation Mode 0: Dual-Mono 1: Stereo
	4	DUALS	0	Surround Channel Peak Compressor Operation Mode 0: Dual-Mono 1: Stereo
	5	DUALC	0	Centre Channel Peak Compressor Operation Mode 0: Dual-Mono 1: Stereo

Table 36 Front, Surround, Front Centre and Rear Centre Channel Dynamic Peak Compressor (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) Front, Surround, Front Centre and Rear Centre Channel Dynamic Peak Compressor	2:0	ATK[2:0]	010	Front, Surround, Front Centre and Rear Centre Channel Attack Rate 000 = 170µs 001 = 330µs 010 = 670µs 011 = 1.33ms 100 = 2.67ms 101 = 5.33ms 110 = 10.7ms 111 = 20.1ms
	5:3	DCY[2:0]	011	Front, Surround, Front Centre and Rear Centre Channel Decay Rate 000 = 340ms 001 = 680ms 010 = 1.36s 011 = 2.73s 100 = 5,46s 101, 110, 111 = 10.9s
	7:6	THRESH[1:0]	11	Front, Surround, Front Centre and Rear Centre Channel Compressor Thresholds 00 = -12dB 01 = -9dB 10 = -6dB 11 = -3dB
	8	FDEP	0	Frequency-dependent decay 0 = disable 1 = enable

Table 37 Front, Surround, Front Centre and Rear Centre Channel Dynamic Peak Compressor (2)

Note: The Dynamic Peak Compressors can be enabled independently for each channel pair (e.g. FL/FR, SL/SR). All channels use the same characteristics (e.g. Attack Rate).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Sub Channel Dynamic Peak Compressor	0	PLENSUB	1	Sub Channel Compressor Enable 0 = disable 1 = enable

Table 38 Subwoofer Channel Dynamic Peak Compressor (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Sub Channel Dynamic Peak Compressor	2:0	ATK[2:0]	010	Sub Channel Attack Rate 000 = 170µs 001 = 330µs 010 = 670µs 011 = 1.33ms 100 = 2.67ms 101 = 5.33ms 110 = 10.7ms 111 = 20.1ms
	5:3	DCY[2:0]	011	Sub Channel Decay Rate 000 = 340ms 001 = 680ms 010 = 1.36s 011 = 2.73s 100 = 5,46s 101, 110, 111 = 10.9s
	7:6	THRESH[1:0]	11	Sub Channel Compressor Thresholds 00 = -12dB 01 = -9dB 10 = -6dB 11 = -3dB
	8	FDEP	0	Frequency-dependent decay 0 = disable 1 = enable

Table 39 Subwoofer Channel Dynamic Peak Compressor (2)

ZERO-CROSS DETECT

The Dynamic Peak Compressor has a zero-cross detect which minimises clicks during gain changes. The zero-cross detect can be enabled/disabled in channel-pairs. The zero-cross has a timeout feature which ensures that the volume will change even if the input has a large DC offset. Once a new gain has been requested from the Dynamic Peak Compressor, the zero-cross detector will wait for a zero-cross for 25 to 50 ms before applying the gain change.

Note that the zero-cross settings programmed here also apply to the Dynamic Peak Compressor.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Volume Control Zero-Cross	0	ZCF	1	Zero-Cross Enable – Front Channels: 0 : Disable Zero-Cross 1: Enable Zero-Cross
	1	ZCS	1	Zero-Cross Enable – Surround Channels: 0 : Disable Zero-Cross 1: Enable Zero-Cross
	2	ZCC	1	Zero-Cross Enable – Front Centre and Rear Centre Channels: 0 : Disable Zero-Cross 1: Enable Zero-Cross
	3	ZCSUB	1	Zero-Cross Enable – Sub Channel: 0 : Disable Zero-Cross 1: Enable Zero-Cross
	4	ZCT	1	Zero Cross Timeout Enable: 0 : Disable Zero-Cross Timeout 1: Enable Zero-Cross Timeout

Table 40 Volume Control Zero-Cross

INTERPOLATION FILTERS

The WM8608 uses two types of interpolation filters, selected according to sampling frequency, as shown in Table 40.

SAMPLING FREQUENCY	FILTER TYPE	INTERPOLATION	
	Main Channels	Main Channels	SUB
32kHz	0	12x	6x
44.1kHz	0	8x	4x
48kHz	0	8x	4x
88.2kHz	0	4x	2x
96kHz	0	4x	2x
176.4kHz	1	2x	1x
192kHz	1	2x	1x

Table 41 Interpolation Filter Types

Note: If the Subwoofer channel is redirected into the Rear Centre (RC) channel the main channel characteristics apply.

FILTER TYPE 0

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter						
Passband		±0.05 dB			0.454	f_s
Stopband		-3dB		0.484		f_s
Passband ripple					±0.05	dB
Stopband Attenuation		f > 0.546fs	-60			dB
Group Delay			23			samples

Table 42 Digital Filter 0 Characteristics

FILTER TYPE 1

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter						
Passband					0.242	f_s
Stopband				0.723		f_s
Passband ripple					±0.05	dB
Stopband Attenuation			-60			dB
Group Delay			6			samples

Table 43 Digital Filter 1 Characteristics

PCM TO PWM CONVERTER

The PCM to PWM converter converters the Pulse-Code Modulated (PCM) signal into a highly linear Pulse-Width Modulated (PWM) signal. Table 44 defines the Pulse Repetition Frequency, (PRF), output clock rate (OBCLK) and minimum pulse width for each supported sampling frequency.

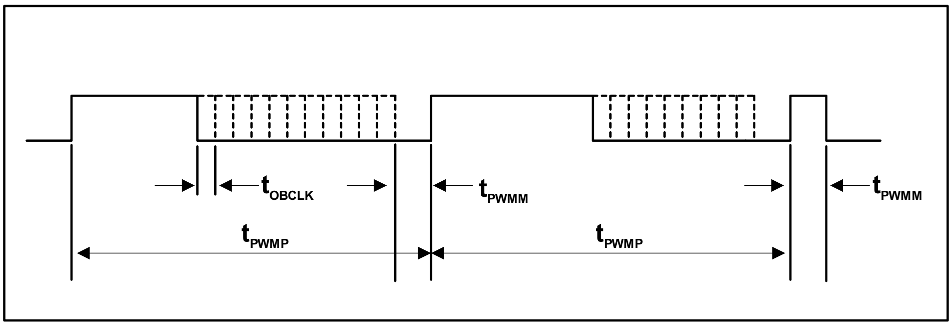


Figure 23 PCM to PWM Converter

The PRF Frequency (T_{PWMP}) of the Sub-woofer channel is half of the frequency defined in Table 44 in order to reduce power dissipation in the output stage.

SAMPLING FREQUENCY	PRF (1/T_{PWMP})		OUTPUT BITCLOCK FREQUENCY (1/T_{OBCLK})	MINIMUM PULSE WIDTH (T_{PWMM})
	Main Channel	SUB		
	[kHz]	[kHz]	[MHz]	[ns]
32kHz	384	192	98.304	122
44.1kHz	352.8	176.4	90.3168	133
48kHz	384	192	98.304	122
88.2kHz	352.8	176.4	90.3168	133
96kHz	384	192	98.304	122
176.4kHz	352.8	176.4	90.3168	133
192kHz	384	192	98.304	122

Table 44 Output Bitclock Frequency

Notes:

1. The correct Output Bitclock Frequency (T_{OBCLK}) is generated by the built-in PLL of the WM8608 device. The incoming clock must meet the jitter specification defined in Table 3.

OUTPUT PHASE

The Phase control word determines whether the output of each channel is non-inverted or inverted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R26 (1Ah) Output Phase	6:0	PH[6:0]	0000000	Bit	Channel	Phase
				0	FL	1 = invert
				1	FR	1 = invert
				2	SL	1 = invert
				3	SR	1 = invert
				4	FC	1 = invert
				5	RC	1 = invert
				6	SUB	1 = invert

Table 45 Phase

PWM OUTPUT CONFIGURATION

Two different PWM output formats are supported. These are:

- CMOS or LVDS
- Tri-state outputs to support power-down.

The PWM output format can be defined with the LVDS and PWMCFG setting defined in Table 46.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) PWM Output Configuration	0	LVDS	0	Output PAD configuration 0 = CMOS 1 = LVDS
	2:1	PWMCFG [1:0]	00	PWM Output State for LVDS=0 when output disabled or in standby mode: 01 = all PWM Outputs high 00 = all PWM Outputs low 10, 11 = high impedance For LVDS=1 when output disabled or in standby mode, the output state is high impedance.
	3	PWMPH	1	PWM Output Phase 0 = PWM outputs in phase 1 = PWM outputs phase shifted to each other
	7	PWMCLK	0	PWM Output Clock 0 = disabled 1 = enabled

Table 46 PWM Output Configuration

OUTPUT CONFIGURATION

If required the WM8608 device can be disabled in a system by setting the TRI bit as defined in Table 47. Setting the TRI bit will set all output pins of the device to high impedance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (1Ch) Output Configuration	0	TRI	0	Output Pins Mode 0 = Normal 1 = High Impedance

Table 47 Output Configuration

STANDBY, OUTPUT DISABLE AND RESET MODES

STANDBY

Setting the STDBY register bit selects a low power mode, and immediately configures the output to produce an output defined in Table 46 (PWMCFG). All trace of the previous input samples is removed, but all control register settings are preserved.

OUTPUT DISABLE (OPDIS) PIN AND REGISTER (OPDISR)

The OPDIS pin is provided to immediately shutdown the outputs, primarily for their protection. This is useful for short-circuit or thermal protection. The OPDIS pin can be configured in 2 modes:

- Synchronous
- Latched

In *synchronous* mode if OPDIS is high for longer than 100ns the outputs will be disabled. They will be enabled again at the end of a processing frame when OPDIS goes low for longer than 100ns.

In *latched* mode if OPDIS is high for longer than 100ns, the outputs will be disabled and will remain off until OPDIS is reset via the control interface and the end of a processing frame is reached (Table 49).

The output disable register (OPDISR) also allows the PWM outputs to be disabled via a register write. If OPDISR is set the PWM outputs will be disabled at the end of the next processing frame and enabled if OPDISR is reset at the end of the next processing frame.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) Power Down	0	STDBY	1	Standby select: 0 : Normal Mode 1: Standby Mode
	1	OPDISR	0	Output disable register 0: Normal mode 1: PWM output disabled
	2	MENA	1	OPDIS Mode 0 : Synchronous 1: Latched, reset via Control I/F

Table 48 Power Down

EXTERNAL APPLICATION POWER-DOWN (EAPDB) PIN

The state of the output pin EAPDB shows whether the device is disabled (i.e. OPDIS input pin active or STDBY register set).

EAPDB	STATE	DESCRIPTION
External Application Power Down	1	The device is operating correctly
	0 (default)	The outputs are disabled or the WM8608 device is in Standby (default) mode

Table 49 EAPDB Pin

RESET

The WM8608 device can be reset writing to the Reset register as defined in Table 50.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Reset	0	RLENA	0	Writing 1 to bit 0 of the register will reset OPDIS
	all	RESET	0	Writing all 1's to the register will reset the device and register settings

Table 50 Reset

Note: RESET or RLENA will be applied at the end of the register write and released at the beginning of the next register write. I.e. to reset the OPDIS register write 1 to bit 0 of the Reset register and them write 0 to bit 0.

EXTERNAL POWER SUPPLY CLOCK

The WM8608 device can generate a clock signal for an external PSU (Power Supply Unit) which is available at the CLKPSU pin.

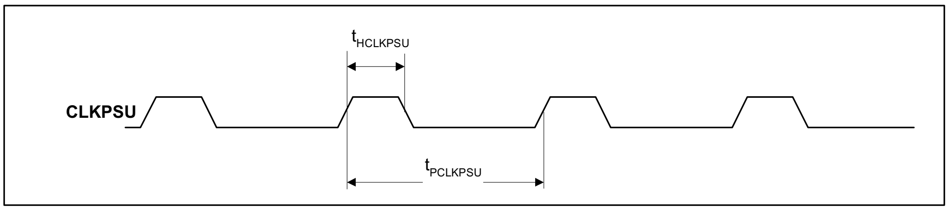


Figure 24 External Power Supply Clock

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) PSU	0	ENPSU	0	CLKPSU enable 1: enabled
	2:1	CLKPSU[1:0]	00	CLKPSU frequency 00: CLKPSU = f_{PRF} 01: CLKPSU = $f_{PRF}/2$ 10: CLKPSU = $f_{PRF}/4$ 11: CLKPSU = $f_{PRF}/6$
	4:3	DCYPSU[1:0]	00	CLKPSU duty cycle 00: $t_{hclkpsu}/t_{pclkpsu}$ = 0.5 (50%) 01: $t_{hclkpsu}/t_{pclkpsu}$ = 0.125 (12.5%) 10: $t_{hclkpsu}/t_{pclkpsu}$ = 0.0625 (6.25%) 11: $t_{hclkpsu}/t_{pclkpsu}$ = 0.03125 (3.125%)

Table 51 PSU Clock

Note: See Table 44 for specification of f_{PRF}.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. There are 32 registers with 9 bits per register. These can be controlled using the Control Interface.

REGISTER	ADDRESS	REMARKS	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT	PAGE REF
R0 (00h)	00_0000	Clocking	0	0	0	0	0	CLKDIV2	MEDGE	MPEG	CMAST	0_0000_0011	20
R1 (01h)	00_0001	Sample Rate	0	0	0	0	SRDET	SR				0_0001_0000	20
R2 (02h)	00_0010	Audio IF Format	BCLKINV	MS	LRSWAP	SUBSWP	LRP	WL		FORMAT		0_0000_1010	19
R3 (03h)	00_0011	Input/Output Configuration	0	0	0	SUBCFG	OPCFG		RCCFG	IPCFG		0_0001_1001	26
R4 (04h)	00_0100	Front-Left Volume	UPDATE	VOLFL (Front Left) Volume								0_1011_0001	32
R5 (05h)	00_0101	Front-Right Volume	UPDATE	VOLFR (Front Right) Volume								0_1011_0001	32
R6 (06h)	00_0110	Surround-Left Volume	UPDATE	VOLSL (Surround Left) Volume								0_1011_0001	32
R7 (07h)	00_0111	Surround-Right Volume	UPDATE	VOLSR (Surround Right) Volume								0_1011_0001	33
R8 (08h)	00_1000	Front-Centre Volume	UPDATE	VOLFC (Front Centre) Volume								0_1011_0001	33
R9 (09h)	00_1001	Rear-Centre Volume	UPDATE	VOLRC (Rear Centre) Volume								0_1011_0001	33
R10 (0Ah)	00_1010	Subwoofer Volume	UPDATE	VOLS (Subwoofer) Volume								0_1011_0001	33
R11 (0Bh)	00_1011	Dual Volume Control	0	0	0	0	0	0	DVCC	DVCS	DVCF	0_0000_0000	34
R12 (0Ch)	00_1100	Mute	0	0	0	0	AMUTESB	AMUTEC	AMUTES	AMUTEF	SMUTE	0_0001_1110	35
R13 (0Dh)	00_1101	Bass (1)	0	0	0	0	0	0	LFEBOOST	LPHPCO		0_0000_0001	29
R14 (0Eh)	00_1110	Bass (2)	0	0	0	LPENC	LPENS	LPENF	HPENC	HPENS	HPENF	0_0011_1111	29
R15 (0Fh)	00_1111	EQ Band 1 Gain Control	0	EQ1GFC				EQ1GF				0_1111_1111	30
R16 (10h)	01_0000	EQ Band 2 Gain Control	0	EQ2GFC				EQ2GF				0_1111_1111	30
R17 (11h)	01_0001	EQ Band 3 Gain Control	0	EQ3GFC				EQ3GF				0_1111_1111	30
R18 (12h)	01_0010	EQ Frequency Control	0	0	0	EQ3CFC	EQ3CF	EQ2CFC	EQ2CF	EQ1CFC	EQ1CF	0_0011_1111	31
R19(13h)	01_0011	Speaker Equaliser	0	0	0	0	0	LSEQ			LSCO	0_0000_1000	31
R20 (14h)	01_0100	Deemphasis	0	0	0	0	0	0	0	0	DEEMPH	0_0000_0000	32
R21 (15h)	01_0101	Peak Compressor F, S, C (1)	0	0	0	DUALC	DUALS	DUALF	PLENC	PLENS	PLENF	0_0000_0111	36
R22 (16h)	01_0110	Peak Compressor F, S, C, (2)	FDEP	THRESH		DCY			ATK			0_1101_1010	37
R23 (17h)	01_0111	Peak Compressor SUB (1)	0	0	0	0	0	0	0	0	PLENSUB	0_0000_0001	37
R24 (18h)	01_1000	Peak Compressor SUB (2)	FDEP	THRESH		DCY			ATK			0_1101_1010	38
R25 (19h)	01_1001	Zero Cross	0	0	0	0	ZCT	ZCSUB	ZCC	ZCS	ZCF	0_0001_1111	39
R26 (1Ah)	01_1010	Output phase	0	0	PH							0_0000_0000	41
R27 (1Bh)	01_1011	PWM Output Config	0	PWMCLK	0	0	0	PWMPH	PWMCFG		LVDS	0_0000_1000	41
R28 (1Ch)	01_1100	Output Config	0	0	0	0	0	0	0	0	TRI	0_0000_0000	41
R29 (1Dh)	01_1101	Power Down	0	0	0	0	0	0	MENA	OPDISR	STDBY	0_0000_0101	42
R30 (1Eh)	01_1110	Reset	0	0	0	0	0	0	0	0	RLENA	0_0000_0000	43
R31 (1Fh)	01_1111	PSU	0	0	0	0	DCYPSU		CLKPSU		ENPSU	0_0000_0000	43
R32 (20h)	10_0000	Synchroniser (1)	0	0	0	HOLD	GMAX		GMIN		SYNCEN	0_0001_0101	23
R33 (21h)	10_0001	Synchroniser (2)	0	0	0	0	0	0	SYNTO			0_0000_0100	23

Table 52 Register Map Description

DIGITAL FILTER CHARACTERISTICS

FILTER RESPONSES

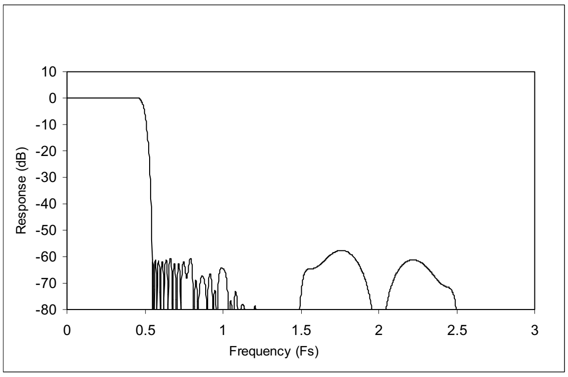


Figure 25 Digital Filter Frequency Response – 32KHz

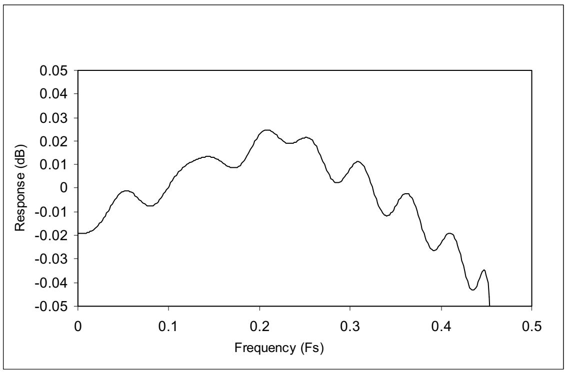


Figure 26 Digital Filter Ripple –32kHz

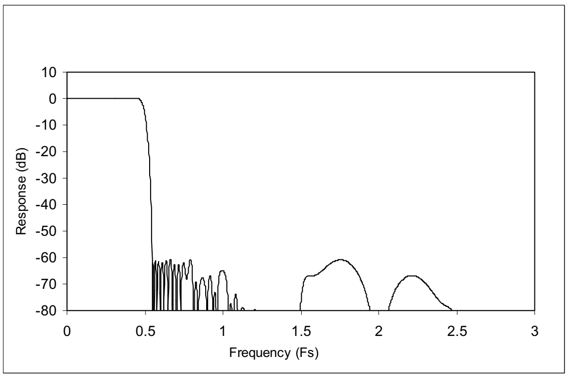


Figure 27 Digital Filter Frequency Response – 44.1, 48 and 96KHz

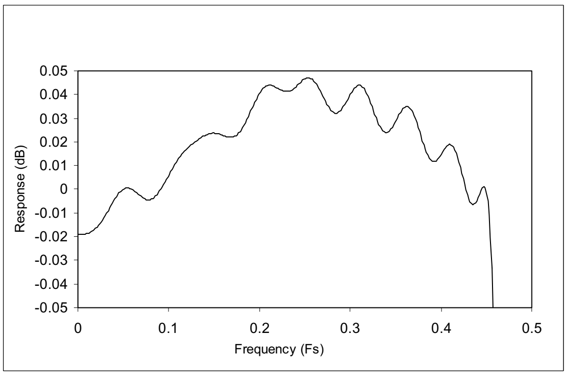


Figure 28 Digital Filter Ripple –44.1, 48 and 96kHz

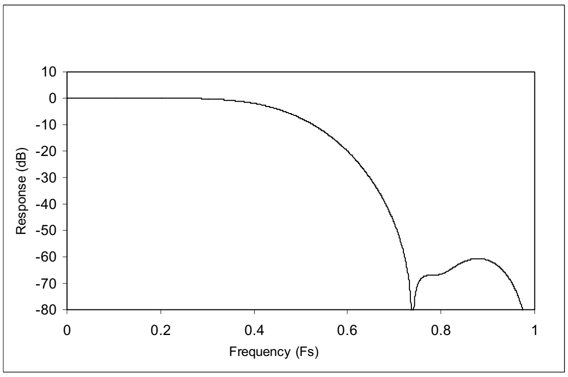


Figure 29 Digital Filter Frequency Response – 192KHz

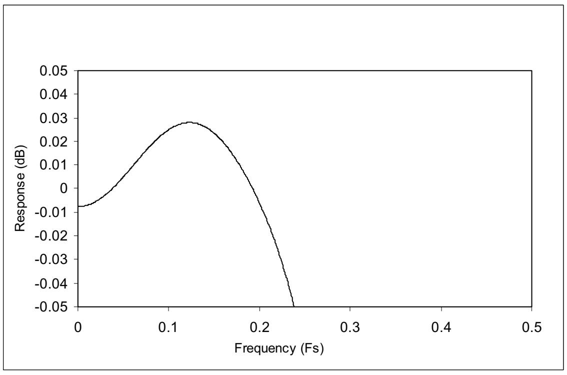


Figure 30 Digital filter Ripple – 192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

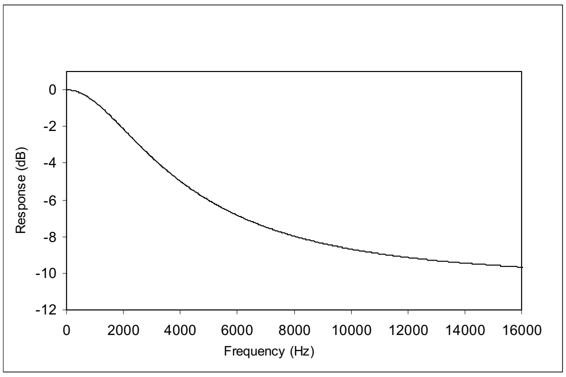


Figure 31 De-Emphasis Frequency Response (32kHz)

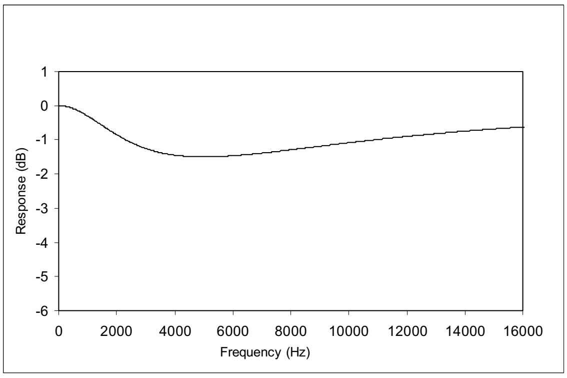


Figure 32 De-Emphasis Error (32KHz)

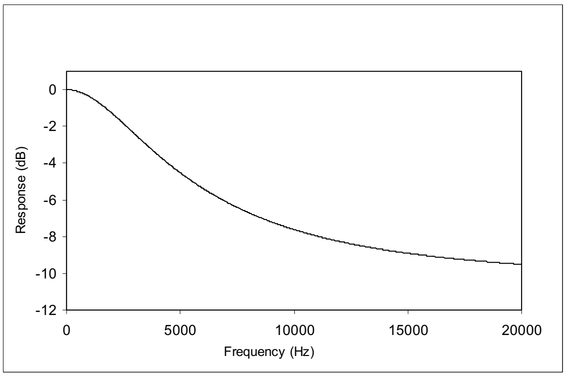


Figure 33 De-Emphasis Frequency Response (44.1KHz)

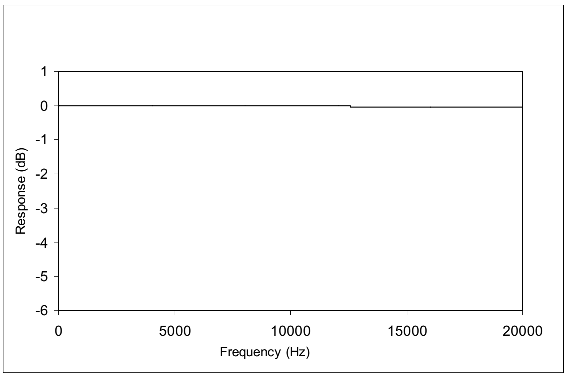


Figure 34 De-Emphasis Error (44.1KHz)

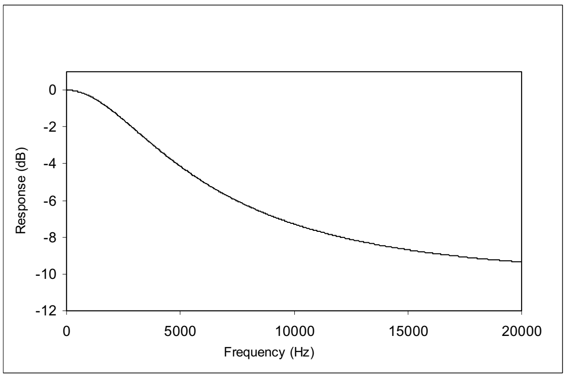


Figure 35 De-Emphasis Frequency Response (48kHz)

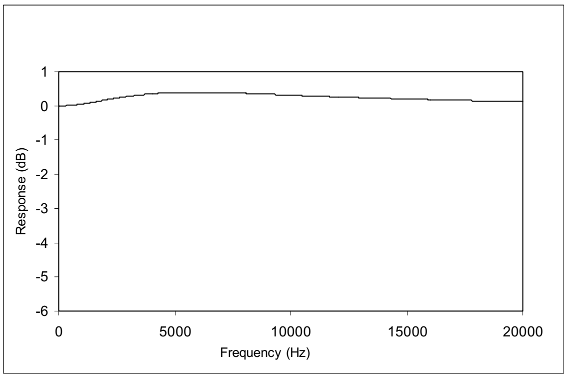


Figure 36 De-Emphasis Error (48kHz)

APPLICATION NOTES

START-UP

The WM8608 per default is switched off and the PWM output pins are static high, to protect any external circuit. When the device has been properly initialized and the output configuration has been defined then the device can safely be switched on. A typical start-up sequence is show in Figure 37.

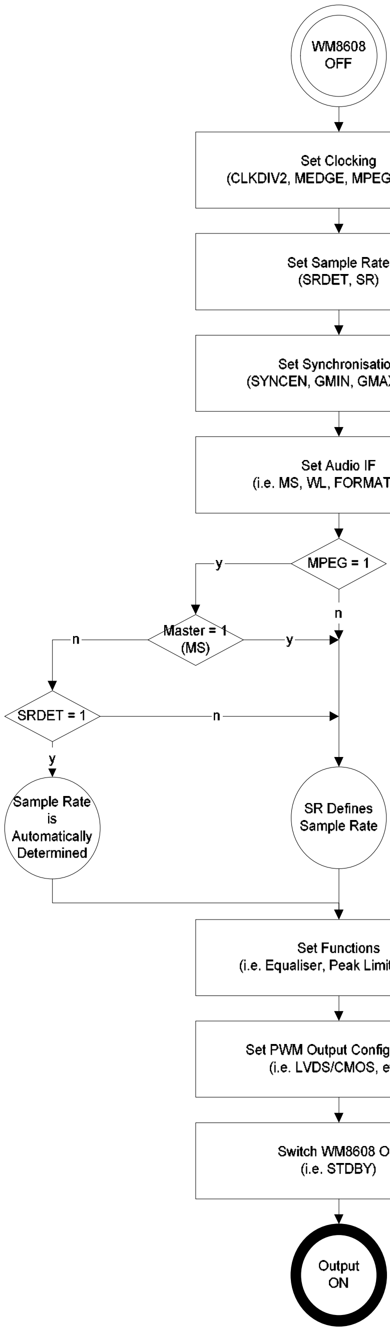


Figure 37 WM8608 Start-up

POWER SUPPLY CONNECTIONS

The WM8608 has got 3 individual power supplies. Figure 38 shows how these power supplies are connected and used on the chip and package.

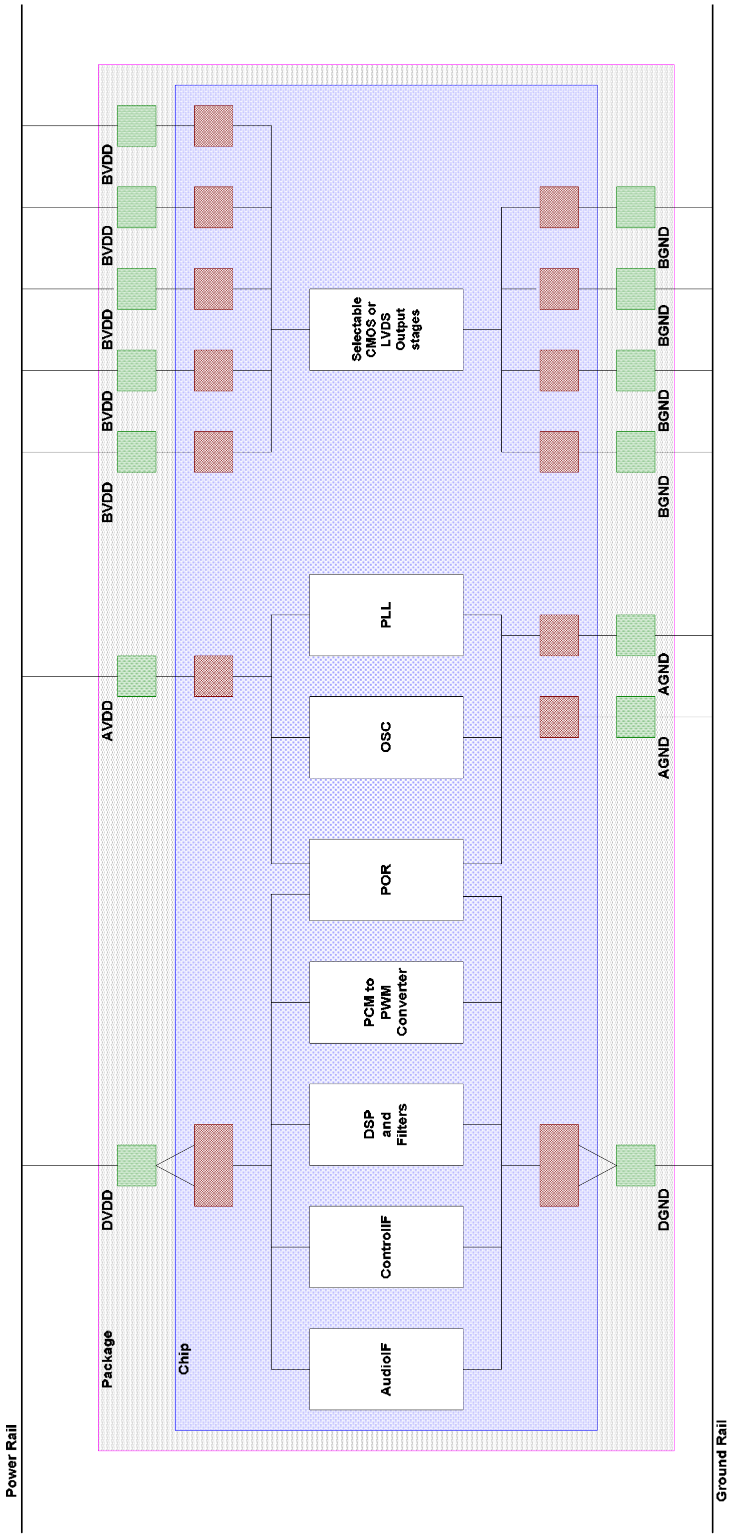


Figure 38 WM8608 Power Supply Connections

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

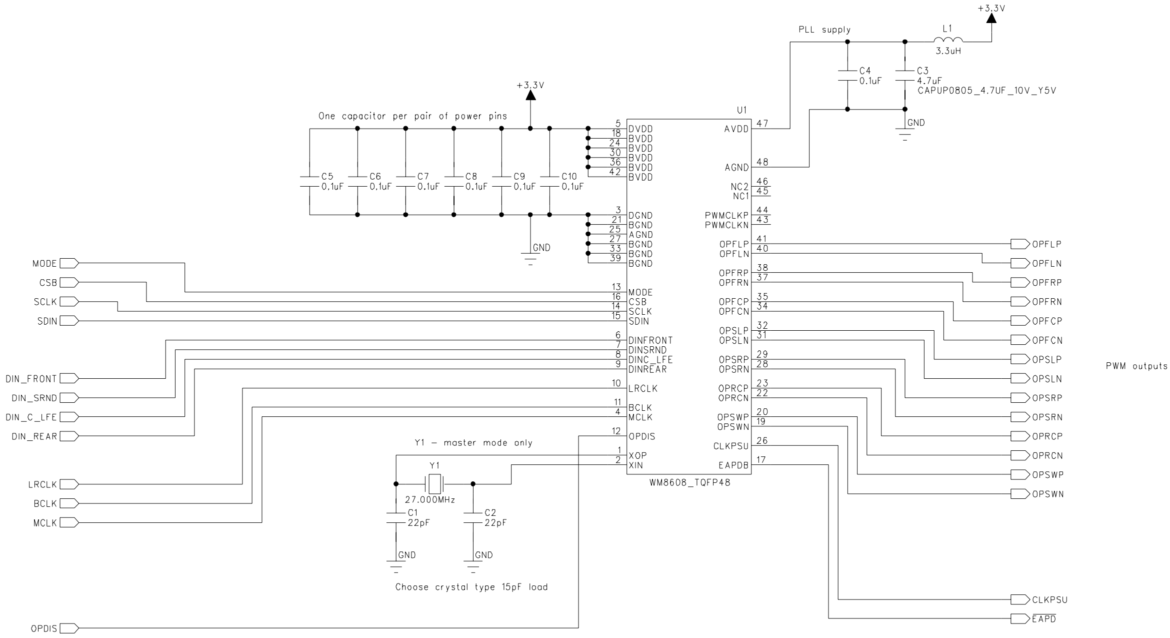


Figure 39 WM8608 External Component Diagram

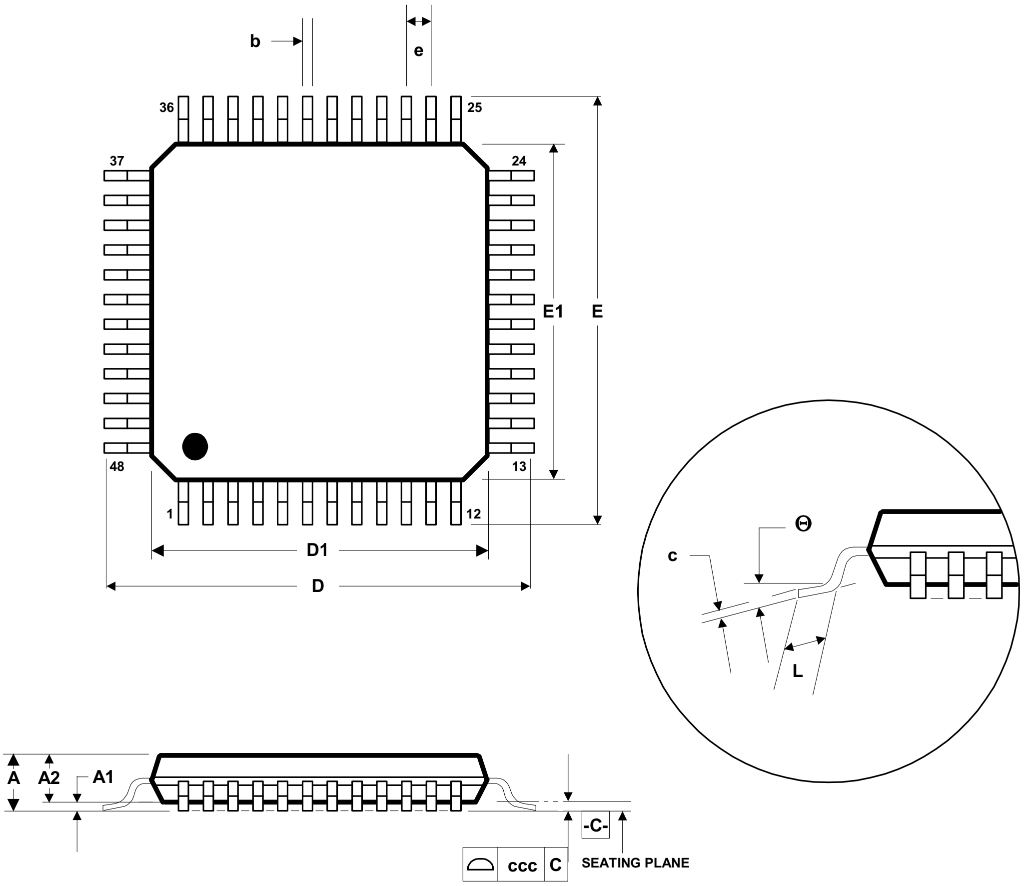
RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
Y1	24.576 / 27.000MHz	Crystal (15pF load)
C1, C2	22pF	Capacitor NP0 0603
C3	4.7µF	Capacitor Y5V 0805
C4-C10	0.1µF	Capacitor X7R 0603

Table 53 External Components Description

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^{o}	3.5^{o}	7^{o}
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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