HA17555GS, HA17555PS, HA17555

●Precision Timer

HA17555 is an IC designed for accurate time delays or oscillations.
It provides both of trigger terminal and reset terminal in order to enable a wide scope of application including Mono Multi Vibrator and Astable Multi Vibrator, and the number of external components is fewer. Further, it's compatible with NE555 of Signetics.

Industrial Use: HA17555GS, HA17555PS
Commercial Use: HA17555

■ FEATURES

- Mono Multi Vibrator can be constructed with one resistor and one capacitor.
- Astable Multi Vibrator can be constructed with two resistors and one capacitor.
- Delay time can be established widely from several µseconds to several hours.
- Pulse Duty can be controlled.
- The maximum value of both sink current and source current is 200mA.
- Direct connection of output to TTL is possible.
- Temperature/delay time ratio is 50ppm/°C (typ).
- Output is normally in the ON and OFF states.

■ APPLICATIONS

- Delay Time Generator (Mono Multi Vibrator)
- Pulse Generator (Astable Multi Vibrator)
- Pulse Width Modulator
- Pulse Location Modulator
- Miss Pulse Detector

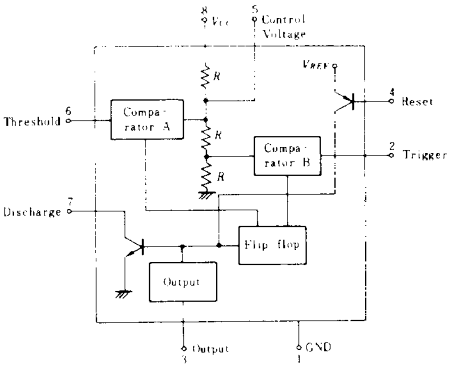
HA17555GS

(DG-8)

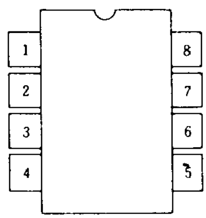
HA17555PS
HA17555

(DP-8)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

1	GND Terminal
2	Trigger Terminal
3	Output Terminal
4	Reset Terminal
5	Control Voltage Terminal
6	Threshold Terminal
7	Discharge Terminal
8	V_{CC} Terminal

■ ABSOLUTO MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	1)HA17555GS	2)HA17555PS	2)HA17555	Unit
Supply Voltage	V_{CC}	18	18	18	V
Discharge Current	I_T	200	200	200	mA
Output Source Current	I_{source}	200	200	200	mA
Output Sink Current	I_{sink}	200	200	200	mA
.Power Dissipation	P_T*	600	600	600	W
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	℃
Storage Temperature	T_{stg}	65 to +150	−55 to +125	− 55 to +125	℃

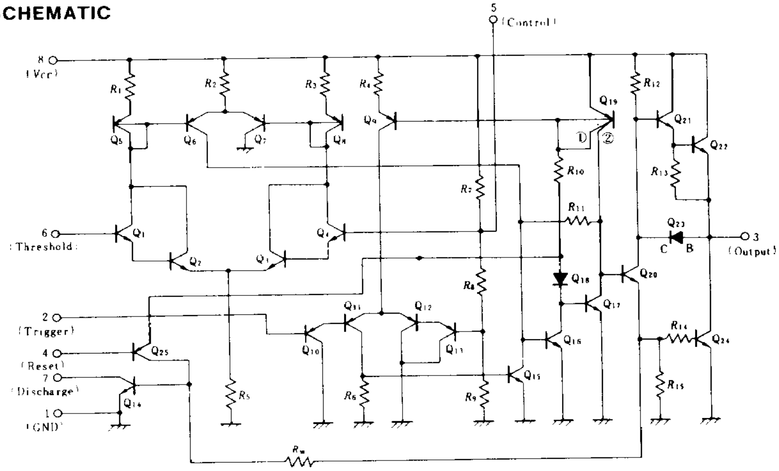
*1) : Value under the condition of $Ta \leq 35°C$. In case of more than it, 6.7mW/℃ derating shall be performed.
2) : Value under the condition of Ta · 60°C. In case of more than it, 6.7mW/℃ derating shall be performed.

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5$ to 15V, $Ta = 25°C$)

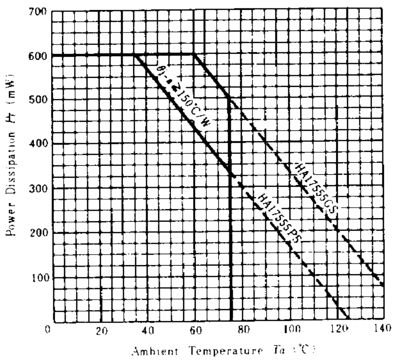
Item		Symbol	Test Condition		Min	Typ	Max	Uuit
Supply Voltage		V_{CC}			4.5	—	16	V
Supply Current *		I_{CC}	$V_{CC}=5V$, $R_L=\infty$		—	3.0	6.0	mA
			$V_{CC}=15V$, $R_L=\infty$		—	10	15	
Timing Error **	Inherent Error	E_t			—	1.0	—	%
	Ta Dependency		Ta 20 to +75℃		—	50		ppm/℃
	Voltage Dependency		V_{CC} =5 to 15V		—	0.01	—	%/V
Threshold Voltage		V_{th}			—	2/3		xVcc
Trigger Voltage		V_T	V_{CC} = 15V		—	5.0	—	V
			V_{CC} =5V		—	1.67	—	
Trigger Current		I_T			—	0.5	—	μA
Reset Voltage		V_R			0.2	0.5	1.0	V
Reset Current		I_R			—	0.1		mA
Threshold Current		I_{th}***			—	0.1	0.25	μA
Control Voltage		V_{CO}	V_{CC} =15V		9	10	11	V
			V_{CC} 5V		2.6	3.33	4.0	
Output Voltage		V_{OL}	V_{CC} =15V	I_{sink}=10mA	—	0.1	0.25	V
				I_{sink}=50mA		0.4	0.75	
				I_{sink} 100mA	—	2.0	2.5	
				I_{sink}=200mA	—	2.5	—	
			V_{CC} =5V, I_{sink}=5mA		—	0.25	0.35	
		V_{OH}	V_{CC} =15V	I_{source}=200mA	—	12.5	—	V
				I_{source}=100mA	12.75	13.3		
			V_{CC} =5V, I_{source}=100mA		2.75	3.3	—	
Output Rise Time		t_r	No loading		—	100	—	ns
Output Fall Time		t_f			—	100	—	ns
Oscillation Pulse Width		t_w	****		10.0	—	—	μs

*When output is Low (When it is high, I is lower by 1mA typically.)
**R_A, R_B 1k to 100kΩ, C 0.1μF, V 5V or 15V
***(R_A + R_B) at V 15V is determined by the value of Ith. It is 20MΩ max.
****Output pulse width at mono multi circuit Output high level pulse width at astable circuit

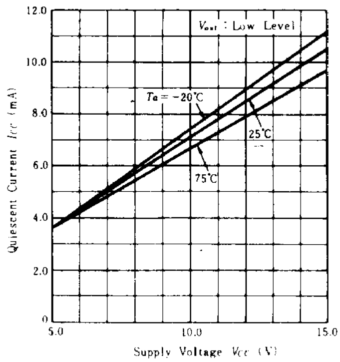
■ CIRCUIT SCHEMATIC



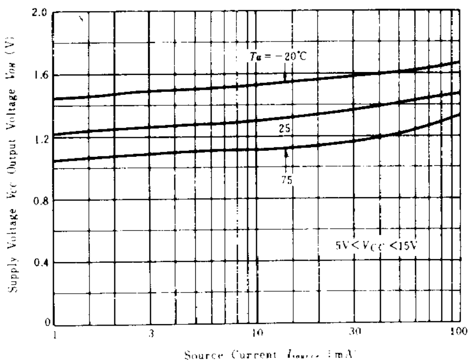
DERATING CURVE



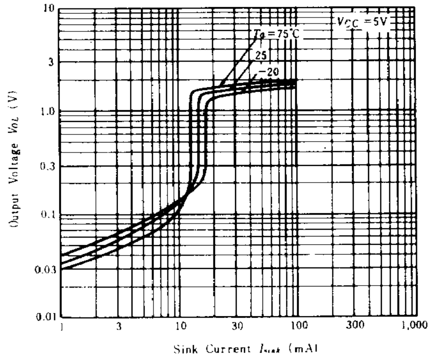
QUIESCENT CURRENT VS. SUPPLY VOLTAGE



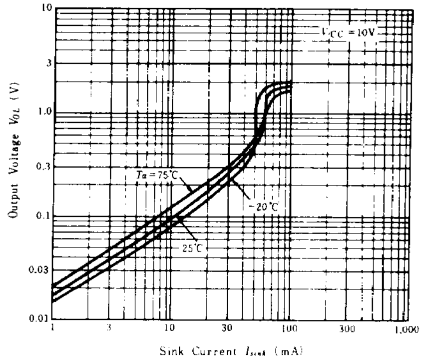
SUPPLY VOLTAGE (V_{CC})-OUTPUT VOLTAGE (V_{OH}) VS. SOURCE CURRENT



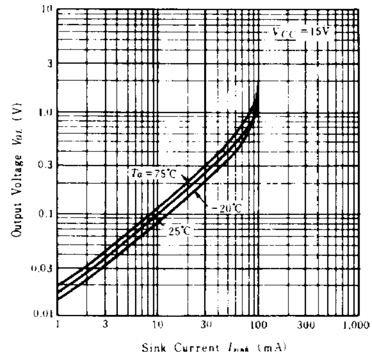
OUTPUT VOLTAGE (V_{OL}) VS. SINK CURRENT (1)



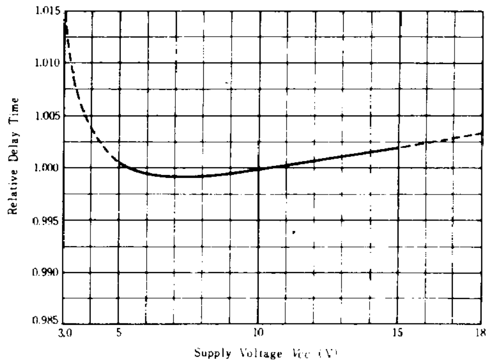
OUTPUT VOLTAGE (V_{OL}) VS. SINK CURRENT (2)



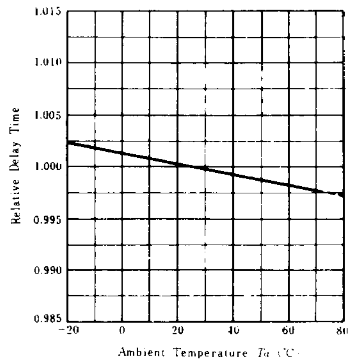
OUTPUT VOLTAGE (V_{OL}) VS. SINK CURRENT (3)



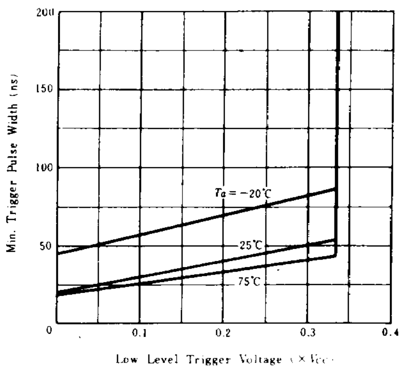
RELATIVE DELAY TIME VS. AMBIENT TEMPERATURE



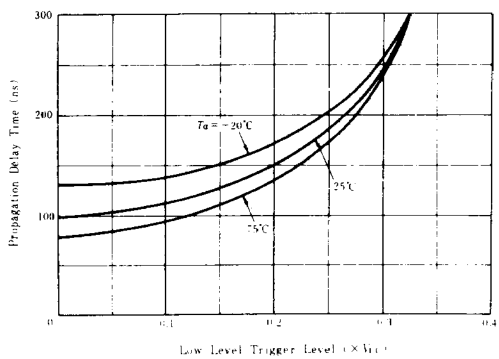
RELATIVE DELAY TIME VS. SUPPLY VOLTAGE



MINIMUM TRIGGER PULSE WIDTH VS. LOW LEVEL TRIGGER VOLTAGE



PROPAGATION DELAY TIME VS. LOW LEVEL TRIGGER VOLTAGE



DESCRIPTION OF HA17555 OPERATION

HA17555 is an Integrated circuit which can provide accurate a time delay and oscillation. As for time delay or mono multi operation, output pulse width can be determined by an external resistor and a capacitor. At astable operation, oscillation frequency and duty cycle can be controlled by two external resistors and an external capacitor separately. It is possible to attract and induce 200mA current by output. And also, operating voltage can be used at a wide range of supply voltage, 5 to 15V. Particularly when supply voltage is 5V, output level is compatible with TTL input.
HA17555 consists of reference voltage circuit, two kinds of comparators, flip-flop, output circuit, reset and discharge circuits.

1. Reference Voltage Circuit

Supply voltage is divided into three by 5kΩ resistance of R_7, R_8 and R_9. The edge of (2/3) Vcc is connected to comparator A, the edge of (1/3) Vcc is connected to comparator B. And (2/3) Vcc is drown out as a control terminal. By impressing bias at (2/3) Vcc from the outside, it is possible to change threshold level and trigger level of comparator.

2. Comparator A

Comparator A consists of Q_1 and Q_8, R_1, R_2, R_3 and R_5. The base of Q_4 is connected to reference voltage (2/3) Vcc. It switches when voltage of threshold terminal switches (2/3) Vcc off. In other words, when voltage of threshold terminal is beyond (2/3) Vcc, Q_1 and Q_2 which have been cut off is turned "ON", and Q_3 and Q_4 are turned "OFF". So, Q_6 is turned "ON" and resets flip-flop.

3. Comparator B

Comparator B consists of Q_9 through Q_{13}, R_4 and R_6. The base of Q_{13} is connected to reference voltage (1/3) Vcc, it switches when voltage of trigger terminal cuts (1/3) Vcc off. In other words, when voltage of trigger terminal decreased to less than (1/3) Vcc, Q_{10} and Q_{11} which have been cut off are turned "ON". Q_{12} and Q_{13} are turned "OFF". So, trigger is supplied to the set side of flip-flop from the collector of Q_{11}, and flip-flop is set.

4. Flipflop

PS flip-flop consists of Q_{15} through Q_{19}, R_{10} and R_{11}. It is stabilized when Q_{16} is turned "ON" and Q_{17} "OFF", by reset signal from comparator A. On the other hand, it is stabilized when Q_{16} is turned "OFF" and Q_{17} "ON", by set signal from comparator A.

5. Output Circuit

Output circuit consists of Q_{20} through Q_{24}, R_{12} through R_{15}. Output level is determined, according to the state of output transistor Q_{17} of flip-flop. When Q_{17} is "ON", output level is "Higg", and when Q_{17} is "OFF", it is "Low".

6. Reset

By making reset terminal "Low" level, prior to any other input, the reset function can make it "Low" level and starting point of a new cycle.

7. Discharge Circuit

Discharge circuit can discharge or charge timing constant connected to the both edges, by "ON" or "OFF" of Q_{14}. Q_{14} is turned "ON" and discharged at "Low" level or when the above reset is made.

■ AN EXAMPLE OF OPERATING CIRCUIT

1. Mono Multi Operation

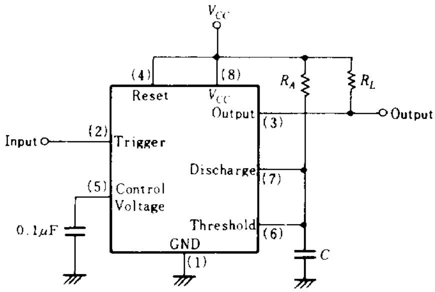


Fig.1 Mono Multi Circuit

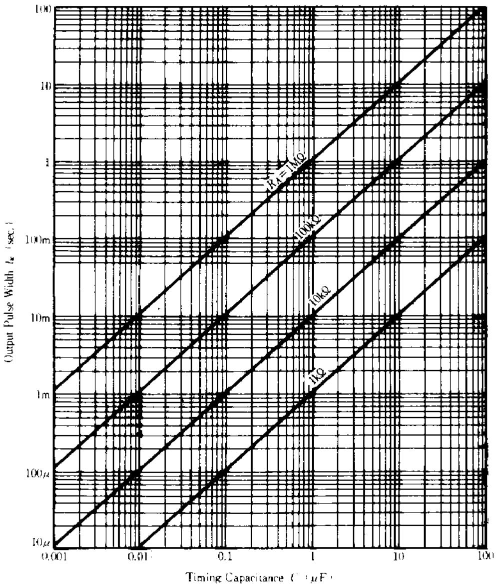


Fig.2 Output Pulse Width vs. Timing Capacitacne

Fig. 1 shows a mono multi circuit using HA17555. It is assumed that the external capacitor C is discharged by discharge transistor Q_{14} inside IC in the beginning.
By adding trigger terminal to negative-going input trigger pulse, flip-flop is set and Q_{14} us turned "OFF". Output is driven to "High".
Capacitor C is charged through resistor R_A at time constant $\tau = R_A C$. When voltage at both edges of capacitor C reach threshold voltage of comparator A, flip-flop is reset and Q_{14} is conducted, capacitor C is discharged. So, output is returned to "Low". Mono multi operation is occurred when negative-going input pulse reaches trigger level. When once mono multi operation is occurred, re-trigger could be made, even if re-trigger signal is added during this period.
According to Fig. 1 and Fig. 2, output pulse width is determined to be tw = 1.1 $R_A C$. If negative-going pulse is added to reset and trigger terminals at the same time during mono multi operation, capacitor C is discharged and mono multi operation is occurred again at positive edge of reset pulse. Output remains "Low" as long as reset terminal is "Low". When the reset terminal is not used, it is better to connect reset terminal to Vcc in order to prevent miss operation. Fig. 2 shows the characteristics of output pulse width when the values of R_A and C are changed. Operating waveform is shown in Fig. 3. If the reset terminal is connected to mono multi circuit subordinately, it is possible to make sequential timer.

2. Astable Operation

If the second resistor R_B is added to the circuit shown in Fig. 1 and threshold terminal is connected to trigger terminal, HA17555 operates as an astable circuit. Fig. 4 shows the circuit construction of HA17555.
Capacitor C is charged through R_A and R_B, discharged through R_B in this circuit. Therefore, duty cycle can be controlled by R_A and R_B. In Fig. 4, capacitor C charges and discharges between threshold voltage (about 0.67 Vcc) and trigger voltage level (about 0.33 Vcc). Fig. 5 shows a typical example of astable operation. In this figure, time (t_H) when output is "High" level, time (t_L) when output is "Low", oscillation frequency (f) and duty cycle (D) are calculated as follows;

$$t_H = 0.693(R_A + R_B)C$$

$$t_L = 0.693 R_B \cdot C$$

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} \quad D = \frac{R_B}{(R_A + 2R_B)}$$

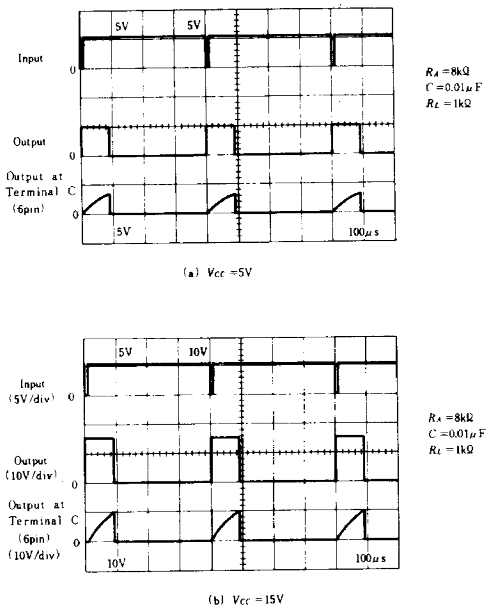


Fig.3 Operation Waveform of Mono multi circuit

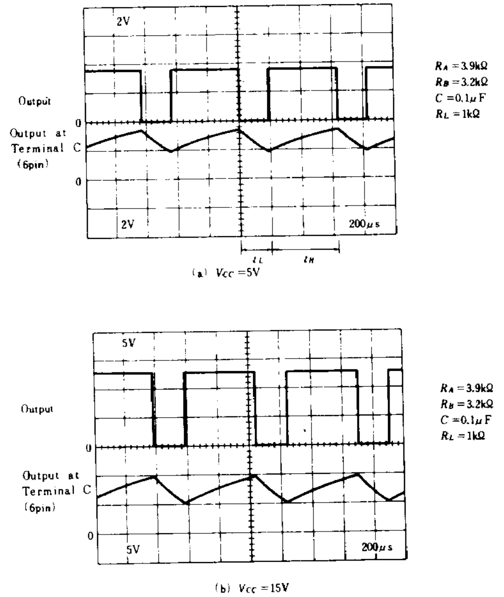


Fig.5 Operation Waveform of Astable Circuit

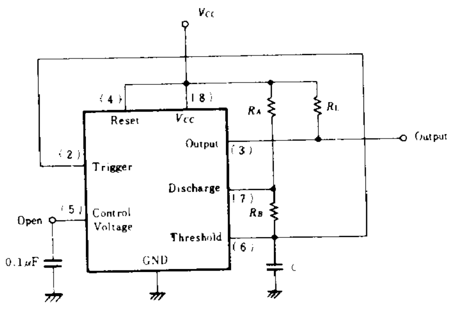
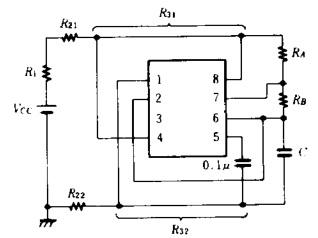


Fig.4 Astable Circuit

3. Cautions in Use

Such integrated circuit for timer as HA17555 type may produce switching noise on power supply and GND line during usage. In this case, abnormal output waveform may be produced by impedance inside power supply or impedance between power supply and GND. So, please take consideration in order to make impedance of each wiring less than the following value at packaging.



R_1 : Power supply output impedance
$R_1 \leqq 50m\Omega$

R_{21}, R_{22} : Lead wiring resistor
$R_{21} + R_{22} \leqq 100m\Omega$

R_{31}, R_{32} : Substrate wiring resistor
$R_{31} + R_{32} \leqq 20m\Omega$