+2.5 V to +5.5 V, 230 μA, Dual Rail-to-Rail Voltage Output 8-/10-/12-Bit DACs

AD5303/AD5313/AD5323*

FEATURES

AD5303: Two Buffered 8-Bit DACs in One Package
AD5313: Two Buffered 10-Bit DACs in One Package
AD5323: Two Buffered 12-Bit DACs in One Package
16-Lead TSSOP Package
Micropower Operation: 300 μA @ 5 V (Including Reference Current)
Power-Down to 200 nA @ 5 V, 50 nA @ 3 V
+2.5 V to +5.5 V Power Supply
Double-Buffered Input Logic
Guaranteed Monotonic By Design Over All Codes
Buffered/Unbuffered Reference Input Options
Output Range: 0–V_{REF} or 0–2 V_{REF}
Power-On-Reset to Zero Volts
SDO Daisy-Chaining Option
Simultaneous Update of DAC Outputs via $\overline{LDAC}$ Pin
Asynchronous $\overline{CLR}$ Facility
Low Power Serial Interface with Schmitt-Triggered Inputs
On-Chip Rail-to-Rail Output Buffer Amplifiers

APPLICATIONS

Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

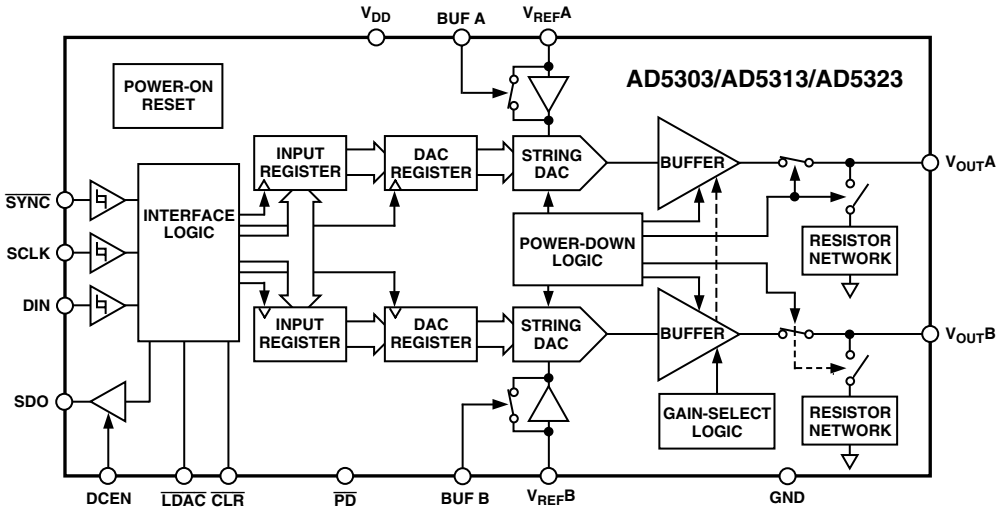
GENERAL DESCRIPTION

The AD5303/AD5313/AD5323 are dual 8-, 10- and 12-bit buffered voltage output DACs in a 16-lead TSSOP package that operate from a single +2.5 V to +5.5 V supply consuming 230 μA at 3 V. Their on-chip output amplifiers allow the outputs to swing rail-to-rail with a slew rate of 0.7 V/μs. The AD5303/AD5313/AD5323 utilize a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI™, QSPI, MICROWIRE™ and DSP interface standards.

The references for the two DACs are derived from two reference pins (one per DAC). These reference inputs may be configured as buffered or unbuffered inputs. The parts incorporate a power-on-reset circuit that ensures that the DAC outputs power-up to 0 V and remain there until a valid write to the device takes place. There is also an asynchronous active low $\overline{CLR}$ pin that clears both DACs to 0 V. The outputs of both DACs may be updated simultaneously using the asynchronous $\overline{LDAC}$ input. The parts contain a power-down feature that reduces the current consumption of the devices to 200 nA at 5 V (50 nA at 3 V) and provides software-selectable output loads while in power-down mode. The parts may also be used in daisy-chaining applications using the SDO pin.

The low power consumption of these parts in normal operation make them ideally suited to portable battery operated equipment. The power consumption is 1.5 mW at 5 V, 0.7 mW at 3 V, reducing to 1 μW in power-down mode.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5684481; other patents pending.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

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AD5303/AD5313/AD5323–SPECIFICATIONS

(V_{DD} = +2.5 V to +5.5 V; V_{REF} = +2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE[3, 4]					
AD5303					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by Design Over All Codes
AD5313					
Resolution		10		Bits	
Relative Accuracy		±0.5	±3	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by Design Over All Codes
AD5323					
Resolution		12		Bits	
Relative Accuracy		±2	±12	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic by Design Over All Codes
Offset Error		±0.4	±3	% of FSR	See Figures 3 and 4
Gain Error		±0.15	±1	% of FSR	See Figures 3 and 4
Lower Deadband		10	60	mV	See Figures 3 and 4
Offset Error Drift[5]		–12		ppm of FSR/°C	
Gain Error Drift[5]		–5		ppm of FSR/°C	
Power Supply Rejection Ratio[5]		–60		dB	ΔV_{DD} = ±10%
DC Crosstalk[5]		30		μV	
DAC REFERENCE INPUTS[5]					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference Mode
	0		V_{DD}	V	Unbuffered Reference Mode
V_{REF} Input Impedance		>10		MΩ	Buffered Reference Mode
		180		kΩ	Unbuffered Reference Mode. 0–V_{REF} Output Range, Input Impedance = R_{DAC}
		90		kΩ	Unbuffered Reference Mode. 0–2 V_{REF} Output Range, Input Impedance = R_{DAC}
Reference Feedthrough		–90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		–80		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[5]					
Minimum Output Voltage[6]		0.001		V min	This is a measure of the minimum and maximum
Maximum Output Voltage[6]		V_{DD} – 0.001		V max	drive capability of the output amplifier.
DC Output Impedance		0.5		Ω	
Short Circuit Current		50		mA	V_{DD} = +5 V
		20		mA	V_{DD} = +3 V
Power-Up Time		2.5		μs	Coming Out of Power-Down Mode. V_{DD} = +5 V
		5		μs	Coming Out of Power-Down Mode. V_{DD} = +3 V
LOGIC INPUTS[5]					
Input Current			±1	μA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5 V ± 10%
			0.6	V	V_{DD} = +3 V ± 10%
			0.5	V	V_{DD} = +2.5 V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = +5 V ± 10%
	2.1			V	V_{DD} = +3 V ± 10%
	2.0			V	V_{DD} = +2.5 V
Pin Capacitance		2	3.5	pF	
LOGIC OUTPUT (SDO)[5]					
V_{DD} = +5 V ± 10%					
Output Low Voltage			0.4	V	I_{SINK} = 2 mA
Output High Voltage	4.0			V	I_{SOURCE} = 2 mA
V_{DD} = +3 V ± 10%					
Output Low Voltage			0.4	V	I_{SINK} = 2 mA
Output High Voltage	2.4			V	I_{SOURCE} = 2 mA
Floating-State Leakage Current			1	μA	DCEN = GND
Floating State O/P Capacitance		3		pF	DCEN = GND
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	I_{DD} Specification Is Valid for All DAC Codes
I_{DD} (Normal Mode)					Both DACs Active and Excluding Load Currents
V_{DD} = +4.5 V to +5.5 V		300	450	μA	Both DACs in Unbuffered Mode. V_{IH} = V_{DD} and
V_{DD} = +2.5 V to +3.6 V		230	350	μA	V_{IL} = GND. In Buffered Mode, extra current is typically x μA per DAC where x = 5 μA + V_{REF}/R_{DAC}.
I_{DD} (Full Power-Down)					
V_{DD} = +4.5 V to +5.5 V		0.2	1	μA	
V_{DD} = +2.5 V to +3.6 V		0.05	1	μA	

NOTES
[1]See Terminology.
[2]Temperature range: B Version: –40°C to +105°C.
[3]DC specifications tested with the outputs unloaded.
[4]Linearity is tested using a reduced code range: AD5303 (Code 8 to 248); AD5313 (Code 28 to 995); AD5323 (Code 115 to 3981).
[5]Guaranteed by design and characterization, not production tested.
[6]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF} = V_{DD} and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

AC CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Units	Conditions/Comments
Output Voltage Settling Time					V_{REF} = V_{DD} = +5 V
AD5303		6	8	µs	1/4 Scale to 3/4 Scale Change (40 Hex to C0 Hex)
AD5313		7	9	µs	1/4 Scale to 3/4 Scale Change (100 Hex to 300 Hex)
AD5323		8	10	µs	1/4 Scale to 3/4 Scale Change (400 Hex to C00 Hex)
Slew Rate		0.7		V/µs	
Major-Code Transition Glitch Energy		12		nV-s	1 LSB Change Around Major Carry (011 . . . 11 to 100 . . . 00)
Digital Feedthrough		0.10		nV-s	
Analog Crosstalk		0.01		nV-s	
DAC-to-DAC Crosstalk		0.01		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p. Unbuffered Mode
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology.
[3]Temperature range: B Version: –40°C to +105°C.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2, 3] (V_{DD} = +2.5 V to +5.5 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	$\overline{\text{SCLK}}$ Low Time
t_4	0	ns min	$\overline{\text{SYNC}}$ to SCLK Rising Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_8	100	ns min	Minimum $\overline{\text{SYNC}}$ High Time
t_9	20	ns min	$\overline{\text{LDAC}}$ Pulsewidth
t_{10}	20	ns min	SCLK Falling Edge to $\overline{\text{LDAC}}$ Rising Edge
t_{11}	20	ns min	$\overline{\text{CLR}}$ Pulsewidth
t_{12}[4, 5]	5	ns min	SCLK Falling Edge to SDO Invalid
t_{13}[4, 5]	20	ns max	SCLK Falling Edge to SDO Valid
t_{14}[5]	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_{15}[5]	10	ns min	$\overline{\text{SYNC}}$ Rising Edge to SCLK Rising Edge

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[3]See Figures 1 and 2.
[4]These are measured with the load circuit of Figure 1.
[5]Daisy-Chain Mode only (see Figure 45).

Specifications subject to change without notice.

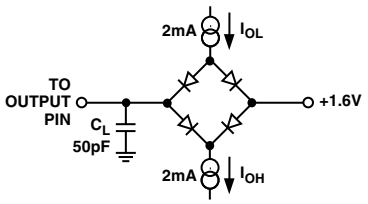


Figure 1. Load Circuit for Digital Output (SDO) Timing Specifications

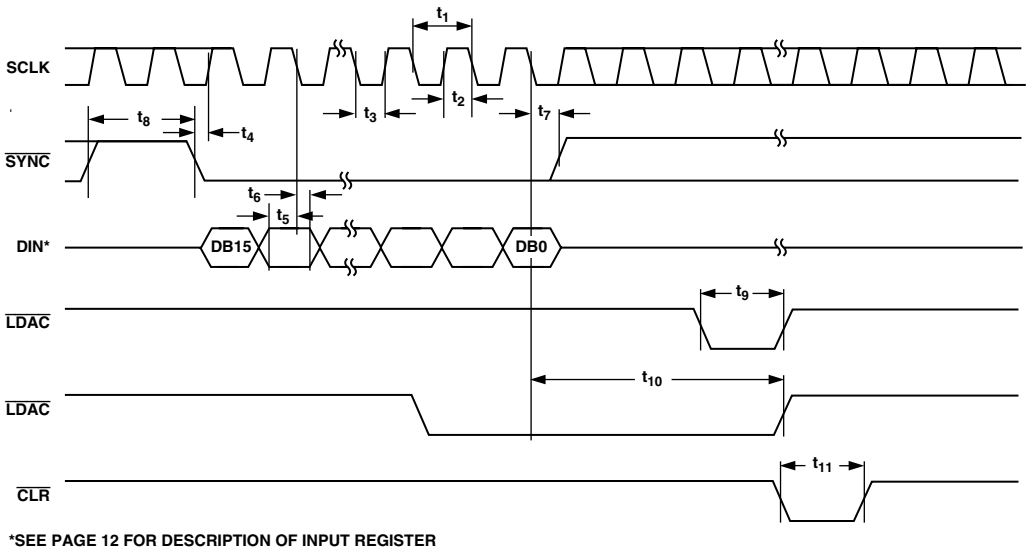


Figure 2. Serial Interface Timing Diagram

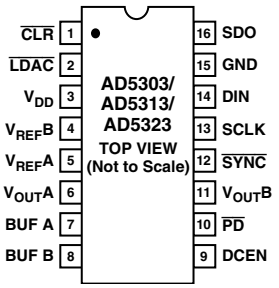
ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
$V_{OUT}A$, $V_{OUT}B$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J Max) . . . . . +150°C
16-Lead TSSOP Package
  Power Dissipation . . . . . (T_J Max – T_A)/θ_{JA}
  θ_{JA} Thermal Impedance . . . . . 160°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5303BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5313BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5323BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5303/AD5313/AD5323 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$\overline{CLR}$	Active low control input that loads all zeroes to both input and DAC registers.
2	$\overline{LDAC}$	Active low control input that transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows either or both DAC registers to be updated if the input registers have new data. This allows simultaneous update of both DAC outputs
3	V_{DD}	Power Supply Input. These parts can be operated from +2.5 V to +5.5 V and the supply should be decoupled to GND.
4	$V_{REF}B$	Reference Input Pin for DAC B. This is the reference for DAC B. It may be configured as a buffered or an unbuffered input, depending on the state of the BUF B pin. It has an input range from 0 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
5	$V_{REF}A$	Reference Input Pin for DAC A. This is the reference for DAC A. It may be configured as a buffered or an unbuffered input depending on the state of the BUF A pin. It has an input range from 0 to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
6	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
7	BUF A	Control pin that controls whether the reference input for DAC A is unbuffered or buffered. If this pin is tied low, the reference input is unbuffered. If it is tied high, the reference input is buffered.
8	BUF B	Control pin that controls whether the reference input for DAC B is unbuffered or buffered. If this pin is tied low, the reference input is unbuffered. If it is tied high, the reference input is buffered.
9	DCEN	This pin is used to enable the daisy-chaining option. This should be tied high if the part is being used in a daisy-chain. The pin should be tied low if it is being used in stand-alone mode.
10	$\overline{PD}$	Active low control input that acts as a hardware power-down option. This pin overrides any software power-down option. Both DACs go into power-down mode when this pin is tied low. The DAC outputs go into a high impedance state and the current consumption of the part drops to 200 nA @ 5 V (50 nA @ 3 V).
11	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers-on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 16 clocks. If $\overline{SYNC}$ is taken high before the 16th falling edge, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the device.
13	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz. The SCLK input buffer is powered-down after each write cycle.
14	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered-down after each write cycle.
15	GND	Ground reference point for all circuitry on the part.
16	SDO	Serial Data Output that can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data output is valid on the falling edge of the clock.

TERMINOLOGY

RELATIVE ACCURACY

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 5.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 8.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

OFFSET ERROR DRIFT

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

MAJOR-CODE TRANSITION GLITCH ENERGY
Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

DIGITAL FEEDTHROUGH
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{SYNC}$ held high). It is specified in nV secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s and vice versa.

ANALOG CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a change in the output of the other DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ high. Then pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-secs.

DAC-TO-DAC CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of the other DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ low and monitoring the output of the other DAC. The area of the glitch is expressed in nV-secs.

DC CROSSTALK
This is the dc change in the output level of one DAC in response to a change in the output of the other DAC. It is measured with a full-scale output change on one DAC while monitoring the other DAC. It is expressed in μV.

POWER SUPPLY REJECTION RATIO (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at +2 V and V_{DD} is varied ±10%.

REFERENCE FEEDTHROUGH
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{LDAC}$ is high). It is expressed in dBs.

TOTAL HARMONIC DISTORTION
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

MULTIPLYING BANDWIDTH
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

CHANNEL-TO-CHANNEL ISOLATION
This is a ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of the other DAC. It is measured in dBs.

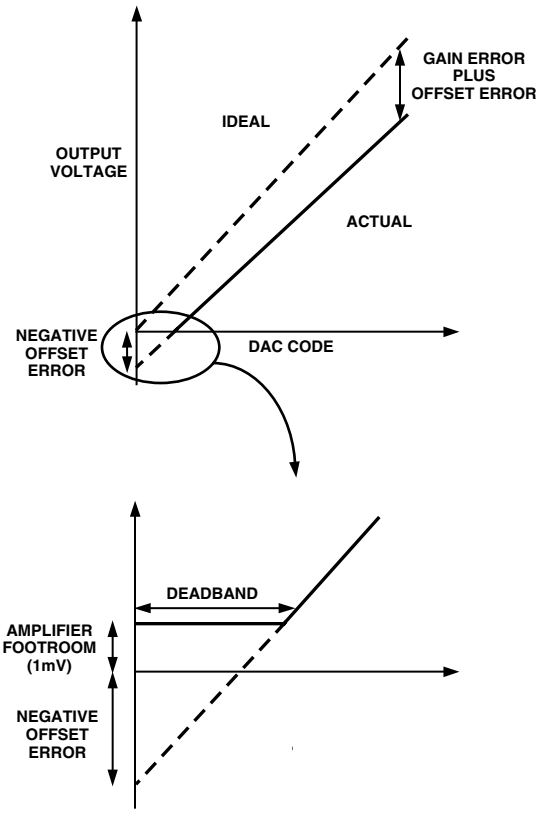


Figure 3. Transfer Function with Negative Offset

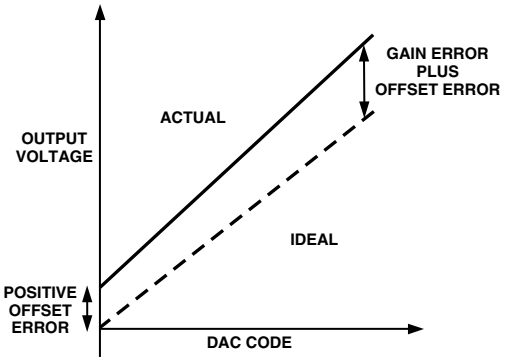


Figure 4. Transfer Function with Positive Offset

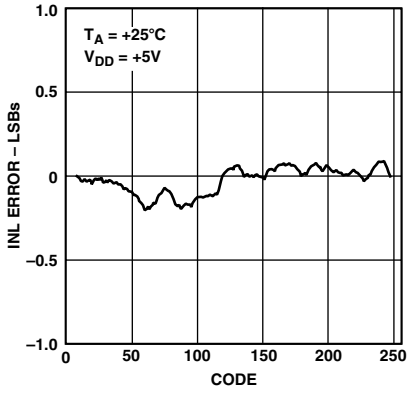


Figure 5. AD5303 Typical INL Plot

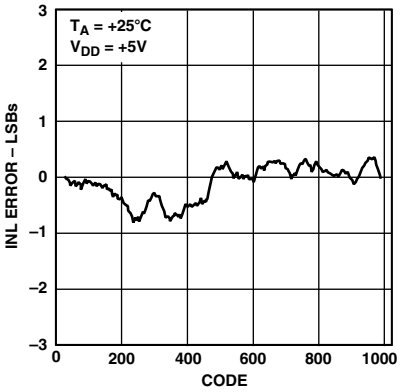


Figure 6. AD5313 Typical INL Plot

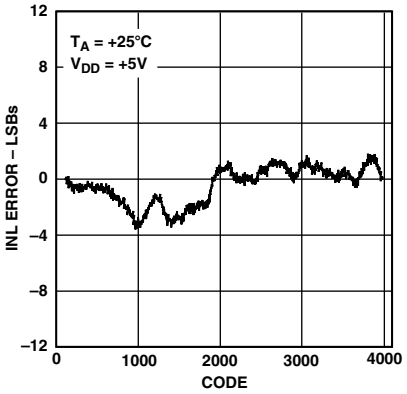


Figure 7. AD5323 Typical INL Plot

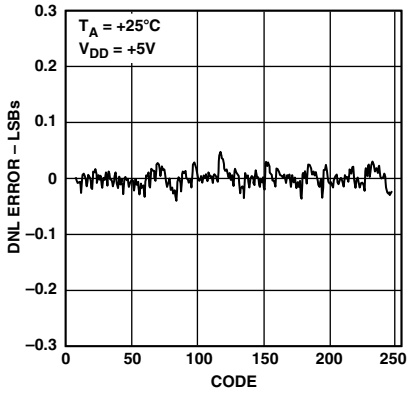


Figure 8. AD5303 Typical DNL Plot

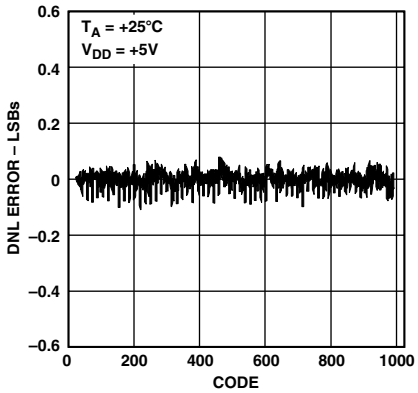


Figure 9. AD5313 Typical DNL Plot

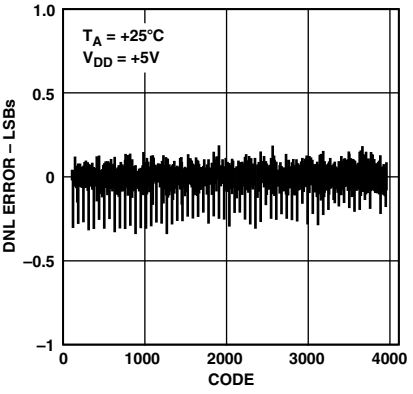


Figure 10. AD5323 Typical DNL Plot

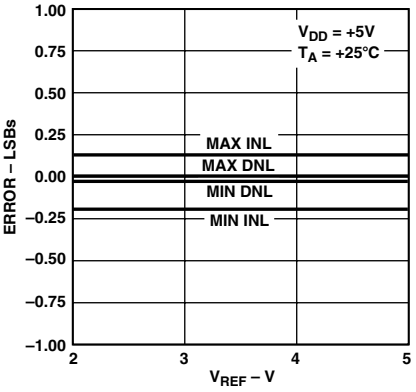


Figure 11. AD5303 INL and DNL Error vs. V_{REF}

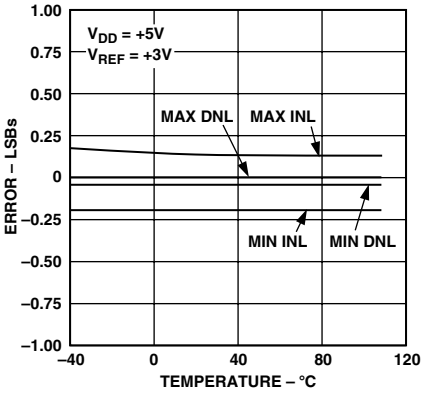


Figure 12. AD5303 INL Error and DNL Error vs. Temperature

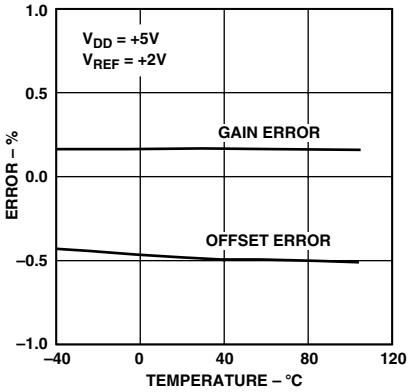


Figure 13. Offset Error and Gain Error vs. Temperature

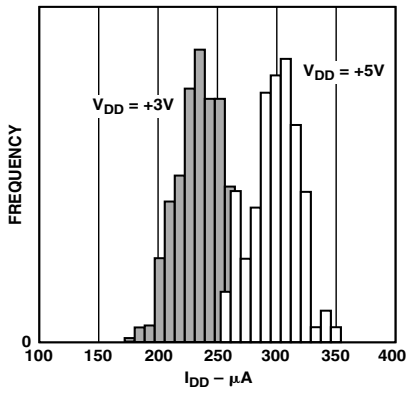


Figure 14. I_{DD} Histogram with V_{DD} = +3 V and V_{DD} = +5 V

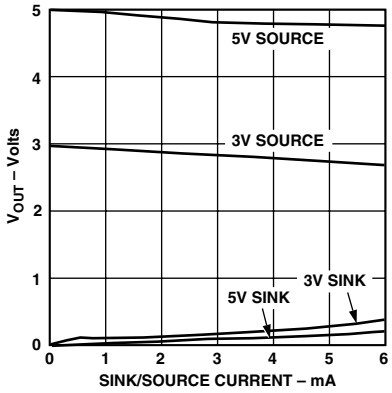


Figure 15. Source and Sink Current Capability

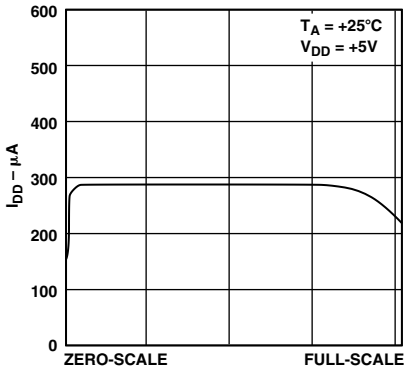


Figure 16. Supply Current vs. Code

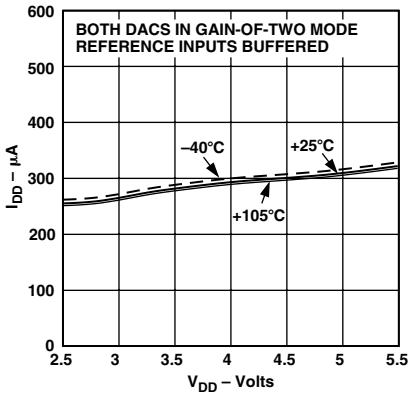


Figure 17. Supply Current vs. Supply Voltage

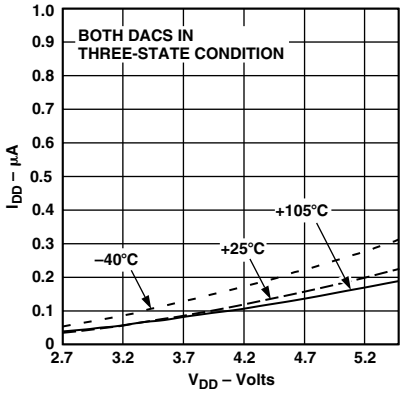


Figure 18. Power-Down Current vs. Supply Voltage

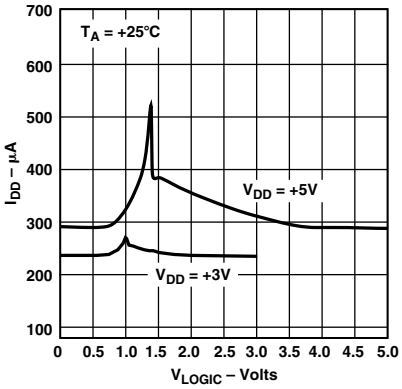


Figure 19. Supply Current vs. Logic Input Voltage

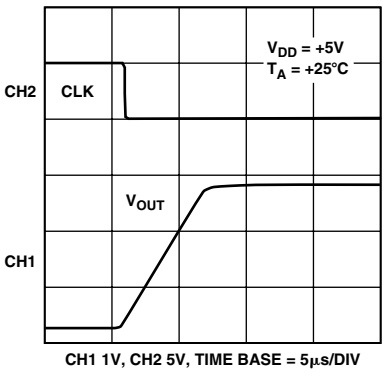


Figure 20. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

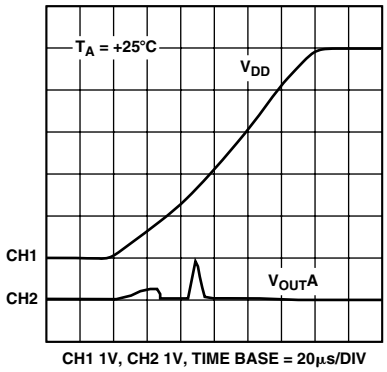


Figure 21. Power-On Reset to 0 V

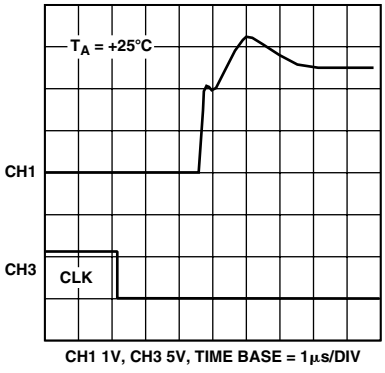


Figure 22. Exiting Power-Down to Midscale

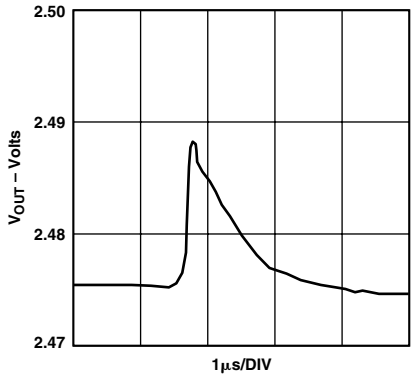


Figure 23. AD5323 Major-Code Transition

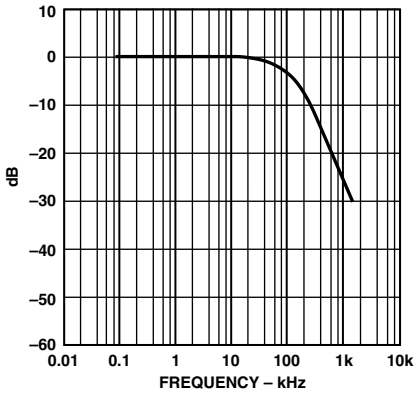


Figure 24. Multiplying Bandwidth (Small-Signal Frequency Response)

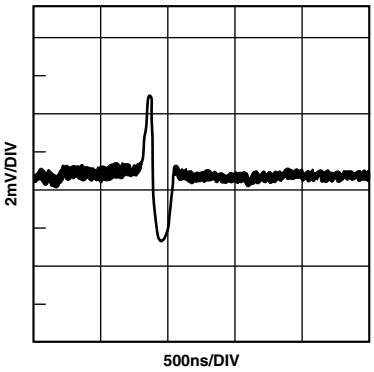


Figure 25. DAC-DAC Crosstalk

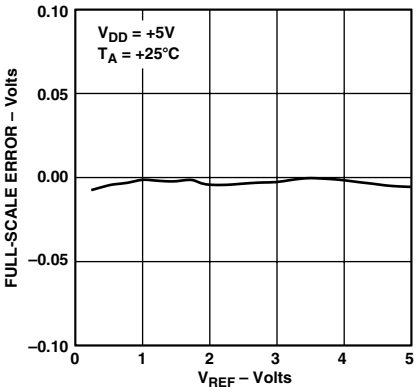


Figure 26. Full-Scale Error vs. V_{REF} (Buffered)

FUNCTIONAL DESCRIPTION

The AD5303/AD5313/AD5323 are dual resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10 and 12 bits respectively. They contain reference buffers, output buffer amplifiers and are written to via a 3-wire serial interface. They operate from single supplies of +2.5 V to +5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/μs. Each DAC is provided with a separate reference input, which may be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from GND to V_{DD}. The devices have three programmable power-down modes, in which one or both DACs may be turned off completely with a high-impedance output, or the output may be pulled low by an on-chip resistor.

Digital-to-Analog Section

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 27 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where

D = decimal equivalent of the binary code, which is loaded to the DAC register;

0–255 for AD5303 (8 Bits)
0–1023 for AD5313 (10 Bits)
0–4095 for AD5323 (12 Bits)

N = DAC resolution

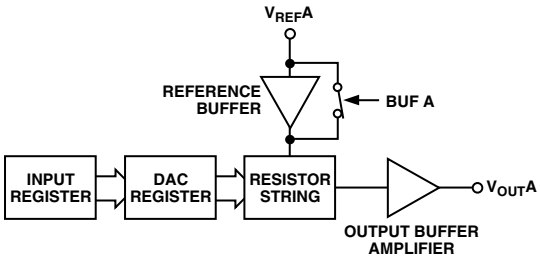


Figure 27. Single DAC Channel Architecture

Resistor String

The resistor string section is shown in Figure 28. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

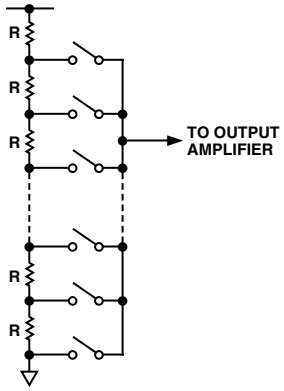


Figure 28. Resistor String

DAC Reference Inputs

There is a reference input pin for each of the two DACs. The reference inputs are buffered but can also be configured as unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However, if the unbuffered mode is used, the user can have a reference voltage as low as GND and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier.

If there is a buffered reference in the circuit (e.g., REF192), there is no need to use the on-chip buffers of the AD5303/AD5313/AD5323. In unbuffered mode the input impedance is still large at typically 180 kΩ per reference input for 0–V_{REF} mode and 90 kΩ for 0–2 V_{REF} mode.

The buffered/unbuffered option is controlled by the BUF A and BUF B pins. If the BUF pin is tied high, the reference input is buffered, if tied low, it is unbuffered.

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail which gives an output range of 0.001 V to V_{DD} – 0.001 V when the reference is V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 500 pF to GND and V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 15.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 μs.

POWER-ON RESET

The AD5303/AD5313/AD5323 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

– Normal operation.
– 0–V_{REF} output range.
– Output voltage set to 0 V.

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

Clear Function ($\overline{CLR}$)

The $\overline{CLR}$ pin is an active low input which, when pulled low, loads all zeros to both input registers and both DAC registers. This enables both analog outputs to be cleared to 0 V.

SERIAL INTERFACE

The AD5303/AD5313/AD5323 are controlled over a versatile, 3-wire serial interface, which operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE and DSP interface standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 2. The 16-bit word consists of four control bits followed by 8, 10 or 12 bits of DAC data, depending on the device type. The first bit loaded is the MSB (Bit 15), which determines whether the data is for DAC A or DAC B. Bit 14 determines the output range (0–V_{REF} or 0–2 V_{REF}). Bits 13 and 12 control the operating mode of the DAC.

Table I. Control Bits

Bit	Name	Function	Power-On Default
15	$\overline{A}$/B	0: Data Written to DAC A 1: Data Written to DAC B	N/A
14	GAIN	0: Output Range of 0–V_{REF} 1: Output Range of 0-2 V_{REF}	0
13	PD1	Mode Bit	0
12	PD0	Mode Bit	0

The remaining bits are DAC data bits, starting with the MSB and ending with the LSB. The AD5323 uses all 12 bits of DAC data, the AD5313 uses 10 bits and ignores the two LSBs. The AD5303 uses eight bits and ignores the last four bits. The data format is straight binary, with all zeroes corresponding to 0 V output, and all ones corresponding to full-scale output (V_{REF} – 1 LSB).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low observing the minimum $\overline{SYNC}$ to SCLK active edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. Any data and clock pulses after the 16th will be ignored, and no further serial data transfer will occur until $\overline{SYNC}$ is taken high and low again.

$\overline{SYNC}$ may be taken high after the falling edge of the 16th SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t_7.

After the end of serial data transfer, data will automatically be transferred from the input shift register to the input register of the selected DAC. If $\overline{SYNC}$ is taken high before the 16th falling edge of SCLK, the data transfer will be aborted and the input registers will not be updated.

When data has been transferred into both input registers, the DAC registers of both DACs may be simultaneously updated, by taking $\overline{LDAC}$ low. $\overline{CLR}$ is an active-low, asynchronous clear that clears the input and DAC registers of both DACs to all zeroes.

Low Power Serial Interface

To reduce the power consumption of the device even further, the interface only powers up fully when the device is being written to. As soon as the 16-bit control word has been written to the part, the SCLK and DIN input buffers are powered-down. They only power-up again following a falling edge of $\overline{SYNC}$.

Double-Buffered Interface

The AD5303/AD5313/AD5323 DACs all have double-buffered interfaces consisting of two banks of registers—input registers and DAC registers. The input register is connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it.

This is useful if the user requires simultaneous updating of both DAC outputs. The user may write to both input registers individually and then, by pulsing the $\overline{LDAC}$ input low, both outputs will update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the

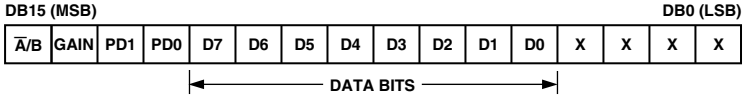


Figure 29. AD5303 Input Shift Register Contents

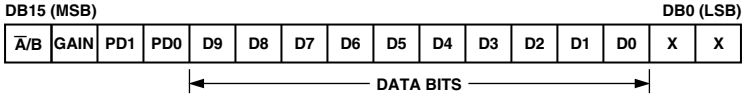


Figure 30. AD5313 Input Shift Register Contents

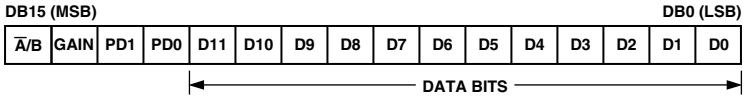


Figure 31. AD5323 Input Shift Register Contents

contents of the input registers. In the case of the AD5303/AD5313/AD5323, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated thereby removing unnecessary digital crosstalk.

POWER-DOWN MODES

The AD5303/AD5313/AD5323 have very low power consumption, dissipating only 0.7 mW with a 3 V supply and 1.5 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into one of three power-down modes, which are selected by Bits 13 and 12 (PD1 and PD0) of the control word. Table II shows how the state of the bits corresponds to the mode of operation of that particular DAC.

Table II. PD1/PD0 Operating Modes

PD1	PD0	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ Load to GND)
1	0	Power-Down (100 kΩ Load to GND)
1	1	Power-Down (High Impedance Output)

When both bits are set to 0, the DACs work normally with their normal power consumption of 300 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V) when both DACs are powered down. Not only does the supply current drop but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or it is left in a high impedance state (Three-State). The output stage is illustrated in Figure 32.

The bias generator, the output amplifier, the resistor string and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs when V_{DD} = 3 V. See Figure 22 for a plot.

The software power-down modes programmed by PD0 and PD1 are overridden by the $\overline{PD}$ pin. Taking this pin low puts both DACs into power-down mode simultaneously and both outputs are put into a high impedance state. If $\overline{PD}$ is not used it should be tied high.

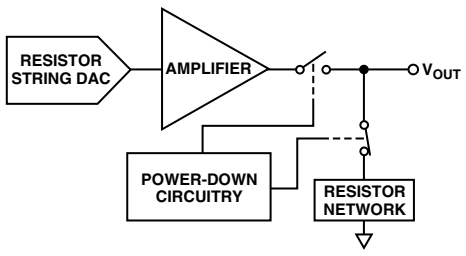


Figure 32. Output Stage During Power-Down

MICROPROCESSOR INTERFACING

AD5303/AD5313/AD5323 to ADSP-2101/ADSP-2103 Interface

Figure 33 shows a serial interface between the AD5303/AD5313/AD5323 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active-Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

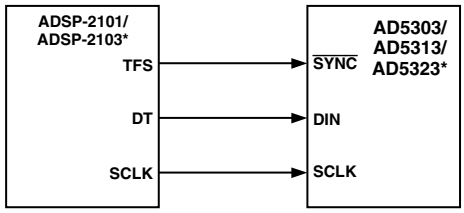


Figure 33. AD5303/AD5313/AD5323 to ADSP-2101/ADSP-2103 Interface

AD5303/AD5313/AD5323 to 68HC11/68L11 Interface

Figure 34 shows a serial interface between the AD5303/AD5313/AD5323 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5303/AD5313/AD5323, while the MOSI output drives the serial data line (DIN) of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5303/AD5313/AD5323, PC7 is left low after the first eight bits are transferred, a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

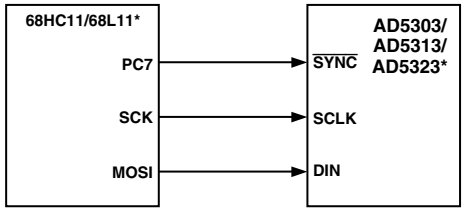


Figure 34. AD5303/AD5313/AD5323 to 68HC11/68L11 Interface

AD5303/AD5313/AD5323 to 80C51/80L51 Interface

Figure 35 shows a serial interface between the AD5303/AD5313/AD5323 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5303/AD5313/AD5323, while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case port line P3.3 is used. When data is to be transmitted to the AD5303/AD5313/AD5323, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5303/AD5313/AD5323 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

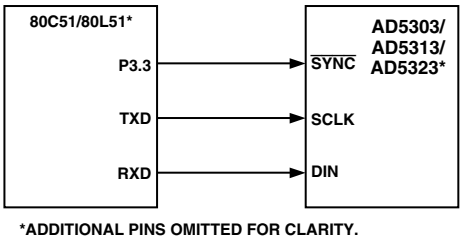


Figure 35. AD5303/AD5313/AD5323 to 80C51/80L51 Interface

AD5303/AD5313/AD5323 to MICROWIRE Interface

Figure 36 shows an interface between the AD5303/AD5313/AD5323 and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5303/AD5313/AD5323 on the rising edge of the SK.

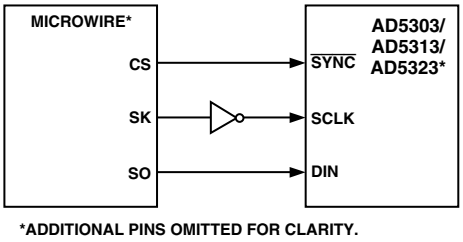


Figure 36. AD5303/AD5313/AD5323 to MICROWIRE Interface

APPLICATIONS INFORMATION

Typical Application Circuit

The AD5303/AD5313/AD5323 can be used with a wide range of reference voltages, especially if the reference inputs are configured to be unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0 V to V_{DD}.

More typically, the AD5303/AD5313/AD5323 may be used with a fixed, precision reference voltage. Figure 37 shows a typical setup for the AD5303/AD5313/AD5323 when using an external reference. If the reference inputs are unbuffered, the reference input range is from 0 V to V_{DD}, but if the on-chip reference buffers are used, the reference range is reduced. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference would be the REF191, a 2.048 V reference.

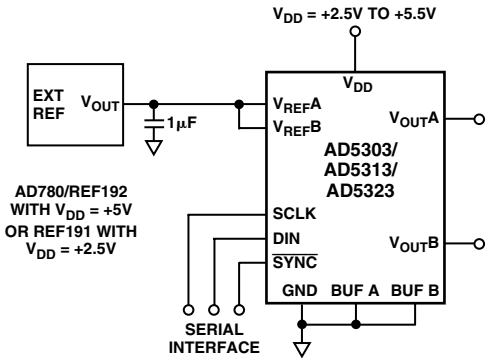


Figure 37. AD5303/AD5313/AD5323 Using External Reference

If an output range of 0 V to V_{DD} is required when the reference inputs are configured as unbuffered (for example 0 V to +5 V) then the simplest solution is to connect the reference inputs to V_{DD}. As this supply may not be very accurate and may be noisy, then the AD5303/AD5313/AD5323 may be powered from the reference voltage, for example using a 5 V reference such as the REF195, as shown in Figure 38. The REF195 will output a steady supply voltage for the AD5303/AD5313/AD5323. The current required from the REF195 is 300 µA supply current and approximately 30 µA or 60 µA into each of the reference inputs (if unbuffered). This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10 kΩ load on each output) is:

$$360\ \mu A + 2\ (5\ V/10\ k\Omega) = 1.36\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.7 ppm (13.5 µV) for the 1.36 mA current drawn from it. This corresponds to a 0.0007 LSB error at 8 bits and 0.011 LSB error at 12 bits.

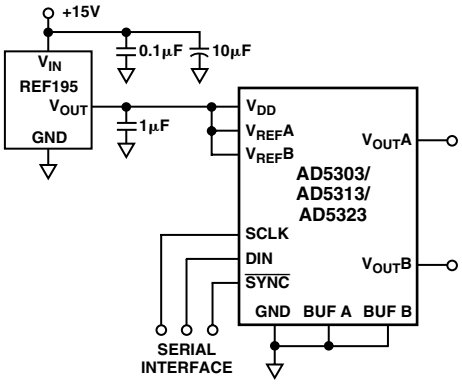


Figure 38. Using an REF195 as Power and Reference to the AD5303/AD5313/AD5323

Bipolar Operation Using the AD5303/AD5313/AD5323

The AD5303/AD5313/AD5323 has been designed for single supply operation, but bipolar operation is also achievable using the circuit shown in Figure 39. The circuit shown has been configured to achieve an output voltage range of –5 V < V_{OUT} < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

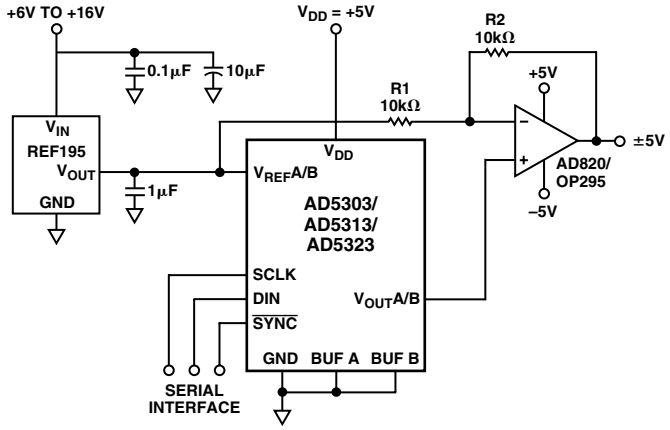


Figure 39. Bipolar Operation Using the AD5303/AD5313/AD5323

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = [(V_{REF} \times D/2^N) \times (R1+R2)/R1 - V_{REF} \times (R2/R1)]$$

where:

D is the decimal equivalent of the code loaded to the DAC and N is the DAC resolution.

V_{REF} is the reference voltage input, and gain bit = 0.

with:

V_{REF} = 5 V
$R1 = R2$ = 10 kΩ and V_{DD} = 5 V
$V_{OUT} = (10 \times D/2^N) - 5$ V

Opto-Isolated Interface for Process Control Applications

The AD5303/AD5313/AD5323 has a versatile 3-wire serial interface making it ideal for generating accurate voltages in process control and industrial applications. Due to noise, safety requirements or distance, it may be necessary to isolate the AD5303/AD5313/AD5323 from the controller. This can easily be achieved by using opto-isolators, which will provide isolation in excess of 3 kV. The serial loading structure of the AD5303/AD5313/AD5323 makes it ideally suited for use in opto-isolated applications. Figure 40 shows an opto-isolated interface to the AD5303/AD5313/AD5323 where DIN, SCLK and $\overline{\text{SYNC}}$ are driven from opto-couplers. The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a +5 V regulator provides the +5 V supply required for the AD5303/AD5313/AD5323.

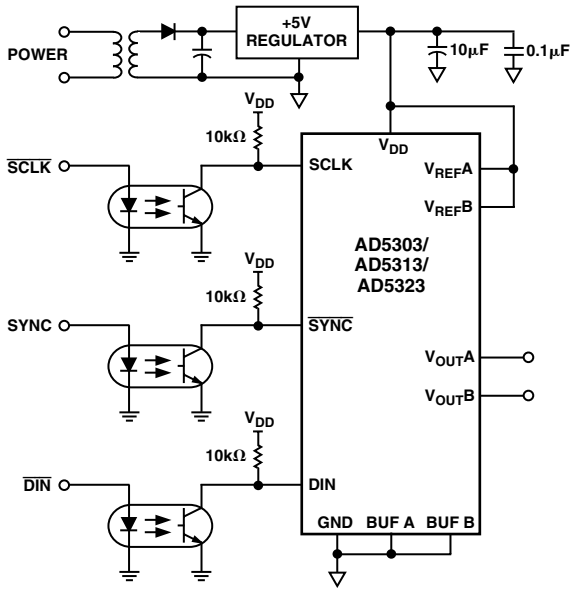


Figure 40. AD5303/AD5313/AD5323 in an Opto-Isolated Interface

Decoding Multiple AD5303/AD5313/AD5323s

The $\overline{\text{SYNC}}$ pin on the AD5303/AD5313/AD5323 can be used in applications to decode a number of DACs. In this application, all the DACs in the system receive the same serial clock and serial data, but only the $\overline{\text{SYNC}}$ to one of the devices will be active at any one time, allowing access to two channels in this 8-channel system. The 74HC139 is used as a 2-to-4 line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 41 shows a diagram of a typical setup for decoding multiple AD5303/AD5313/AD5323 devices in a system.

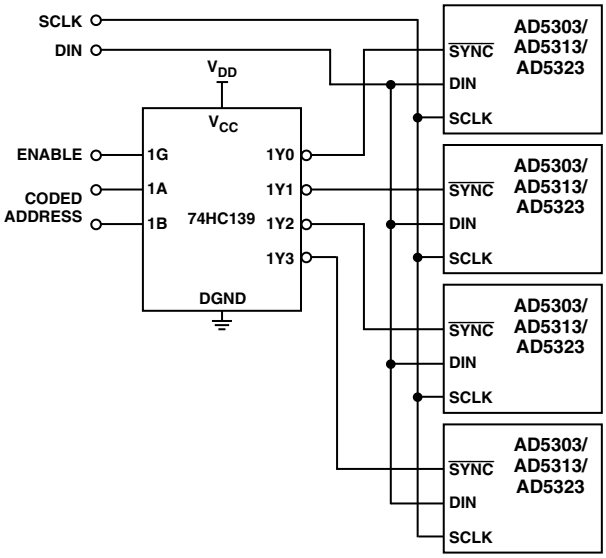


Figure 41. Decoding Multiple AD5303/AD5313/AD5323 Devices in a System

AD5303/AD5313/AD5323 as a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using the two DACs in the AD5303/AD5313/AD5323 is shown in Figure 42. The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, a LED will indicate the fail condition.

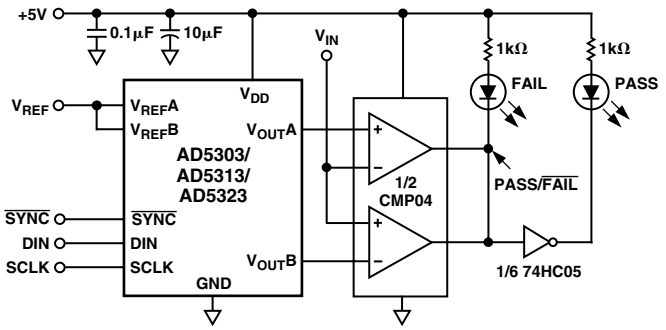


Figure 42. Window Detector Using AD5303/AD5313/AD5323

Coarse and Fine Adjustment Using the AD5303/AD5313/ AD5323

The DACs in the AD5303/AD5313/AD5323 can be paired together to form a coarse and fine adjustment function, as shown in Figure 43. DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 will change the relative effect of the coarse and fine adjustments. With the resistor values and external reference shown, the output amplifier has unity gain for the DAC A output, so the output range is 0 V to 2.5 V – 1 LSB. For DAC B the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range equal to 19 mV.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} may be used. The op amps indicated will allow a rail-to-rail output swing.

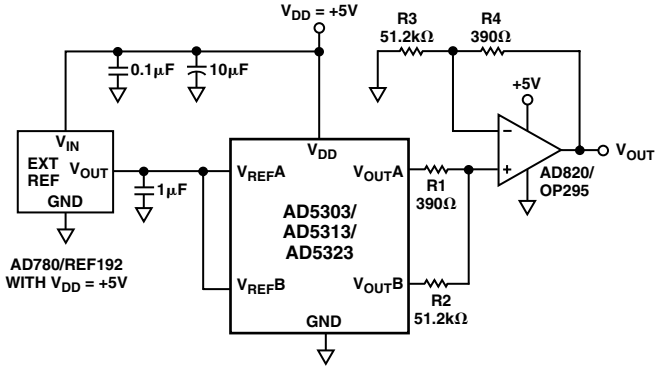


Figure 43. Coarse/Fine Adjustment

Daisy-Chain Mode

This mode is used for updating serially-connected or stand-alone devices on the rising edge of $\overline{SYNC}$. For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin may be used to daisy-chain several devices together and provide serial readback.

By connecting DCEN (Daisy-Chain Enable) pin high, the Daisy-Chain Mode is enabled. It is tied low in the case of Stand-Alone Mode. In Daisy-Chain Mode the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{SYNC}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out after the falling edge of SCLK and is valid on the subsequent rising and falling edges. By connecting this line to the DIN input on the next DAC in the chain, a multiDAC interface is constructed. Sixteen clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{SYNC}$ should be taken high. This prevents any further data being clocked into the input shift register.

A continuous SCLK source may be used if it can be arranged that $\overline{SYNC}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC registers and all analog outputs are updated simultaneously.

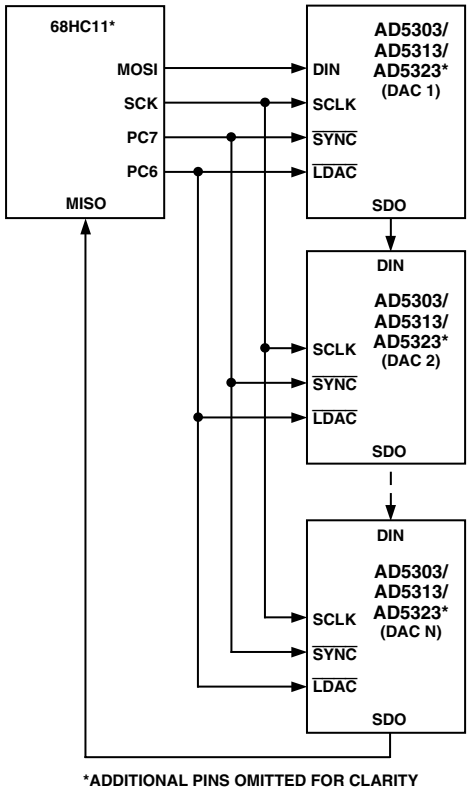


Figure 44. Daisy-Chain Mode

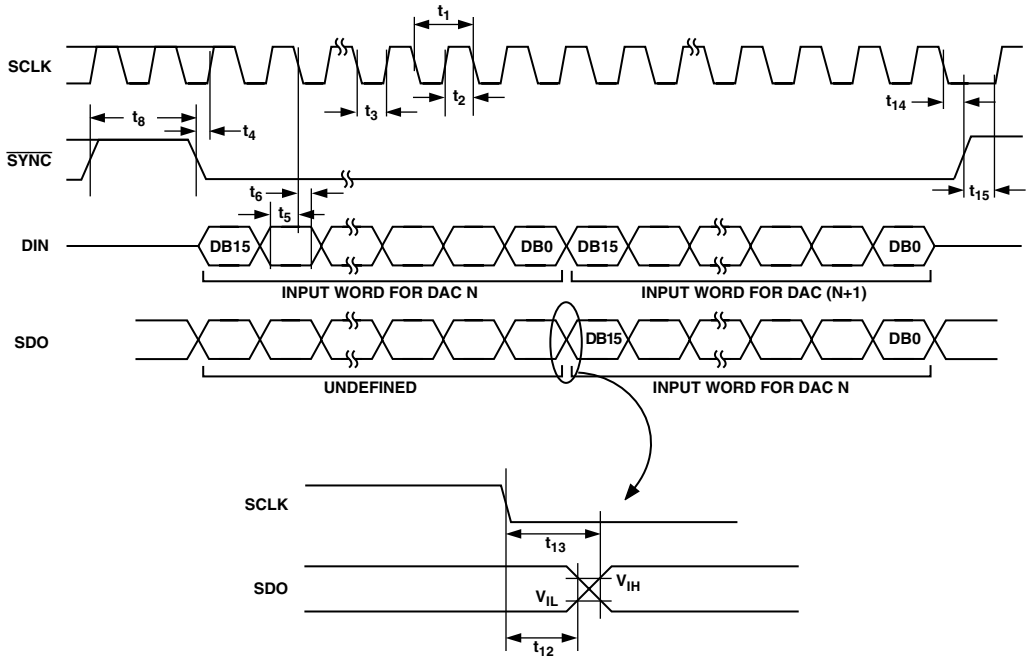


Figure 45. Daisy-Chaining Timing Diagram

Power Supply Bypassing and Grounding

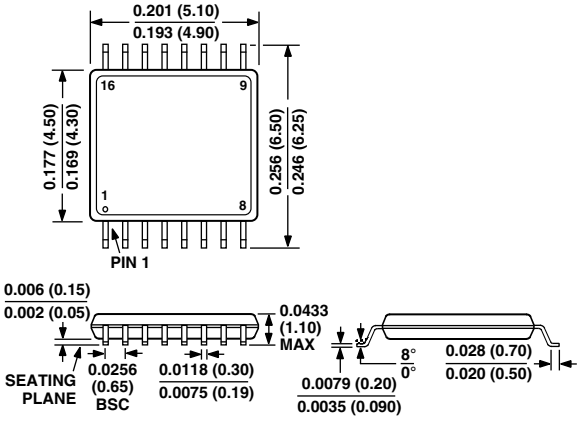
In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5303/AD5313/AD5323 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5303/AD5313/AD5323 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the AD5303/AD5313/AD5323. The AD5303/AD5313/AD5323 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5303/AD5313/AD5323 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)



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