

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 175 \text{ mA}$  at 100 MHz
- Low CMOS standby power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-pin TSOP II and 48-ball VFBGA packages
- Offered in single CE and dual CE options

## Functional Description

The CY7C1061DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

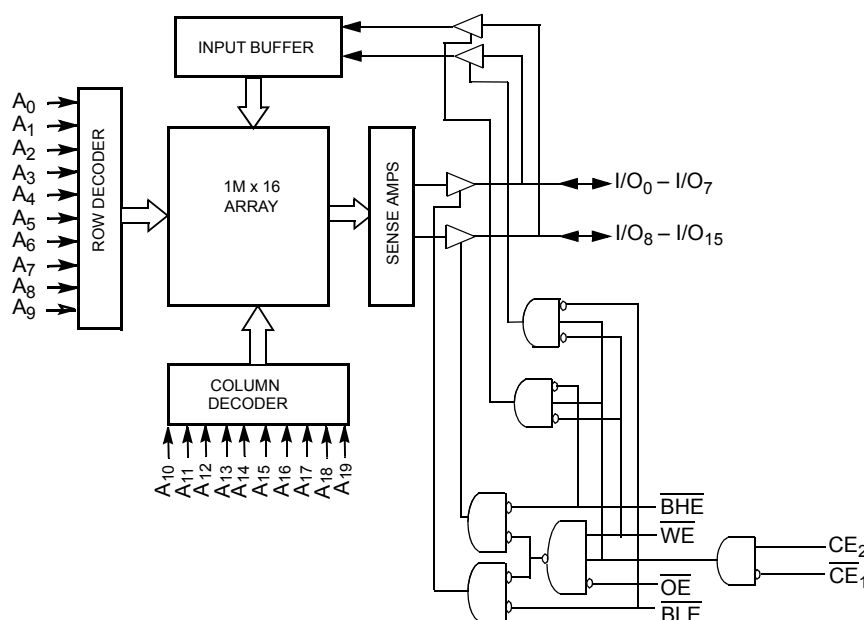
To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See [Truth Table on page 11](#) for a complete description of Read and Write modes.

The input or output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and WE LOW).

The CY7C1061DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and 48-ball VFBGA packages.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



## Contents

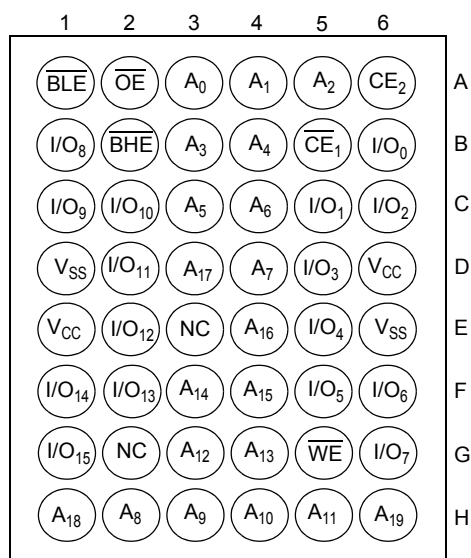
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## Selection Guide

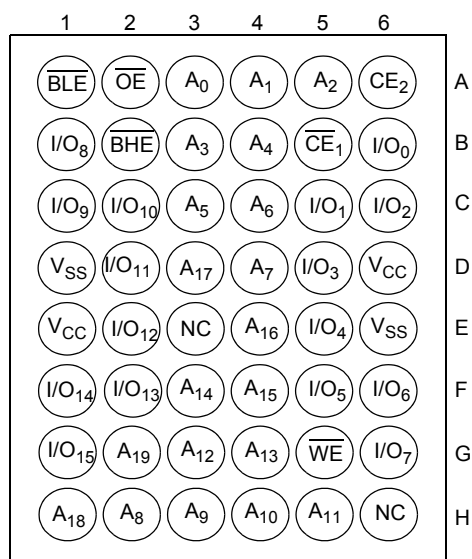
Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

## Pin Configurations

**Figure 1. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable (-BVXI) (Top View)** <sup>[1, 2]</sup>



**Figure 2. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable (-BVJXI) (Top View)** <sup>[1, 2]</sup>

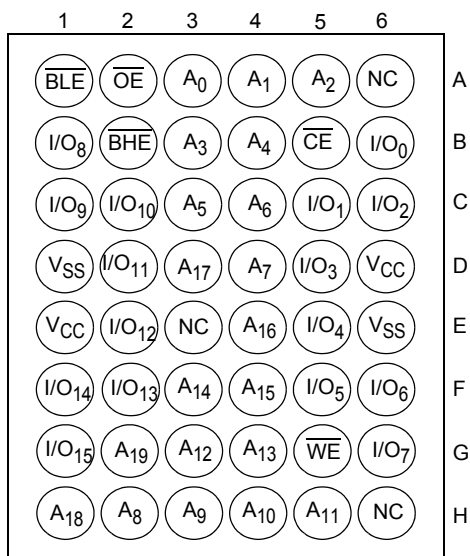


### Notes

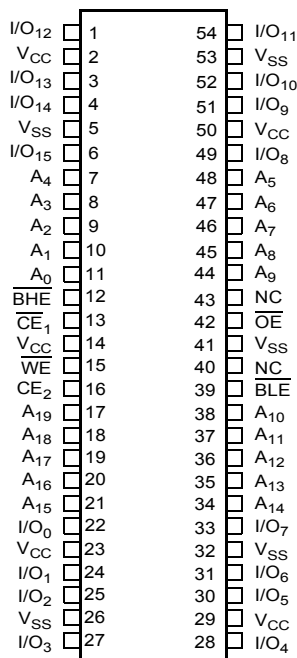
1. NC pins are not connected on the die.
2. In BVXI package, ball H6 is MSB address A19 and ball G2 is NC; in BVJXI package, ball H6 is NC and ball G2 is MSB address A19.

## Pin Configurations (continued)

**Figure 3. 48-ball VFBGA (8 × 9.5 × 1 mm) Single Chip Enable (-BV1XI) (Top View)** <sup>[3, 4]</sup>



**Figure 4. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Top View)** <sup>[3]</sup>



### Notes

- NC pins are not connected on the die.
- In BV1XI package, ball A6 is NC, ball H6 is NC and ball G2 is MSB address A19. BV1XI package has only single Chip Enable ( $\overline{CE}$ ).

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage on  $V_{CC}$   
relative to GND <sup>[5]</sup> ..... -0.5 V to +4.6 V

DC Voltage Applied to Outputs  
in High Z State <sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage <sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V $\pm$ 0.3 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}$ , $I_{OH} = -4.0$ mA	2.4	–	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}$ , $I_{OL} = 8.0$ mA	–	0.4	V
$V_{IH}$	Input HIGH voltage	–	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[5]</sup>	–	-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1	+1	$\mu$ A
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}$ , $f = f_{MAX} = 1/t_{RC}$ , $I_{OUT} = 0$ mA, CMOS levels	–	175	mA
$I_{SB1}$	Automatic CE power down current – TTL inputs	Max $V_{CC}$ , $\overline{CE}_1 \geq V_{IH}$ , $CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	–	30	mA
$I_{SB2}$	Automatic CE power down current – CMOS inputs	Max $V_{CC}$ , $\overline{CE}_1 \geq V_{CC} - 0.3$ V, $CE_2 \leq 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$	–	25	mA

### Note

5.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.

## Capacitance

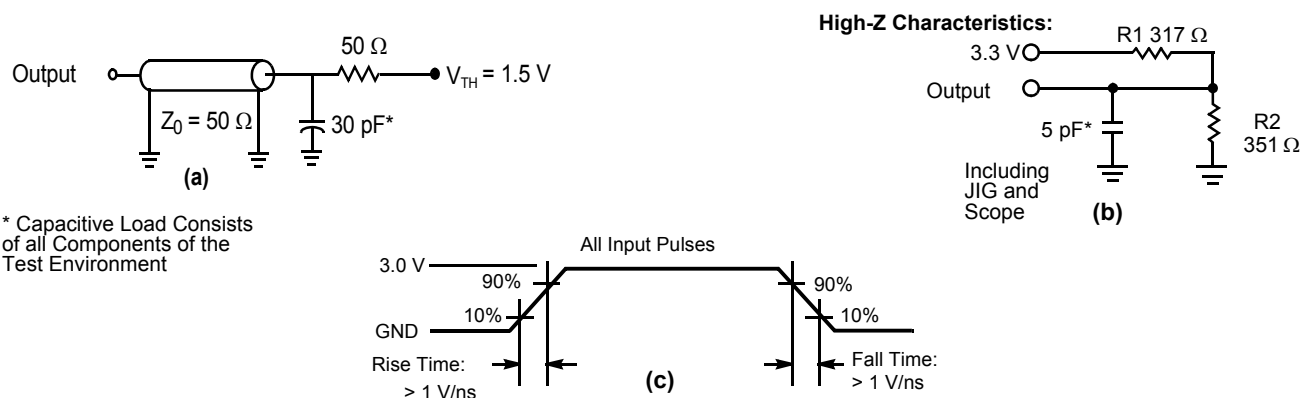
Parameter <sup>[6]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	6	8	pF
$C_{OUT}$	I/O Capacitance		8	10	pF

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four layer printed circuit board	24.18	28.37	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		5.40	5.79	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms <sup>[7]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0 V). 100  $\mu\text{s}$  ( $t_{\text{power}}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation begins including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0 V) voltage.

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[8]</sup>	Description	-10		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub>	V <sub>CC</sub> (typical) to the first access <sup>[9]</sup>	100	–	μs
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub>	Address to data valid	–	10	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to data valid	–	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[10]</sup>	1	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[10]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to low Z <sup>[10]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}_1$ HIGH/CE <sub>2</sub> LOW to high Z <sup>[10]</sup>	–	5	ns
t <sub>PU</sub>	$\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to power-up <sup>[11]</sup>	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}_1$ HIGH/CE <sub>2</sub> LOW to power-down <sup>[11]</sup>	–	10	ns
t <sub>DBE</sub>	Byte enable to data valid	–	5	ns
t <sub>LZBE</sub>	Byte enable to low Z	1	–	ns
t <sub>HZBE</sub>	Byte disable to high Z	–	5	ns
Write Cycle <sup>[12, 13]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to write end	7	–	ns
t <sub>AW</sub>	Address setup to write end	7	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7	–	ns
t <sub>SD</sub>	Data setup to write end	5.5	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to low Z <sup>[10]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to high Z <sup>[10]</sup>	–	5	ns
t <sub>BW</sub>	Byte Enable to End of Write	7	–	ns

### Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of Figure 5 on page 6, unless specified otherwise.
9.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
10.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ ,  $t_{\text{LZWE}}$ , and  $t_{\text{LZBE}}$  are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 6. Transition is measured  $\pm 200$  mV from steady state voltage.
11. These parameters are guaranteed by design and are not tested.
12. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . Chip enables must be active and  $\overline{\text{WE}}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

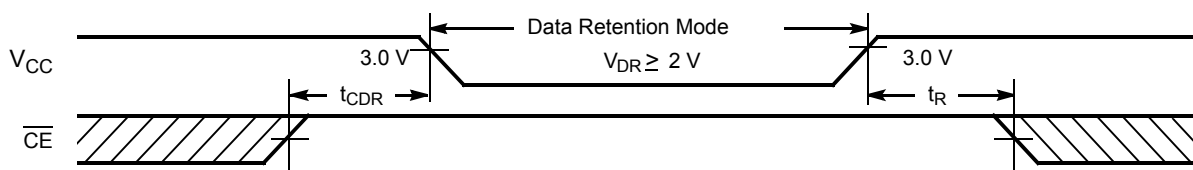
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	–	2	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	25	mA
$t_{CDR}^{[14]}$	Chip deselect to data retention time	–	0	–	ns
$t_R^{[15]}$	Operation recovery time	–	$t_{RC}$	–	ns

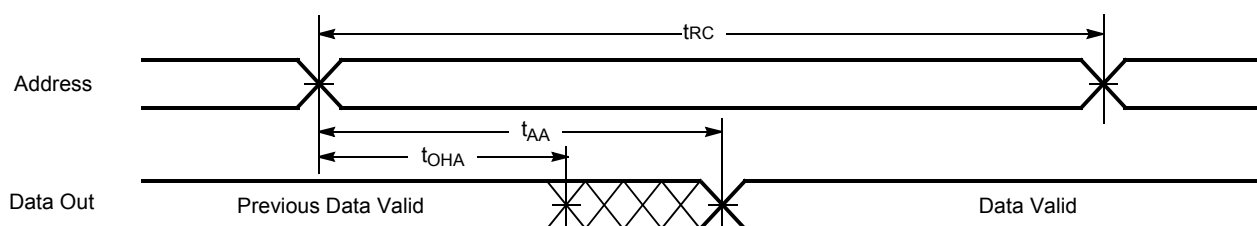
## Data Retention Waveform

Figure 6. Data Retention Waveform <sup>[16]</sup>



## Switching Waveforms

Figure 7. Read Cycle No. 1 (Address Transition Controlled) <sup>[17, 18]</sup>



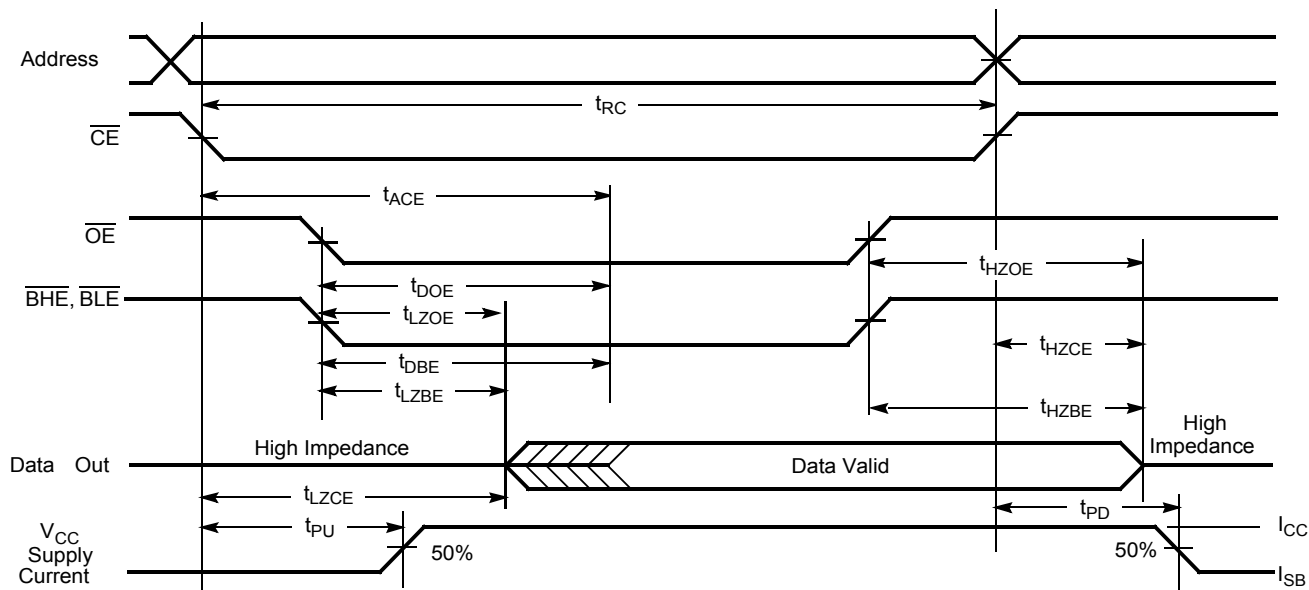
### Notes

14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ .
16. For all packages except -BV1XI,  $\overline{CE}$  is the logical combination of  $CE_1$  and  $CE_2$ . When  $CE_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH. For -BV1XI package,  $\overline{CE}$  refers to  $CE$ .
17. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ .
18.  $\overline{WE}$  is HIGH for read cycle.

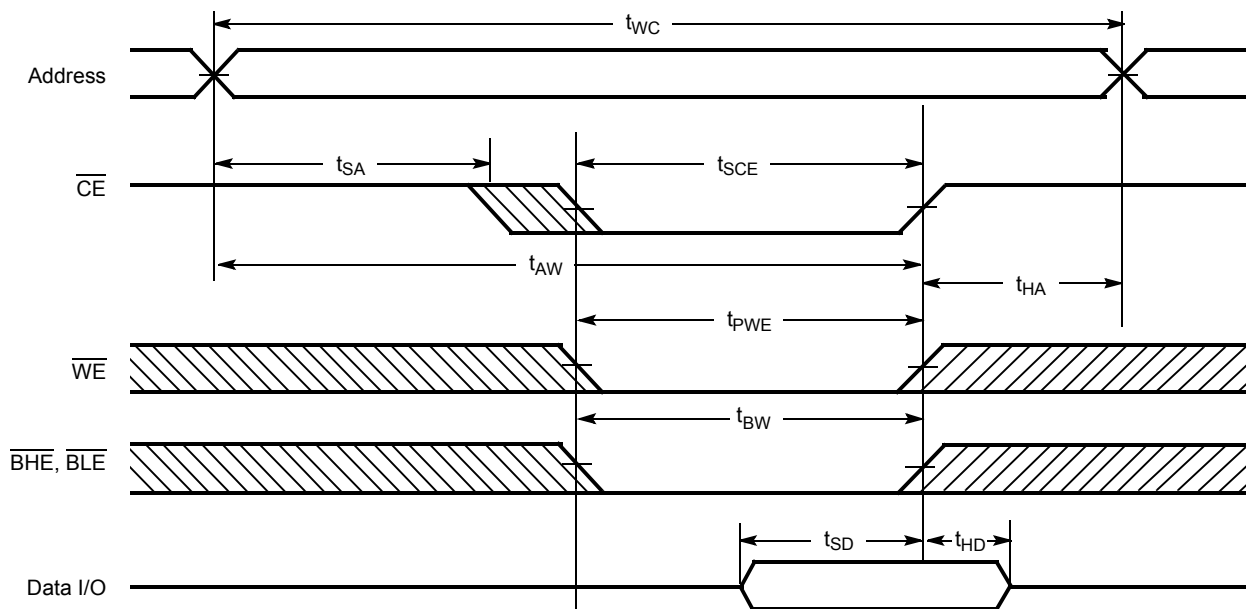


## Switching Waveforms (continued)

**Figure 8. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [19, 20, 21]



**Figure 9. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [19, 22, 23]



### Notes

19. For all packages except -BV1XI,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH. For -BV1XI package,  $\overline{\text{CE}}$  refers to  $\text{CE}_1$ .
20.  $\overline{\text{WE}}$  is HIGH for read cycle.
21. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.
22. Data I/O is high impedance if  $\overline{\text{OE}}$ , BHE, and/or BLE =  $V_{\text{IH}}$ .
23. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

## Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [24, 25, 26]

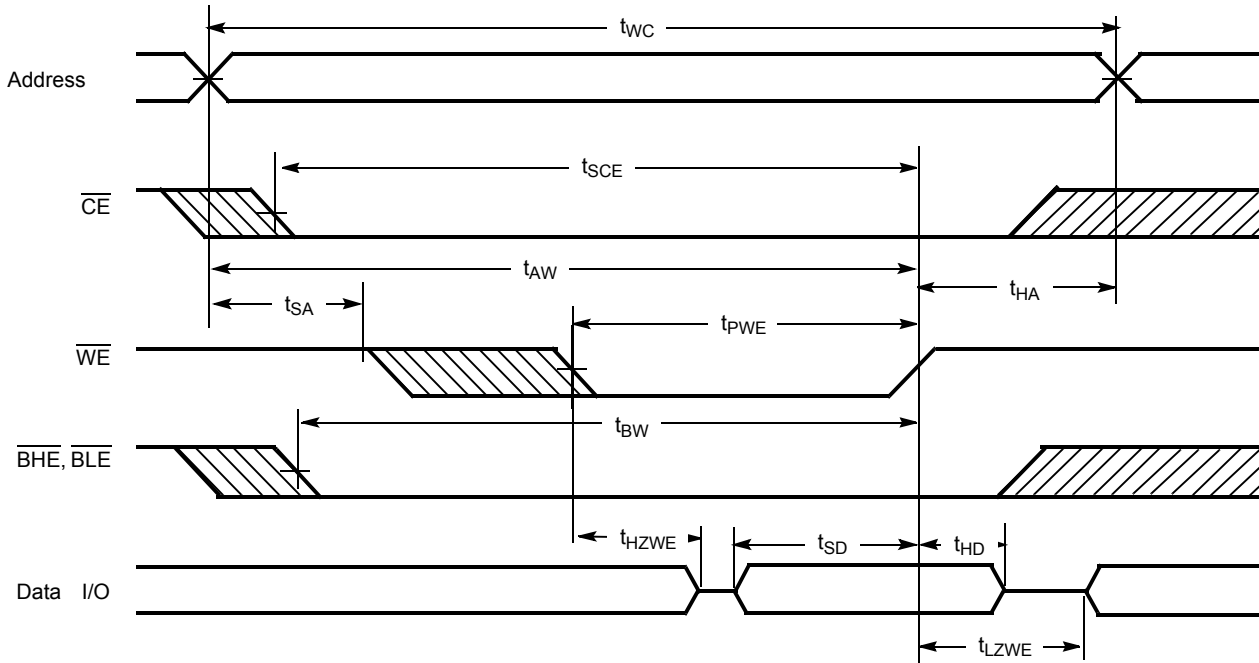
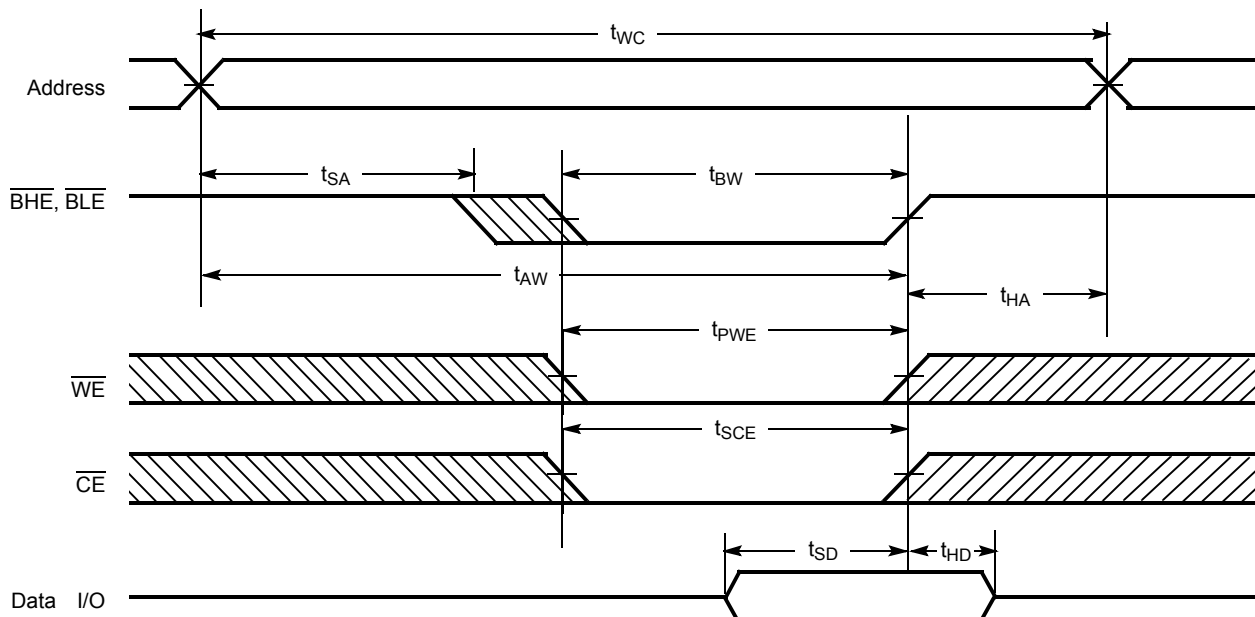


Figure 11. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [24]



### Notes

24. For all packages except -BV1XI,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH. For -BV1XI package,  $\overline{\text{CE}}$  refers to  $\overline{\text{CE}}$ .
25. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .
26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

## Truth Table

For all packages except -BV1XI

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

## Truth Table

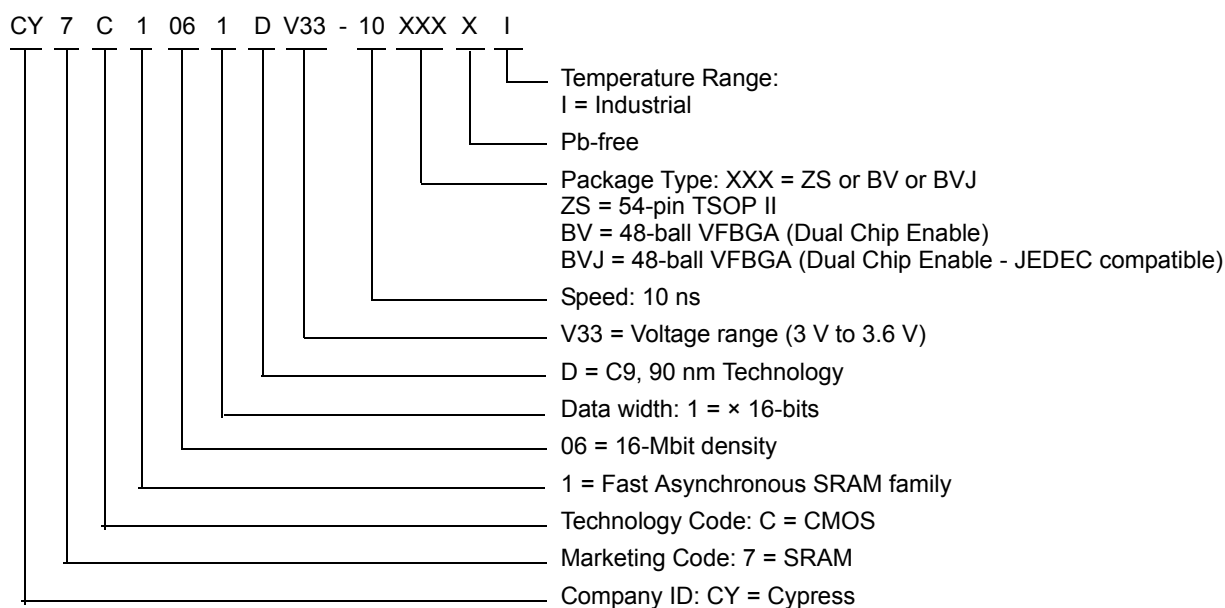
For -BV1XI package only

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061DV33-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Pb-free)	Industrial
	CY7C1061DV33-10BVXI	51-85178	48-ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Dual Chip Enable)	
	CY7C1061DV33-10BVJXI		48-ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Dual Chip Enable - JEDEC compatible)	
	CY7C1061DV33-10BV1XI		48-ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Single Chip Enable)	

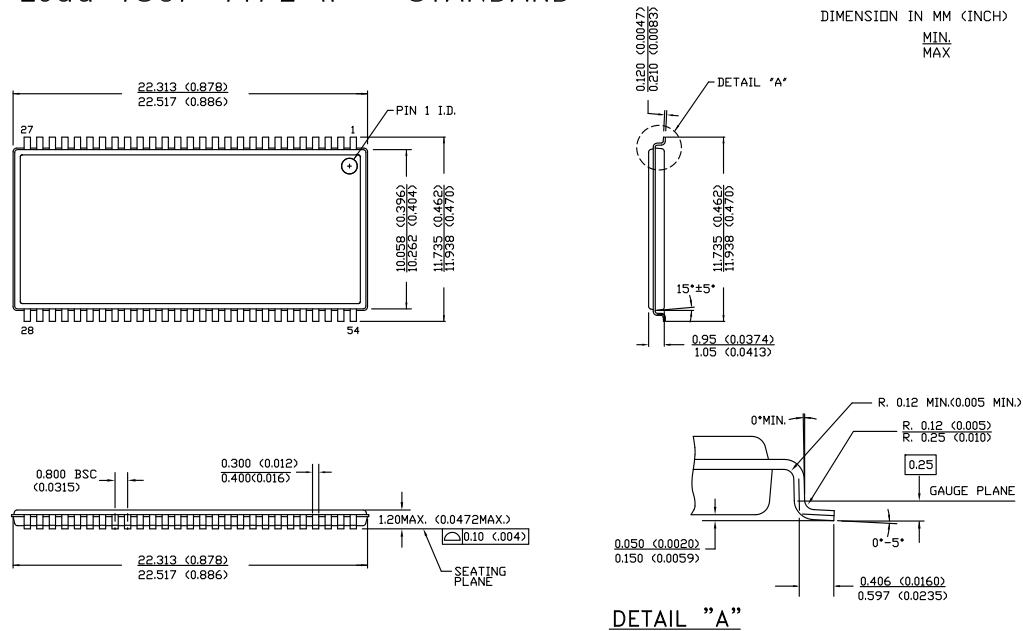
## Ordering Code Definitions



## Package Diagrams

Figure 12. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160

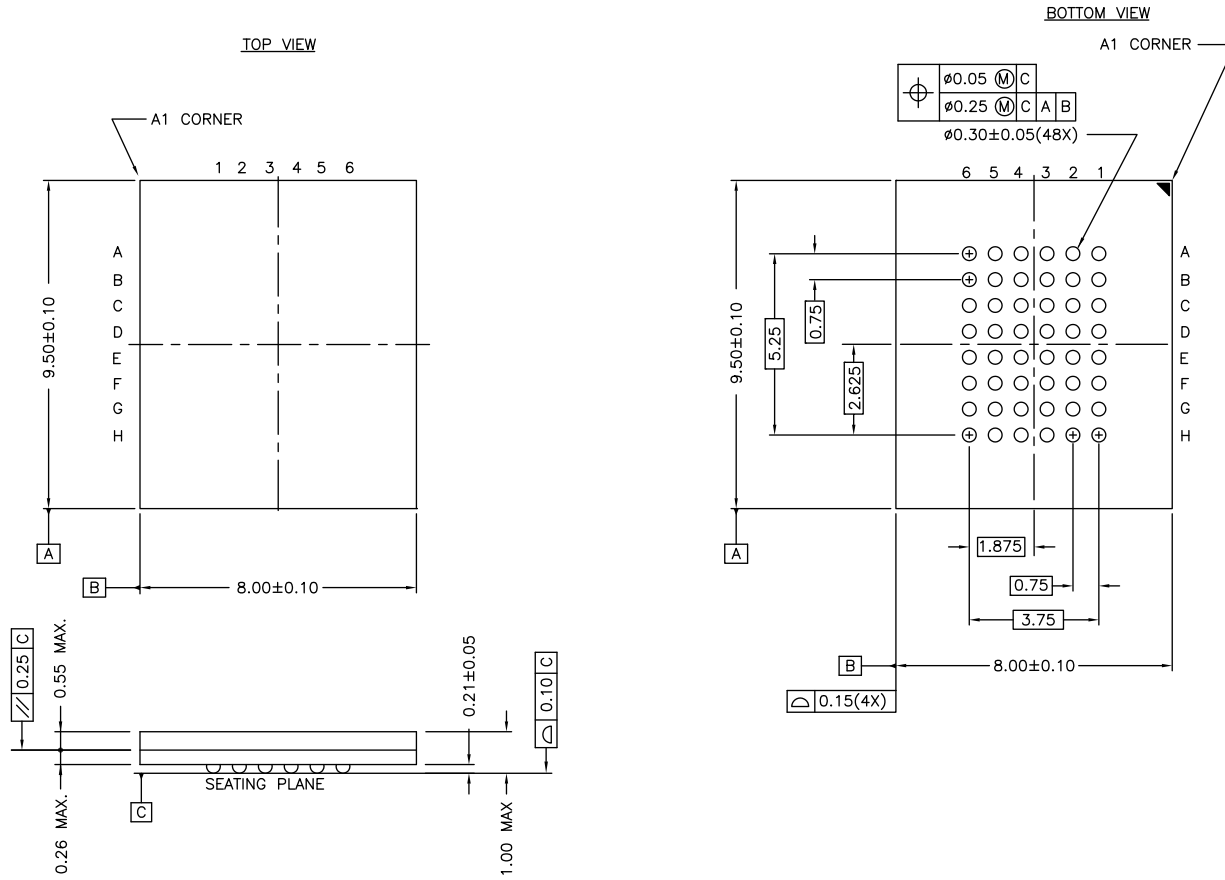
### 54 Lead TSOP TYPE II – STANDARD



51-85160 \*E

Package Diagrams (continued)

Figure 13. 48-ball VFBGA ( $8 \times 9.5 \times 1.0$  mm) BV48B Package Outline, 51-85178



51-85178 °C

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1061DV33, 16-Mbit (1 M × 16) Static RAM Document Number: 38-05476				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance data sheet for C9 IPP
*A	233748	RKF	See ECN	AC, DC parameters are modified as per EROS (Specification number 01-2165) Added Pb-free devices in the Ordering Information
*B	469420	NXR	See ECN	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed –8 and –12 speed bins from product offering Removed Commercial Operating Range Changed 2G-Ball of FBGA and pin 40 of TSOPII from DNU to NC Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed I <sub>CC(Max)</sub> from 220 mA to 125 mA Changed I <sub>SB1(Max)</sub> from 70 mA to 30 mA Changed I <sub>SB2(Max)</sub> from 40 mA to 25 mA Specified the Overshoot specification in footnote 1. Updated the Ordering Information Table
*C	499604	NXR	See ECN	Added note 1 for NC pins Updated Test Condition for I <sub>CC</sub> in DC Electrical Characteristics table Updated the 48-Ball FBGA Package
*D	1462583	VKN / AESA	See ECN	Converted from preliminary to final Changed I <sub>CC</sub> specification from 125 mA to 175 mA Updated thermal specs
*E	2704415	VKN / PYRS	05/11/09	Included 48 FBGA -BVJXI package Added footnote #2
*F	3109102	AJU	12/13/2010	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*G	3126531	PRAS	01/03/2011	Added 48-ball VFBGA Single Chip Enable package. Updated Ordering Information. Added <a href="#">Acronyms</a> .
*H	3414708	TAVA	10/19/2011	Updated <a href="#">Features</a> . Updated <a href="#">DC Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Units of Measure</a> . Updated in new template.
*I	4574311	TAVA	11/19/2014	Added related documentation hyperlink in page 1. Updated the following figures in <a href="#">Package Diagrams</a> : <a href="#">Figure 12</a> (spec 51-85160 *C to *E) and <a href="#">Figure 13</a> (spec 51-85178 *A to *C).



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