# 87C51FB
# CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

**16K Bytes User Programmable EPROM**

**87C51FB—3.5 MHz to 12 MHz, $V_{CC}$ = 5V ± 10%**

**87C51FB-1—3.5 MHz to 16 MHz, $V_{CC}$ = 5V ± 10%**

**87C51FB-2—0.5 MHz to 12 MHz, $V_{CC}$ = 5V ± 10%**

- High Performance CHMOS EPROM
- Three 16-Bit Timer/Counters
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer capabilities
- Up/Down Timer/Counter
- Two Level Program Lock System
- 16K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Quick Pulse Programming™ Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE™ (On-Circuit Emulation) Mode

## MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16K bytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64K bytes of external data memory.

The Intel 87C51FB is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C51FB uses the same powerful instruction set, has the same architecture, and is pin for pin compatible with the existing MCS-51 family of products. The 87C51FB is an enhanced version of the 87C51. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.



October 1989
Order Number: 270563-003

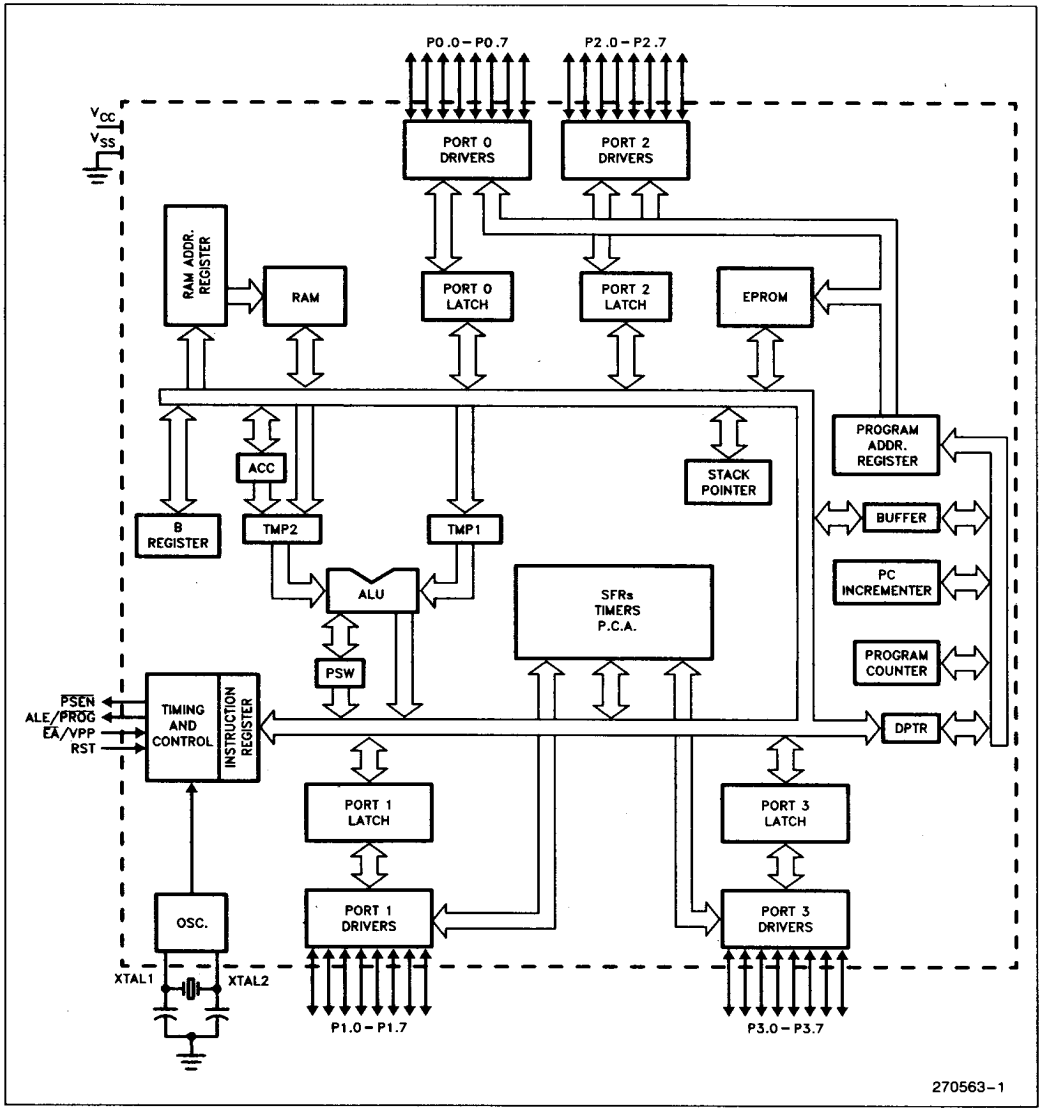


**Figure 1. 87C51FB Block Diagram**

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## PACKAGES

| Part | Prefix | Package Type |
|---|---|---|
| 87C51FB | P | 40-Pin Plastic DIP |
| | D | 40-Pin CERDIP |
| | N | 44-Pin PLCC |

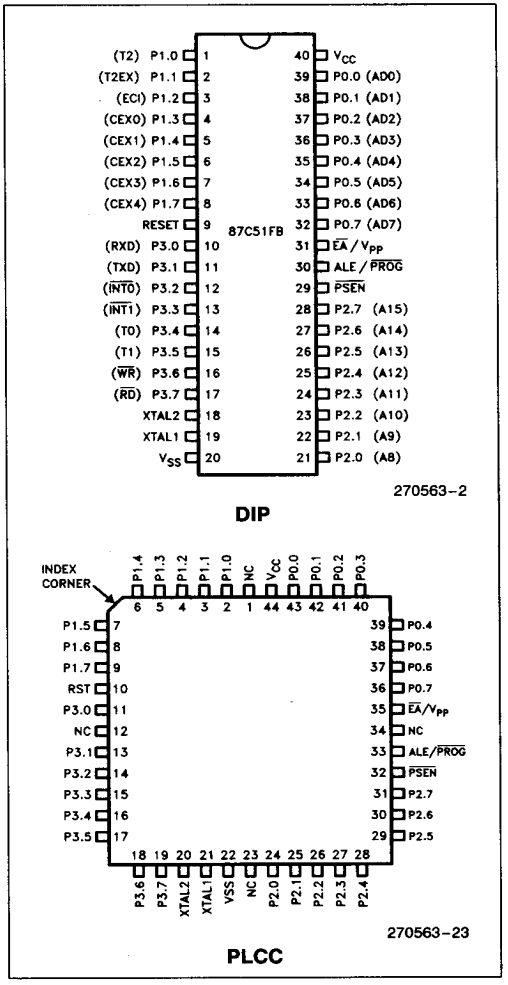


**Figure 2. Pin Connections**

## PIN DESCRIPTIONS

$V_{CC}$: Supply voltage.

$V_{SS}$: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 87C51FB:

| Port Pin | Alternate Function |
|---|---|
| P1.0 | T2 (External Count Input to Timer/ Counter 2) |
| P1.1 | T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control) |
| P1.2 | ECI (External Count Input to the PCA) |
| P1.3 | CEX0 (External I/O for Compare/ Capture Module 0) |
| P1.4 | CEX1 (External I/O for Compare/ Capture Module 1) |
| P1.5 | CEX2 (External I/O for Compare/ Capture Module 2) |
| P1.6 | CEX3 (External I/O for Compare/ Capture Module 3) |
| P1.7 | CEX4 (External I/O for Compare/ Capture Module 4) |

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

| Port Pin | Alternate Function |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (external interrupt 0) |
| P3.3 | $\overline{INT1}$ (external interrupt 1) |
| P3.4 | T0 (Timer 0 external input) |
| P3.5 | T1 (Timer 1 external input) |
| P3.6 | $\overline{WR}$ (external data memory write strobe) |
| P3.7 | $\overline{RD}$ (external data memory read strobe) |

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset with only a capacitor connected to $V_{CC}$.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 87C51FB is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/$V_{PP}$: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to $V_{CC}$ for internal program executions.

This pin also receives the programming supply voltage ($V_{PP}$) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the $V_{IL}$ and $V_{IH}$ specifications the capacitance will not exceed 20 pF.

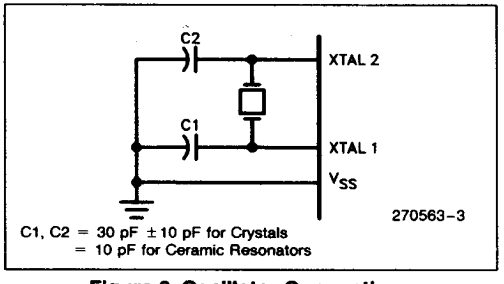


**Figure 3. Oscillator Connections**

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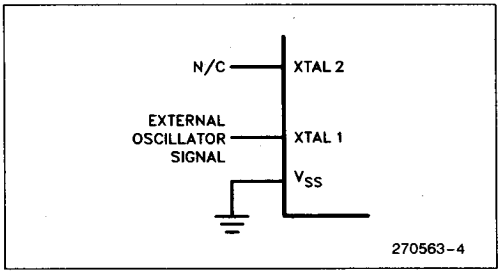


**Figure 4. External Clock Drive Configuration**

## IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

## POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 87C51FB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before $V_{CC}$ is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

## DESIGN CONSIDERATION

- Ambient light is known to affect the internal RAM contents during operation. If the 87C51FB application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## ONCE™ MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 87C51FB without the 87C51FB having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

**Table 1. Status of the External Pins during Idle and Power Down**

| Mode | Program Memory | ALE | $\overline{PSEN}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

**NOTE:**
For more detailed information on the reduced power modes refer to current Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on EA/$V_{PP}$ Pin to $V_{SS}$ . . . . . 0V to +13.0V
Voltage on Any Other Pin to $V_{SS}$ . . −0.5V to +6.5V
$I_{OL}$ Per I/O Pin . . . . . 15 mA
Power Dissipation . . . . . 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

## D.C. CHARACTERISTICS: ($T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V)

| Symbol | Parameter | Min | Typ (Note 4) | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.5 | | 0.2 $V_{CC}$ − 0.1 | V | |
| $V_{IL1}$ | Input Low Voltage $\overline{EA}$ | 0 | | 0.2 $V_{CC}$ − 0.3 | V | |
| $V_{IH}$ | Input High Voltage (Except XTAL1, RST) | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage (XTAL1, RST) | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage (Note 5) (Ports 1, 2, and 3) | | | 0.3 | V | $I_{OL}$ = 100 µA (Note 1) |
| | | | | 0.45 | V | $I_{OL}$ = 1.6 mA (Note 1) |
| | | | | 1.0 | V | $I_{OL}$ = 3.5 mA (Note 1) |
| $V_{OL1}$ | Output Low Voltage (Note 5) (Port 0, ALE, $\overline{PSEN}$) | | | 0.3 | V | $I_{OL}$ = 200 µA (Note 1) |
| | | | | 0.45 | V | $I_{OL}$ = 3.2 mA (Note 1) |
| | | | | 1.0 | V | $I_{OL}$ = 7.0 mA (Note 1) |
| $V_{OH}$ | Output High Voltage (Ports 1, 2, and 3) | $V_{CC}$ − 0.3 | | | V | $I_{OH}$ = −10 µA |
| | | $V_{CC}$ − 0.7 | | | V | $I_{OH}$ = −30 µA |
| | | $V_{CC}$ − 1.5 | | | V | $I_{OH}$ = −60 µA |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$) | $V_{CC}$ − 0.3 | | | V | $I_{OH}$ = −200 µA |
| | | $V_{CC}$ − 0.7 | | | V | $I_{OH}$ = −3.2 mA |
| | | $V_{CC}$ − 1.5 | | | V | $I_{OH}$ = −7.0 mA |
| $I_{IL}$ | Logical 0 Input Current (Ports 1, 2, and 3) | | | −50 | µA | $V_{IN}$ = 0.45V |
| $I_{LI}$ | Input leakage Current (Port 0) | | | ±10 | µA | 0.45 < $V_{IN}$ < $V_{CC}$ − 0.3V |
| $I_{TL}$ | Logical 1 to 0 Transition Current (Ports 1, 2, and 3) | | | −650 | µA | $V_{IN}$ = 2V |
| RRST | RST Pulldown Resistor | 40 | | 225 | KΩ | |
| CIO | Pin Capacitance | | | 10 | pF | @1 MHz, 25°C |
| $I_{CC}$ | Power Supply Current: | | | | | (Note 3) |
| | Running at 12 MHz (Figure 5) | | 20 | 40 | mA | |
| | Idle Mode at 12 MHz (Figure 5) | | 5 | 10 | mA | |
| | Power Down Mode | | 15 | 100 | µA | |

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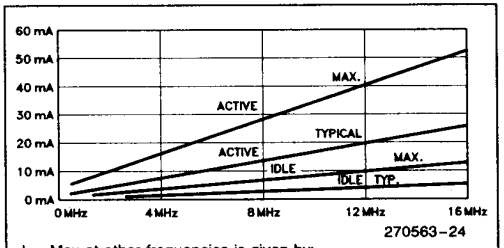
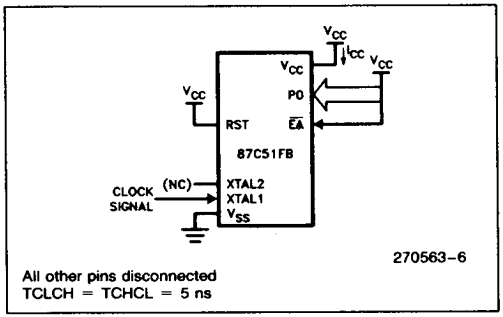
**NOTES:**
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE signal may exceed 0.8V. In these cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an Address Latch with a Schmitt Trigger Strobe input.
2. Capacitive loading on Ports 0 and 2 cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to drop below the 0.9 $V_{CC}$ specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum $V_{CC}$ for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10mA
   Maximum $I_{OL}$ per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA

If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



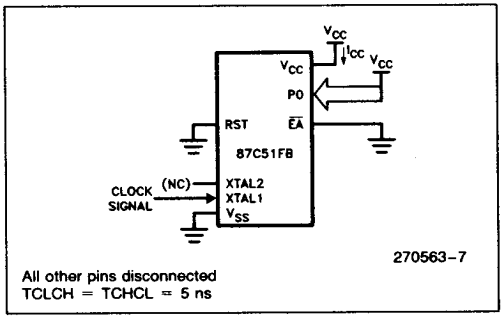

$I_{CC}$ Max at other frequencies is given by:
Active Mode
$I_{CC}$ max = (Osc freq × 3) + 4
Idle Mode
$I_{CC}$ max = (Osc freq × 0.5) + 4
Where Osc Freq is in MHz and $I_{CC}$ is in mA.

**Figure 5. $I_{CC}$ vs Frequency**



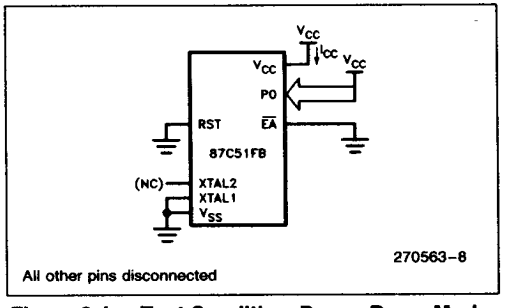

All other pins disconnected
TCLCH = TCHCL = 5 ns

**Figure 6. $I_{CC}$ Test Condition, Active Mode**




All other pins disconnected
TCLCH = TCHCL = 5 ns

**Figure 7. $I_{CC}$ Test Condition Idle Mode**




All other pins disconnected

**Figure 8. $I_{CC}$ Test Condition, Power Down Mode. $V_{CC}$ = 2.0V to 5.5V.**

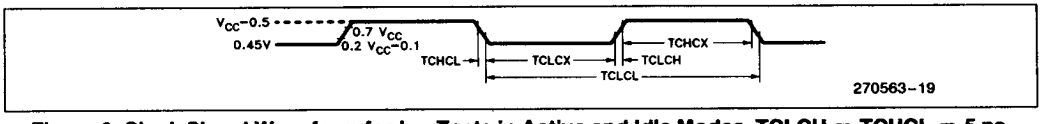



**Figure 9. Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.**

## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

## A.C. CHARACTERISTICS ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±10%, $V_{SS}$ = 0V, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

**ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION**

### EXTERNAL PROGRAM MEMORY CHARACTERISTICS

| Symbol | Parameter | 12 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1/TCLCL | Oscillator Frequency | | | 0.5 | 16 | MHz |
| TLHLL | ALE Pulse Width | 127 | | 2TCLCL−40 | | ns |
| TAVLL | Address Valid to ALE Low | 43 | | TCLCL−40 | | ns |
| TLLAX | Address Hold After ALE Low | 53 | | TCLCL−30 | | ns |
| TLLIV | ALE Low to Valid Instruction In | | 234 | | 4TCLCL−100 | ns |
| TLLPL | ALE Low to $\overline{PSEN}$ Low | 53 | | TCLCL−30 | | ns |
| TPLPH | $\overline{PSEN}$ Pulse Width | 205 | | 3TCLCL−45 | | ns |
| TPLIV | $\overline{PSEN}$ Low to Valid Instruction In | | 145 | | 3TCLCL−105 | ns |
| TPXIX | Input Instruction Hold After $\overline{PSEN}$ | 0 | | 0 | | ns |
| TPXIZ | Input Instruction Float After $\overline{PSEN}$ | | 59 | | TCLCL−25 | ns |
| TAVIV | Address to Valid Instruction In | | 312 | | 5TCLCL−105 | ns |
| TPLAZ | $\overline{PSEN}$ Low to Address Float | | 10 | | 10 | ns |
| TRLRH | $\overline{RD}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TWLWH | $\overline{WR}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TRLDV | $\overline{RD}$ Low to Valid Data In | | 252 | | 5TCLCL−165 | ns |
| TRHDX | Data Hold After $\overline{RD}$ | 0 | | 0 | | ns |
| TRHDZ | Data Float After $\overline{RD}$ | | 107 | | 2TCLCL−60 | ns |
| TLLDV | ALE Low to Valid Data In | | 517 | | 8TCLCL−150 | ns |
| TAVDV | Address to Valid Data In | | 585 | | 9TCLCL−165 | ns |
| TLLWL | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | 3TCLCL−50 | 3TCLCL+50 | ns |
| TAVWL | Address Valid to $\overline{WR}$ Low | 203 | | 4TCLCL−130 | | ns |
| TQVWX | Data Valid before $\overline{WR}$ | 33 | | TCLCL−50 | | ns |
| TWHQX | Data Hold after $\overline{WR}$ | 33 | | TCLCL−50 | | ns |
| TQVWH | Data Valid to $\overline{WR}$ High | 433 | | 7TCLCL−150 | | ns |
| TRLAZ | $\overline{RD}$ Low to Address Float | | 0 | | 0 | ns |
| TWHLH | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | TCLCL−40 | TCLCL+40 | ns |

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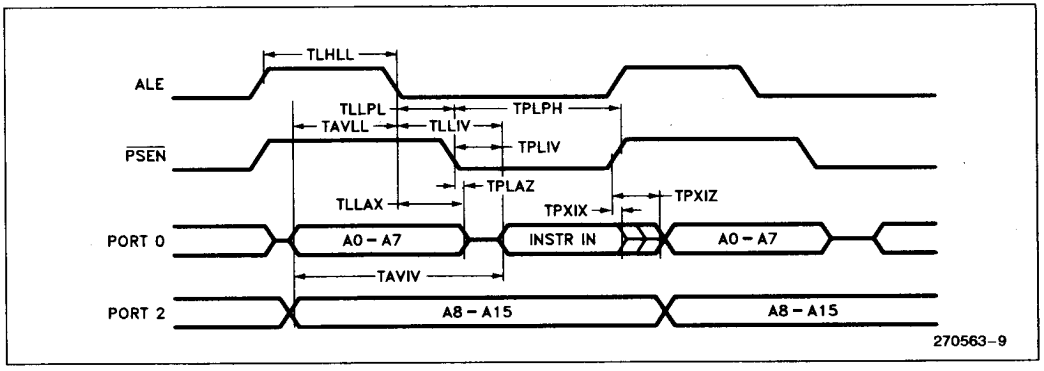
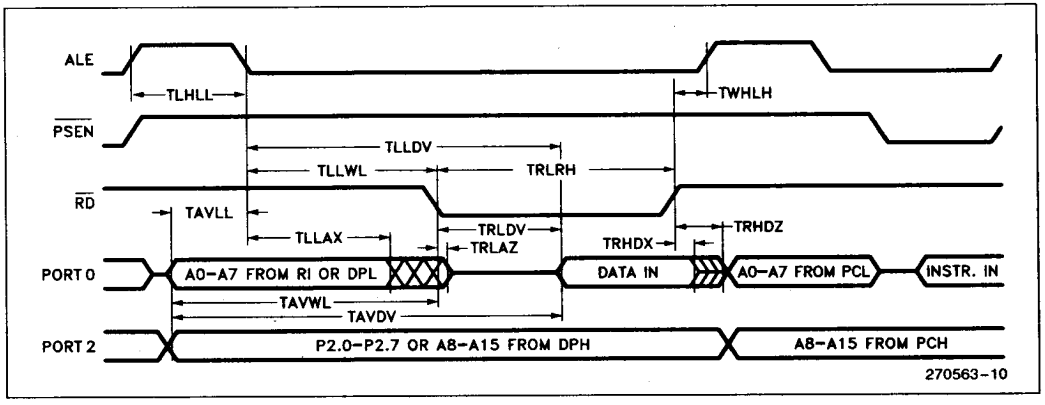
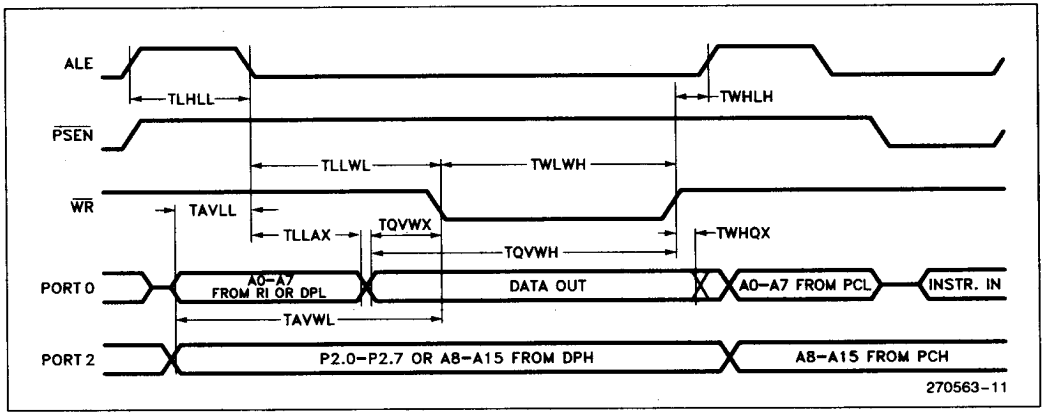
## EXTERNAL PROGRAM MEMORY READ CYCLE




## EXTERNAL DATA MEMORY READ CYCLE




## EXTERNAL DATA MEMORY WRITE CYCLE

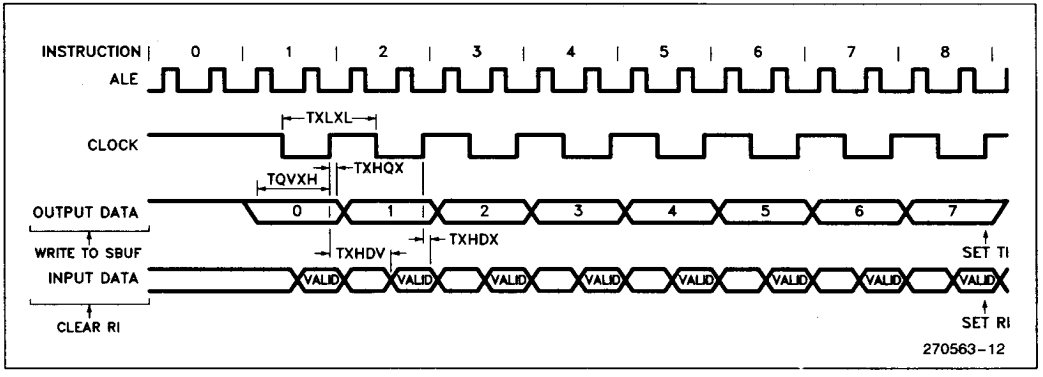


## SERIAL PORT TIMING - SHIFT REGISTER MODE

**Test Conditions:** $T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V; Load Capacitance = 80 pF

| Symbol | Parameter | 12 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TXLXL | Serial Port Clock Cycle Time | 1 | | 12TCLCL | | µs |
| TQVXH | Output Data Setup to Clock Rising Edge | 700 | | 10TCLCL−133 | | ns |
| TXHQX | Output Data Hold after Clock Rising Edge | 50 | | 2TCLCL−117 | | ns |
| TXHDX | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| TXHDV | Clock Rising Edge to Input Data Valid | | 700 | | 10TCLCL−133 | ns |

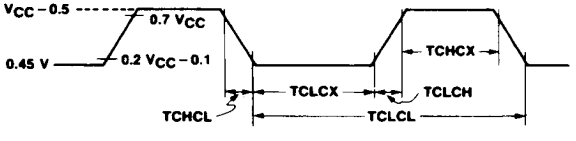
## SHIFT REGISTER MODE TIMING WAVEFORMS




## EXTERNAL CLOCK DRIVE

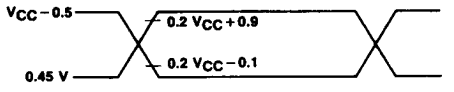
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 1/TCLCL | Oscillator Frequency<br>87C51FB<br>87C51FB-1<br>87C51FB-2 | <br>3.5<br>3.5<br>0.5 | <br>12<br>16<br>12 | MHz |
| TCHCX | High Time | 20 | | ns |
| TCLCX | Low Time | 20 | | ns |
| TCLCH | Rise Time | | 20 | ns |
| TCHCL | Fall Time | | 20 | ns |

## EXTERNAL CLOCK DRIVE WAVEFORM



### A.C. TESTING INPUT

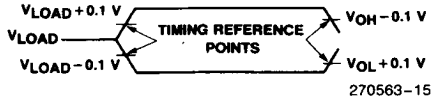
**Input, Output Waveforms**




270563-14

AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at $V_{IH}$ min for a Logic "1" and $V_{IL}$ max for a Logic "0".

**Float Waveforms**




270563-15

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

## EPROM CHARACTERISTICS

Table 2 shows the logic levels for programming the Program Memory, the Encryption Table, and the Lock Bits and for reading the signature bytes.

**Table 2. EPROM Programming Modes**

| Mode | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}$/$V_{PP}$ | P2.7 | P2.6 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|
| Program Code Data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify Code Data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Program Encryption Table Use Addresses 0–1FH | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 0 | 1 |
| Program Lock x = 1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Bits (LBx) x = 2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |
| Read Signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**NOTES:**
"1" = Valid high for that pin
"0" = Valid low for that pin
"VPP" = +12.75V ±0.25V
* ALE/$\overline{PROG}$ is pulsed low for 100 μs for programming. (Quick-Pulse Programming™)

## PROGRAMMING THE EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal EPROM locations.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.5 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST, $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 2. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 10.

Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to $V_{PP}$, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches.

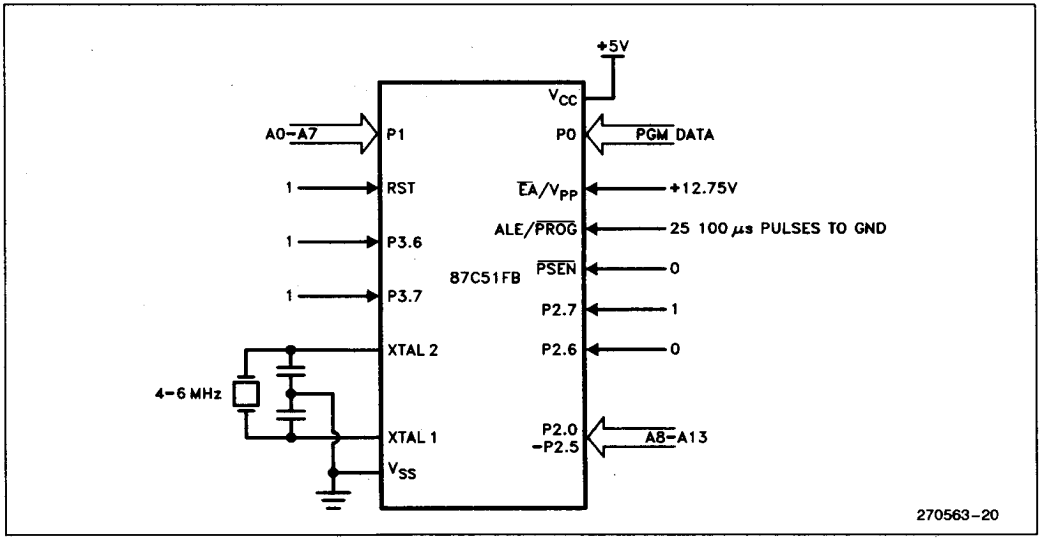



**Figure 10. Programming the EPROM**

## Quick-Pulse Programming™ Algorithm

The 87C51FB can be programmed using the Quick-Pulse Programming™ Algorithm for microcontrollers. The features of the new programming method are a lower $V_{PP}$ (12.75V as compared to 21V) and a shorter programming pulse. It is possible to program the entire 16K Bytes of EPROM memory in less than 50 seconds with this algorithm!

To program the part using the new algorithm, $V_{PP}$ must be 12.75V ±0.25V. ALE/$\overline{PROG}$ is pulsed low for 100 µs, 25 times as shown in Figure 11. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 2. The only difference in programming Program Lock features is that the Program Lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

## Program Verification

If the Program Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.5. The other pins should be held at the "Verify" levels indicated in Table 2. The contents of the addressed locations will come out on Port 0. External pullups are required on Port 0 for this operation.

If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.

The setup, which is shown in Figure 12, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active-low read strobe.

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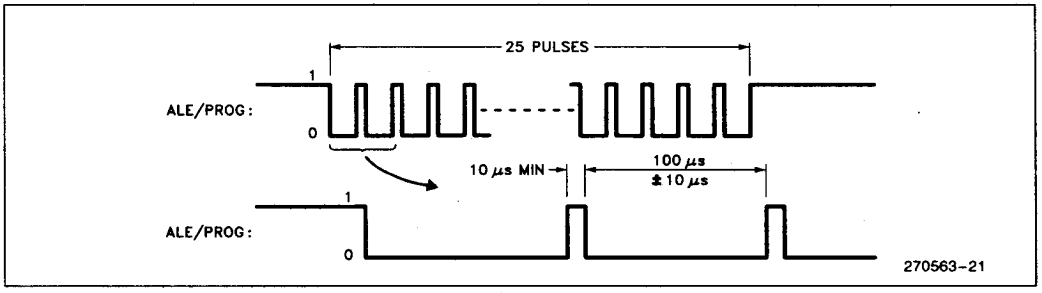


**Figure 11. $\overline{\text{PROG}}$ Waveforms**

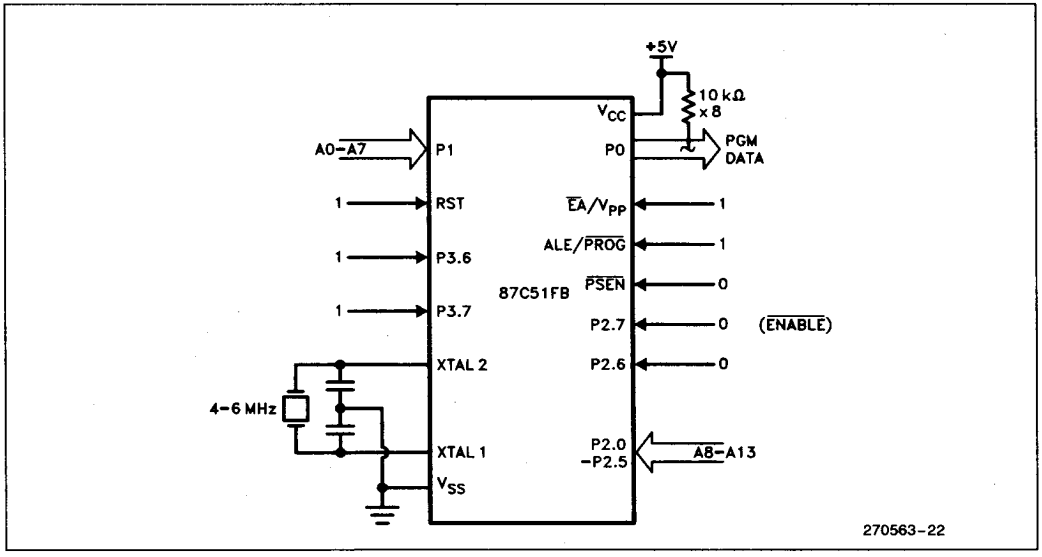


**Figure 12. Verifying the EPROM**

## EPROM Program Lock

The two-level Program Lock system consists of two Program Lock bits and a 32 byte Encryption Array which are used to protect the program memory against software piracy.

## Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form.

## Program Lock Bits

Also included in the EPROM Program Lock scheme are two Program Lock Bits which are programmed as shown in Table 2.

Table 3 outlines the features of programming the Lock Bits.

Erasing the EPROM also erases the Encryption Array and the Program Lock Bits, returning the part to full functionality.

## Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufacture by Intel
(031H) = 5FH indicates 87C51FB

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000 $\mu$W/cm$^2$ rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

**Table 3. Program Lock Bits and their Features**

| Program Lock Bits LB1 | LB2 | Logic Enabled |
|---|---|---|
| U | U | No Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array.) |
| P | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled. |
| P | P | Same as above, but Verify is also disabled |
| U | P | Reserved for Future Definition |

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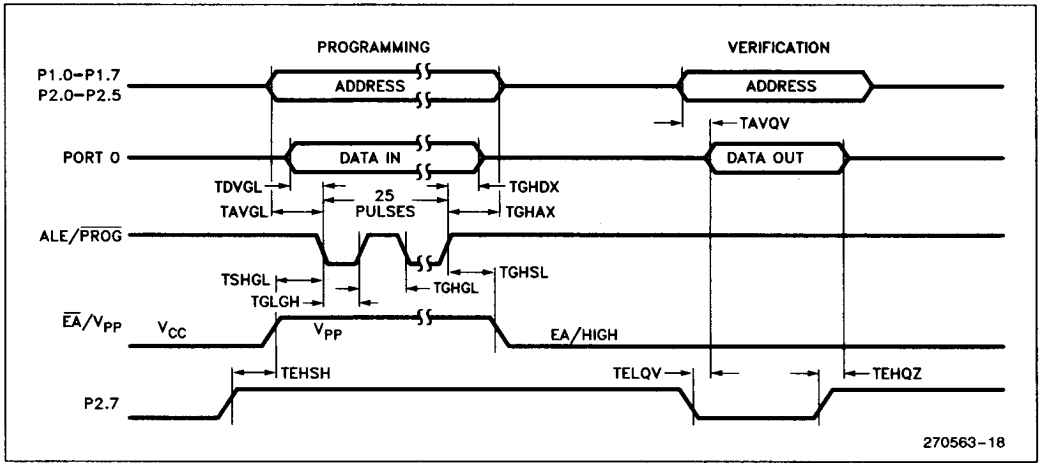
## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

($T_A$ = 21°C to 27°C; $V_{CC}$ = 5V ± 0.25V; $V_{SS}$ = 0V)

### ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 12.5 | 13.0 | V |
| $I_{PP}$ | Programming Supply Current | | 50 | mA |
| 1/TCLCL | Oscillator Frequency | 4 | 6 | MHz |
| TAVGL | Address Setup to $\overline{PROG}$ Low | 48TCLCL | | |
| TGHAX | Address Hold after $\overline{PROG}$ | 48TCLCL | | |
| TDVGL | Data Setup to $\overline{PROG}$ Low | 48TCLCL | | |
| TGHDX | Data Hold after $\overline{PROG}$ | 48TCLCL | | |
| TEHSH | P2.7 (ENABLE) High to $V_{PP}$ | 48TCLCL | | |
| TSHGL | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| TGHSL | $V_{PP}$ Hold after $\overline{PROG}$ | 10 | | µs |
| TGLGH | $\overline{PROG}$ Width | 90 | 110 | µs |
| TAVQV | Address to Data Valid | | 48TCLCL | |
| TELQV | ENABLE Low to Data Valid | | 48TCLCL | |
| TEHQZ | Data Float after ENABLE | 0 | 48TCLCL | |
| TGHGL | $\overline{PROG}$ High to $\overline{PROG}$ Low | 10 | | µs |

## EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



## DATA SHEET REVISION SUMMARY

The following are the key differences between this and the -002 version of the 87C51FB data sheet:

1. Word "maximum" was deleted from the $I_{OL}$ line in the ABSOLUTE MAXIMUM RATINGS.
2. Parameter $V_{IL1}$ was deleted from the DC CHARACTERISTICS.
3. Note 4 was deleted from DC CHARACTERISTICS and from the list of notes and notes were resequenced
4. Parameter $I_{LI1}$ was deleted from the DC CHARACTERISTICS.
5. Figure 5 was replaced to show correct $I_{CC}$ curves.
6. External clock capacitive loading note was added.

The following are the differences between the -002 and the -001 version of the 87C51FB datasheet:

1. Title changed to include -1 and -2 version of the device.
2. PLCC pin connection diagram was added.
3. Package table was added.
4. Exit from power down mode was clarified.
5. Maximum $I_{OL}$ per I/O pin was added to the ABSOLUTE MAXIMUM RATINGS.
6. Note 6 was added to explain the maximum safe current spec.
7. Typical values for ICC table were added.
8. Note 5 was added to explain the test conditions for typical values.
9. Timing specs improved for:
   TLLAX changed from TCLCL − 35 to TCLCL − 30
   TLLPL changed from TCLCL − 40 to TCLCL − 30
   TRHDZ changed from TCLCL − 70 to TCLCL − 60
   TQVWX changed from TCLCL − 60 to TCLCL − 50
   TQVWH was added
10. Data sheet revision summary was added.

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# 87C51FB

*EXPRESS*

- **Extended Temperature Range**
- **3.5 MHz to 12 MHz $V_{CC}$ = 5V ±10%**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the 8051 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with $V_{CC}$ = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.



May 1989
Order Number: 270767-001

## Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

### D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

| Symbol | Parameter | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $I_{OH1}$ | Output High<br>P0, ALE, $\overline{PSEN}$ | $V_{CC} - 0.3$<br>$V_{CC} - 0.7$<br>$V_{CC} - 1.5$ | | V | $I_{OH} = -200\ \mu A$<br>$I_{OH} = -2.5$ mA<br>$I_{OH} = -6.0$ mA |
| $V_{IH1}$ | Input High V (Xtal1, RST) | $0.7\ V_{CC} + 0.1$ | $V_{CC} + 0.5$ | V | |
| $V_{IL}$ | Input Low Voltage | $-0.5$ | $0.2\ V_{CC} - 0.2$ | V | |
| $I_{LI}$ | Input Leakage<br>(P0) | $-10$ | $+10$ | $\mu A$ | $0.45 < V_{IN} < V_{CC}$ |
| $I_{TL}$ | 1 to 0 transition<br>(Ports 1, 2, 3) | | $-825$ | $\mu A$ | $V_{IN} = 2.0V$ |

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**Table 1. Prefix Identification**

| Prefix | Package Type | Temperature Range(2) | Burn-In(3) |
|---|---|---|---|
| D | Cerdip | Commercial | No |
| TD | Cerdip | Extended | No |
| LD | Cerdip | Extended | Yes |

**NOTES:**
2. Commercial temperature range is 0°C to +70°C. Extended temperature range is −40°C to +85°C.
3. Burn-in is dynamic for a minimum time of 168 hours at +125°C, $V_{CC}$ = 6.9V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

**Examples:**

D87C51FB indicates 87C51FB in a cerdip package and specified for commercial temperature range, without burn-in.
LD87C51FB indicates 87C51FB in a cerdip package and specified for extended temperature range with burn-in.