

**SN54LVTH540, SN74LVTH540
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

SCBS681G – MARCH 1997 – REVISED OCTOBER 2003

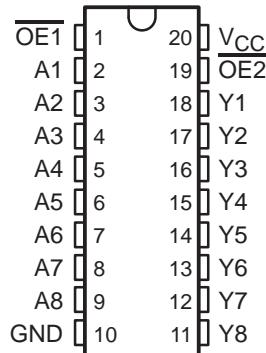
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

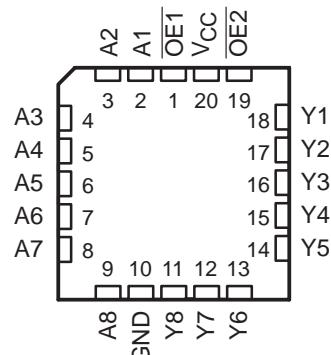
These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH540 devices are ideal for driving bus lines or buffer-memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

**SN54LVTH540 . . . J OR W PACKAGE
SN74LVTH540 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)**



**SN54LVTH540 . . . FK PACKAGE
(TOP VIEW)**



ORDERING INFORMATION

| T_A | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|----------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74LVTH540DW | LVTH540 |
| | | Tape and reel | SN74LVTH540DWR | |
| | SOP – NS | Tape and reel | SN74LVTH540NSR | LVTH540 |
| | SSOP – DB | Tape and reel | SN74LVTH540DBR | LXH540 |
| | TSSOP – PW | Tube | SN74LVTH540PW | LXH540 |
| | | Tape and reel | SN74LVTH540PWR | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54LVTH540J | SNJ54LVTH540J |
| | CFP – W | Tube | SNJ54LVTH540W | SNJ54LVTH540W |
| | LCCC - FK | Tube | SNJ54LVTH540FK | SNJ54LVTH540FK |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

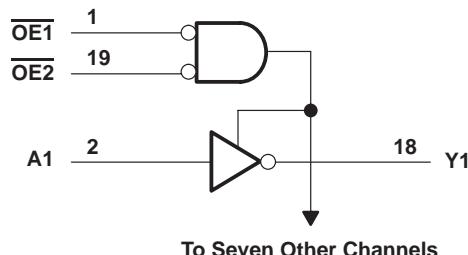
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|--------|-----|---|-------------|
| OE1 | OE2 | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 4)

| | | SN54LVTH540 | | SN74LVTH540 | | UNIT |
|---------------------|------------------------------------|-------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | | 5.5 | | 5.5 | V |
| I _{OH} | High-level output current | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54LVTH540 | | | SN74LVTH540 | | | UNIT |
|--------------------|--|--|-------------------------------------|-------------|----------------|-----------|------|---------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$ | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | | V |
| | $V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$ | 2.4 | | | 2.4 | | | |
| | $V_{CC} = 3 \text{ V}$ | $I_{OH} = -24 \text{ mA}$ | 2 | | | | 2 | |
| | | $I_{OH} = -32 \text{ mA}$ | | | | | | |
| V_{OL} | $V_{CC} = 2.7 \text{ V}$ | $I_{OL} = 100 \mu\text{A}$ | | 0.2 | | 0.2 | | V |
| | | $I_{OL} = 24 \text{ mA}$ | | 0.5 | | 0.5 | | |
| | $V_{CC} = 3 \text{ V}$ | $I_{OL} = 16 \text{ mA}$ | | 0.4 | | 0.4 | | |
| | | $I_{OL} = 32 \text{ mA}$ | | 0.5 | | 0.5 | | |
| | | $I_{OL} = 48 \text{ mA}$ | | 0.55 | | | | |
| | | $I_{OL} = 64 \text{ mA}$ | | | | 0.55 | | |
| | | | | | | | | |
| I_I | $V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$ | | | 10 | | 10 | | μA |
| | Control inputs | $V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$ | | ± 1 | | ± 1 | | |
| | | $V_I = V_{CC}$ | | 1 | | 1 | | |
| | Data inputs | $V_{CC} = 3.6 \text{ V}$ | $V_I = 0$ | -5 | | -5 | | |
| I_{off} | $V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$ | | | | | ± 100 | | μA |
| $I_I(\text{hold})$ | Data inputs | $V_{CC} = 3 \text{ V}$ | $V_I = 0.8 \text{ V}$ | 75 | | 75 | | μA |
| | | | $V_I = 2 \text{ V}$ | -75 | | -75 | | |
| | | $V_{CC} = 3.6 \text{ V}^\ddagger$ | $V_I = 0 \text{ to } 3.6 \text{ V}$ | | | ± 500 | | |
| I_{OZH} | $V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$ | | | 5 | | 5 | | μA |
| I_{OZL} | $V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$ | | | -5 | | -5 | | μA |
| I_{OZPU} | $V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE = \text{don't care}$ | | | $\pm 100^*$ | | ± 100 | | μA |
| I_{OZPD} | $V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE = \text{don't care}$ | | | $\pm 100^*$ | | ± 100 | | μA |
| I_{CC} | $V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$ | Outputs high | | 0.19 | | 0.19 | | mA |
| | | Outputs low | | 5 | | 5 | | |
| | | Outputs disabled | | 0.19 | | 0.19 | | |
| ΔI_{CC}^\S | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$ | | | 0.2 | | 0.2 | | mA |
| C_I | $V_I = 3 \text{ V or } 0$ | | | 3 | | 3 | | pF |
| C_O | $V_O = 3 \text{ V or } 0$ | | | 7 | | 7 | | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH540 | | SN74LVTH540 | | UNIT | | | |
|-----------|--------------------------------------|----------------|--|-----|--------------------------|-----|------|-----|-----|----|
| | | | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CC} = 2.7 \text{ V}$ | | | | | |
| | | | MIN | MAX | MIN | MAX | | | | |
| t_{PLH} | A | Y | 1 | 3.9 | 4.7 | 1.1 | 2.4 | 3.8 | 4.6 | ns |
| t_{PHL} | | | 1 | 3.9 | 4.7 | 1.1 | 2.7 | 3.8 | 4.6 | |
| t_{PZH} | $\overline{OE1}$ or $\overline{OE2}$ | Y | 1.4 | 5.3 | 6.3 | 1.5 | 3.4 | 5.2 | 6.2 | ns |
| t_{PZL} | | | 1.4 | 5.5 | 6.1 | 1.5 | 3.7 | 5.3 | 5.9 | |
| t_{PHZ} | $\overline{OE1}$ or $\overline{OE2}$ | Y | 1.4 | 5.9 | 6.2 | 1.5 | 3.9 | 5.6 | 5.9 | ns |
| t_{PLZ} | | | 1.4 | 5.5 | 5.8 | 1.5 | 3.5 | 5 | 5.3 | |

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

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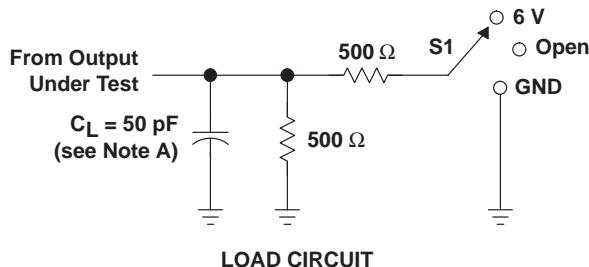


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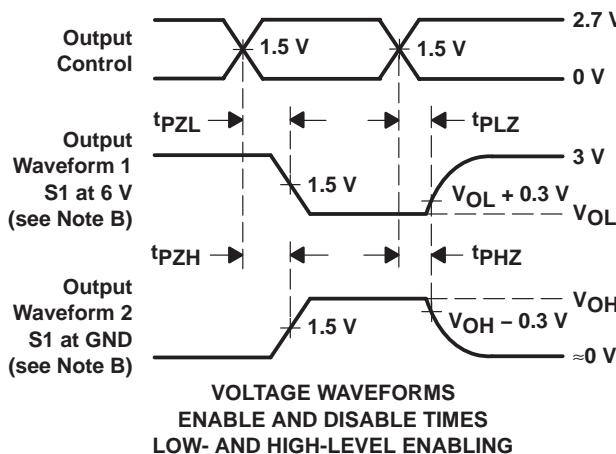
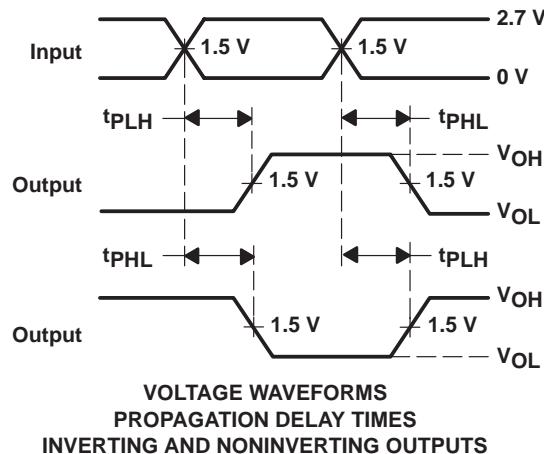
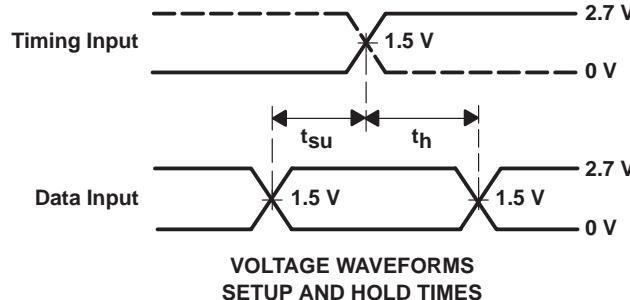
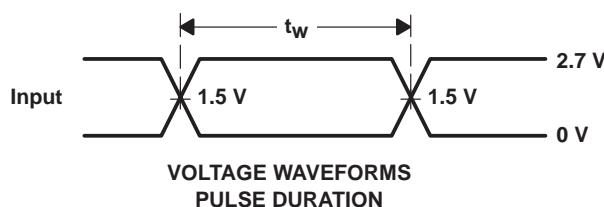
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{PHL}/t_{PLH} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVTH540DBLE | OBsolete | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74LVTH540DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PWLE | OBsolete | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74LVTH540PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH540PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

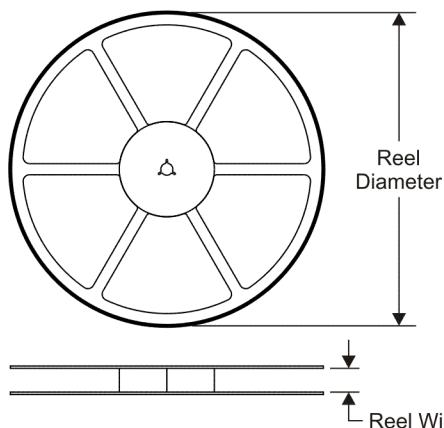
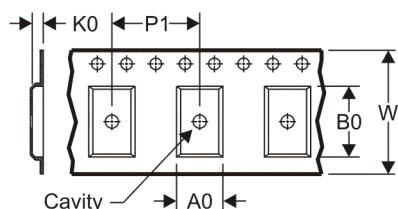
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

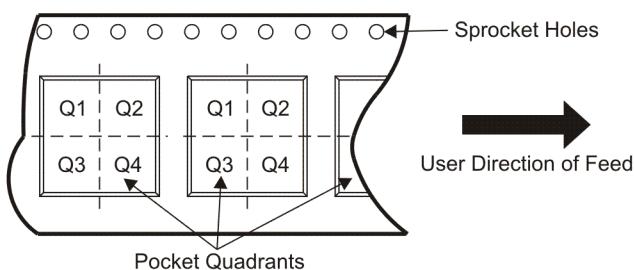
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


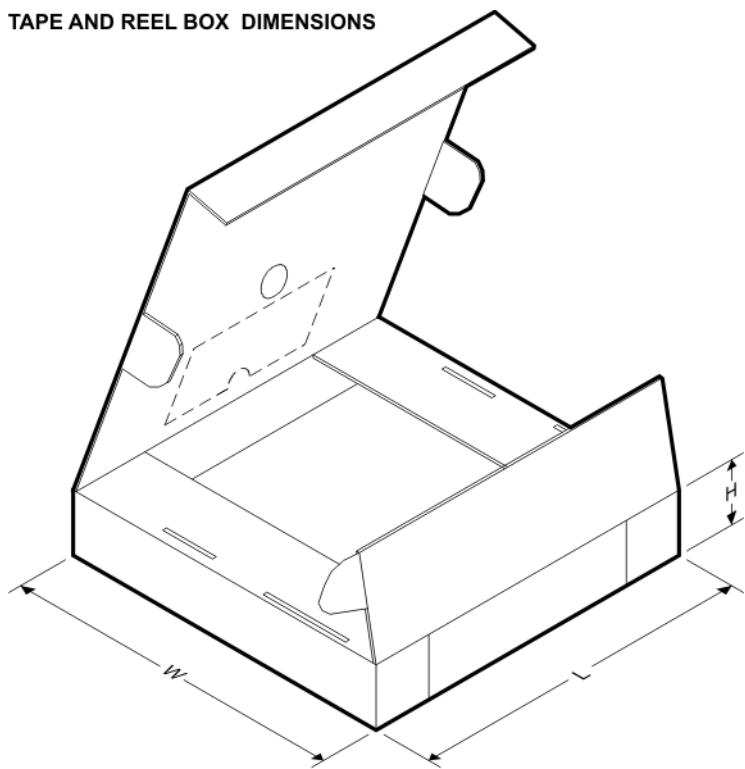
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH540DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH540DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVTH540NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVTH540PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



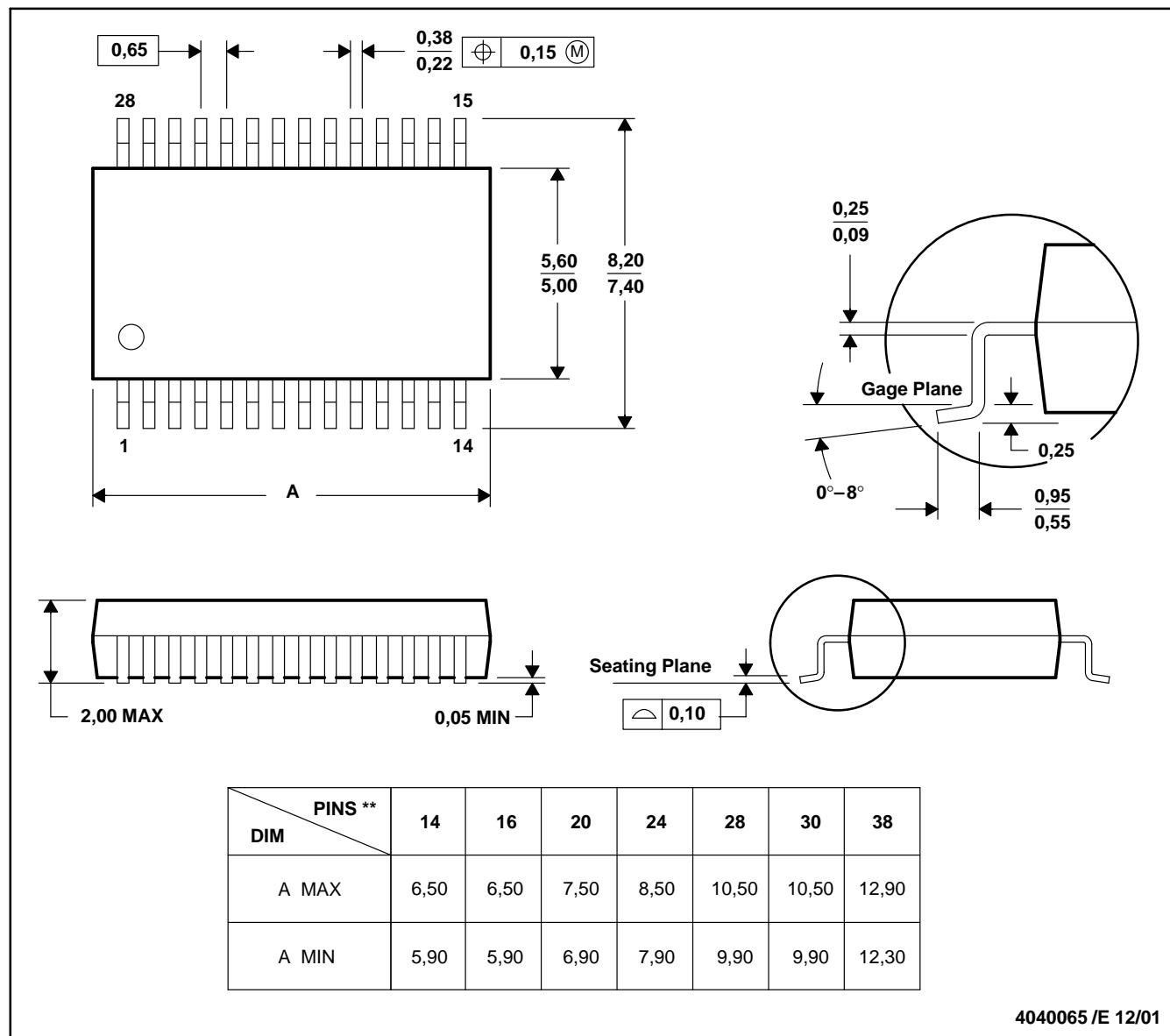
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH540DBR | SSOP | DB | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LVTH540DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVTH540NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVTH540PWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



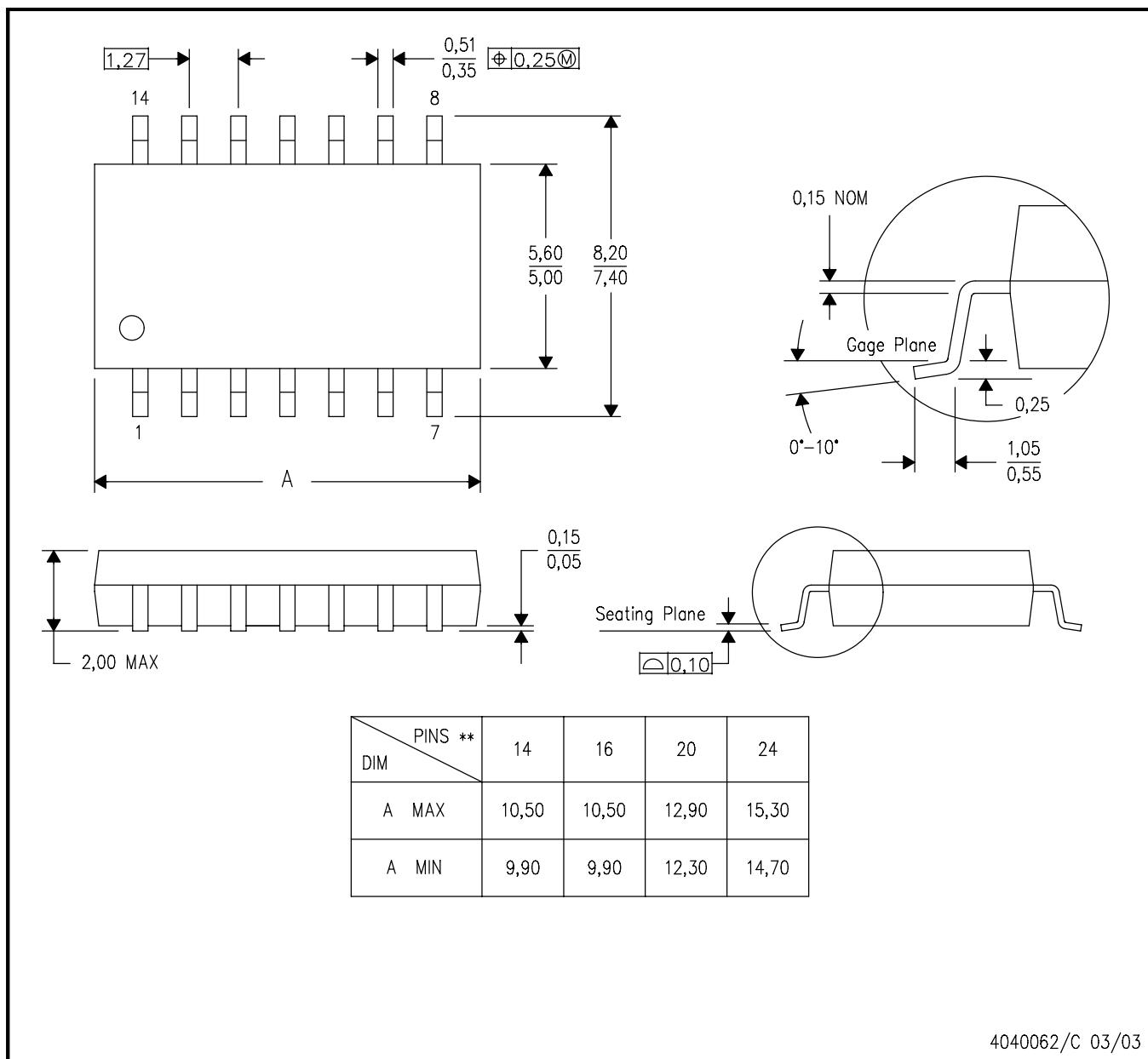
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



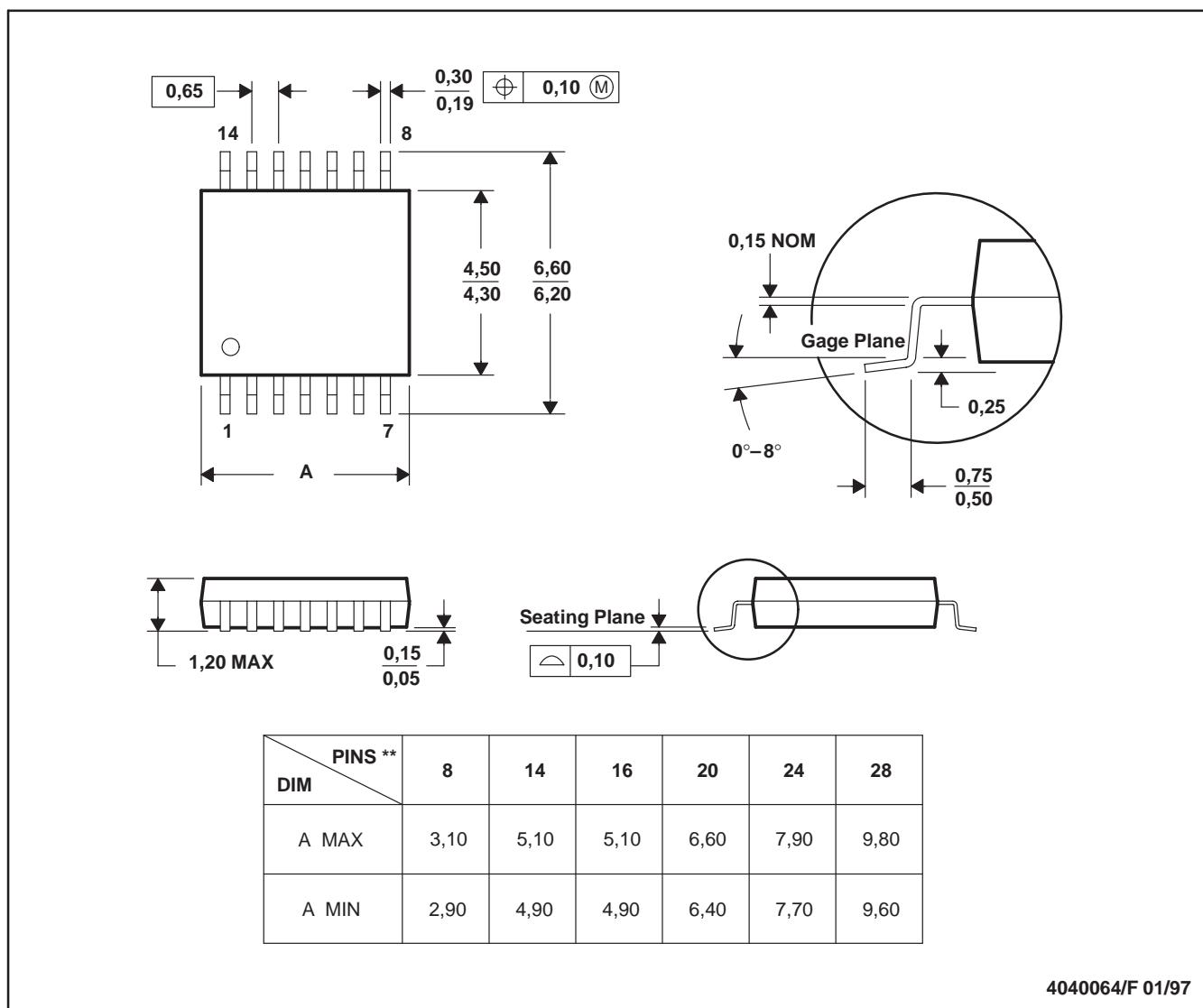
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NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

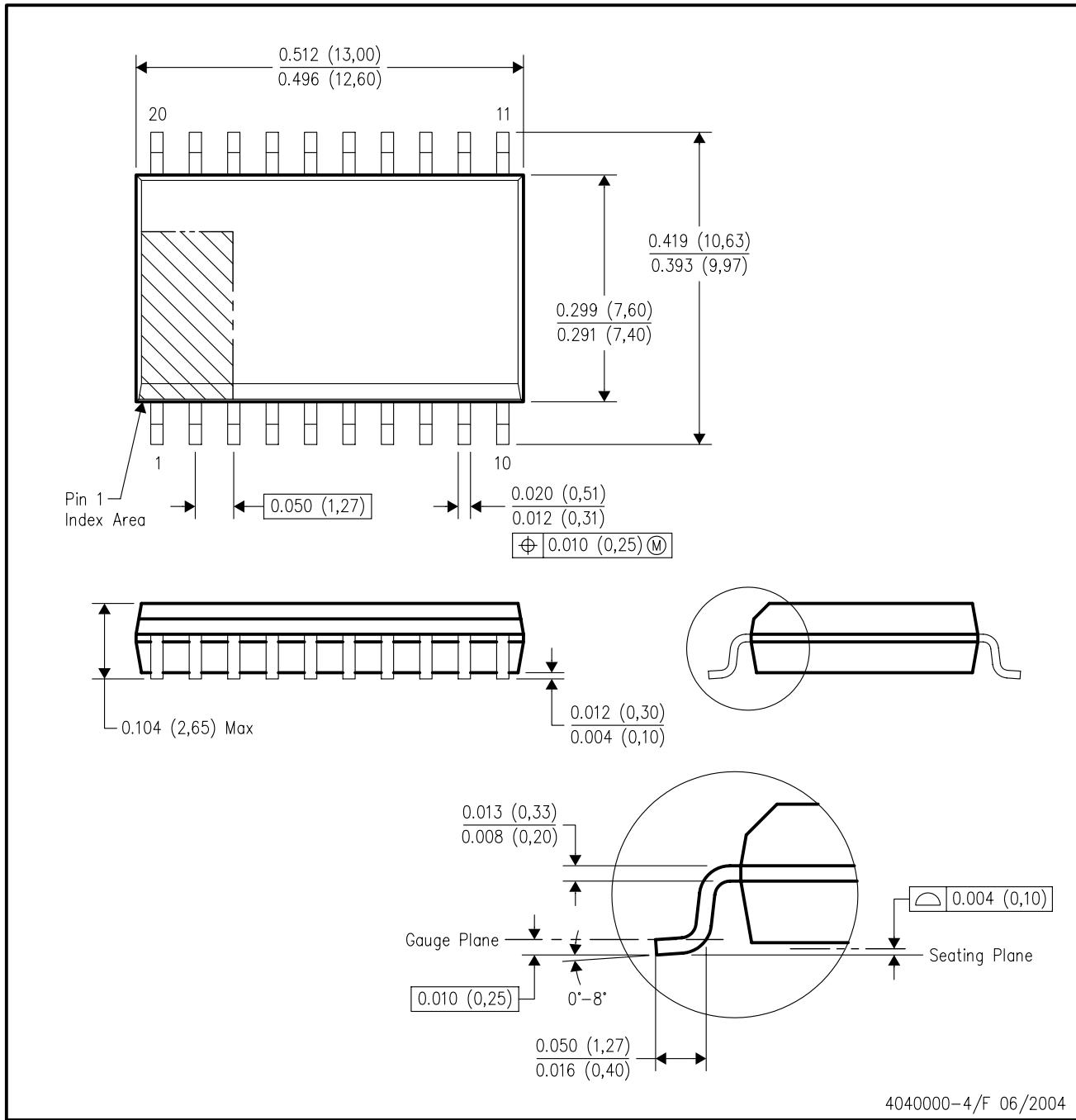


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

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