DS96F172M/DS96F174C/DS96F174M EIA-485/EIA-422 Quad Differential Drivers

Check for Samples: DS96F172M, DS96F174C, DS96F174M

FEATURES

- **Meets EIA-485 and EIA-422 Standards**
- **Monotonic Differential Output Switching**
- **Tri-state Outputs**
- **Designed for Multipoint Bus Transmission**
- **Common Mode Output Voltage Range: −7.0V to +12V**
- **Operates from Single +5.0V Supply**
- **Reduced Power Consumption**
- **Thermal Shutdown Protection**
- **DS96F172 and DS96F174 are Lead and Function Compatible with the SN75172/174 or the AM26LS31/MC3487**
- **Military Temperature Range Available**
- **Qualified for MIL-STD-883C**
- **Standard Military Drawings Available (SMD)**
- **Available in CDIP (NFE), LCCC (NAJ), and CLGA (NAD) Packages**

DESCRIPTION

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

The DS96F172 and the DS96F174 have tri-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Logic Diagrams

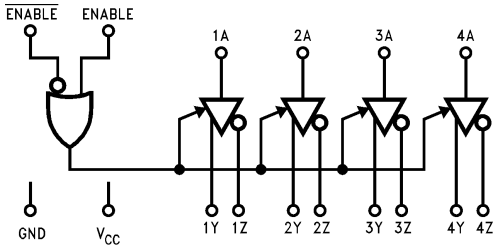


Figure 1. DS96F172

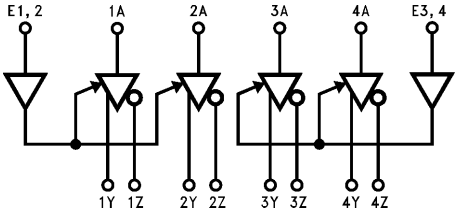


Figure 2. DS96F174

Function Tables

(Each Driver)

Table 1. DS96F172 (1)

Input	Enable		Outputs	
A	**E**	**$\overline{E}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

Table 2. DS96F174 (1)

Input	Enable	Outputs	
A	**E**	**Y**	**Z**
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings COMMERCIAL(1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range (T_{STG})		−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)		300°C
Maximum Package Power Dissipation (2) at 25°C	Ceramic DIP (NFE)	1500 mW
	Supply Voltage	7.0V
	Enable Input Voltage	5.5V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics provide conditions for actual device operation.
(2) Derate “NFE” package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F174C	4.75	5.0	5.25	V
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)DS96F174C	0		+70	°C

Electrical Characteristics (1) (2)

Over recommended supply voltage and operating temperature range, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ (3)	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW		T_A = 0°C to +70°C			0.8	V
			T_A = −55°C to +125°C			0.7	
V_{OH}	Output Voltage HIGH	I_{OH} = −33 mA	T_A = 0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 33 mA	T_A = 0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, See *Figure 3*	T_A = −55°C	1.2	2.0		V
				1.5			
		R_L = 100Ω, See *Figure 3*		2.0	2.3		
V_{OD}	Differential Output Voltage	*See Figure 4*	T_A = 0°C to +70°C	1.0			V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential	R_L = 54Ω or 100Ω, *Figure 3*	−40°C to +125°C			±0.2	V
	Output Voltage (4)		−55°C to +125°C			±0.4	
V_{OC}	Common Mode Output Voltage (5)	R_L = 54Ω or 100Ω, See *Figure 3*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (4)	R_L = 54Ω or 100Ω, See *Figure 3*				±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±50	µA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±20	±50	µA
I_{IH}	Input Current HIGH	V_I = 2.4V				20	µA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	µA
I_{OS}	Short Circuit Output Current (6)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			30	

(1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96F174C. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.
(3) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics provide conditions for actual device operation.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
(5) In EIA-422A and EIA-485 standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(6) Only one output at a time should be shorted.

COMMERCIAL Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, See *Figure 5*		15	20	ns
t_{TD}	Differential Output Transition Time			15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, See *Figure 6*		12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, See Figure 6		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, See *Figure 8*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, See *Figure 7*		25	30	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, See *Figure 8*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	*See Figure 8*		300		ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω		1.0	4.0	ns

Absolute Maximum RatingsMIL-STD-883C(1)

For complete Military Specifications, refer to the appropriate SMD or MDS.

Storage Temperature Range (T_{STG})		−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)		300°C
Maximum Package Power Dissipation (2) at 25°C	Ceramic LCCC (NAJ)	2000 mW
	Ceramic DIP (NFE)	1800 mW
	Ceramic Flatpak (NAD)	1000 mW
	Supply Voltage	7.0V
	Enable Input Voltage	5.5V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics provide conditions for actual device operation.
(2) Above T_A = 25°C, derate “NAJ” package 13.4, “NFE” package 12.5, “NAD” package 7.1 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F172M/DS96F174M	4.50	5.0	5.50	V
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A) DS96F172M/DS96F174M	−55		+125	°C

Electrical Characteristics (1) (2)

Over recommended supply voltage and operating temperature range unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Input Voltage HIGH			2.0		V
V_{IL}	Input Voltage LOW		T_A = 25°C		0.8	V
			T_A = −55°C, or +125°C		0.7	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, V_{CC} = 4.5V *See Figure 3*	T_A = −55°C	1.2		V
			T_A = 25°C, or +125°C	1.5		
		R_L = 100Ω, V_{CC} = 4.5V, See *Figure 3*		2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (3)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, See *Figure 3*	T_A = 25°C, or +125°C		±0.2	V
			T_A = −55°C		±0.4	V
V_{OC}	Common Mode Output Voltage (4)	R_L = 54Ω or 100Ω, See *Figure 3*			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (3)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, See *Figure 3*			±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V			±50	µA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	µA
I_{IH}	Input Current HIGH	V_I = 2.4V			20	µA
I_{IL}	Input Current LOW	V_I = 0.4V			−50	µA
I_{OS}	Short Circuit Output Current (5)	V_O = −7.0V			−250	mA
		V_O = 0V			−150	
		V_O = V_{CC}			150	
		V_O = +12V			250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	mA
I_{CCX}			Outputs Disabled		30	

(1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96F174C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

(2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

(4) In EIA-422A and EIA-485 standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

(5) Only one output at a time should be shorted.

MIL-STD-883C Switching Characteristics[1][2]

V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = 55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{DD}	Differential Output Delay Time	R_L = 60Ω, C_L = 15 pF, See *Figure 5*	15	22	30	30	ns
t_{TD}	Differential Output Transition Time		15	22	40	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, C_L = 15 pF, See *Figure 6*	12	16	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		12	16	25	25	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, See *Figure 7*	25	32	40	40	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, See *Figure 8*	25	35	100	100	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, See *Figure 7*, [3]	25	30	80	80	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, See *Figure 8*	20	25	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	*See Figure 8*	300				ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω	1.0	4.0	10	10	ns

(1) DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.
(2) To test the active low Enable $\overline{E}$ of DS96F172 ground E and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.
(3) Not tested for DS96F172MW-MIL device.

Parameter Measurement Information

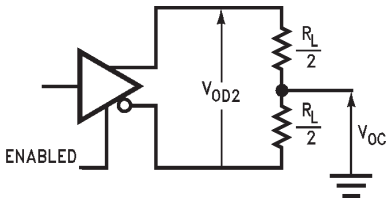


Figure 3. Differential and Common Mode Output Voltage(4)

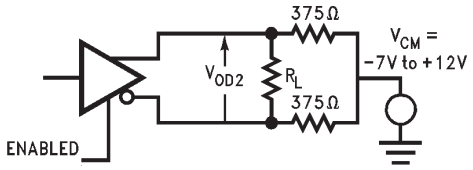


Figure 4. Differential Output Voltage with Varying Common Mode Voltage(4)

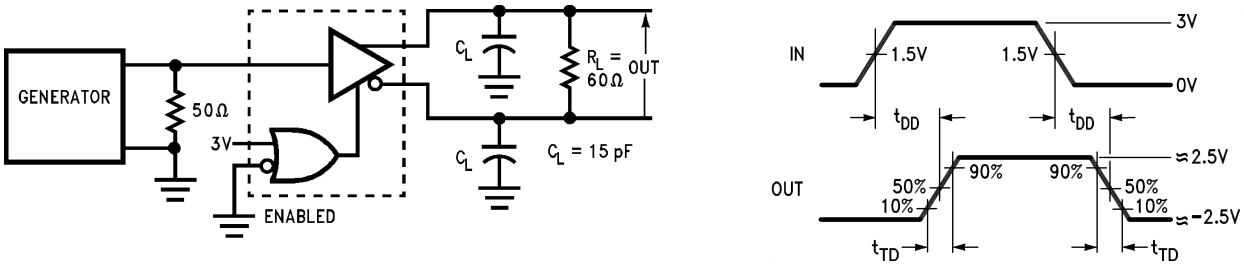


Figure 5. Differential Output Delay and Transition Times(5)(4)

(4) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \le 5.0$ ns, $t_f \le 5.0$ ns, $Z_O = 50\Omega$.

(5) Above $T_A = 25°C$, derate “NAJ” package 13.4, “NFE” package 12.5, “NAD” package 7.1 mW/°C

Parameter Measurement Information (continued)

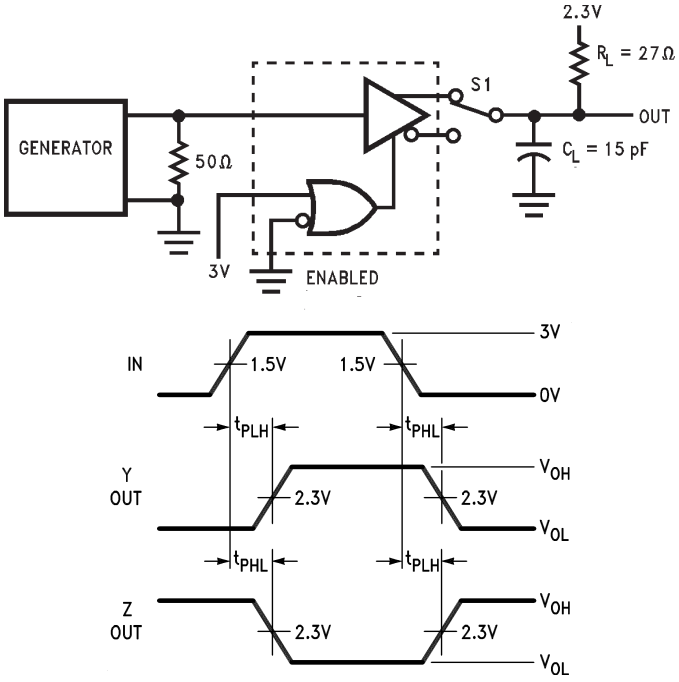


Figure 6. Propagation Delay Times (6)(7)

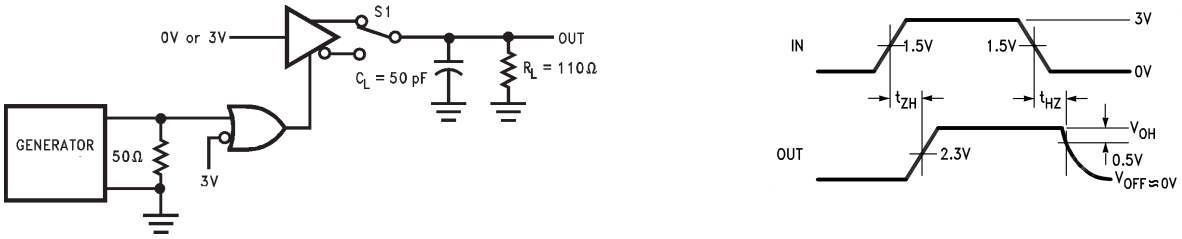


Figure 7. t_{ZH} and t_{HZ} (6)(8)

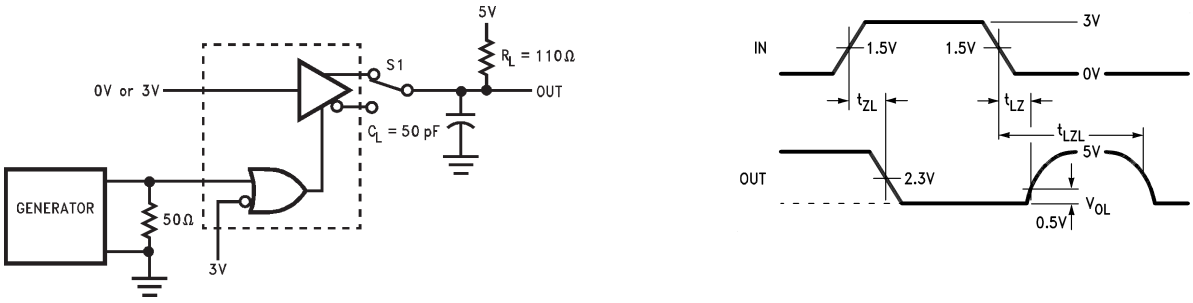


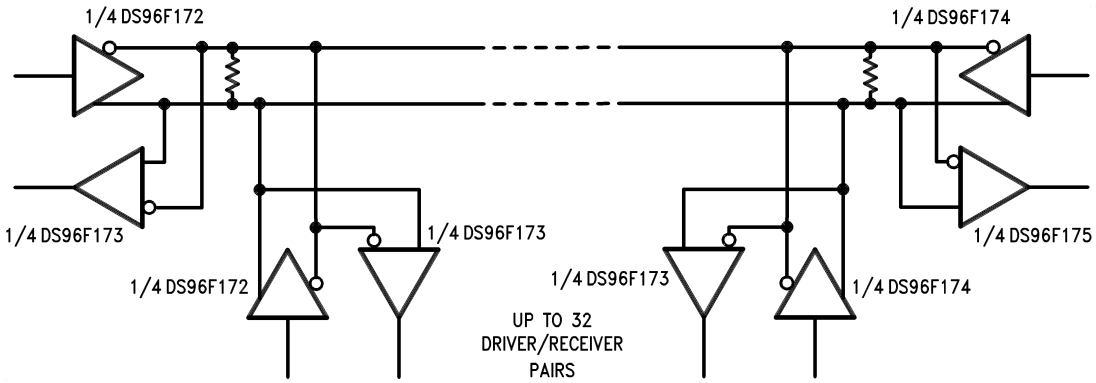
Figure 8. t_{ZL}, t_{LZ}, t_{LZL} (6)(8)

(6) Above T_A = 25°C, derate “NAJ” package 13.4, “NFE” package 12.5, “NAD” package 7.1 mW/°C

(7) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \le 5.0$ ns, $t_f \le 5.0$ ns, Z_O = 50Ω.

(8) C_L includes probe and jig capacitance

TYPICAL APPLICATION



NOTE

The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Connection Diagrams

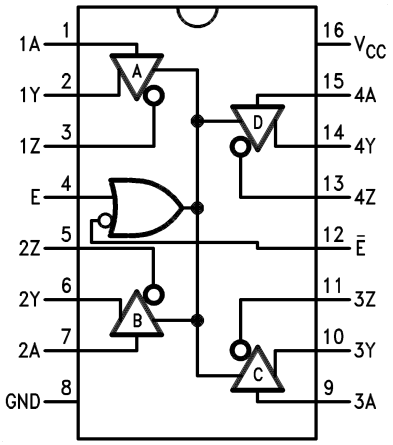


Figure 9. DS96F172 (Top View)
CDIP - 16-Lead Ceramic Dual-In-Line Package
See Package Number NFE

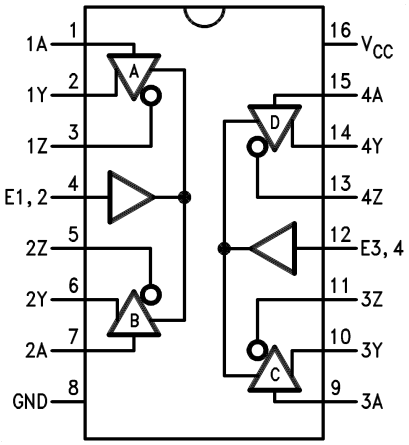
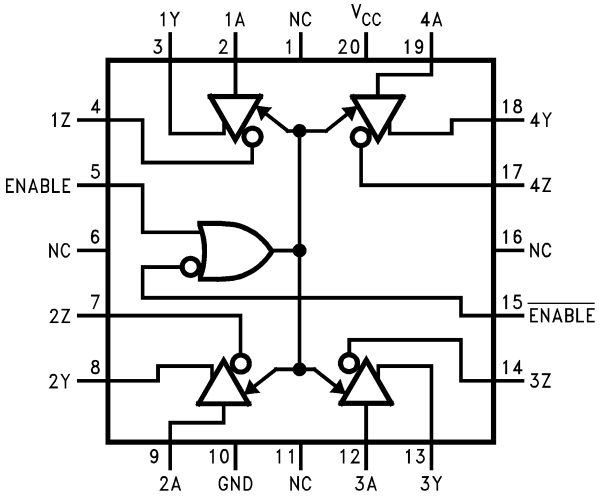
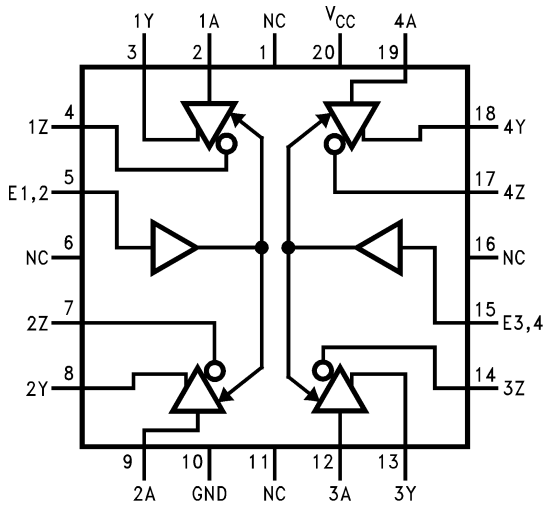


Figure 10. DS96F174 (Top View)
CDIP - 16-Lead Ceramic Dual-In-Line Package
See Package Number NFE



NC = No connection

Figure 11. 20-Lead Ceramic Leadless Chip Carrier - LCCC (Top View)
See Package Number NAJ



NC = No connection

Figure 12. 20-Lead Ceramic Leadless Chip Carrier - LCCC (Top View)
See Package Number NAJ

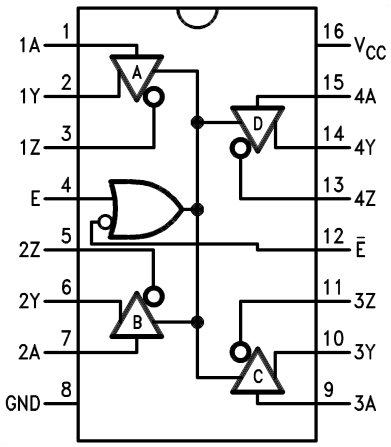


Figure 13. 16-Lead Ceramic Flatpack - CLGA (Top View)
See Package Number NAD

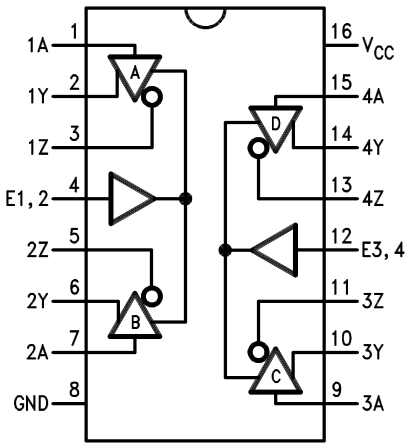


Figure 14. 16-Lead Ceramic Flatpack - CLGA (Top View)
See Package Number NAD

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	13

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