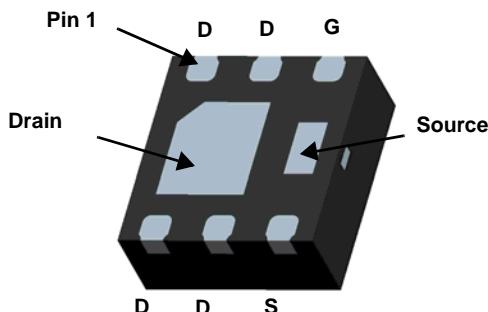


FDMA510PZ

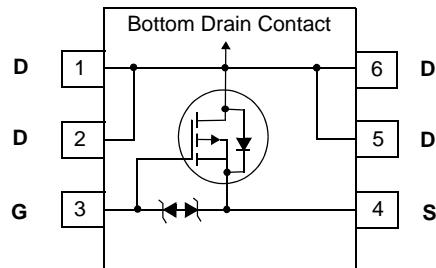
Single P-Channel PowerTrench® MOSFET -20V, -7.8A, 30mΩ

Features

- Max $r_{DS(on)}$ = 30mΩ at $V_{GS} = -4.5V$, $I_D = -7.8A$
- Max $r_{DS(on)}$ = 37mΩ at $V_{GS} = -2.5V$, $I_D = -6.6A$
- Max $r_{DS(on)}$ = 50mΩ at $V_{GS} = -1.8V$, $I_D = -5.5A$
- Max $r_{DS(on)}$ = 90mΩ at $V_{GS} = -1.5V$, $I_D = -2.0A$
- Low profile - 0.8mm maximum - in the new package MicroFET 2X2 mm
- HBM ESD protection level > 3KV typical (Note 3)
- RoHS Compliant



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current -Continuous (Note 1a)	-7.8	A
	-Pulsed	-24	
P_D	Power Dissipation (Note 1a)	2.4	W
	Power Dissipation (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
510	FDMA510PZ	MicroFET 2X2	7"	8mm	3000units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-13		$\text{mV/}^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V}$, $V_{GS} = 0\text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{V}$, $V_{DS} = 0\text{V}$			± 10	μA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-0.4	-0.7	-1.5	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		3		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{V}$, $I_D = -7.8\text{A}$		27	30	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}$, $I_D = -6.6\text{A}$		34	37	
		$V_{GS} = -1.8\text{V}$, $I_D = -5.5\text{A}$		46	50	
		$V_{GS} = -1.5\text{V}$, $I_D = -2.0\text{A}$		60	90	
		$V_{GS} = -4.5\text{V}$, $I_D = -7.8\text{A}$, $T_J = 125^\circ\text{C}$		36	40	
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{V}$, $I_D = -7.8\text{A}$		26		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		1110	1480	pF
C_{oss}	Output Capacitance			205	275	pF
C_{rss}	Reverse Transfer Capacitance			185	280	pF

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = -10\text{V}$, $I_D = -7.8\text{A}$ $V_{GS} = -4.5\text{V}$, $R_{\text{GEN}} = 6\Omega$		7	14	ns
t_r	Rise Time			9	18	ns
$t_{d(\text{off})}$	Turn-Off Delay Time			125	200	ns
t_f	Fall Time			64	103	ns
Q_g	Total Gate Charge	$V_{DD} = -5\text{V}$, $I_D = -7.8\text{A}$ $V_{GS} = -4.5\text{V}$		19	27	nC
Q_{gs}	Gate to Source Charge			2.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.2		nC

Drain-Source Diode Characteristics

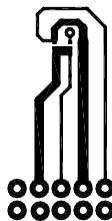
I_S	Maximum Continuous Drain-Source Diode Forward Current			-2	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = -2\text{A}$		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -7.8\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		66	106	ns
Q_{rr}	Reverse Recovery Charge			44	71	nC

Notes:

1. R_{QJA} is determined with the device mounted on a 1in^2 pad of 2 oz copper pad on a 1.5×1.5 in. board of FR-4 material. R_{QJC} is guaranteed by design while R_{QCA} is determined by the user's board design.



a. $52^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper.



b. $145^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

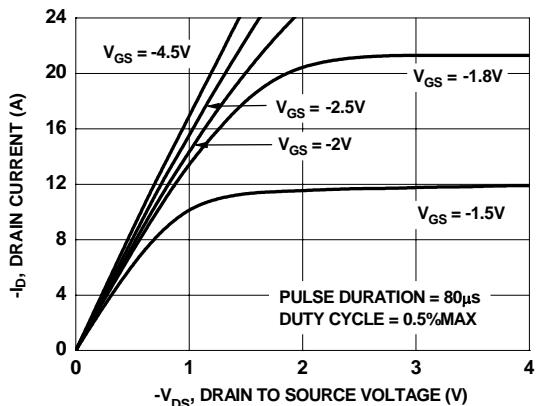


Figure 1. On-Region Characteristics

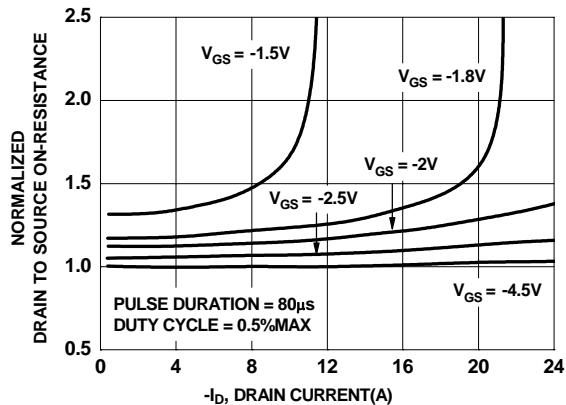


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

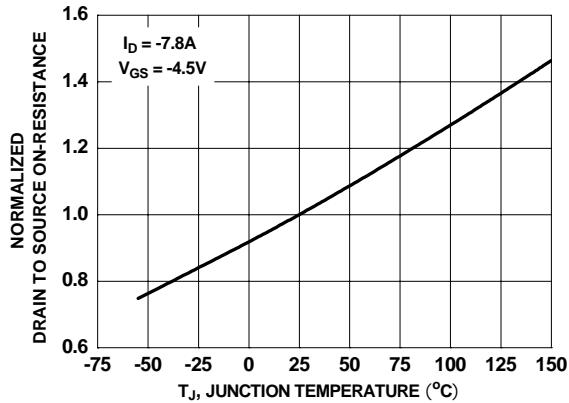


Figure 3. Normalized On-Resistance vs Junction Temperature

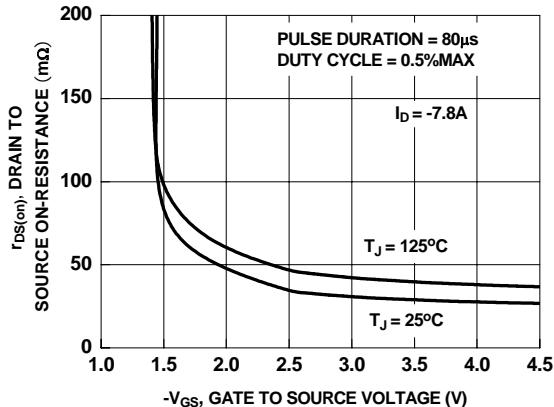


Figure 4. On-Resistance vs Gate to Source Voltage

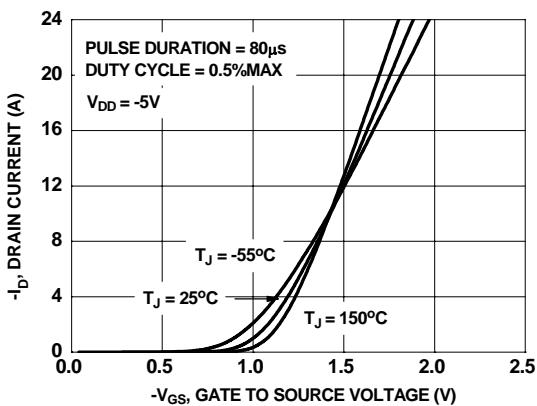


Figure 5. Transfer Characteristics

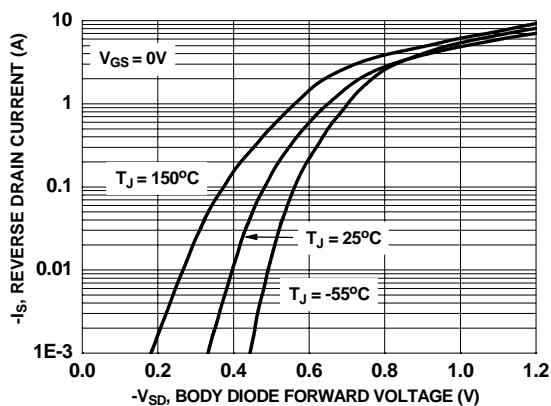


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

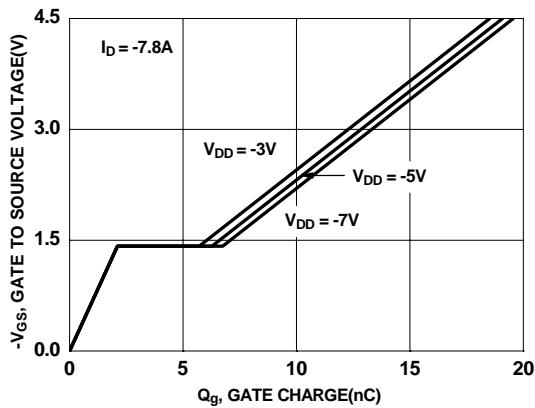


Figure 7. Gate Charge Characteristics

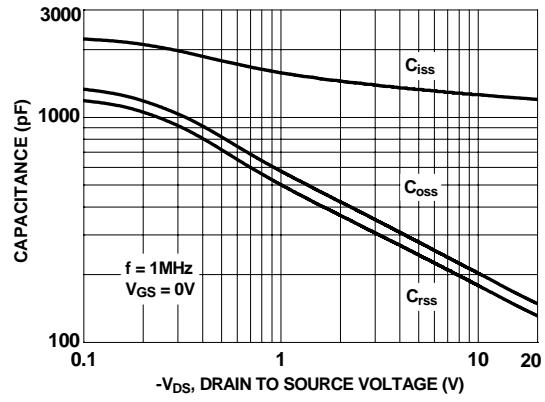


Figure 8. Capacitance vs Drain to Source Voltage

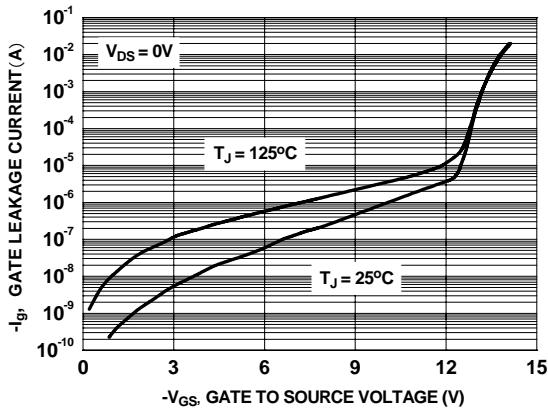


Figure 9. Gate Leakage Current vs Gate to Source Voltage

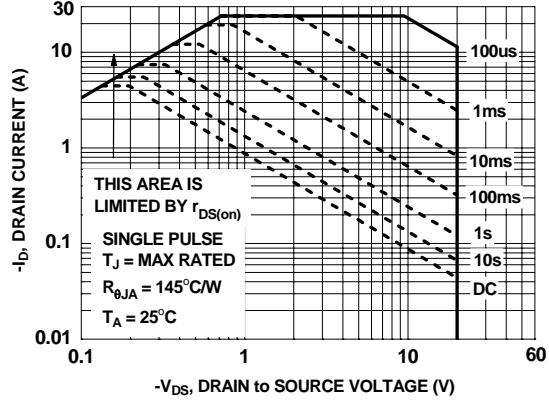


Figure 10. Forward Bias Safe Operating Area

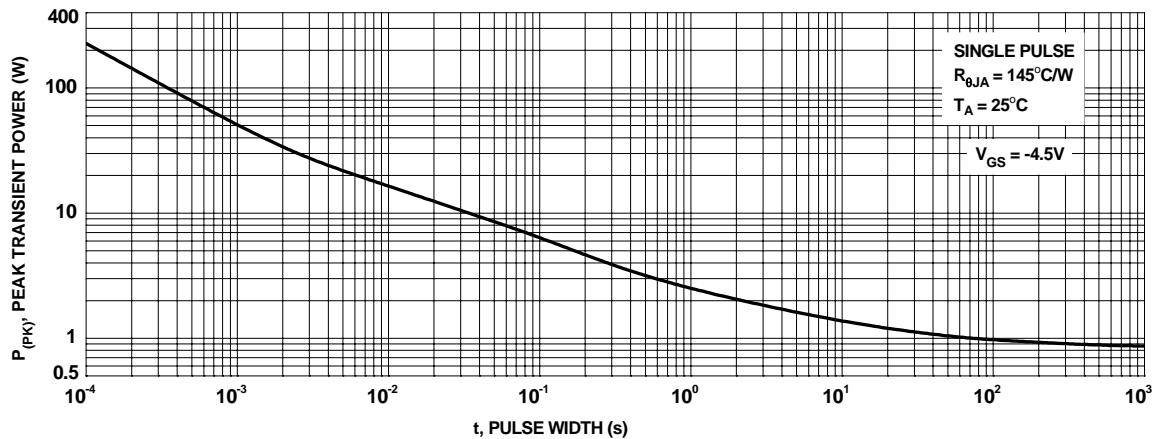


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

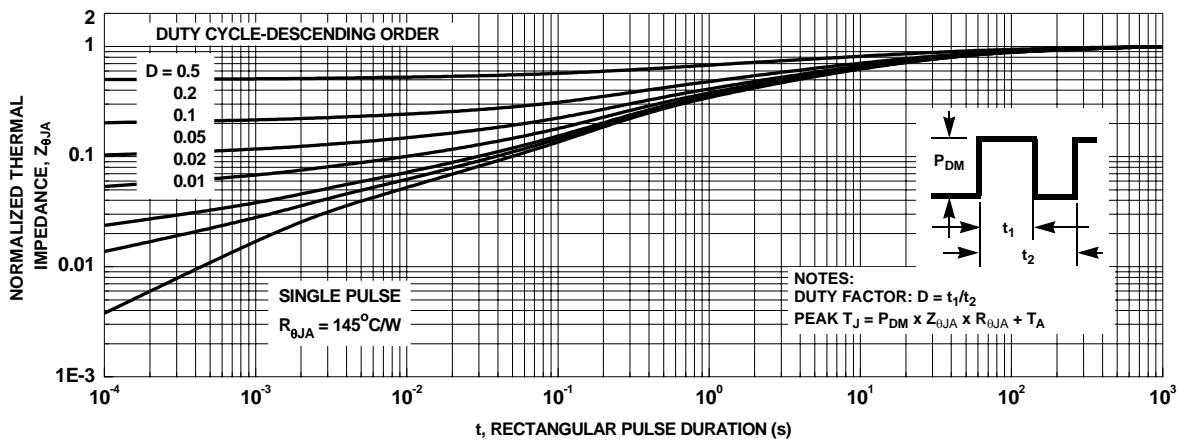
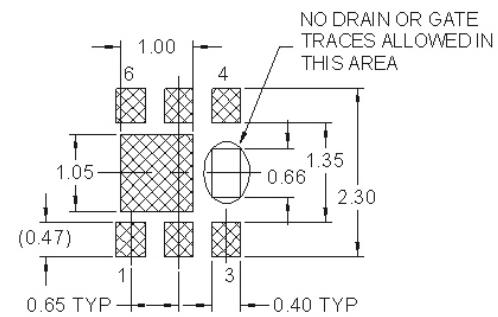
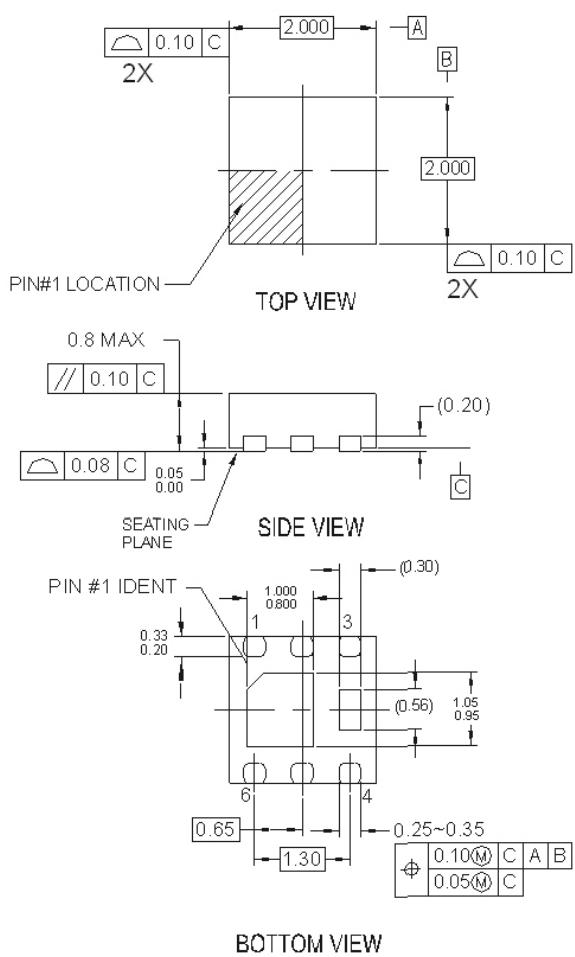
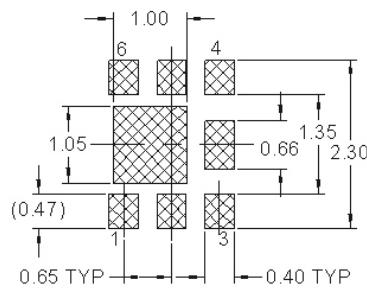


Figure 12. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994
- D. DRAWING FILENAME: MKT-MLP06Lrev2.



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