



2.5A Output Current, High CME Gate Drive Optocoupler

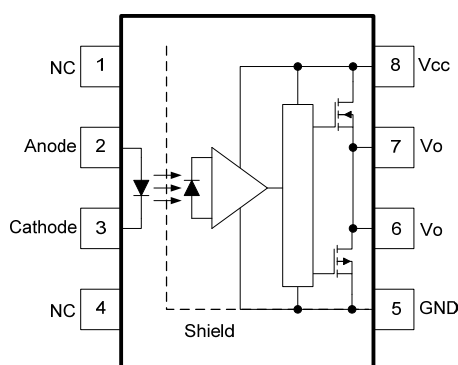


Description

The ICPL3120 optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications and inverters in power supply system. It contains a AlGaAs LED optically coupled to an integrated circuit with a power output stage. The 2.5A peak output current is capable of directly driving most IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the ICPL3120 series can be used to drive a discrete power stage which drives the IGBT gate.

The Optocoupler operational parameters are guaranteed over the temperature range from $-40^{\circ}\text{C} \sim +110^{\circ}\text{C}$.

Functional Diagram



Features

- 2.5 A maximum peak output current
- 25 kV/us minimum Common Mode Rejection (CMR) at $V_{CM} = 1500\text{ V}$
- 3.8 mA maximum supply current (I_{CC})
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating range: 15 to 30 Volts (V_{CC})
- Guaranteed performance over temperature $-40^{\circ}\text{C} \sim +110^{\circ}\text{C}$.
- Offer low power dissipation with $R_{ON} \leq 1\Omega$
- Fast switching speed, 500ns max propagation delay
- Safety approval: UL, cUL, VDE (In process)

Application

- IGBT/MOSFET gate drive
- Uninterruptible power supply (UPS)
- Industrial Inverter
- Induction heating

Truth Table

LED	$V_{CC}\text{-GND}$ (Turn-ON, +ve going)	$V_{CC}\text{-GND}$ (Turn-OFF, -ve going)	V_o
OFF	0 - 30 V	0 - 30 V	Low
ON	0 - 11.5 V	0 - 10 V	Low
ON	11.5 - 13.5 V	10 - 12 V	Transition
ON	13.5 - 30 V	12 - 30 V	High

A 0.1 μF bypass Capacitor must be connected between Pin 5 and 8. (Note 8)

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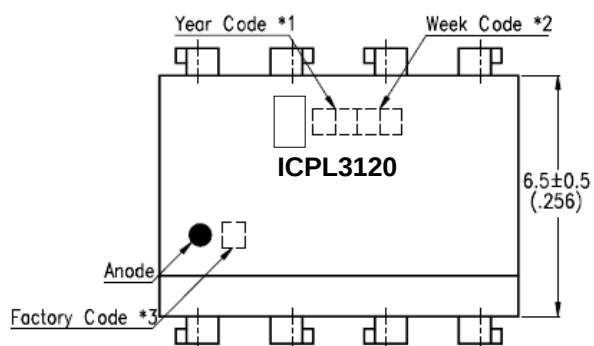
Ordering Information

Part	Option	Remarks
ICPL3120		DIP-8
	G	Wide Lead Spacing, DIP-8
	SM	Surface Mount, SMD-8
	T&R	Surface Mount, SMD-8, Pin 1 location at lower right of the reel
	T&R1	Surface Mount, SMD-8, Pin 1 location at upper left of the reel

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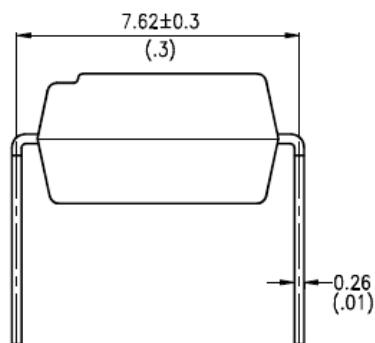
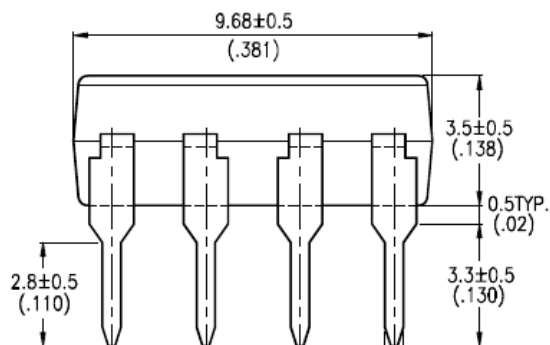
Package Dimensions

8-pin DIP Package (ICPL3120)



- *1. Year date code.
- *2. 2-digit work week.
- *3. Factory identification mark

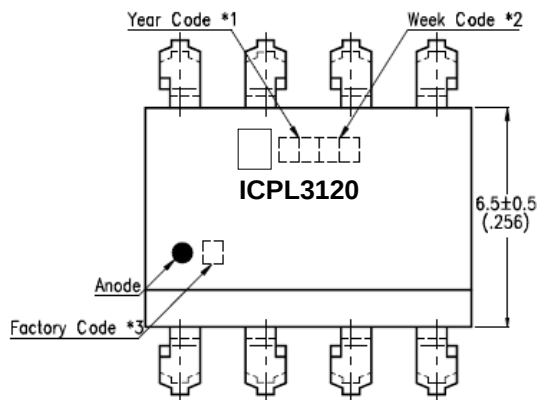
Dimensions are in Millimeters and (Inches).



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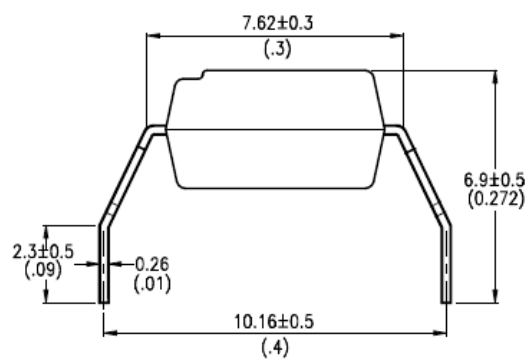
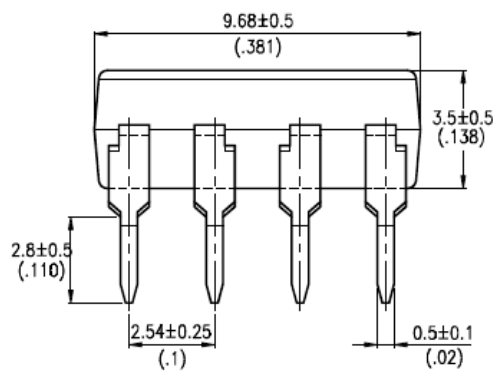
Package Dimensions

8-pin DIP Wide Lead Spacing Package (ICPL3120G)



- *1. Year date code.
- *2. 2-digit work week.
- *3. Factory identification mark

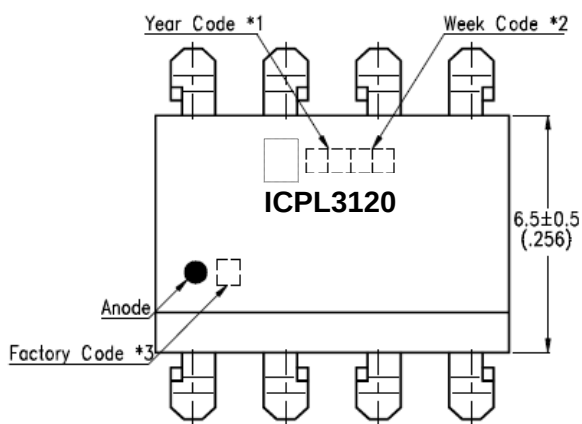
Dimensions are in Millimeters and (Inches).



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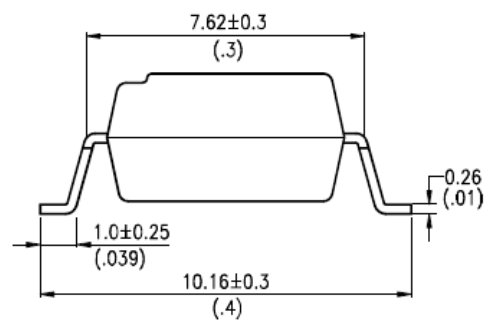
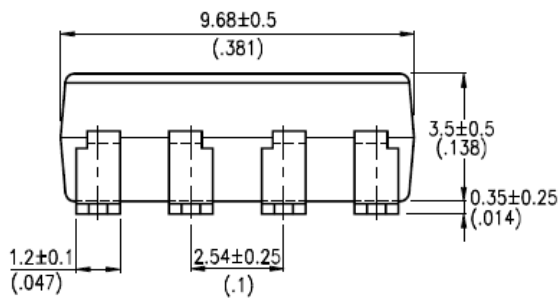
Package Dimensions

8-pin DIP Surface Mount Package (ICPL3120SM)



- *1. Year date code.
- *2. 2-digit work week.
- *3. Factory identification mark

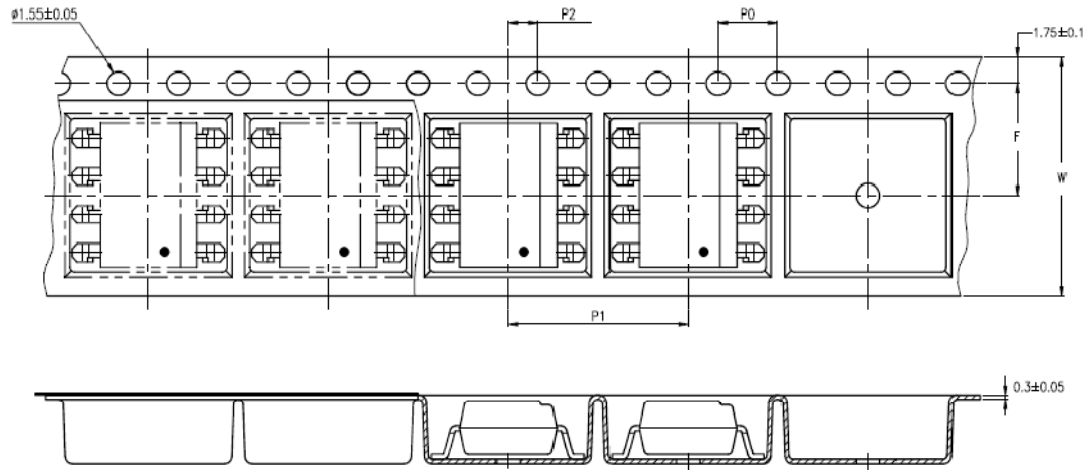
Dimensions are in Millimeters and (Inches).



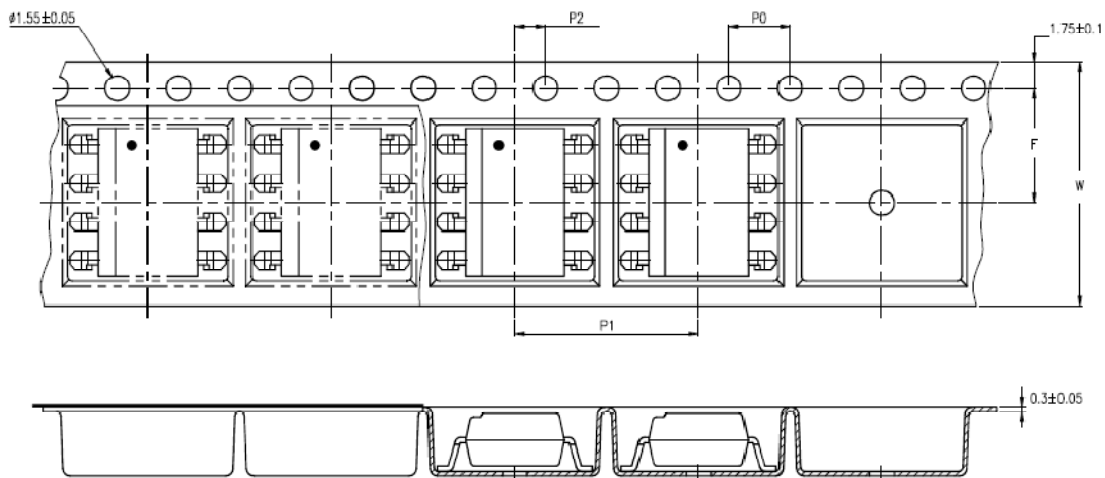
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Taping Dimensions

ICPL3120SM-TA



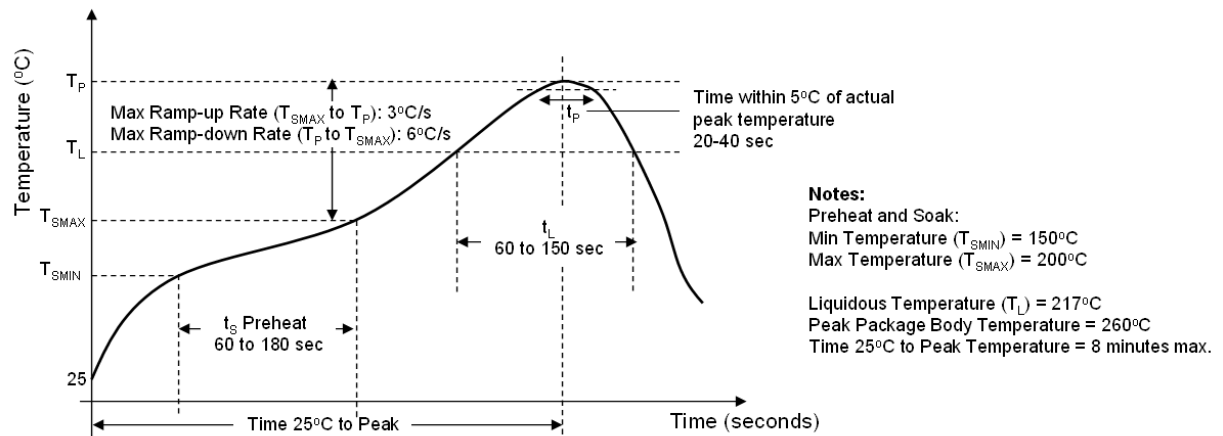
ICPL3120SM-TA1



Description	Symbol	Dimensions in millimeters (inches)
Tape wide	W	16 ± 0.3 (.63)
Pitch of sprocket holes	P0	4 ± 0.1 (.15)
Distance of compartment	F	7.5 ± 0.1 (.295)
Distance of compartment to compartment	P1	2 ± 0.1 (.079)
Distance of compartment to compartment	P1	12 ± 0.1 (.472)

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Recommended Lead Free Reflow Profile



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Absolute Maximum Ratings

Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T _{ST}	-55	125	°C
Operating Temperature	T _A	-40	110	°C
Isolation Voltage	V _{ISO}	5000		V _{RMS}
Supply Voltage	V _{CC}	0	35	V
Lead Solder Temperature ⁽⁹⁾	T _{SOL}		260	°C
Input				
Average Forward Input Current	I _{F(AVG)}		25	mA
Reverse Input Voltage	V _R		5	V
Peak Transient Input Current (<1 μs pulse width, 300 pps)	I _{F(TRAN)}		1	A
Input Current (Rise/Fall Time)	t _{r(IN)} / t _{f(IN)}		500	ns
Input Power Dissipation ⁽¹⁰⁾	P _I		45	mW
Output				
“High” Peak Output Current ⁽¹⁾	I _{OH(PEAK)}		2.5	A
“Low” Peak Output Current ⁽¹⁾	I _{OL(PEAK)}		2.5	A
Output Voltage	V _O		V _{CC}	V
Output Power Dissipation ⁽¹¹⁾	P _O		250	mW
Total Power Dissipation	P _T		295	mW

8) At least a 0.1μF or bigger bypass capacitor must be connected across pin 8 and pin 5. Failure to provide the bypass may impair the switching property.

9) 260°C for 10 seconds. Refer to Lead Free Reflow Profile

10) Derating Linearly above 70°C free-air temperature at a rate of -0.47 mW/°C

11) Derating Linearly above 70°C free-air temperature at a rate of 4.8mW/°C

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Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T_A	-40	110	°C
Supply Voltage	V_{CC}	15	30	V
Input Current (ON)	$I_{FL(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V

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Electrical Specifications

Parameters	Test Condition	Symbol	Min	Typ	Max	Units	Figure
Input							
Input Forward Voltage	$I_F = 10\text{mA}$	V_F	1.2	1.37	1.8	V	15
Input Forward Voltage Temperature Coefficient	$I_F = 10\text{mA}$	$\Delta V_F / \Delta T$		-1.237		mV/°C	
Input Reverse Voltage	$I_R = 10\mu\text{A}$	BV_R	5			V	
Input Threshold Current (Low to High)	$V_O > 5\text{V}, I_O = 0\text{A}$	I_{FLH}		2.89	5	mA	9,16,21
Input Threshold Voltage (High to Low)	$V_O < 5\text{V}, I_O = 0\text{A}$	V_{FHL}	0.8			V	
Input Capacitance	$f = 1\text{ MHz}, V_F = 0\text{ V}$	C_{IN}		33		pF	
Output							
High Level Supply Current	Output Open, $I_F = 7\text{ to }16\text{ mA}$	I_{CCH}		1	3.0	mA	7,8
Low Level Supply Current	Output Open, $V_F = -3\text{ to }+0.8\text{ V}$	I_{CCL}		1	3.0	mA	7,8
High level output current ⁽¹⁾	$V_O = (V_{CC} - 6\text{ V})$	I_{OH}	-2.0			A	2,3,19
Low level output current ⁽¹⁾	$V_O = (V_{EE} + 6\text{ V})$	I_{OL}	2.0			A	5,6,20
High level output voltage	$I_F = 10\text{mA}, I_O = -100\text{mA}$	V_{OH}	$V_{CC} - 0.25$	$V_{CC} - 0.1$		V	1,3,17
Low level output voltage	$I_F = 0\text{mA}, I_O = 100\text{mA}$	V_{OL}		$V_{EE} + 0.1$	$V_{EE} + 0.25$	V	4,6,18
UVLO Threshold	$V_O > 5\text{V}, I_F = 10\text{ mA}$	V_{UVLO+}	11.5		13.5	V	22
	$V_O < 5\text{V}, I_F = 10\text{ mA}$	V_{UVLO-}	10	11.5	12	V	
UVLO Hysteresis		$UVLO_{HYS}$		1.6		V	

Specified over recommended operating conditions.

All Typical values at $T_A = 25^\circ\text{C}$ and $V_{CC} = 30\text{ V}$, unless otherwise specified.

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Switching Specifications

Parameter	Test Condition	Symbol	Min	Typ	Max	Units	Figure
Propagation Delay Time to High Output Level	$I_F = 7$ to 16 mA, $R_g = 10\ \Omega$, $C_g = 10$ nF, $f = 10$ kHz, Duty Cycle = 50%	T_{PLH}	0.1	0.28	0.5	μs	10,11, 12,13, 14,23
Propagation Delay Time to Low Output Level		T_{PHL}	0.1	0.31	0.5	μs	
Pulse Width Distortion ⁽⁷⁾		PWD			0.1	μs	
Propagation delay difference between any two parts or channels ⁽⁴⁾		PDD	-0.30		0.30	μs	
Output Rise Time (10 to 90%)		T_r		0.1		μs	23
Output Fall Time (90 to 10%)		T_f		0.1		μs	
UVLO turn on delay	$I_F = 10$ mA, $V_O > 5$ V	$T_{UVLO\ ON}$		1.5		μs	
UVLO turn off delay	$I_F = 10$ mA, $V_O < 5$ V	$T_{UVLO\ OFF}$		0.2		μs	
Common mode transient immunity at high level output ⁽⁵⁾	$I_F = 10$ to 16 mA, $V_{CM} = 1500$ V, $T_A = 25^\circ C$, $V_{CC} = 30$ V	CMH	25	35		kV/ μs	24
Common mode transient immunity at low level output ⁽⁶⁾	$V_F = 0$ V, $V_{CM} = 1500$ V, $T_A = 25^\circ C$, $V_{CC} = 30$ V	CML	25	35		kV/ μs	

Specified over recommended operating conditions.

All Typical values at $T_A = 25^\circ C$ and $V_{CC} = 30$ V, unless otherwise specified.

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Isolation Characteristics

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
Withstand Insulation Test Voltage ^{(2) (3)}	$RH \leq 40-60\%$, $t = 1\text{min}$, $T_A = 25^\circ\text{C}$	V_{ISO}	5000			V
Input-Output Resistance ⁽²⁾	$V_{\text{I-O}} = 500\text{V DC}$	$R_{\text{I-O}}$		10^{12}		Ω
Input-Output Capacitance ⁽²⁾	$f = 1\text{MHz}$, $T_A = 25^\circ\text{C}$	$C_{\text{I-O}}$		0.92		pF

Notes:

- 1) Maximum pulse width = 10us, maximum duty cycle = 0.2%.
- 2) Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
- 3) According to UL1577, each optocoupler is tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, $I_{\text{I-O}} \leq 6 \mu\text{A}$).
- 4) The difference between T_{PHL} and T_{PLH} between any two ICPL3120 parts under same test conditions.
- 5) Common mode transient immunity in high stage is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high.
- 6) Common mode transient immunity in low stage is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common mode impulse signal, V_{cm} , to assure that the output will remain low.
- 7) Pulse Width Distortion is defined as $|T_{\text{PHL}} - T_{\text{PLH}}|$ for any given device.

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Typical Performance Curves

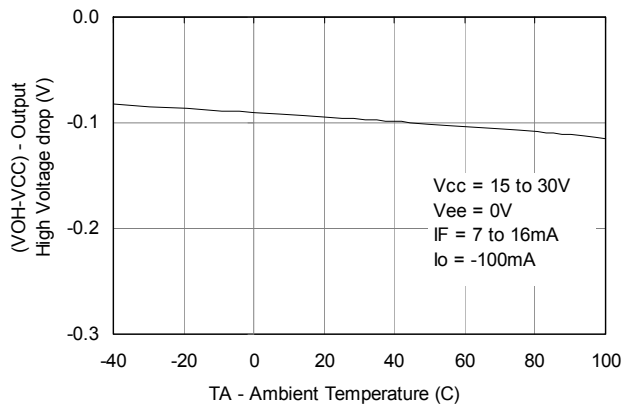


Figure 1: Output High Voltage drop vs Temperature

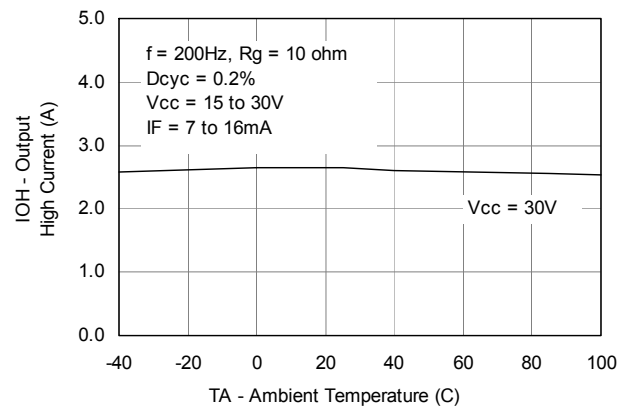


Figure 2: Output High Current vs Temperature

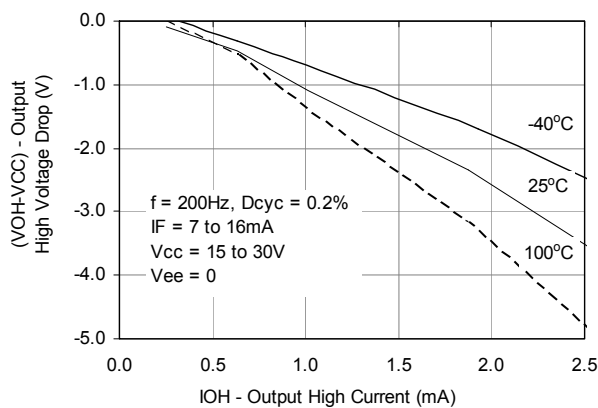


Figure 3: Output High Voltage drop vs High Current

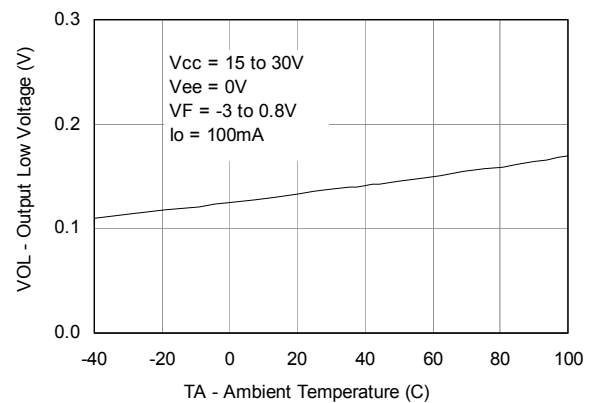


Figure 4: Output Low Voltage vs Temperature

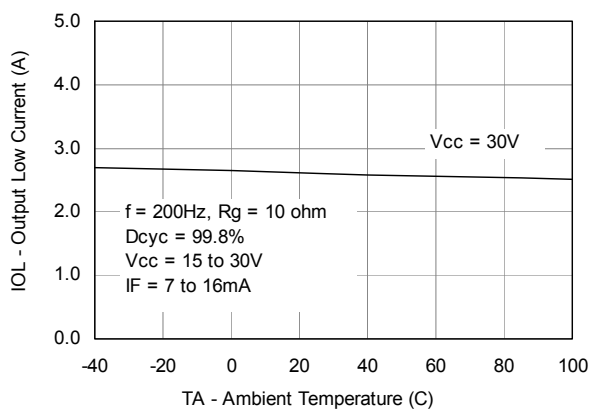


Figure 5: Output Low Current vs Temperature

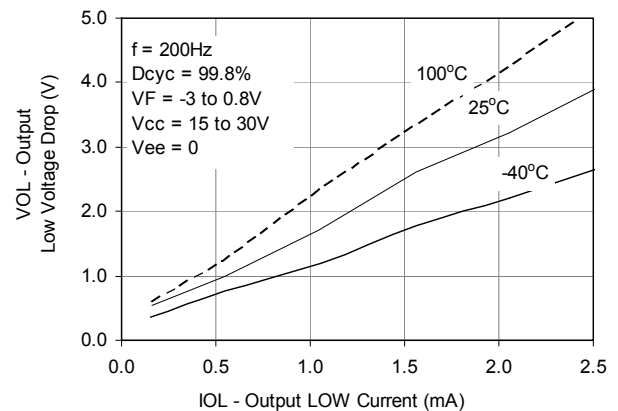


Figure 6: Output Low Voltage vs Low Current

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Typical Performance Curves (Continued)

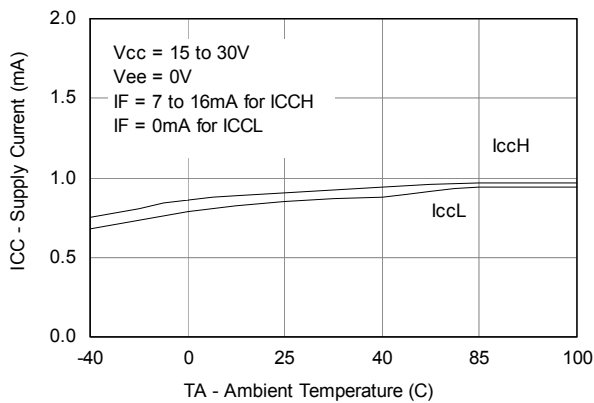


Figure 7: Supply Current vs Temperature

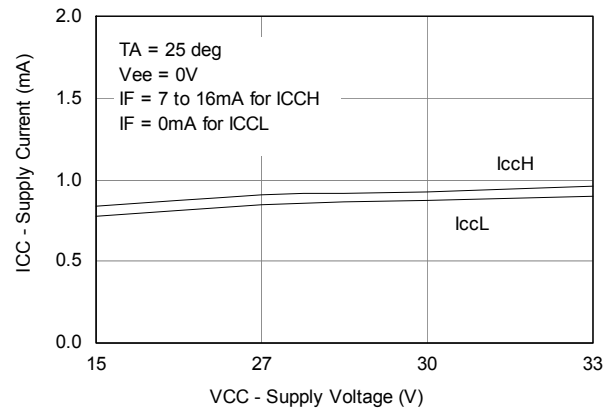


Figure 8: Supply Current vs Supply Voltage

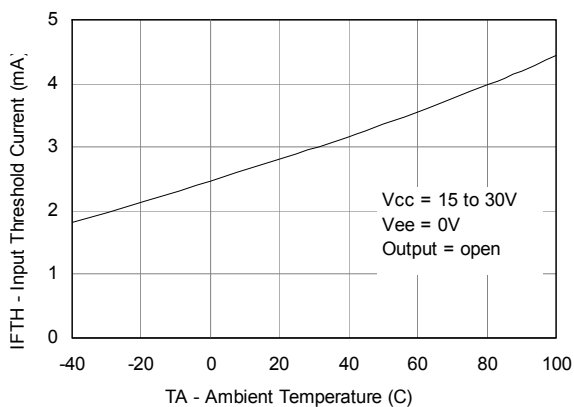


Figure 9: Low to High Threshold Current vs Temperature

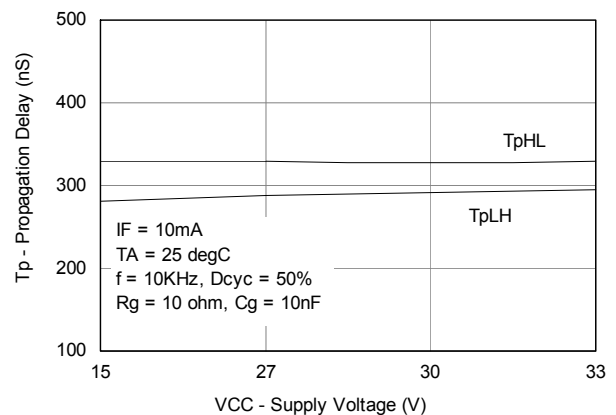


Figure 10: Propagation vs Vcc

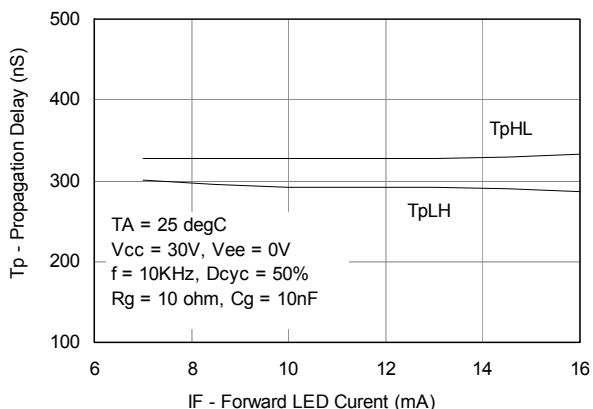


Figure 11: Propagation vs Input Current

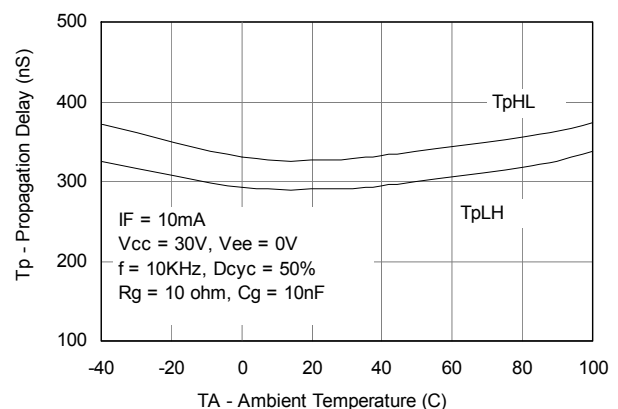


Figure 12: Propagation vs Temperature

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Typical Performance Curves (Continued)

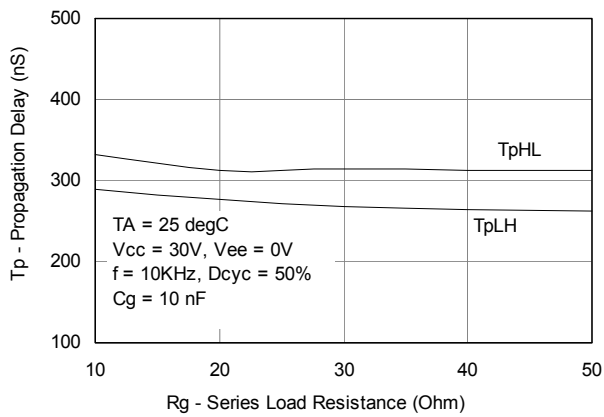


Figure 13: Propagation vs Series Load Resistance

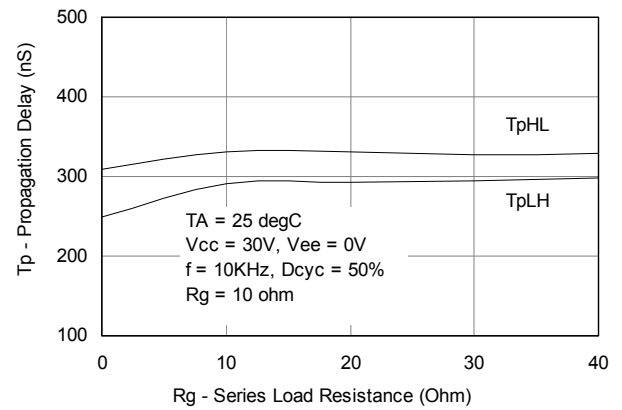


Figure 14: Propagation vs Load Capacitance (nF)

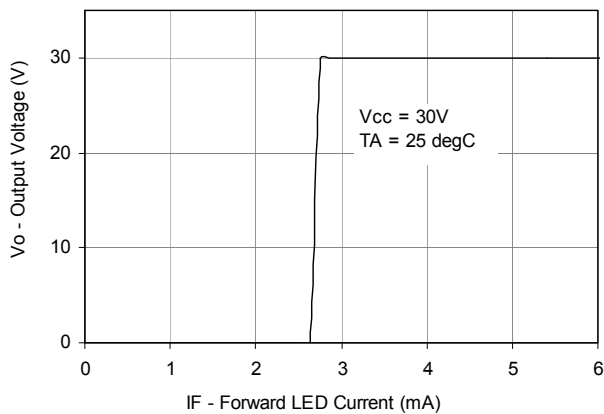


Figure 16: Transfer Characteristics

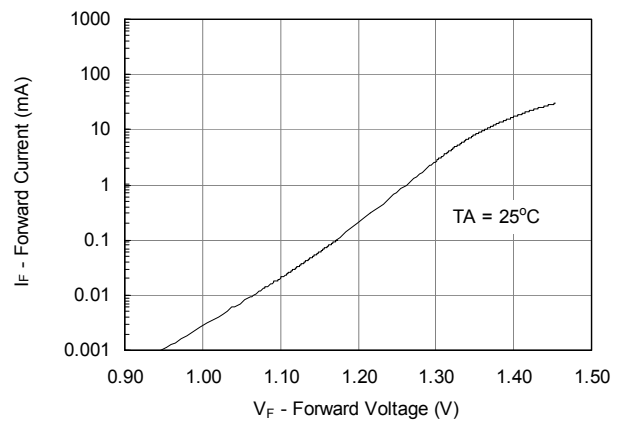


Figure 15: Input Current vs Forward Voltage

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Test Circuit

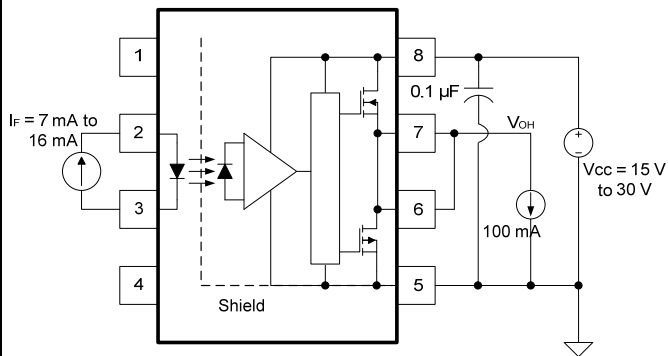


Figure 17 : V_{OH} Test Circuit

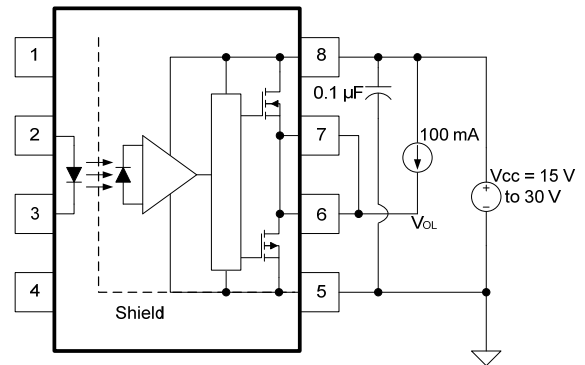


Figure 18 : V_{OL} Test Circuit

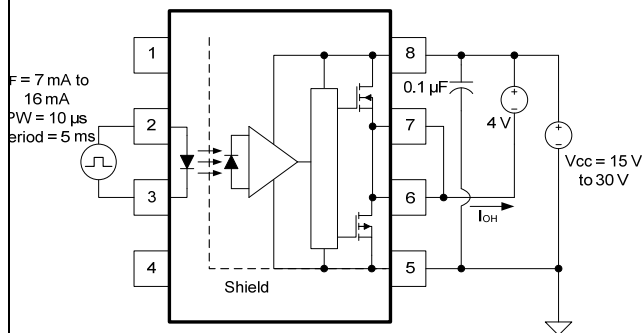


Figure 19 : I_{OH} Test Circuit

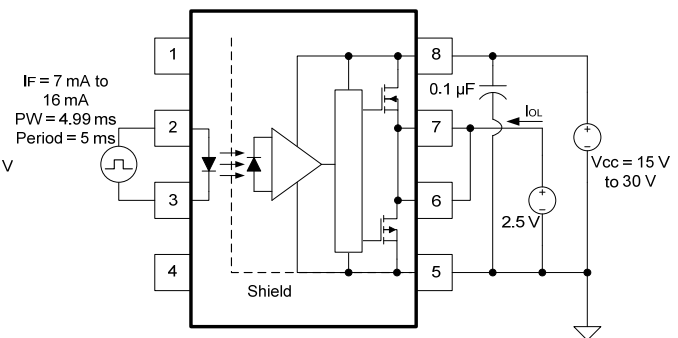


Figure 20 : I_{OL} Test Circuit

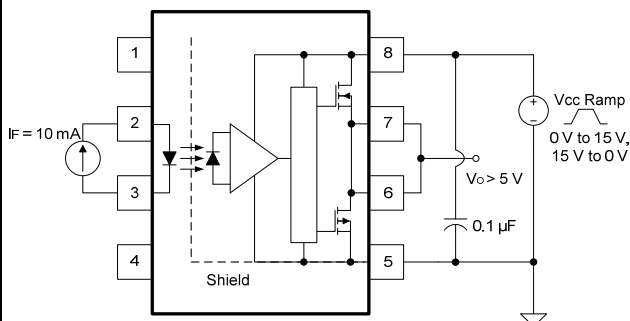


Figure 21 : I_{FLH} Test Circuit

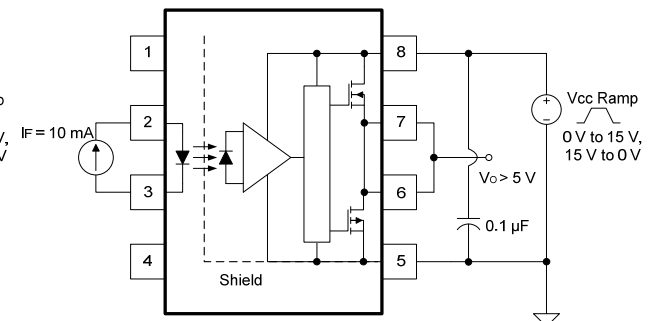


Figure 22 : UVLO Test Circuit

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Test Circuit (Continued)

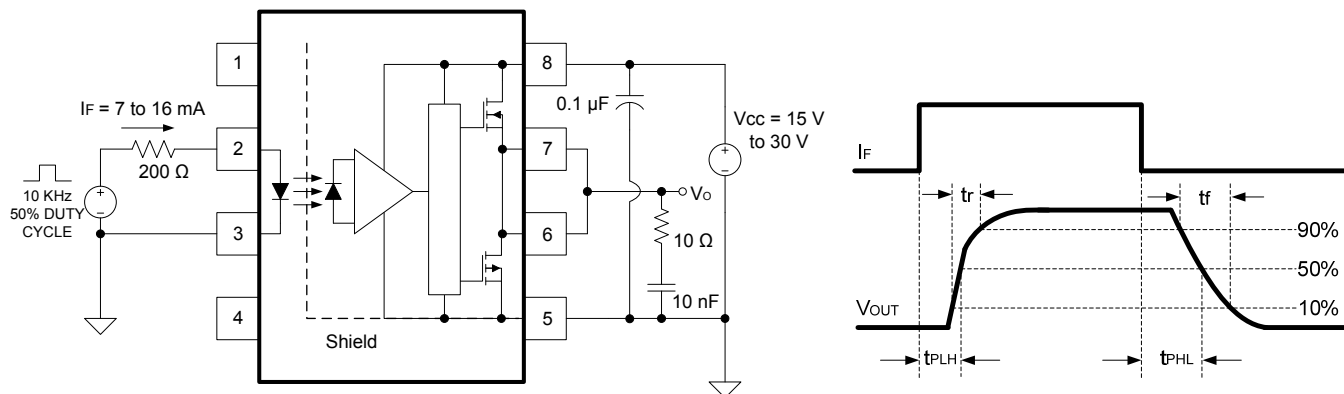


Figure 23 : t_r , t_f , t_{PLH} and t_{PHL} Test Circuit and Waveforms

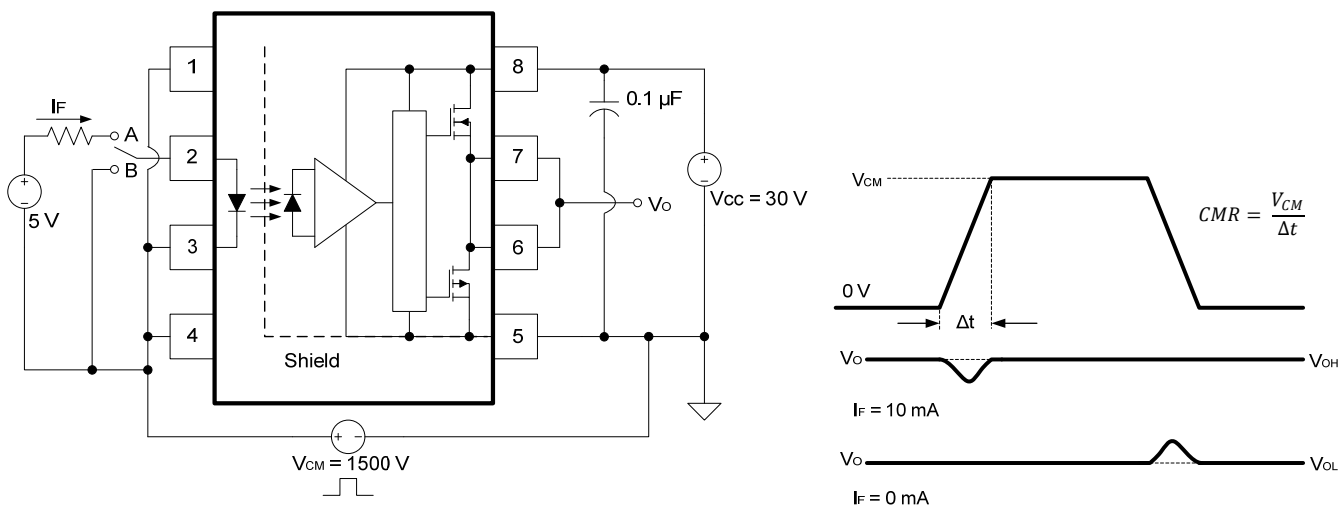


Figure 24 : CMR Test Circuit and Waveforms

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