



CYPRESS

ADVANCED INFORMATION

CY7C1331

CY7C1332

64K x 18 Synchronous Cache 3.3V RAM

Features

- Supports 66-MHz Pentium® processor cache systems with zero wait states
- Single 3.3V power supply
- 64K by 18 common I/O
- Fast clock-to-output times
 - 8.5 ns
- Two-bit wraparound counter supporting the Pentium and 486 burst sequence (CY7C1331)
- Two-bit wraparound counter supporting linear burst sequence (CY7C1332)
- Separate processor and controller address strobes
- Synchronous self-timed write

- Direct interface with the processor and external cache controller
- Asynchronous output enable
- JEDEC-standard pinout
- 52-pin PLCC and PQFP packaging

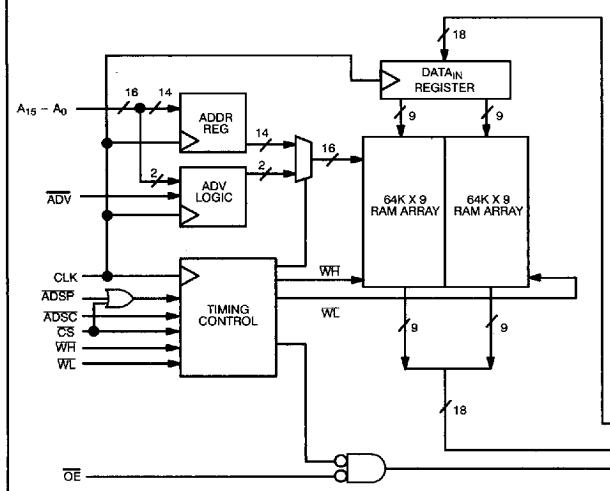
Functional Description

The CY7C1331 and CY7C1332 are 3.3V 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

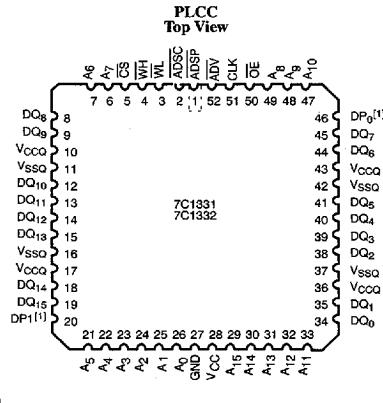
The CY7C1331 is designed for Intel Pentium and i486 CPU-based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1332 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Block Diagram



Pin Configuration



Selection Guide

	7C1331-8 7C1332-8	7C1331-10 7C1332-10	7C1331-12 7C1332-12
Maximum Access Time (ns)	8.5	10	12
Maximum Operating Current (mA)	Commercial: 200 Military: 170	200	200

Note:

1. DP₀ and DP₁ are functionally equivalent to DQ_x.

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Functional Description (continued)

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CS} is LOW and (2) \overline{ADSP} is LOW. \overline{ADSP} -triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1331 and CY7C1332 will be pulled LOW before the next clock rise. \overline{ADSP} is ignored if CS is HIGH.

If WH , WL , or both are LOW at the next clock rise, information presented at DQ_0 – DQ_{15} and DP_0 – DP_1 will be written into the location specified by the address advancement logic. WL controls the writing of DQ_0 – DQ_{15} and DP_0 while WH controls the writing of DQ_8 – DQ_{15} and DP_1 . Because the CY7C1331 and CY7C1332 are common-I/O devices, the output enable signal (OE) must be deasserted before data from the CPU is delivered to DQ_0 – DQ_{15} and DP_0 – DP_1 . As a safety precaution, the appropriate data lines are three-stated in the cycle where WH , WL , or both are sampled LOW, regardless of the state of the OE input.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) \overline{CS} is LOW, (2) \overline{ADSC} is LOW, and (3) WH or WL are LOW. \overline{ADSC} triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at DQ_0 – DQ_{15} and DP_0 – DP_1 will be written into the location specified by the address advancement logic. WL controls the writing of DQ_0 – DQ_7 and DP_0 while WH controls the writing of DQ_8 – DQ_{15} and DP_1 . Since the CY7C1331 and the CY7C1332 are common-I/O devices, the output enable signal (OE) must be deasserted before data from the cache controller is delivered to the data lines. As a safety precaution, the appropriate data lines are three-stated in the cycle where WH , WL , or both are sampled LOW, regardless of the state of the OE input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CS is LOW, (2) \overline{ADSP} or \overline{ADSC} is LOW, and (3) WH and WL are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable (OE) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise.

Burst Sequences

The CY7C1331 provides a 2-bit wraparound counter, fed by pins A_0 – A_1 , that implements the Intel 80486 and Pentium processor address burst sequence (see Table 1). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_0 + 1, A_1$			
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1332 provides a two-bit wraparound counter, fed by pins A_0 – A_1 , that implements a linear address burst sequence (see Table 2).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_0 + 1, A_1$			
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 512-Kbyte secondary cache for a hypothetical 3.3V, 66-MHz Pentium or i486 processor using four CY7C1331 cache RAMs.

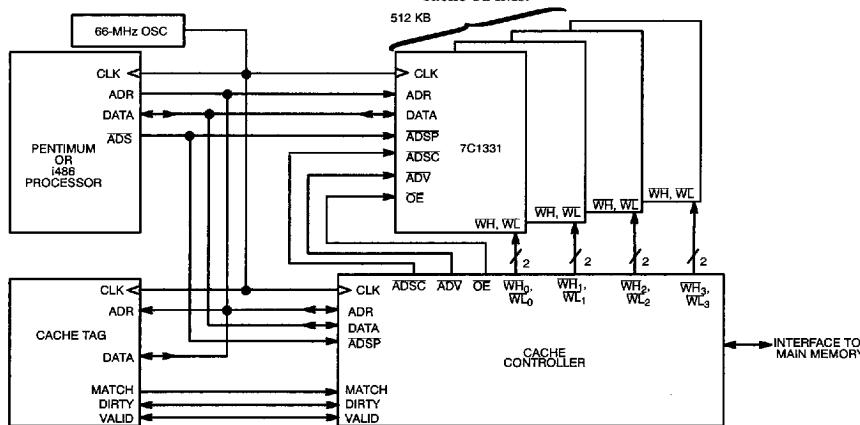


Figure 1. Cache Using Four CY7C1331s

1331-3

Pin Definitions

Signal Name	Type	# of Pins	Description
V _{CC}	Input	1	+ 3.3V Power
V _{CC0}	Input	4	+ 3.3V (Outputs)
GND	Input	1	Ground
V _{SS0}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
A ₁₅ – A ₀	Input	16	Address
ADSP	Input	1	Address Strobe from Processor
ADSC	Input	1	Address Strobe from Cache Controller
WH	Input	1	Write Enable – High Byte
WL	Input	1	Write Enable – Low Byte
ADV	Input	1	Advance
OE	Input	1	Output Enable
CS	Input	1	Chip Select
DQ ₁₅ –DQ ₀	Input/Output	16	Regular Data
DP ₁ –DP ₀	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: ADSP, ADSC, WH, WL, CS, and ADV. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A ₁₅ –A ₀	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if ADSP or ADSC is LOW. The rising edge of the clock also loads the lower two address lines, A ₁ – A ₀ , into the on-chip auto-address-increment logic if ADSP or ADSC is LOW.
ADSP	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or ADSC is asserted, A ₀ –A ₁₅ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both ADSP and ADSC are asserted at the rising edge of CLK, only ADSP will be recognized. The ADSP input should be connected to the ADS output of the processor. ADSP is ignored when CS is HIGH.
ADSC	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or ADSP is asserted, A ₀ –A ₁₅ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The ADSC input should not be connected to the ADS output of the processor.

Signal Name	I/O	Description
WH	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WH is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₁₅ – DQ ₈ and DP ₁ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WH, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WH, is ignored. Note that ADSP has no effect on WH if CS is HIGH.
WL	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If WL is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of DQ ₇ – DQ ₀ and DP ₀ from the on-chip data register into the selected RAM location. There is one exception to this. If ADSP, WL, and CS are asserted (LOW) at the rising edge of CLK, the write signal, WL, is ignored. Note that ADSP has no effect on WL if CS is HIGH.
ADV	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the two-bit on-chip auto-address-increment counter. In the CY7C1332, the address will be incremented linearly. In the CY7C1331, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if ADSP or ADSC is asserted concurrently with CS. Note that ADSP has no effect on ADV if CS is HIGH.
CS	I	Chip select. This signal is sampled by the rising edge of CLK. If CS is HIGH and ADSC is LOW, the SRAM is deselected. If CS is LOW and ADSC or ADSP is LOW, a new address is captured by the address register. If CS is HIGH, ADSP is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description	Signal Name	I/O	Description
OE	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If OE is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as CS was asserted when it was sampled at the beginning of the cycle). If OE is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.	DP ₁ -DP ₀	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as DQ ₁₅ - DQ ₀ , but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP ₁ is an input to and an output from the high-order half of the RAM array, while DP ₀ is an input to and an output from the lower-order half of the RAM array.
Bidirectional Signals					
DQ ₁₅ -DQ ₀	I/O	Sixteen bidirectional data I/O lines. DQ ₁₅ - DQ ₈ are inputs to and outputs from the high-order half of the RAM array, while DQ ₇ - DQ ₀ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by OE: when OE is high, the data pins are three-stated and can be used as inputs; when OE is low, the data pins are driven by the output buffers and are outputs. DQ ₁₅ - DQ ₈ and DQ ₇ - DQ ₀ are also three-stated when $W\bar{H}$ and $W\bar{L}$, respectively, are sampled LOW at clock rise.			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)	Storage Temperature	-65°C to +150°C	Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Ambient Temperature with			Latch-Up Current	>200 mA
Power Applied	-55°C to +125°C			
Supply Voltage on V _{CC} Relative to GND	-0.5V to +3.6V			
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to V _{CC} + 0.3V		Ambient Temperature ^[3]	
DC Input Voltage ^[2]	-0.5V to V _{CC} + 0.3V		Range	V _{CC} , V _{CCQ}
Current into Outputs (LOW)	20 mA		Com'l	0°C to +70°C
			Mil	-55°C to +125°C

Electrical Characteristics Over the Operating Range^[4]

Parameter	Description	Test Conditions	7C1331-8 7C1332-8		7C1331-10 7C1332-10		7C1331-12 7C1332-12		Unit
			Min.	Max.	Min.	Max.	Min.	Min.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _X	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	µA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{out} = 0mA, f = f _{MAX} = 1/t _{CYC}	Com'l	200		200		170	mA
			Mil					200	

Notes:

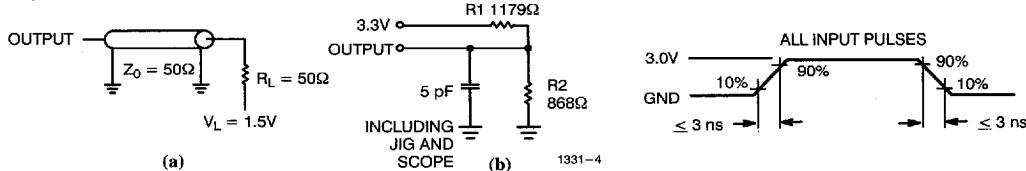
2. Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range^[4](continued)

Parameter	Description	Test Conditions	7C1331-8 7C1332-8		7C1331-10 7C1332-10		7C1331-12 7C1332-12		Unit
			Min.	Max.	Min.	Max.	Min.	Min.	
I _{SB1}	Automatic CE Power-Down Current - TTL Inputs	Max. V _{CC} , CS ≥ V _{IH} , V _{IN} ≥ V _{IL} or V _{IN} ≤ V _{IL} , f=f _{MAX}	Com'l	60		60		40	mA
			Mil					40	
I _{SB2}	Automatic CE Power-Down Current -CMOS Inputs	Max. V _{CC} , CS ≥ V _{CC} -0.3V, V _{IN} ≥ V _{CC} -0.3V or V _{IN} ≤ 0.3V, f=f _{MAX} ^[6]	Com'l	20		20		20	mA
			Mil					20	

Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	Com'l	5 pF
C _{IN} : Other Inputs	Input Capacitance		Mil	6 pF
C _{OUT}	Output Capacitance		Com'l	5 pF
			Mil	8 pF
			Com'l	8 pF
			Mil	16 pF

AC Test Loads and Waveforms


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Notes:

6. Inputs are disabled, clock is allowed to run at speed.

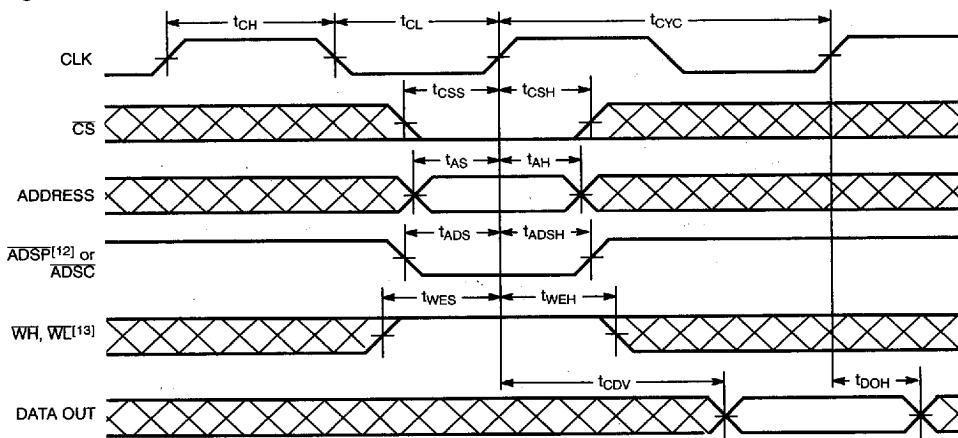
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[8]

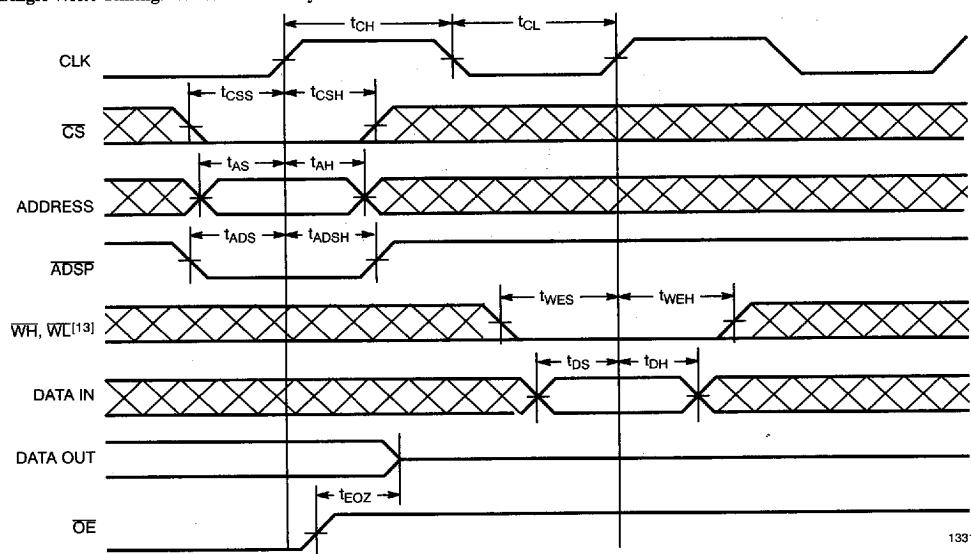
Parameter	Description	7C1331-8 7C1332-8		7C1331-10 7C1332-10		7C1331-12 7C1332-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		8.5		10		12	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	ADSP, ADSC Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADSH}	ADSP, ADSC Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	WH, WL Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{WEH}	WH, WL Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	ADV Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADVH}	ADV Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSOZ}	Chip Select Sampled to Output High Z ^[9]	2	6	2	6	2	7	ns
t_{EOZ}	OE HIGH to Output High Z ^[9]	2	6	2	6	2	7	ns
t_{EOV}	OE LOW to Output Valid		5		5		6	ns
t_{WEOZ}	WH or WL Sampled LOW to Output High Z ^[9,10]		5		6		7	ns
t_{WEOV}	WH or WL Sampled HIGH to Output Valid ^[10]		8.5		10		12	ns

Notes:

8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance as shown in (a) and (b) of AC Test Loads.
9. t_{CSOZ} , t_{EOZ} , and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms
Single Read^[11]


1331-7

Single Write Timing: Write Initiated by ADSP


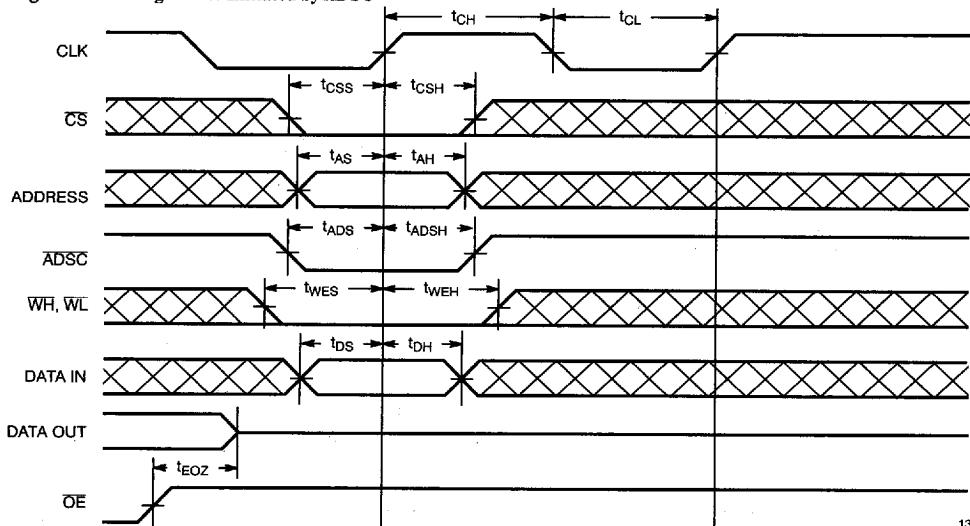
1331-6

Notes:

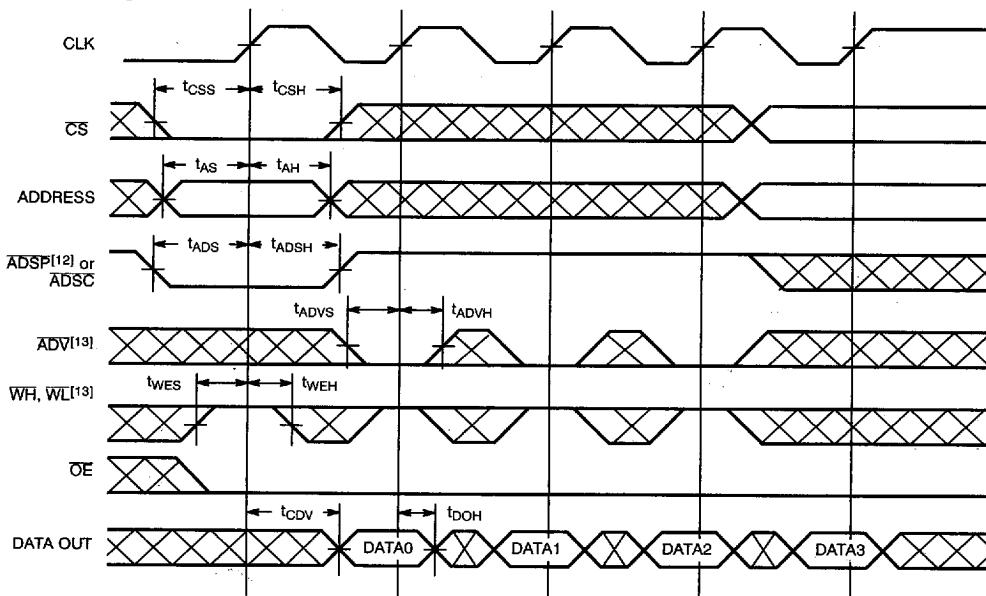
11. OE is LOW throughout.

12. If ADSP is asserted while CS is HIGH, ADSP will be ignored.

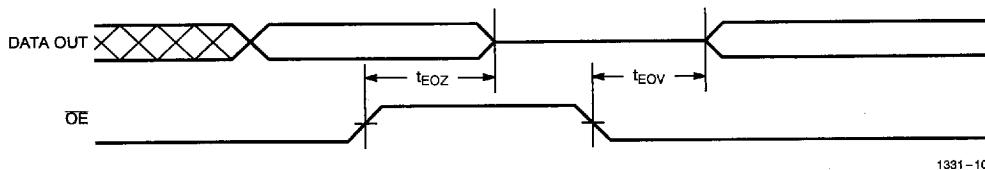
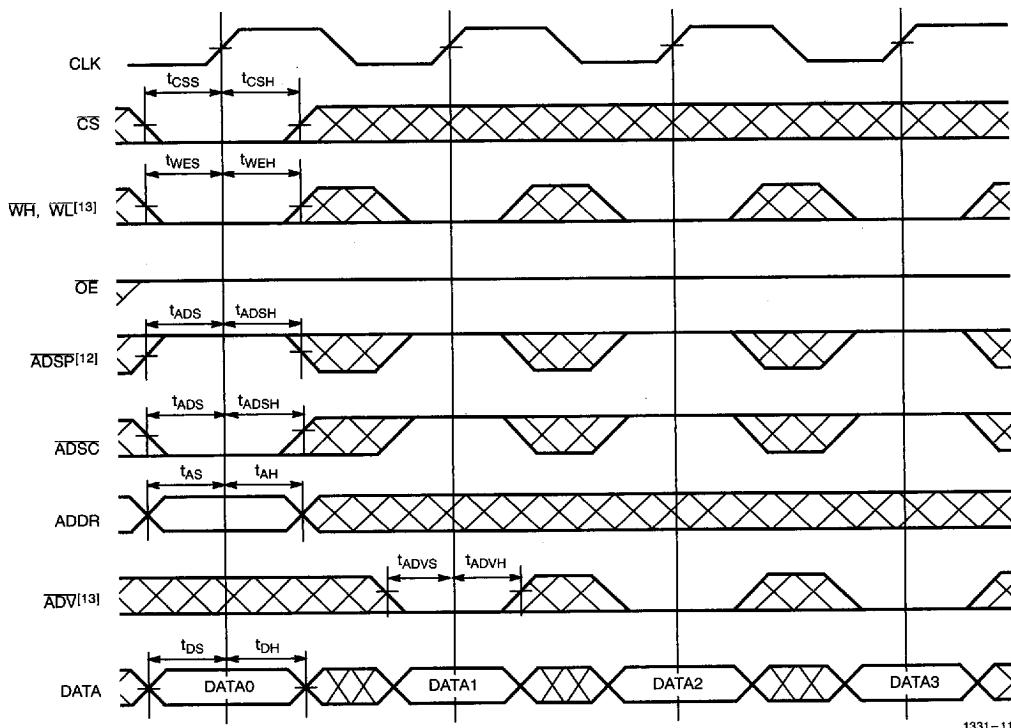
13. ADSP has no effect on ADV, WH, and WL if CS is HIGH.

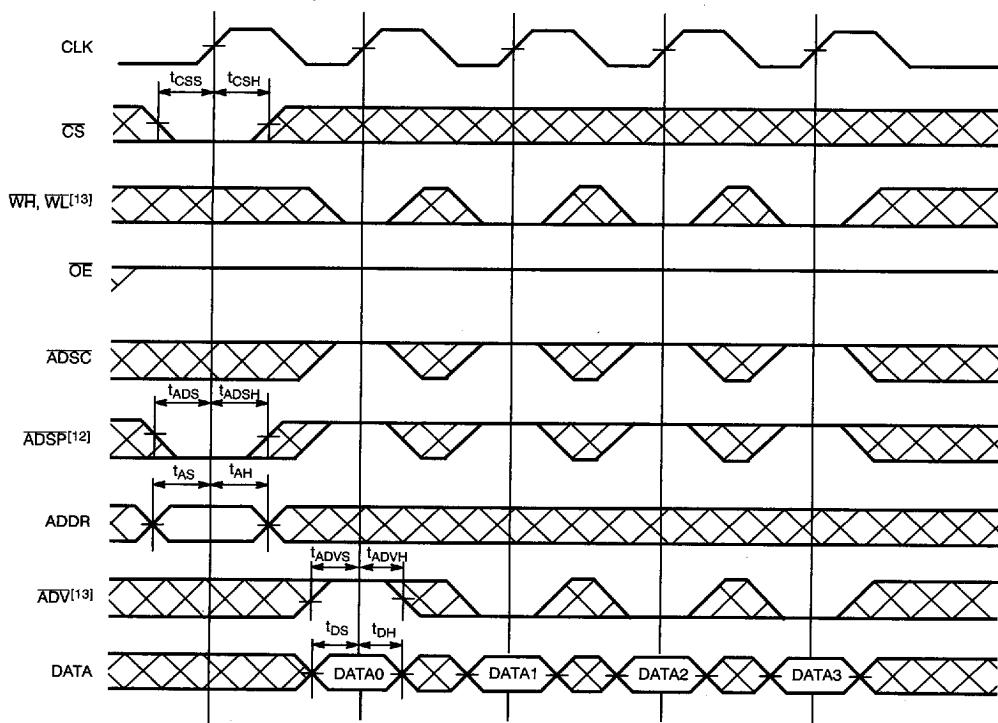
Switching Waveforms (continued)
Single Write Timing: Write Initiated by ADSC


1331-8

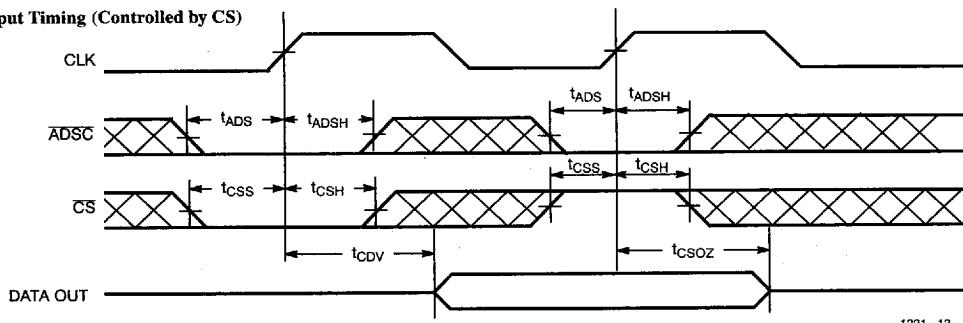
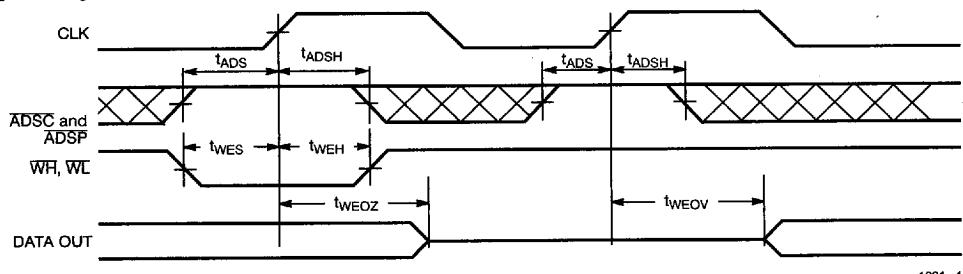
Burst Read Sequence with Four Accesses


1331-9

Switching Waveforms (continued)
Output (Controlled by \overline{OE})

Write Burst Timing: Write Initiated by \overline{ADSC}


Switching Waveforms (continued)
Write Burst Timing: Write Initiated by ADSP


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Switching Waveforms (continued)
Output Timing (Controlled by CS)

Output Timing (Controlled by WH/WL)

Truth Table

Inputs						Address	Operation
CS	ADSP	ADSC	ADV	WH or WL	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle (ADSP ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence (ADSP ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle (ADSP ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence (ADSP ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, begin burst
X	H	H	H	L	L→H	Same address as previous cycle	Read cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle



CYPRESS

ADVANCED INFORMATION

CY7C1331

CY7C1332

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1331-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1331-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1331-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331-12NC	N52	52-Lead Plastic Quad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8.5	CY7C1332-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-8NC	N52	52-Lead Plastic Quad Flatpack	
10	CY7C1332-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-10NC	N52	52-Lead Plastic Quad Flatpack	
12	CY7C1332-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332-12NC	N52	52-Lead Plastic Quad Flatpack	

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