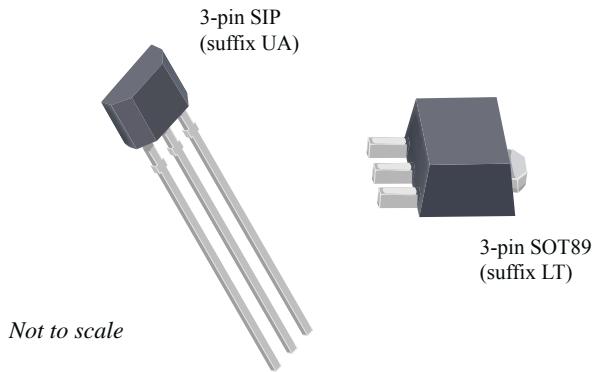


Hall Effect Latch for High Temperature Operation

Features and Benefits

- Symmetrical switchpoints
- Superior temperature stability
- Operation from unregulated supply
- Open-drain 25 mA output
- Reverse Battery protection
- Activate with small, commercially available permanent magnets
- Solid-state reliability
- Small size
- Resistant to physical stress
- Enhanced ESD structures result in 8 kV HBM ESD performance without external protection components
- Internal protection circuits enable 40 V load dump compliance without external protection components

Packages:



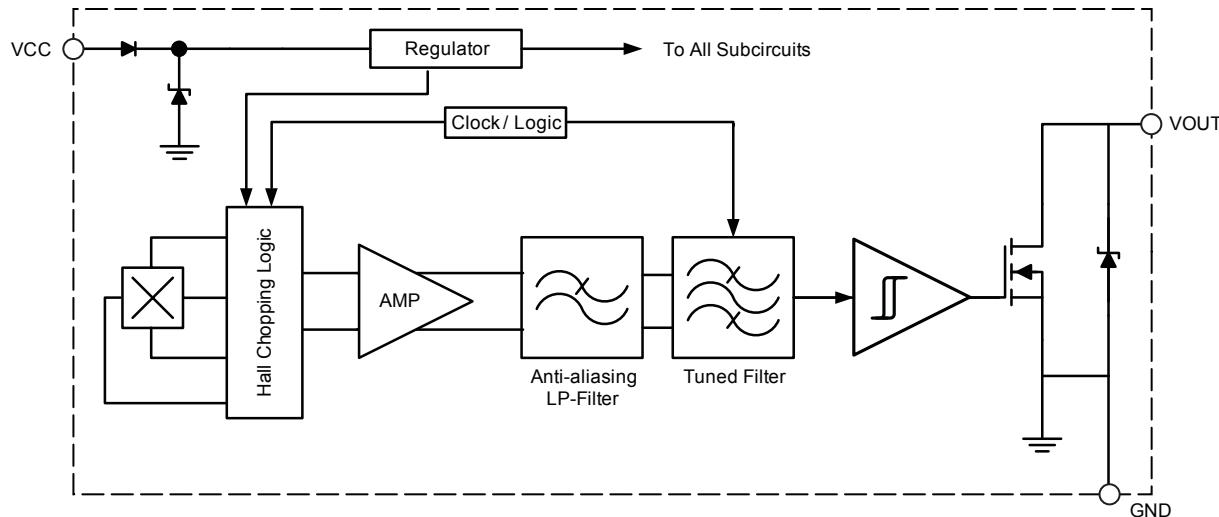
Description

These Hall-effect latches are extremely temperature-stable and stress resistant sensor ICs especially suited for operation over extended temperature ranges to 150°C. Superior high-temperature performance is made possible through a novel Schmitt trigger circuit that maintains operate and release point symmetry by compensating for temperature changes in the Hall element. Additionally, internal compensation provides magnetic switchpoints that become more sensitive with temperature, hence offsetting the usual degradation of the magnetic field with temperature. The symmetry capability makes these devices ideal for use in pulse-counting applications where duty cycle is an important parameter. The three basic devices (A1225, A1227, and A1229) are identical except for magnetic switchpoints.

Each device includes on a single silicon chip a voltage regulator, Hall-voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and a buffered open-drain output to sink up to 25 mA. The on-board regulator permits operation with supply voltages of 3.8 to 24 V.

The first character of the part number suffix determines the device operating temperature range. Suffix L is for -40°C to 150°C. Two package styles provide a magnetically optimized package for most applications. Suffix LT is a miniature SOT89/TO-243AA transistor package for surface-mount applications, suffix UA is a three-lead ultra-mini-SIP. Both packages are lead (Pb) free with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Packing*	Package	Ambient Temperature, T_A	$B_{RP}(\text{min})$ (G)	$B_{OP}(\text{max})$ (G)
A1225LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–300	300
A1225LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1227LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–175	175
A1227LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1229LLTTK-T	13-in. reel, 4000 pieces/reel	3-pin SOT89 surface mount	–40°C to 150°C	–200	200
A1229LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			

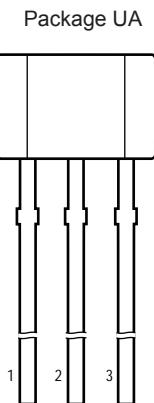
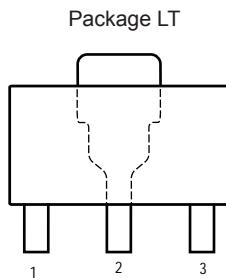
*Contact Allegro™ for additional packaging options.



Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		–30	V
Output Off Voltage	V_{OUT}		30	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Continuous Output Current	$I_{OUT(SINK)}$		25	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_J(\text{max})$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pin-out Diagrams



Terminal List Table

Number	Name	Function
1	V_{CC}	Input power supply
2	GND	Ground
3	V_{OUT}	Output signal

ELECTRICAL CHARACTERISTICS Valid at $T_A = -40^\circ\text{C}$ to 150°C , $C_{\text{BYPASS}} = 0.1 \mu\text{F}$, $V_{\text{CC}} = 12 \text{ V}$; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. ¹	Max.	Unit ²
Electrical Characteristics						
Supply Voltage	V_{CC}	Operating; $T_J \leq 165^\circ\text{C}$	3.8	—	24	V
Supply Current	I_{CC}	$B < B_{\text{RP}}$ (Output off)	—	—	6	mA
		$B > B_{\text{OP}}$ (Output on)	—	—	6	mA
Supply Zener Voltage	$V_{Z(\text{sup})}$	$I_{\text{CC}} = 9 \text{ mA}$, $T_A = 25^\circ\text{C}$	28	—	—	V
Reverse Battery Current	$I_{Z(\text{sup})}$	$V_{\text{RCC}} = -28 \text{ V}$, $T_A = 25^\circ\text{C}$	—	—	-5	mA
Power-On Time ³	t_{PO}		—	—	12	μs
Power-On State	POS	$B < B_{\text{OP}}$	—	HIGH	—	—
Chopping Frequency	f_{chop}		—	400	—	kHz
Output Stage Characteristics						
Output Saturation Voltage	$V_{\text{OUT}(\text{sat})}$	$I_{\text{OUT}} = 20 \text{ mA}$	—	175	400	mV
Output Leakage Current	I_{OFF}	$V_{\text{OUT}} = 24 \text{ V}$, $B < B_{\text{RP}}$	—	< 1	10	μA
Output Rise Time ^{3,4}	t_r	$R_L = 820 \Omega$, $C_L = 20 \text{ pF}$	—	200	2000	ns
Output Fall Time ^{3,4}	t_f	$R_L = 820 \Omega$, $C_L = 20 \text{ pF}$	—	200	2000	ns
Output Zener Voltage	$V_{Z(\text{out})}$	$I_{\text{OUT}} = 3 \text{ mA}$, $T_A = 25^\circ\text{C}$	30	—	—	V
Magnetic Characteristics						
Operate Point	B_{OP}	A1225	$T_A = 25^\circ\text{C}$	170	—	G
			Over operating temperature range	140	—	300
		A1227	$T_A = 25^\circ\text{C}$	50	—	150
			Over operating temperature range	50	—	175
		A1229	$T_A = 25^\circ\text{C}$	100	—	180
			Over operating temperature range	80	—	200
Release Point	B_{RP}	A1225	$T_A = 25^\circ\text{C}$	-270	—	-170
			Over operating temperature range	-300	—	-140
		A1227	$T_A = 25^\circ\text{C}$	-150	—	-50
			Over operating temperature range	-175	—	-50
		A1229	$T_A = 25^\circ\text{C}$	-180	—	-100
			Over operating temperature range	-200	—	-80
Hysteresis ($B_{\text{OP}} - B_{\text{RP}}$)	B_{HYS}	A1225	$T_A = 25^\circ\text{C}$	340	—	540
			Over operating temperature range	280	—	600
		A1227	$T_A = 25^\circ\text{C}$	100	—	300
			Over operating temperature range	100	—	350
		A1229	$T_A = 25^\circ\text{C}$	200	—	360
			Over operating temperature range	160	—	400

¹Typical data are at $T_A = 25^\circ\text{C}$ and $V_{\text{CC}} = 12 \text{ V}$, and are for design estimations only.

²1 G (gauss) = 0.1 mT (millitesla).

³Minimum and maximum specifications verified by bench characterization and not guaranteed by Allegro final test.

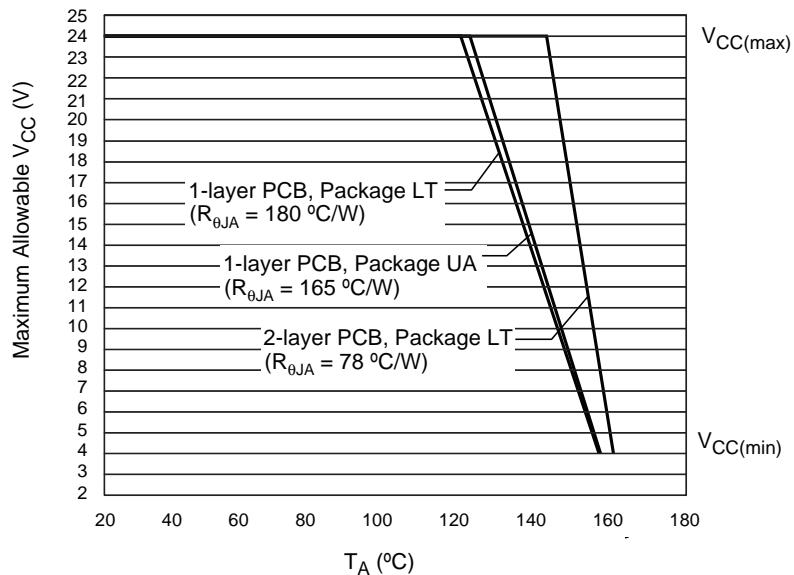
⁴ C_L = oscilloscope probe capacitance.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

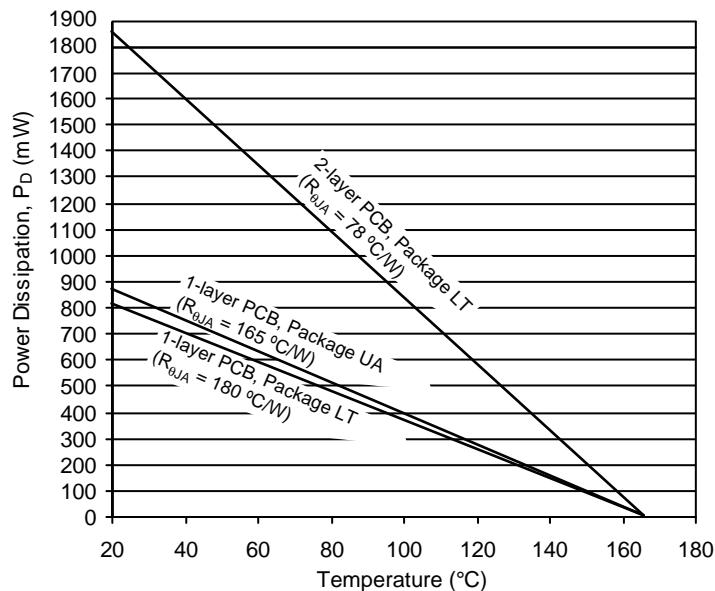
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LT, 1-layer PCB with copper limited to solder pads	180	$^{\circ}\text{C}/\text{W}$
		Package LT, 2-layer PCB with 0.94 in ² copper each side	78	$^{\circ}\text{C}/\text{W}$
		Package UA, 1-layer PCB with copper limited to solder pads	165	$^{\circ}\text{C}/\text{W}$

*Additional thermal information available on Allegro website.

Power Derating Curve



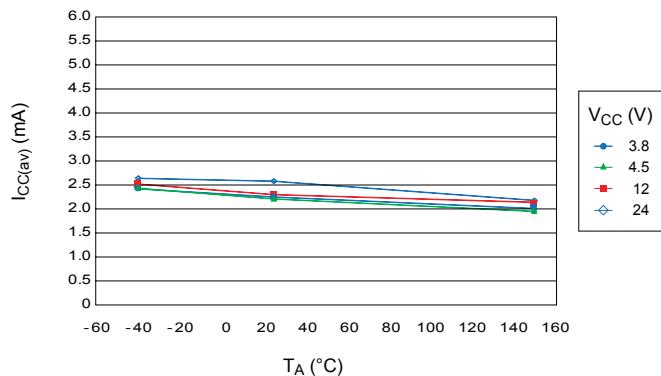
Power Dissipation



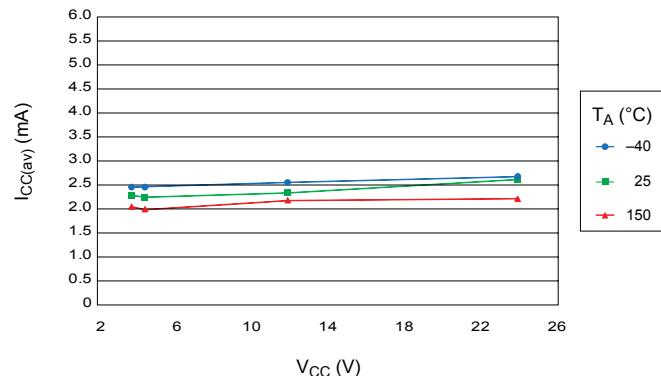
Characteristic Performance

A1225, A1227, and A1229 Electrical Characteristics

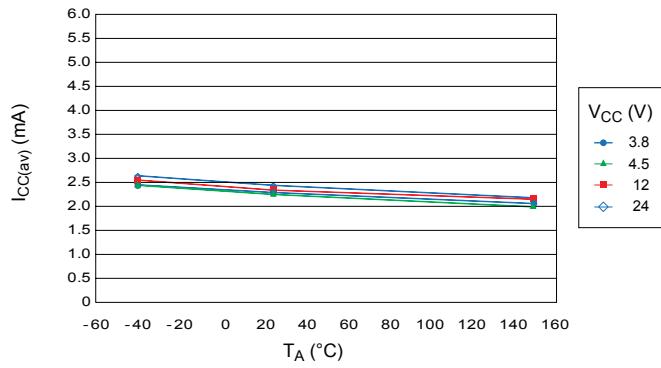
Average Supply Current (On) versus Ambient Temperature



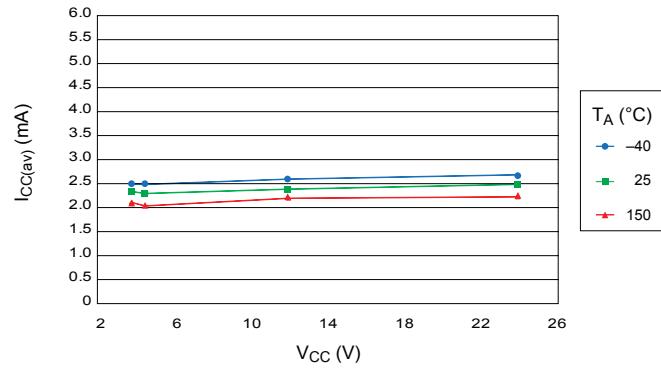
Average Supply Current (On) versus Supply Voltage



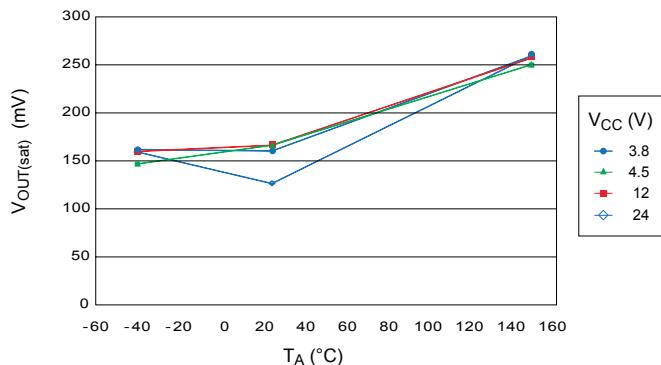
Average Supply Current (Off) versus Ambient Temperature



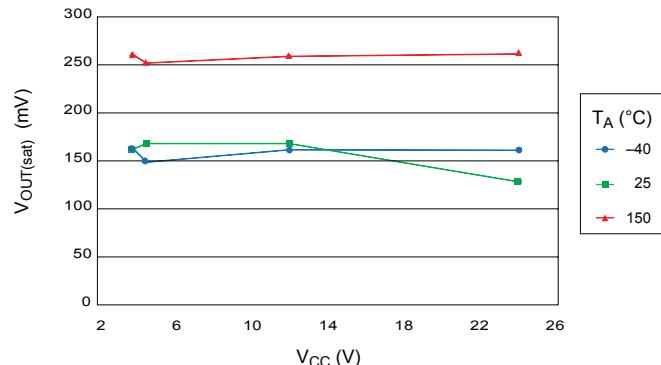
Average Supply Current (Off) versus Supply Voltage



Average Output Saturation Voltage versus Ambient Temperature

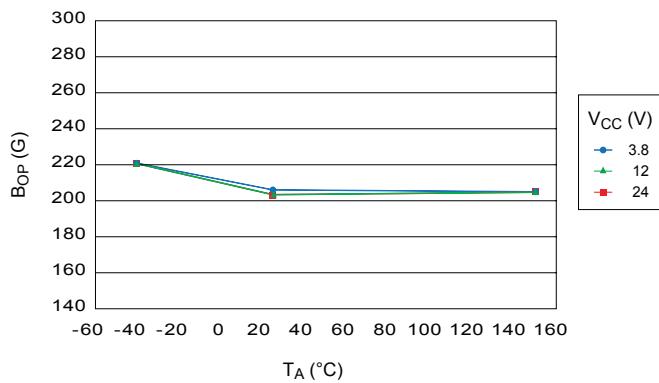


Average Output Saturation Voltage versus Supply Voltage

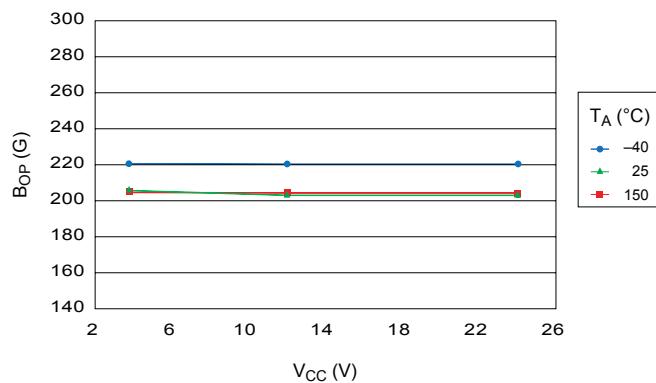


A1225 Magnetic Characteristics

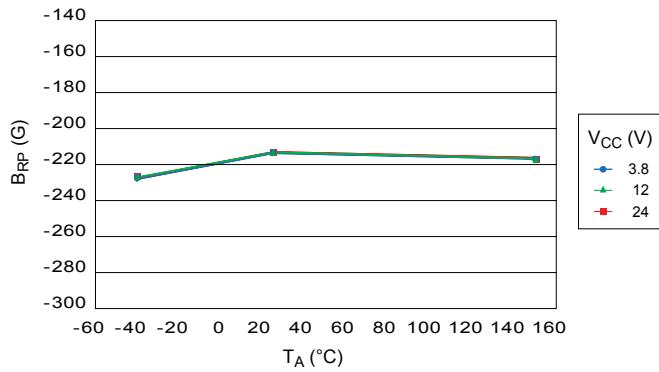
Operate Point versus Ambient Temperature



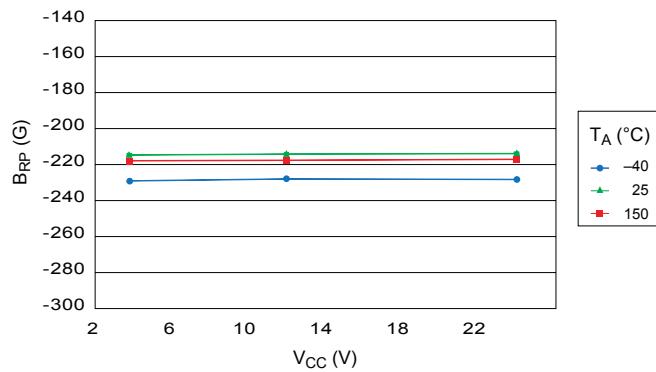
Operate Point versus Supply Voltage



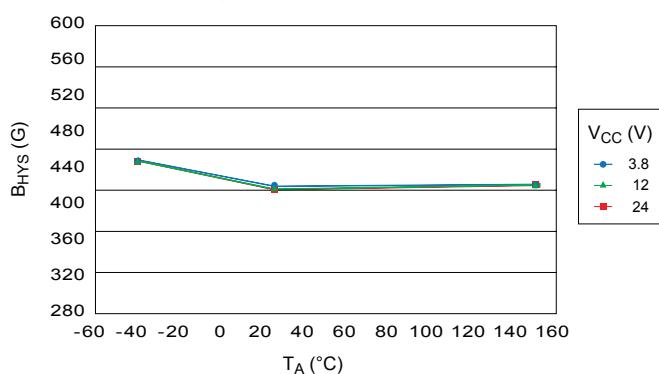
Release Point versus Ambient Temperature



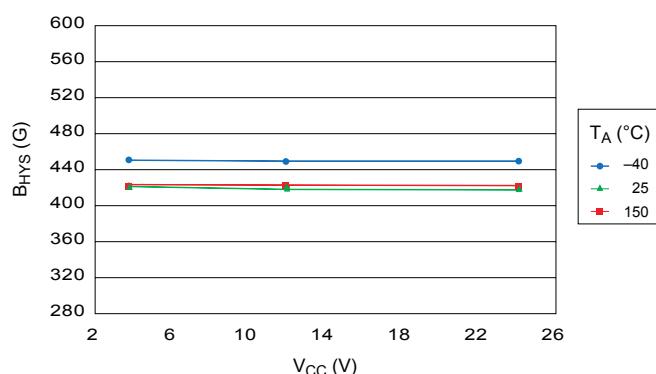
Release Point versus Supply Voltage



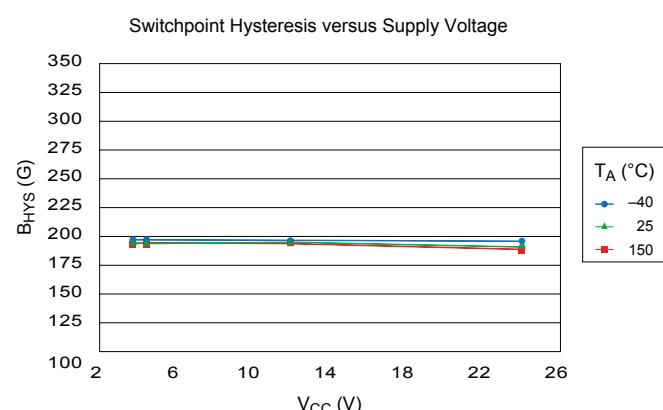
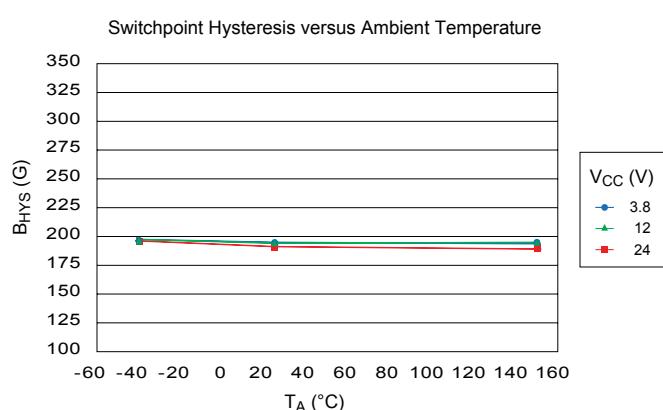
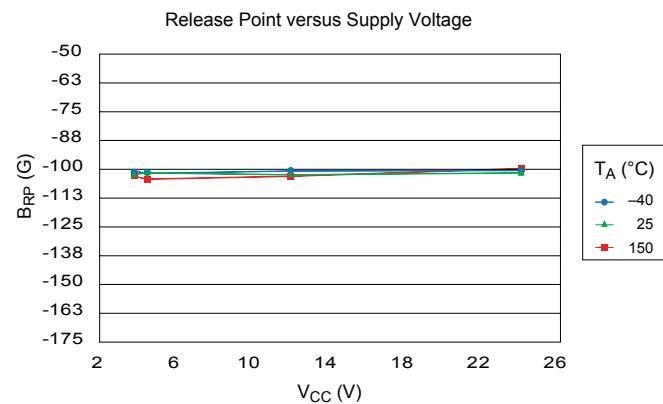
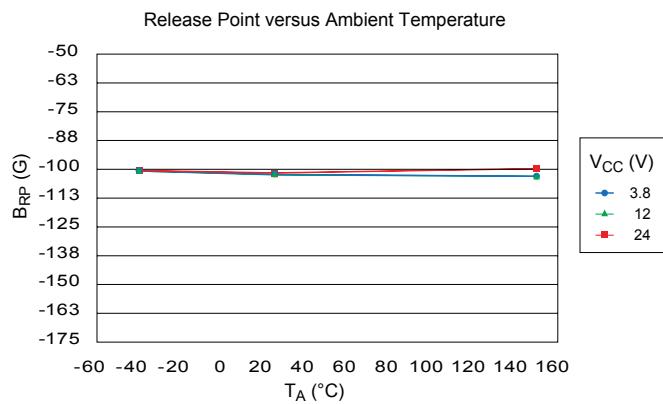
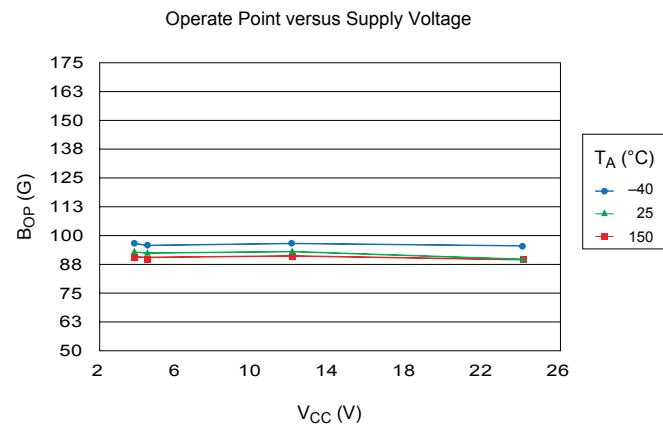
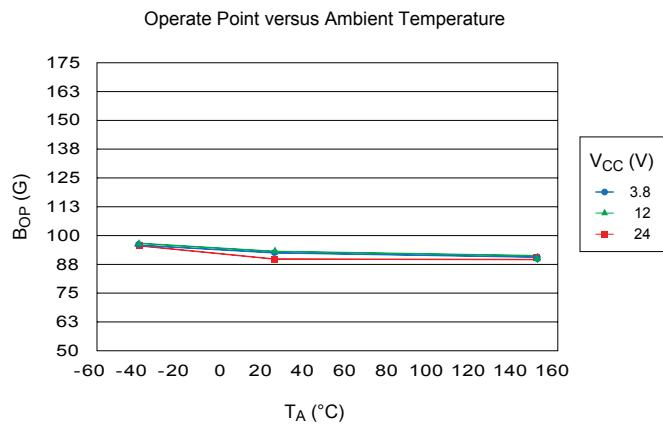
Switchpoint Hysteresis versus Ambient Temperature



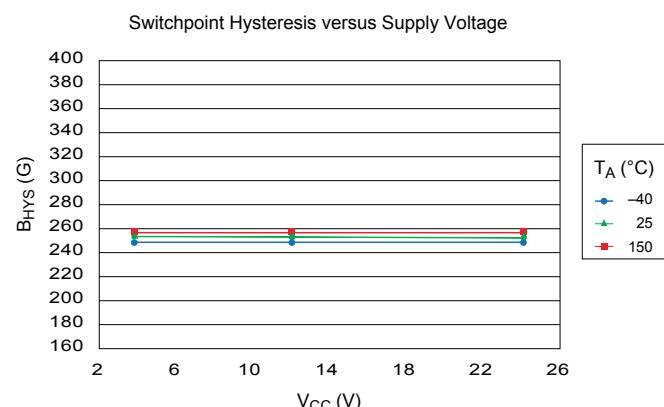
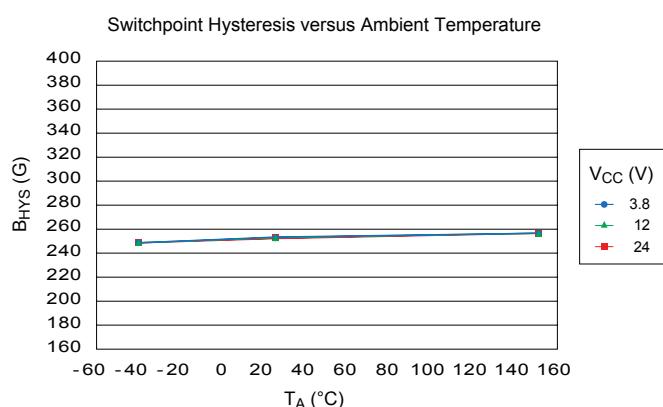
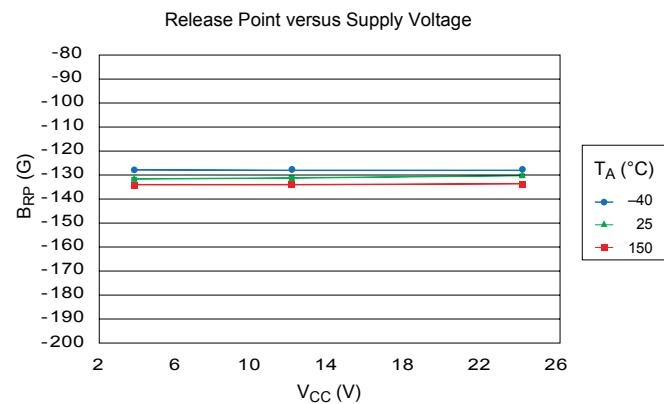
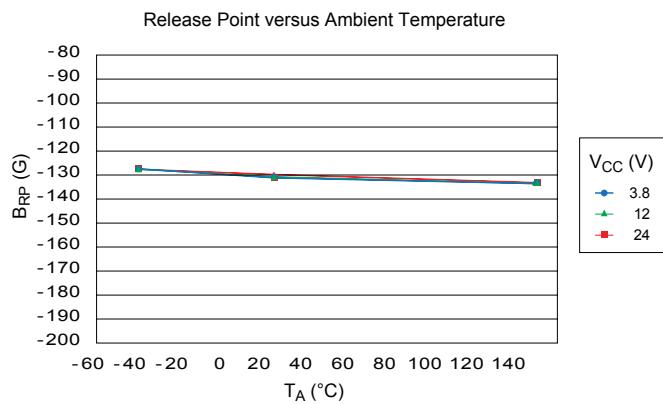
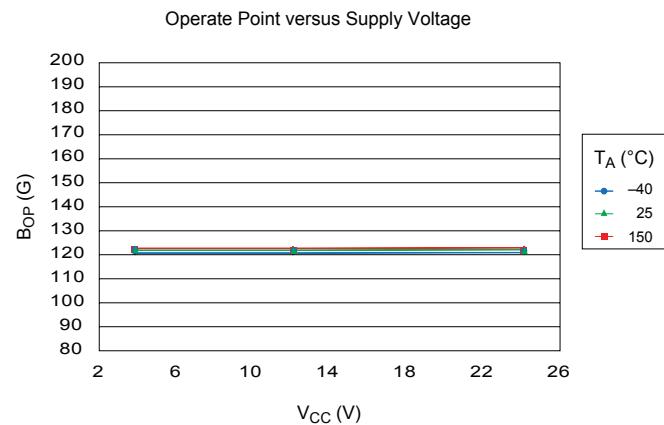
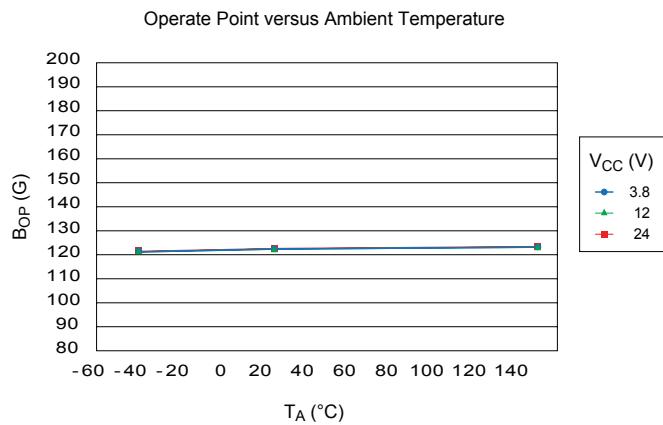
Switchpoint Hysteresis versus Supply Voltage



A1227 Magnetic Characteristics



A1229 Magnetic Characteristics



Functional Description and Application Information

Switching Behavior

The output of the A1225, A1227, and A1229 devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see figure 1). After turn-on, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(sat)}$. Notice that the device latches; that is, a south pole of sufficient strength towards the branded surface of the device turns the device on, and the device remains on with removal of the south pole.

When the magnetic field is reduced below the release point, B_{RP} , the device output goes high (turns off). The difference between the magnetic operate point and release point is the hysteresis, B_{HYS} , of the device. This built-in hysteresis allows clean switching of the output, even in the presence of external mechanical vibration and electrical noise.

When the device is powered-on in the hysteresis range, less than B_{OP} and higher than B_{RP} , the device output goes high. The correct output state is attained after the first excursion beyond B_{OP} or B_{RP} .

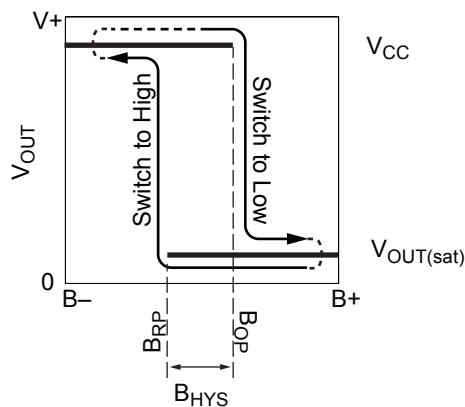


Figure 1. Output switching characteristics

Application Information

The simplest form of magnet that will operate these devices is a ring magnet, as shown in figure 2. Other methods of operation are possible.

In three-wire applications the device output is connected through a pull-up resistor to the supply pin or separate battery voltage (figure 3). Switching of the output signal indicates sufficient change of the magnetic field.

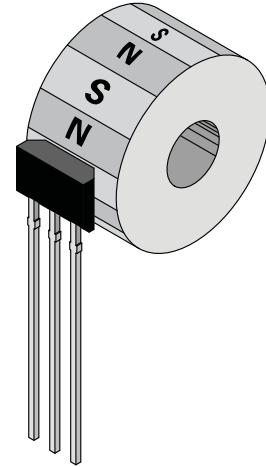


Figure 2. Typical magnetic target configuration using a ring magnet

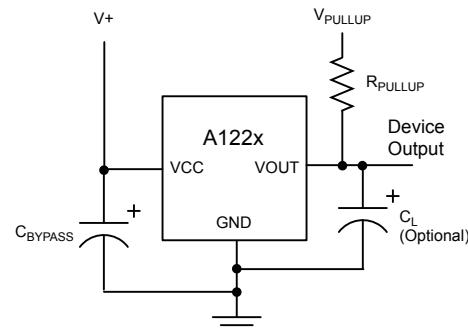


Figure 3. Typical 3-wire application circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a patented technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset

becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For the demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

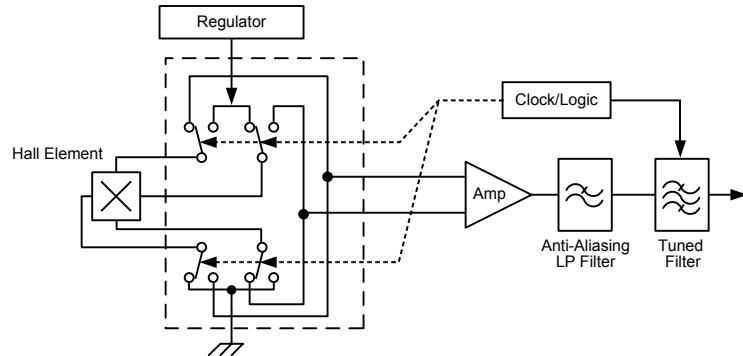
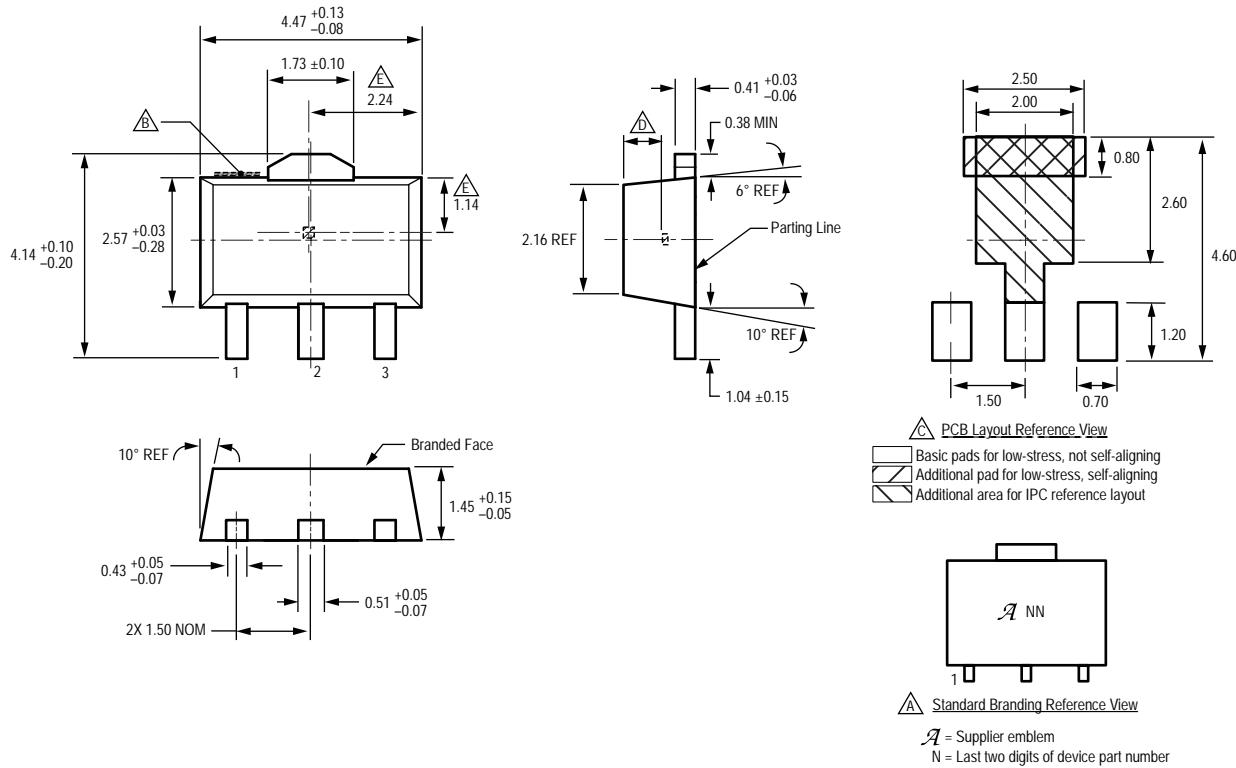


Figure 4. Chopper stabilization technique

Package LT 3-Pin SOT-89



Updated package drawing only. Allegro package assembly tooling has not changed.
For Reference Only; not for tooling use (reference DWG-9064)

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown

Branding scale and appearance at supplier discretion

Gate and tie bar burr area

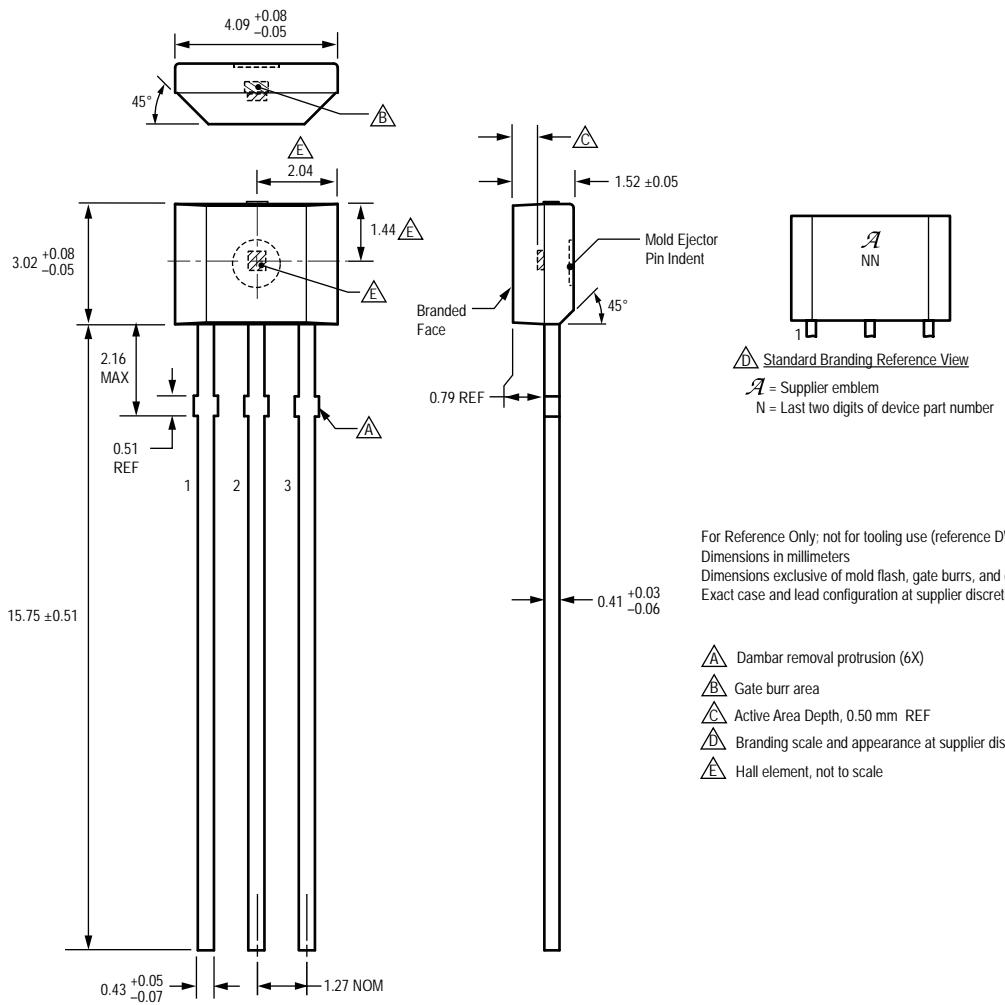
Reference land pattern layout:

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Active Area Depth, 0.77 mm

Hall element: not to scale

Package UA 3-Pin SIP



Revision History

Revision	Revision Date	Description of Revision
Rev. 2	May 8, 2013	Update product offerings, editorial correction to $I_{Z(sup)}$

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