ADSP-2100 Family DSP Microcomputers

ADSP-21xx

SUMMARY

16-Bit Fixed-Point DSP Microprocessors with On-Chip Memory
Enhanced Harvard Architecture for Three-Bus Performance: Instruction Bus & Dual Data Buses
Independent Computation Units: ALU, Multiplier/ Accumulator, and Shifter
Single-Cycle Instruction Execution & Multifunction Instructions
On-Chip Program Memory RAM or ROM & Data Memory RAM
Integrated I/O Peripherals: Serial Ports, Timer, Host Interface Port (ADSP-2111 Only)

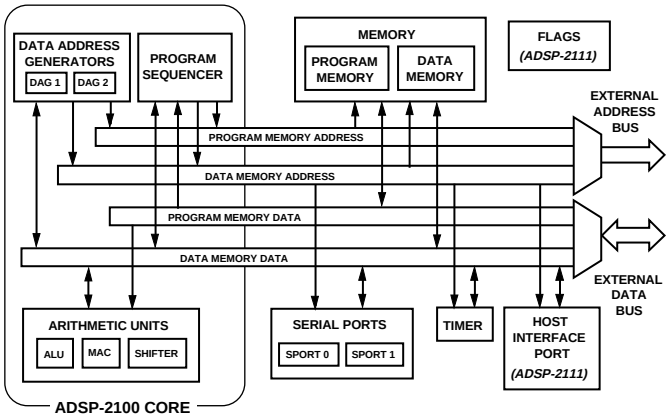
FEATURES

25 MIPS, 40 ns Maximum Instruction Rate
Separate On-Chip Buses for Program and Data Memory
Program Memory Stores Both Instructions and Data (Three-Bus Performance)
Dual Data Address Generators with Modulo and Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM)
Double-Buffered Serial Ports with Companding Hardware, Automatic Data Buffering, and Multichannel Operation
ADSP-2111 Host Interface Port Provides Easy Interface to 68000, 80C51, ADSP-21xx, Etc.
Automatic Booting of ADSP-2111 Program Memory Through Host Interface Port
Three Edge- or Level-Sensitive Interrupts
Low Power IDLE Instruction
PGA, PLCC, PQFP, and TQFP Packages
MIL-STD-883B Versions Available

GENERAL DESCRIPTION

The ADSP-2100 Family processors are single-chip microcomputers optimized for digital signal processing (DSP) and other high speed numeric processing applications. The ADSP-21xx processors are all built upon a common core. Each processor combines the core DSP architecture—computation units, data address generators, and program sequencer—with differentiating features such as on-chip program and data memory RAM, a programmable timer, one or two serial ports, and, on the ADSP-2111, a host interface port.

FUNCTIONAL BLOCK DIAGRAM



This data sheet describes the following ADSP-2100 Family processors:

ADSP-2101	
ADSP-2103	*3.3 V Version of ADSP-2101*
ADSP-2105	*Low Cost DSP*
ADSP-2111	*DSP with Host Interface Port*
ADSP-2115	
ADSP-2161/62/63/64	*Custom ROM-programmed DSPs*

The following ADSP-2100 Family processors are *not* included in this data sheet:

ADSP-2100A	*DSP Microprocessor*
ADSP-2165/66	*ROM-programmed ADSP-216x processors with powerdown and larger on-chip memories (12K Program Memory ROM, 1K Program Memory RAM, 4K Data Memory RAM)*
ADSP-21msp5x	*Mixed-Signal DSP Processors with integrated on-chip A/D and D/A plus powerdown*
ADSP-2171	*Speed and feature enhanced ADSP-2100 Family processor with host interface port, powerdown, and instruction set extensions for bit manipulation, multiplication, biased rounding, and global interrupt masking*
ADSP-2181	*ADSP-21xx processor with ADSP-2171 features plus 80K bytes of on-chip RAM configured as 16K words of program memory and 16K words of data memory.*

Refer to the individual data sheet of each of these processors for further information.

REV. B

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Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 25 MHz with a 40 ns instruction cycle time. Every instruction can execute in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family's flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP-21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation
- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

TABLE OF CONTENTS

GENERAL DESCRIPTION 1
Development Tools 4
Additional Information 4
ARCHITECTURE OVERVIEW 4
Serial Ports 5
Host Interface Port (ADSP-2111) 6
Interrupts 6
Pin Definitions 7
SYSTEM INTERFACE 7
Clock Signals 7
Reset 8
Program Memory Interface 10
Program Memory Maps 10
Data Memory Interface 12
Data Memory Map 12
Boot Memory Interface 12
Bus Interface 12
Low Power IDLE Instruction 13
ADSP-216x Prototyping 13
Ordering Procedure for ADSP-216x ROM Processors 13
Wafer Products 14
Functional Differences for Older Revision Devices 14
Instruction Set 15
SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163) 17
Recommended Operating Conditions 17
Electrical Characteristics 17
Supply Current & Power (ADSP-2101/2161/2163) 18
Power Dissipation Example 19
Environmental Conditions 19
Capacitive Loading 19
Test Conditions 20
SPECIFICATIONS (ADSP-2111) 21
Recommended Operating Conditions 21
Electrical Characteristics 21
Supply Current & Power 22
Power Dissipation Example 23
Environmental Conditions 23
Capacitive Loading 23
Test Conditions 24
SPECIFICATIONS (ADSP-2103/2162/2164) 25
Recommended Operating Conditions 25
Electrical Characteristics 25
Supply Current & Power 26
Power Dissipation Example 27
Environmental Conditions 27
Capacitive Loading 27
Test Conditions 28
TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163) 29
Clock Signals 30
Interrupts & Flags 31
Bus Request–Bus Grant 32
Memory Read 33
Memory Write 34
Serial Ports 35
Host Interface Port (ADSP-2111) 36
TIMING PARAMETERS (ADSP-2103/2162/2164) 44
Clock Signals 45
Interrupts & Flags 46
Bus Request–Bus Grant 47
Memory Read 48
Memory Write 49
Serial Ports 50
PIN CONFIGURATIONS
68-Pin PGA (ADSP-2101) 51
68-Lead PLCC (ADSP-2101/2103/2105/2115/216x) 52
80-Lead PQFP (ADSP-2101/2103/2115/216x) 53
80-Lead TQFP (ADSP-2115) 53
100-Pin PGA (ADSP-2111) 54
100-Lead PQFP (ADSP-2111) 55
PACKAGE OUTLINE DIMENSIONS
68-Pin PGA 56
68-Lead PLCC 57
80-Lead PQFP, 80-Lead TQFP 58
100-Pin PGA 59
100-Lead PQFP 60
ORDERING GUIDE 61-62

Table I. ADSP-21xx Processor Features

Feature	2101	2103	2105	2115	2111
Data Memory (RAM)	1K	1K	½K	½K	1K
Program Memory (RAM)	2K	2K	1K	1K	2K
Timer	●	●	●	●	●
Serial Port 0 (Multichannel)	●	●	–	●	●
Serial Port 1	●	●	●	●	●
Host Interface Port	–	–	–	–	●
Speed Grades *(Instruction Cycle Time)*					
10.24 MHz *(76.9 ns)*	–	●	–	–	–
13.0 MHz *(76.9 ns)*	–	–	–	–	●
13.824 MHz *(72.3 ns)*	–	–	●	–	–
16.67 MHz *(60 ns)*	●	–	–	●	●
20.0 MHz *(50 ns)*	●	–	●	●	●
25 MHz *(40 ns)*	●	–	–	●	–
Supply Voltage	5 V	3.3 V	5 V	5 V	5 V
Packages					
68-Pin PGA	●	–	–	–	–
68-Lead PLCC	●	●	●	●	–
80-Lead PQFP	●	●	–	●	–
80-Lead TQFP	–	–	–	●	–
100-Pin PGA	–	–	–	–	●
100-Lead PQFP	–	–	–	–	●
Temperature Grades					
K *Commercial* 0°C to +70°C	●	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●	●
T *Extended* –55°C to +125°C	●	–	–	–	●

Table II. ADSP-216x ROM-Programmed Processor Features

Feature	2161	2162	2163	2164
Data Memory (RAM)	½K	½K	½K	½K
Program Memory (ROM)	8K	8K	4K	4K
Program Memory (RAM)	–	–	–	–
Timer	●	●	●	●
Serial Port 0 (Multichannel)	●	●	●	●
Serial Port 1	●	●	●	●
Supply Voltage	5 V	3.3 V	5 V	3.3 V
Speed Grades *(Instruction Cycle Time)*				
10.24 MHz *(97.6 ns)*	–	●	–	●
16.67 MHz *(60 ns)*	●	–	●	–
25 MHz *(40 ns)*	–	–	●	–
Packages				
68-Lead PLCC	●	●	●	●
80-Lead PQFP	●	●	●	●
Temperature Grades				
K *Commercial* 0°C to +70°C	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●

The ADSP-216x series are memory-variant versions of the ADSP-2101 and ADSP-2103 that contain factory-programmed on-chip ROM program memory. These devices offer different amounts of on-chip memory for program and data storage. Table II shows the features available in the ADSP-216x series of custom ROM-coded processors.

The ADSP-216x products eliminate the need for an external boot EPROM in your system, and can also eliminate the need for any external program memory by fitting the entire application program in on-chip ROM. These devices thus provide an excellent option for volume applications where board space and system cost constraints are of critical concern.

Development Tools

The ADSP-21xx processors are supported by a complete set of tools for system development. The ADSP-2100 Family Development Software includes C and assembly language tools that allow programmers to write code for any of the ADSP-21xx processors. The ANSI C compiler generates ADSP-21xx assembly source code, while the runtime C library provides ANSI-standard and custom DSP library routines. The ADSP-21xx assembler produces object code modules which the linker combines into an executable file. The processor simulators provide an interactive instruction-level simulation with a reconfigurable, windowed user interface. A PROM splitter utility generates PROM programmer compatible files.

EZ-ICE® in-circuit emulators allow debugging of ADSP-21xx systems by providing a full range of emulation functions such as modification of memory and register values and execution breakpoints. EZ-LAB® demonstration boards are complete DSP systems that execute EPROM-based programs.

The EZ-Kit Lite is a very low-cost evaluation/development platform that contains both the hardware and software needed to evaluate the ADSP-21xx architecture.

Additional details and ordering information is available in the *ADSP-2100 Family Software & Hardware Development Tools* data sheet (ADDS-21xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

Additional Information

This data sheet provides a general overview of ADSP-21xx processor functionality. For detailed design information on the architecture and instruction set, refer to the *ADSP-2100 Family User's Manual*, available from Analog Devices.

ARCHITECTURE OVERVIEW

Figure 1 shows a block diagram of the ADSP-21xx architecture. The processors contain three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be used as the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21xx executes looped code with zero overhead—no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to (and from) on-chip memory.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA, DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD, DMD) share a single external data bus. The $\overline{\text{BMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{PMS}}$ signals indicate which memory space is using the external buses.

Program memory can store both instructions and data, permitting the ADSP-21xx to fetch two operands in a single cycle, one from program memory and one from data memory. The processor can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of the processor's buses with the use of the bus request/grant signals ($\overline{\text{BR}}$, $\overline{\text{BG}}$).

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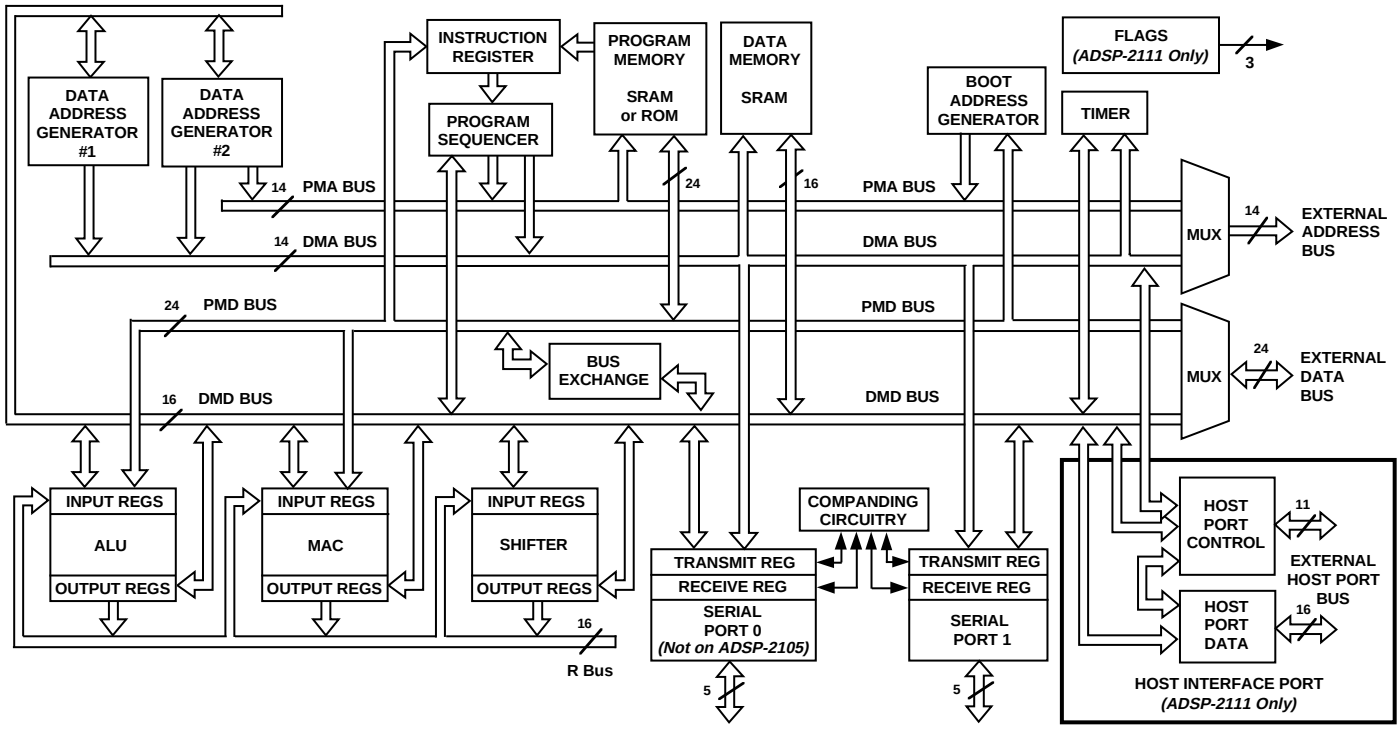


Figure 1. ADSP-21xx Block Diagram

One bus grant execution mode (GO Mode) allows the ADSP-21xx to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

Each ADSP-21xx processor can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer, serial ports, and, on the ADSP-2111, the host interface port. There is also a master $\overline{\text{RESET}}$ signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use a 200 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device. The ADSP-2111 has three additional flag outputs whose states are controlled through software.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-21xx processors include two synchronous serial ports (“SPORTs”) for serial communications and multiprocessor communication. All of the ADSP-21xx processors have two serial ports (SPORT0, SPORT1) except for the ADSP-2105, which has only SPORT1.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

Signal Name	Function
SCLK	Serial Clock (I/O)
RFS	Receive Frame Synchronization (I/O)
TFS	Transmit Frame Synchronization (I/O)
DR	Serial Data Receive
DT	Serial Data Transmit

The ADSP-21xx serial ports offer the following capabilities:

Bidirectional—Each SPORT has a separate, double-buffered transmit and receive function.

Flexible Clocking—Each SPORT can use an external serial clock or generate its own clock internally.

Flexible Framing—The SPORTs have independent framing for the transmit and receive functions; each function can run in a frameless mode or with frame synchronization signals internally generated or externally generated; frame sync signals may be active high or inverted, with either of two pulse widths and timings.

Different Word Lengths—Each SPORT supports serial data word lengths from 3 to 16 bits.

Companding in Hardware—Each SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711.

Flexible Interrupt Scheme—Receive and transmit functions can generate a unique interrupt upon completion of a data word transfer.

Autobuffering with Single-Cycle Overhead—Each SPORT can automatically receive or transmit the contents of an entire circular data buffer with only one overhead cycle per data word; an interrupt is generated after the transfer of the entire buffer is completed.

Multichannel Capability (SPORT0 Only)—SPORT0 provides a multichannel interface to selectively receive or transmit a 24-word or 32-word, time-division multiplexed serial bit stream; this feature is especially useful for T1 or CEPT interfaces, or as a network communication scheme for multiple processors. (Note that the ADSP-2105 includes only SPORT1, not SPORT0, and thus does not offer multichannel operation.)

Alternate Configuration—SPORT1 can be alternatively configured as two external interrupt inputs ($\overline{IRQ0}$, $\overline{IRQ1}$) and the Flag In and Flag Out signals (FI, FO).

Host Interface Port (ADSP-2111)

The ADSP-2111 includes a Host Interface Port (HIP), a parallel I/O port that allows easy connection to a host processor. Through the HIP, the ADSP-2111 can be accessed by the host processor as a memory-mapped peripheral. The host interface port can be thought of as an area of dual-ported memory, or mailbox registers, that allows communication between the computational core of the ADSP-2111 and the host computer. The host interface port is completely asynchronous. The host processor can write data into the HIP while the ADSP-2111 is operating at full speed.

Three pins configure the HIP for operation with different types of host processors. The HSIZE pin configures HIP for 8- or 16-bit communication with the host processor. HMD0 configures the bus strobes, selecting either separate read and write strobes or a single read/write select and a host data strobe. HMD1 selects either separate address (3-bit) and data (16-bit) buses or a multiplexed 16-bit address/data bus with address latch enable. Tying these pins to appropriate values configures the ADSP-2111 for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

The HIP contains six data registers (HDR5-0) and two status registers (HSR7-6) with an associated HMASK register for masking interrupts from individual HIP data registers. The HIP data registers are memory-mapped in the internal data memory of the ADSP-2111. The two status registers provide status information to both the ADSP-2111 and the host processor. HSR7 contains a software reset bit which can be set by both the ADSP-2111 and the host.

HIP transfers can be managed using either interrupts or polling. The HIP generates an interrupt whenever an HDR register receives data from a host processor write. It also generates an interrupt when the host processor has performed a successful read of any HDR. The read/write status of the HDRs is also stored in the HSR registers.

The HMASK register bits can be used to mask the generation of read or write interrupts from individual HDR registers. Bits in the IMASK register enable and disable all HIP read interrupts or all HIP write interrupts. So, for example, a write to HDR4 will cause an interrupt only if both the *HDR4 Write* bit in HMASK and the *HIP Write* interrupt enable bit in IMASK are set.

The HIP provides a second method of booting the ADSP-2111 in which the host processor loads instructions into the HIP. The ADSP-2111 automatically transfers the data, in this case opcodes, to internal program memory. The BMODE pin determines whether the ADSP-2111 boots from the host processor through the HIP or from external EPROM over the data bus.

Interrupts

The ADSP-21xx's interrupt controller lets the processor respond to interrupts with a minimum of overhead. Up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$, are provided. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of Serial Port 1. The ADSP-21xx also supports internal interrupts from the timer, the serial ports, and the host interface port (on the ADSP-2111). The interrupts are internally prioritized and individually maskable (except for $\overline{RESET}$ which is non-maskable). The $\overline{IRQx}$ input pins can be programmed for either level- or edge-sensitivity. The interrupt priorities for each ADSP-21xx processor are shown in Table III.

The ADSP-21xx uses a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt received. Interrupts can be optionally nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length so that simple service routines can be coded entirely in this space. Longer service routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in the IMASK register; the highest-priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on bit 4 in ICNTL, interrupt service routines can either be nested (with higher priority interrupts taking precedence) or be processed sequentially (with only one interrupt service active at a time).

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

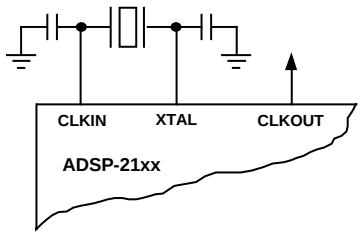


Figure 2. External Crystal Connections

A clock output signal (CLKOUT) is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a complete reset of the ADSP-21xx. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. If the $\overline{\text{RESET}}$ signal is applied during initial power-up, it must be held long enough to allow the processor's internal clock to stabilize. If $\overline{\text{RESET}}$ is activated at any time after power-up and the input clock frequency does not change, the processor's internal clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles will ensure that the PLL has locked (this does not, however, include the crystal oscillator start-up time). During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

To generate the $\overline{\text{RESET}}$ signal, use either an RC circuit with an external Schmidt trigger or a commercially available reset IC. (Do not use only an RC circuit.)

Table IV. ADSP-21xx Pin Definitions

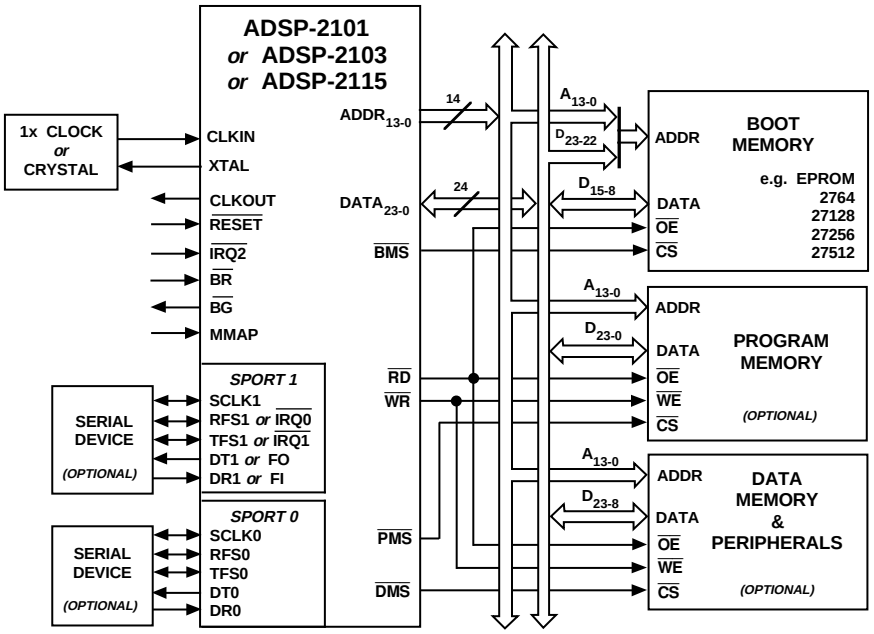
Pin Name(s)	# of Pins	Input / Output	Function
Address	14	O	Address outputs for program, data and boot memory.
Data[1]	24	I/O	Data I/O pins for program and data memories. Input only for boot memory, with two MSBs used for boot memory addresses. Unused data lines may be left floating.
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{IRQ2}}$	1	I	External Interrupt Request #2
$\overline{\text{BR}}$[2]	1	I	External Bus Request Input
$\overline{\text{BG}}$	1	O	External Bus Grant Output
$\overline{\text{PMS}}$	1	O	External Program Memory Select
$\overline{\text{DMS}}$	1	O	External Data Memory Select
$\overline{\text{BMS}}$	1	O	Boot Memory Select
$\overline{\text{RD}}$	1	O	External Memory Read Enable
$\overline{\text{WR}}$	1	O	External Memory Write Enable
MMAP	1	I	Memory Map Select Input
CLKIN, XTAL	2	I	External Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
V_{DD}			Power Supply Pins
GND			Ground Pins
SPORT0[3]	5	I/O	Serial Port 0 Pins *(TFS0, RFS0, DT0, DR0, SCLK0)*
SPORT1	5	I/O	Serial Port 1 Pins *(TFS1, RFS1, DT1, DR1, SCLK1)*
or Interrupts & Flags:			
$\overline{\text{IRQ0}}$ *(RFS1)*	1	I	External Interrupt Request #0
$\overline{\text{IRQ1}}$ *(TFS1)*	1	I	External Interrupt Request #1
FI *(DR1)*	1	I	Flag Input Pin
FO *(DT1)*	1	O	Flag Output Pin
FL2–0 *(ADSP-2111 Only)*	3	O	General Purpose Flag Output Pins
Host Interface Port (ADSP-2111 Only)			
$\overline{\text{HSEL}}$	1	I	HIP Select Input
$\overline{\text{HACK}}$	1	O	HIP Acknowledge Output
HSIZE	1	I	8/16-Bit Host Select *(0 = 16-Bit, 1 = 8-Bit)*
BMODE	1	I	Boot Mode Select *(0 = Standard EPROM Booting, 1 = HIP Booting)*
HMD0	1	I	Bus Strobe Select *(0 =* $\overline{\text{RD}}$/$\overline{\text{WR}}$*, 1 =* RW/$\overline{\text{DS}}$*)*
HMD1	1	I	HIP Address/Data Mode Select *(0 = Separate, 1 = Multiplexed)*
$\overline{\text{HRD}}$/HRW	1	I	HIP Read Strobe *or* Read/Write Select
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP Write Strobe *or* Host Data Strobe Select
HD15–0/HAD15-0	16	I/O	HIP Data *or* HIP Data and Address
HA2/ALE	1	I	Host Address 2 Input *or* Address Latch Enable Input
HA1–0/Unused	2	I	Host Address 1 and 0 Inputs

NOTES

[1]Unused data bus lines may be left floating.

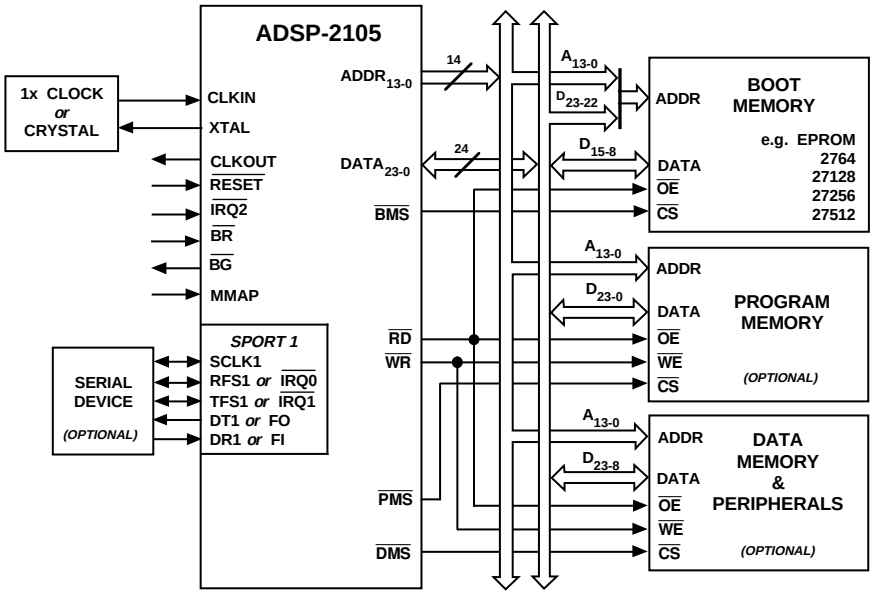
[2]$\overline{\text{BR}}$ must be tied high (to V_{DD}) if not used.

[3]ADSP-2105 does not have SPORT0. (SPORT0 pins are No Connects on the ADSP-2105.)



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2101/ADSP-2103/ADSP-2115 System



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 4. ADSP-2105 System

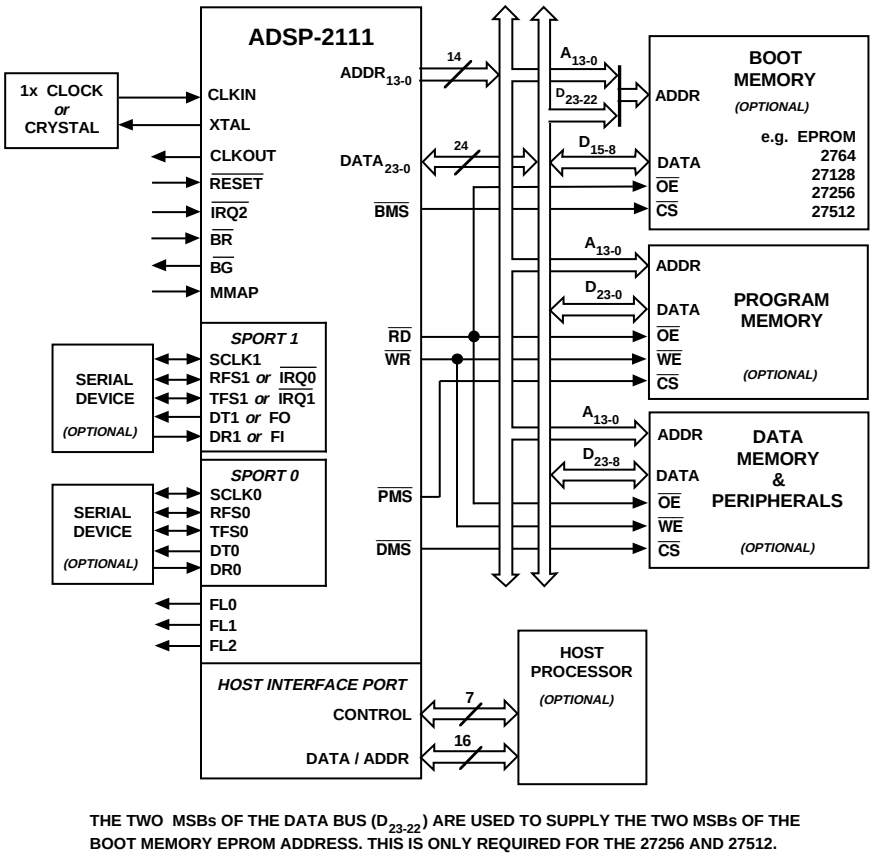


Figure 5. ADSP-2111 System

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with MMAP = 0). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide. For the ADSP-2101, ADSP-2103, and ADSP-2111, these lines can directly address up to 16K words, of which 2K are on-chip. For the ADSP-2105 and ADSP-2115, the address lines can directly address up to 15K words, of which 1K is on-chip.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-21xx processors write data from their 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 6 shows the two program memory maps for the ADSP-2101, ADSP-2103, and ADSP-2111. Figure 8 shows the program memory maps for the ADSP-2105 and ADSP-2115. Figures 7 and 9 show the program memory maps for the ADSP-2161/62 and ADSP-2163/64, respectively.

ADSP-2101/ADSP-2103/ADSP-2111

When MMAP = 0, on-chip program memory RAM occupies 2K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not booted although it can be written to and read under program control.

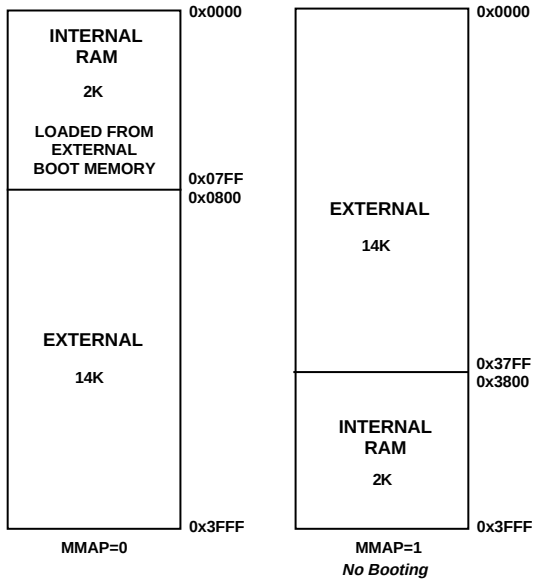


Figure 6. ADSP-2101/ADSP-2103/ADSP-2111 Program Memory Maps

ADSP-2105/ADSP-2115

When MMAP = 0, on-chip program memory RAM occupies 1K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the 1K words between addresses 0x3800–0x3BFF. In this configuration, program memory is not booted although it can be written to and read under program control.

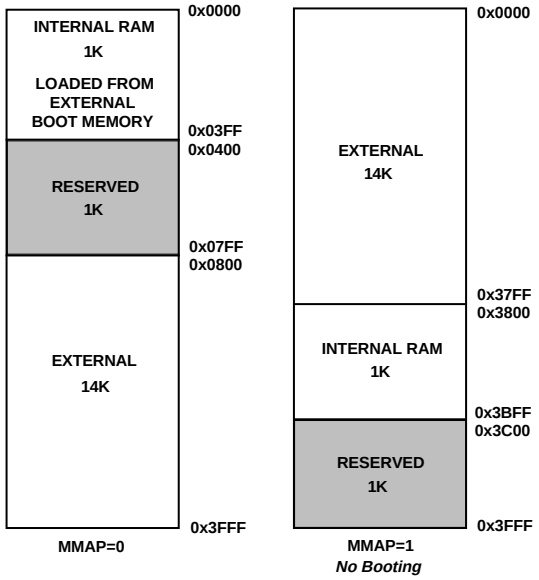


Figure 8. ADSP-2105/ADSP-2115 Program Memory Maps

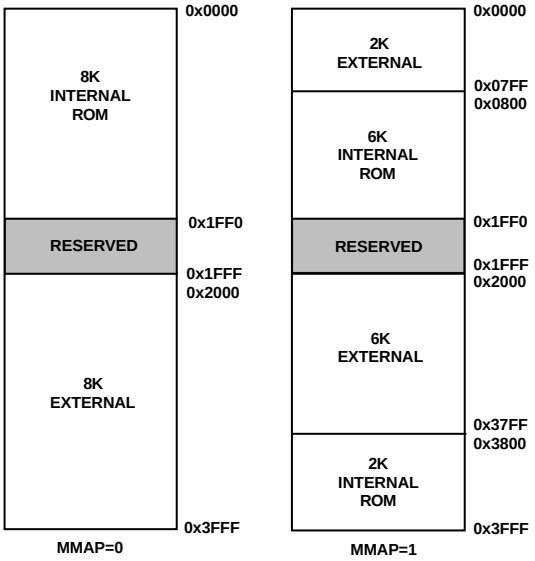


Figure 7. ADSP-2161/62 Program Memory Maps

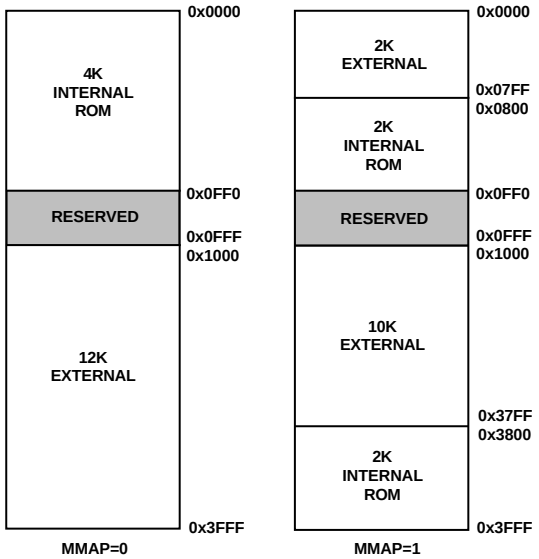


Figure 9. ADSP-2163/64 Program Memory Maps

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

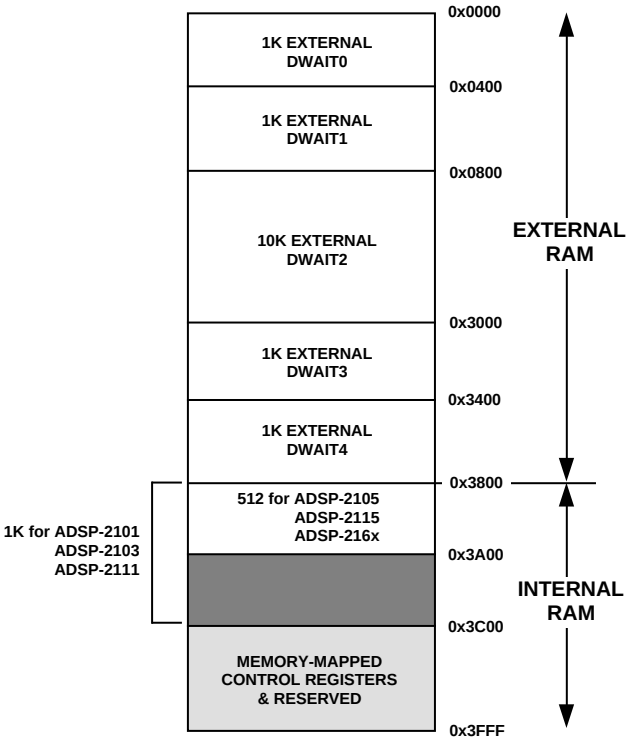


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21xx is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes (up to eight cycles later depending on the number of wait states). The instruction does not need to be completed when the bus is granted; the ADSP-21xx will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active. If this feature is not used, the $\overline{BR}$ input should be tied high (to V_{DD}).

Low Power IDLE Instruction

The IDLE instruction places the ADSP-21xx processor in low power state in which it waits for an interrupt. When an interrupt occurs, it is serviced and execution continues with instruction following IDLE. Typically this next instruction will be a JUMP back to the IDLE instruction. This implements a low-power standby loop.

The *IDLE n* instruction is a special version of IDLE that slows the processor's internal clock signal to further reduce power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor, *n*, given in the IDLE instruction. The syntax of the instruction is:

IDLE n;

where *n* = 16, 32, 64, or 128.

The instruction leaves the chip in an idle state, operating at the slower rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and the timer clock, are reduced by the same ratio. Upon receipt of an enabled interrupt, the processor will stay in the IDLE state for up to a maximum of *n* CLKIN cycles, where *n* is the divisor specified in the instruction, before resuming normal operation.

When the *IDLE n* instruction is used, it slows the processor's internal clock and thus its response time to incoming interrupts– the 1-cycle response time of the standard IDLE state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-21xx will remain in the IDLE state for up to a maximum of *n* CLKIN cycles (where *n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE n* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the IDLE state (a maximum of *n* CLKIN cycles).

ADSP-216x Prototyping

You can prototype your ADSP-216x system with either the ADSP-2101 or ADSP-2103 RAM-based processors. When code is fully developed and debugged, it can be submitted to Analog Devices for conversion into a ADSP-216x ROM product.

The ADSP-2101 EZ-ICE emulator can be used for development of ADSP-216x systems. For the 3.3 V ADSP-2162 and ADSP-2164, a voltage converter interface board provides 3.3 V emulation.

Additional overlay memory is used for emulation of ADSP-2161/62 systems. It should be noted that due to the use of off-chip overlay memory to emulate the ADSP-2161/62, a performance loss may be experienced when both executing instructions and fetching program memory data from the off-chip overlay memory in the same cycle. This can be overcome by locating program memory data in on-chip memory.

Ordering Procedure for ADSP-216x ROM Processors

To place an order for a custom ROM-coded ADSP-2161, ADSP-2162, ADSP-2163, or ADSP-2164 processor, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:

   ADSP-216x ROM Specification Form

   ROM Release Agreement

   ROM NRE Agreement & Minimum Quantity Order (MQO) Acceptance Agreement for Pre-Production ROM Products

2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for the IBM PC (DOS 2.01 or higher).

3. Place a purchase order with Analog Devices for non-recurring engineering changes (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM Memory Map, a hard copy of the .EXE file, and a ROM Data Verification form are returned to you for inspection.

A signed ROM Verification Form and a purchase order for production units are required prior to any product being manufactured. Prototype units may be applied toward the minimum order quantity.

Upon completion of prototype manufacture, Analog Devices will ship prototype units and a delivery schedule update for production units. An invoice against your purchase order for the NRE charges is issued at this time.

There is a charge for each ROM mask generated and a minimum order quantity. Consult your sales representative for details. A separate order must be placed for parts of a specific package type, temperature range, and speed grade.

Functional Differences for Older Revision Devices

Older revisions of the ADSP-21xx processors have slight differences in functionality. The two differences are as follows:

- Bus Grant ($\overline{BG}$) is asserted in the same cycle that Bus Request ($\overline{BR}$) is recognized (i.e. when setup and hold time requirements are met for the $\overline{BR}$ input). Bus Request input is a synchronous input rather than asynchronous. (In newer revision devices, $\overline{BG}$ is asserted in the cycle *after* $\overline{BR}$ is recognized.)
- Only the standard IDLE instruction is available, not the clock-reducing *IDLE n* instruction.

To determine the revision of a particular ADSP-21xx device, inspect the marking on the device. For example, an ADSP-2101 of revision 6.0 will have the following marking:

← *Package & Speed*
← *Lot # & Revision Code*
← *Date Code*

The revision codes for the older versions of each ADSP-21xx device are as follows:

Processor	Old Functionality	New Functionality
ADSP-2101	Revision Code ≤ 5.0	Revision Code ≥ 6.0
ADSP-2105	*No Revision Code*	Revision Code ≥ 1.0
ADSP-2115	Revision Code < 1.0	Revision Code ≥ 1.0
ADSP-2111	RevisionCode < 2.0	Revision Code ≥ 2.0
ADSP-2103	Revision code ≤ 5.0	Revision code ≥ 6.0

Instruction Set

The ADSP-21xx assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics.

Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Multifunction instructions perform one or two data moves and a computation.

The instruction set is summarized below. The *ADSP-2100 Family Users Manual* contains a complete reference to the instruction set.

ALU Instructions

[IF cond]	AR|AF	=	xop + yop [+ C] ;	*Add/Add with Carry*
		=	xop – yop [+ C– 1] ;	*Subtract X – Y/Subtract X – Y with Borrow*
		=	yop – xop [+ C– 1] ;	*Subtract Y – X/Subtract Y – X with Borrow*
		=	xop AND yop ;	*AND*
		=	xop OR yop ;	*OR*
		=	xop XOR yop ;	*XOR*
		=	PASS xop ;	*Pass, Clear*
		=	– xop ;	*Negate*
		=	NOT xop ;	*NOT*
		=	ABS xop ;	*Absolute Value*
		=	yop + 1 ;	*Increment*
		=	yop – 1 ;	*Decrement*
		=	DIVS yop, xop ;	*Divide*
		=	DIVQ xop ;	

MAC Instructions

[IF cond]	MR|MF	=	xop * yop ;	*Multiply*
		=	MR + xop * yop ;	*Multiply/Accumulate*
		=	MR – xop * yop ;	*Multiply/Subtract*
		=	MR ;	*Transfer MR*
		=	0 ;	*Clear*
IF MV	SAT MR ;			*Conditional MR Saturation*

Shifter Instructions

[IF cond]	SR = [SR OR] ASHIFT xop ;	*Arithmetic Shift*
[IF cond]	SR = [SR OR] LSHIFT xop ;	*Logical Shift*
	SR = [SR OR] ASHIFT xop BY <exp>;	*Arithmetic Shift Immediate*
	SR = [SR OR] LSHIFT xop BY <exp>;	*Logical Shift Immediate*
[IF cond]	SE = EXP xop ;	*Derive Exponent*
[IF cond]	SB = EXPADJ xop ;	*Block Exponent Adjust*
[IF cond]	SR = [SR OR] NORM xop ;	*Normalize*

Data Move Instructions

reg = reg ;	*Register-to-Register Move*
reg = <data> ;	*Load Register Immediate*
reg = DM (<addr>) ;	*Data Memory Read (Direct Address)*
dreg = DM (Ix , My) ;	*Data Memory Read (Indirect Address)*
dreg = PM (Ix , My) ;	*Program Memory Read (Indirect Address)*
DM (<addr>) = reg ;	*Data Memory Write (Direct Address)*
DM (Ix , My) = dreg ;	*Data Memory Write (Indirect Address)*
PM (Ix , My) = dreg ;	*Program Memory Write (Indirect Address)*

Multifunction Instructions

<ALU>|<MAC>|<SHIFT> , dreg = dreg ;	*Computation with Register-to-Register Move*
<ALU>|<MAC>|<SHIFT> , dreg = DM (Ix , My) ;	*Computation with Memory Read*
<ALU>|<MAC>|<SHIFT> , dreg = PM (Ix , My) ;	*Computation with Memory Read*
DM (Ix , My) = dreg , <ALU>|<MAC>|<SHIFT> ;	*Computation with Memory Write*
PM (Ix , My) = dreg , <ALU>|<MAC>|<SHIFT> ;	*Computation with Memory Write*
dreg = DM (Ix , My) , dreg = PM (Ix , My) ;	*Data & Program Memory Read*
<ALU>|<MAC> , dreg = DM (Ix , My) , dreg = PM (Ix , My) ;	*ALU/MAC with Data & Program Memory Read*

Program Flow Instructions

DO <addr> [UNTIL term] ;	*Do Until Loop*
[IF cond] JUMP (Ix) ;	*Jump*
[IF cond] JUMP <addr>;	
[IF cond] CALL (Ix) ;	*Call Subroutine*
[IF cond] CALL <addr>;	
IF [NOT] FLAG_IN JUMP <addr>;	*Jump/Call on Flag In Pin*
IF [NOT] FLAG_IN CALL <addr>;	
[IF cond] SET|RESET|TOGGLE FLAG_OUT [, ...] ;	*Modify Flag Out Pin*
[IF cond] RTS ;	*Return from Subroutine*
[IF cond] RTI ;	*Return from Interrupt Service Routine*
IDLE [(n)] ;	*Idle*

Miscellaneous Instructions

NOP ;	*No Operation*
MODIFY (Ix , My);	*Modify Address Register*
[PUSH STS] [, POP CNTR] [, POP PC] [, POP LOOP] ;	*Stack Control*
ENA|DIS SEC_REG [, ...] ;	*Mode Control*
BIT_REV	
AV_LATCH	
AR_SAT	
M_MODE	
TIMER	
G_MODE	

Notation Conventions

Ix	Index registers for indirect addressing
My	Modify registers for indirect addressing
<data>	Immediate data value
<addr>	Immediate address value
<exp>	Exponent (shift value) in shift immediate instructions (8-bit signed number)
<ALU>	Any ALU instruction (except divide)
<MAC>	Any multiply-accumulate instruction
<SHIFT>	Any shift instruction (except shift immediate)
cond	Condition code for conditional instruction
term	Termination code for DO UNTIL loop
dreg	Data register (of ALU, MAC, or Shifter)
reg	Any register (including dregs)
;	A semicolon terminates the instruction
,	Commas separate multiple operations of a single instruction
[ ]	Optional part of instruction
[, ...]	Optional, multiple operations of an instruction
option1 | *option2*	List of options; choose one.

Assembly Code Example

The following example is a code fragment that performs the filter tap update for an adaptive filter based on a least-mean-squared algorithm. Notice that the computations in the instructions are written like algebraic equations.

```
        MF=MX0*MY1(RND), MX0=DM(I2,M1);       {MF=error*beta}
        MR=MX0*MF(RND), AY0=PM(I6,M5);
        DO adapt UNTIL CE;
           AR=MR1+AY0, MX0=DM(I2,M1), AY0=PM(I6,M7);
adapt:     PM(I6,M6)=AR, MR=MX0*MF(RND);

        MODIFY(I2,M3);                        {Point to oldest data}
        MODIFY(I6,M7);                        {Point to start of data}
```

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	–55	+125	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[8]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	µA
C_I	Input Pin Capacitance[1, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 8, 9, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0 (not on ADSP-2105).
[3]Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0 (not on ADSP-2105), SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[5]Input-only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[7]Although specified for TTL outputs, all ADSP-21xx outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[8]Guaranteed but not tested.
[9]Applies to PGA, PLCC, PQFP package types.
[10]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . –55ºC to +125ºC
Storage Temperature Range . . . . . –65ºC to +150ºC
Lead Temperature (10 sec) PGA . . . . . +300ºC
Lead Temperature (5 sec) PLCC, PQFP, TQFP . . . . +280ºC

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

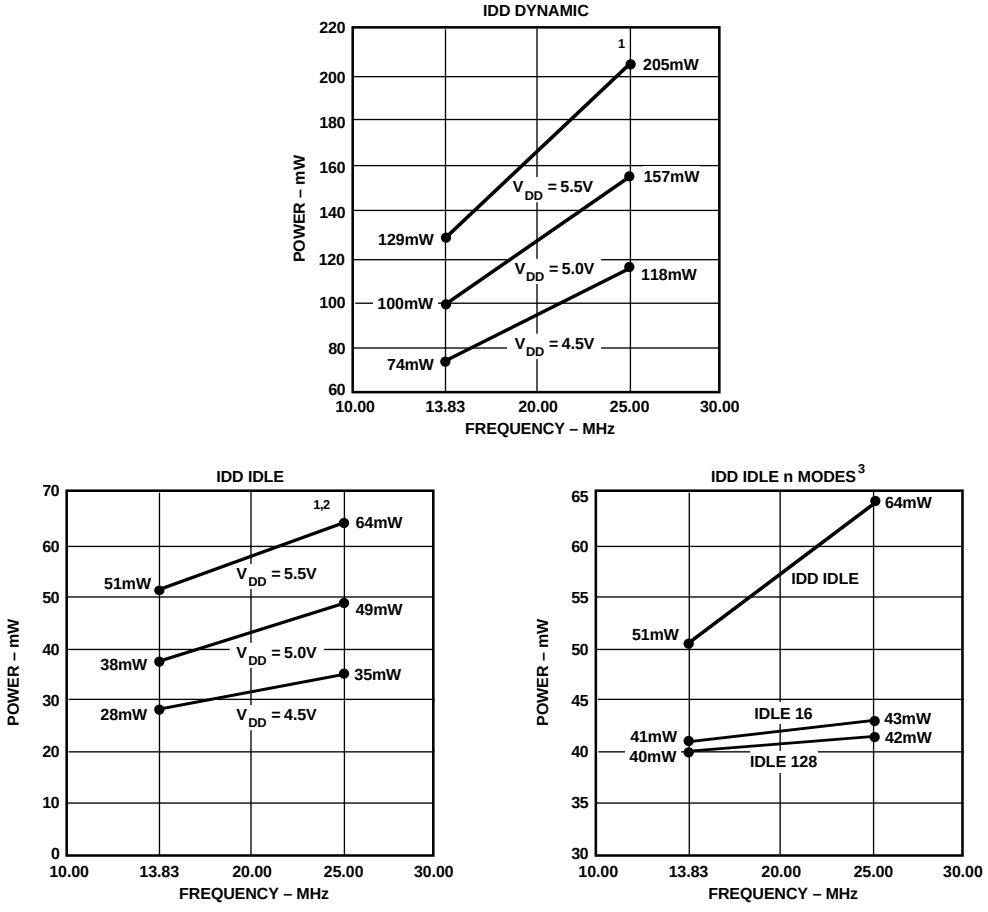
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21xx processors feature proprietary ESD protection circuitry to dissipate high energy electrostatic discharges (Human Body Model), permanent damage may occur to devices subjected to such discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before the devices are removed. Per method 3015 of MIL-STD-883, the ADSP-21xx processors have been classified as Class 1 devices.

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2101/2105/2115/2161/2163)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 40 ns[2]		38	mA
		@ V_{DD} = max, t_{CK} = 50 ns[2]		31	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns[2]		24	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 40 ns[4]		12	mA
		@ V_{DD} = max, t_{CK} = 50 ns		11	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns		10	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[4]ADSP-2105 is not available in a 25 MHz speed grade.
For typical supply current (internal power dissipation) figures, see Figure 11.



VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3 MAXIMUM POWER DISSIPATION AT V_{DD} = 5.5V DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 11. ADSP-2101 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an ADSP-2101 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 11).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	18°C/W	9°C/W	9°C/W
PLCC	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W
TQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 12 and 13 show capacitive loading characteristics for the ADSP-2101, ADSP-2105, ADSP-2115, and ADSP-2161/2163.

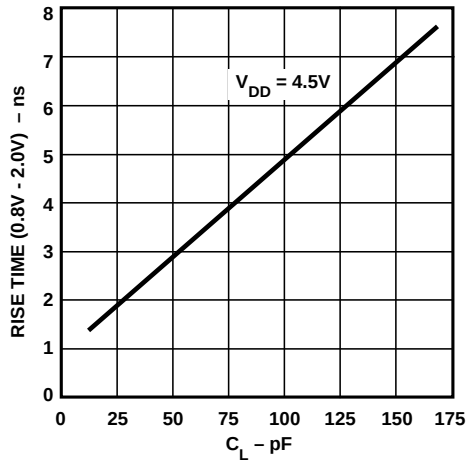


Figure 12. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

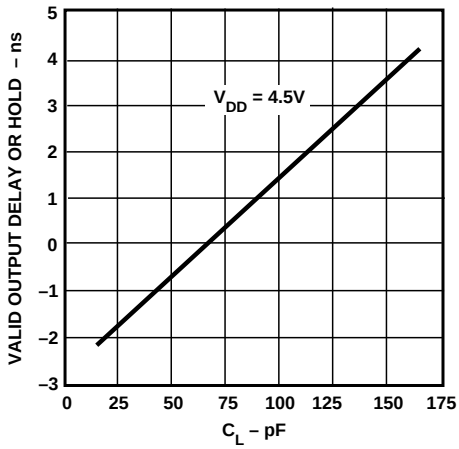


Figure 13. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

TEST CONDITIONS

Figure 14 shows voltage reference levels for ac measurements.

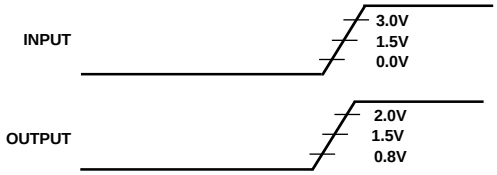


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 15. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

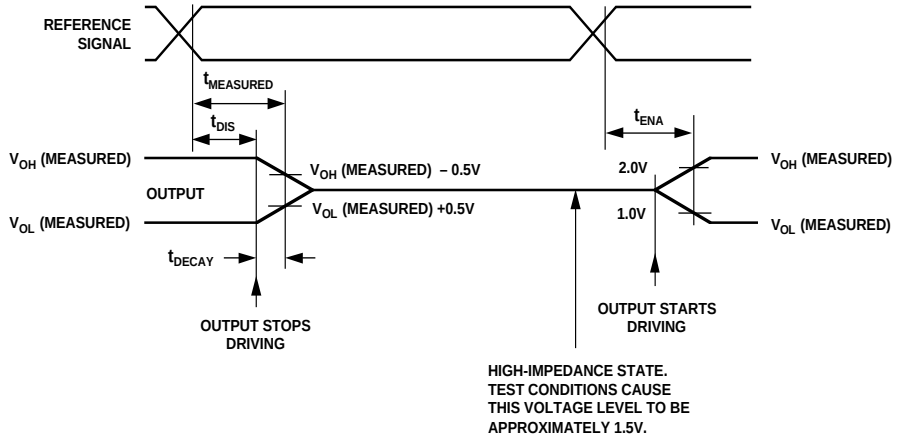


Figure 15. Output Enable/Disable

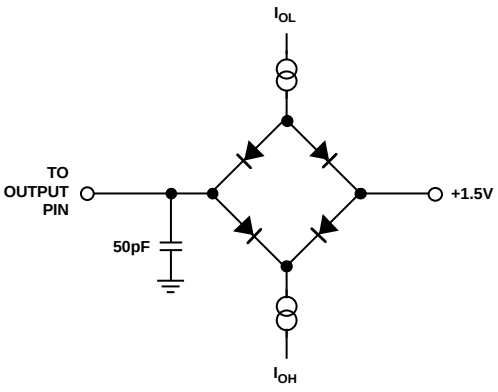


Figure 16. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	–55	+125	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[8]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0V		10	µA
I_{OZH}	Tristate Leakage Curren[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0V[6]		10	µA
C_I	Input Pin Capacitance[1, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 8, 9, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HRW, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1-0.
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0, $\overline{\text{HACK}}$, FL2-0.
[3]Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0, HD0–HD15/HAD0–HAD15.
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0, HD0–HD15/HAD0–HAD15.
[5]Input-only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HRW, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1-0.
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[7]Although specified for TTL outputs, all ADSP-2111 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[8]Guaranteed but not tested.
[9]Applies to ADSP-2111 PGA and PQFP packages.
[10]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (ADSP-2111)

SUPPLY CURRENT & POWER (ADSP-2111)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		60	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		52	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns[2]		46	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 17.

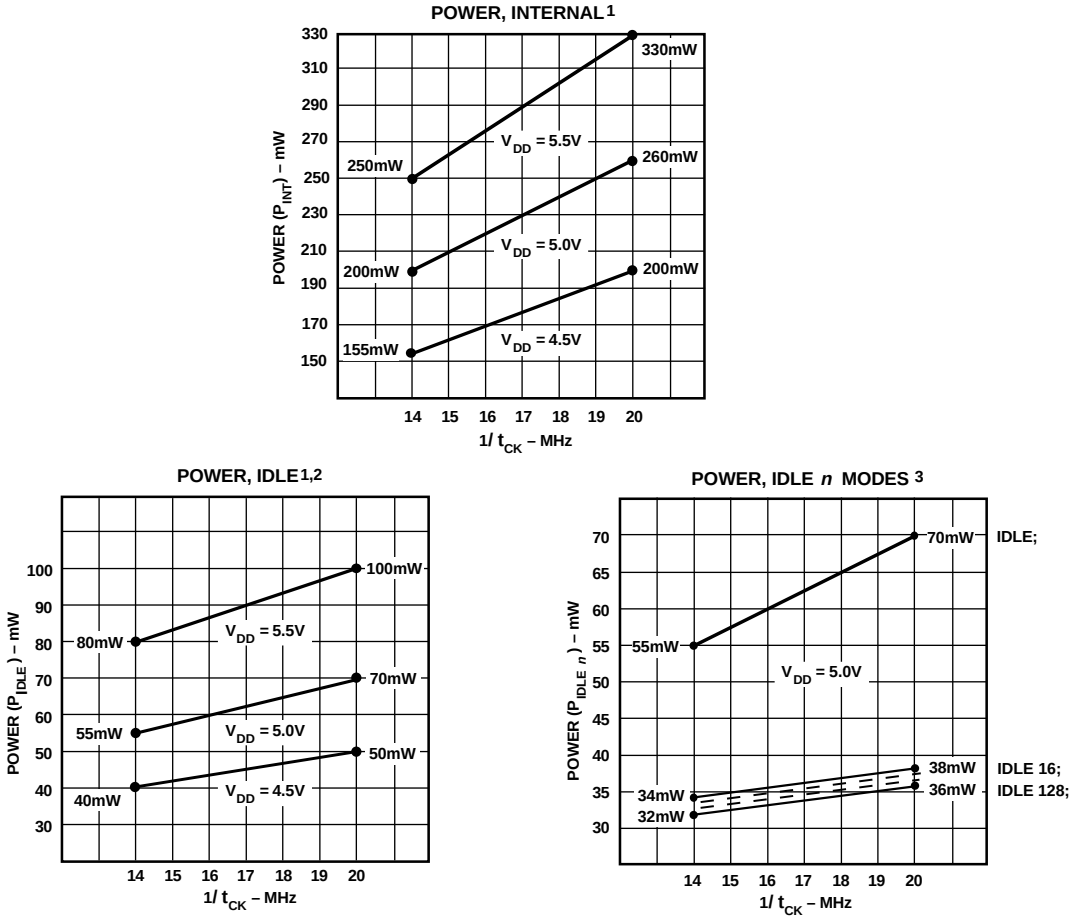


Figure 17. ADSP-2111 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 17).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 18 and 19 show capacitive loading characteristics for the ADSP-2111.

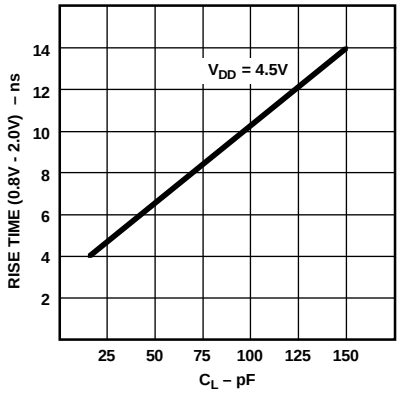


Figure 18. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

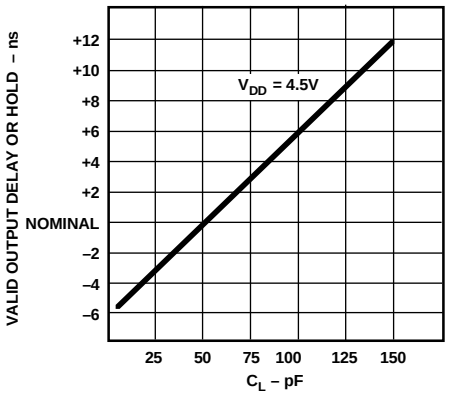


Figure 19. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2111)

TEST CONDITIONS

Figure 20 shows voltage reference levels for ac measurements.

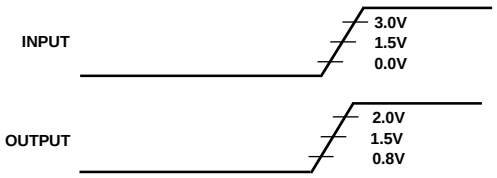


Figure 20. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 21. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 21. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

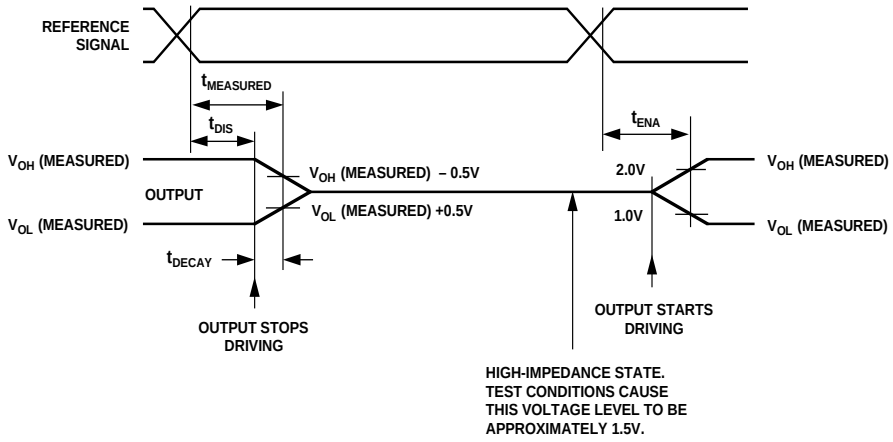


Figure 21. Output Enable/Disable

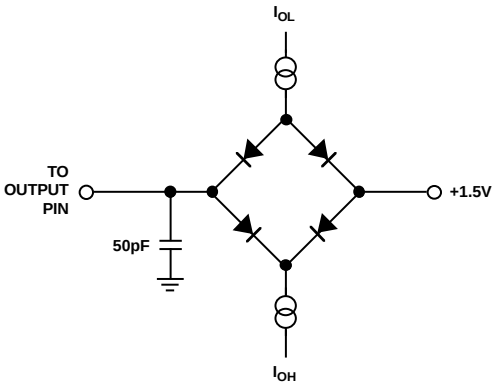


Figure 22. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	3.00	3.60	3.00	3.60	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 3]	@ V_{DD} = max	2.0		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.4	V
V_{OH}	Hi-Level Output Voltage[2, 3, 6]	@ V_{DD} = min, I_{OH} = –0.5 mA[6]	2.4		V
V_{OL}	Lo-Level Output Voltage[2, 3, 6]	@ V_{DD} = min, I_{OL} = 2 mA[6]		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[5]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[5]		10	µA
C_I	Input Pin Capacitance[1, 7, 8]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 7, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0.
[2] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0.
[3] Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0.
[4] Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0.
[5] 0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[6] All ADSP-2103, ADSP-2162, and ADSP-2164 outputs are CMOS and will drive to V_{DD} and GND with no dc loads.
[7] Guaranteed but not tested.
[8] Applies to PLCC and PQFP package types.
[9]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.5 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) PLCC, PQFP . . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

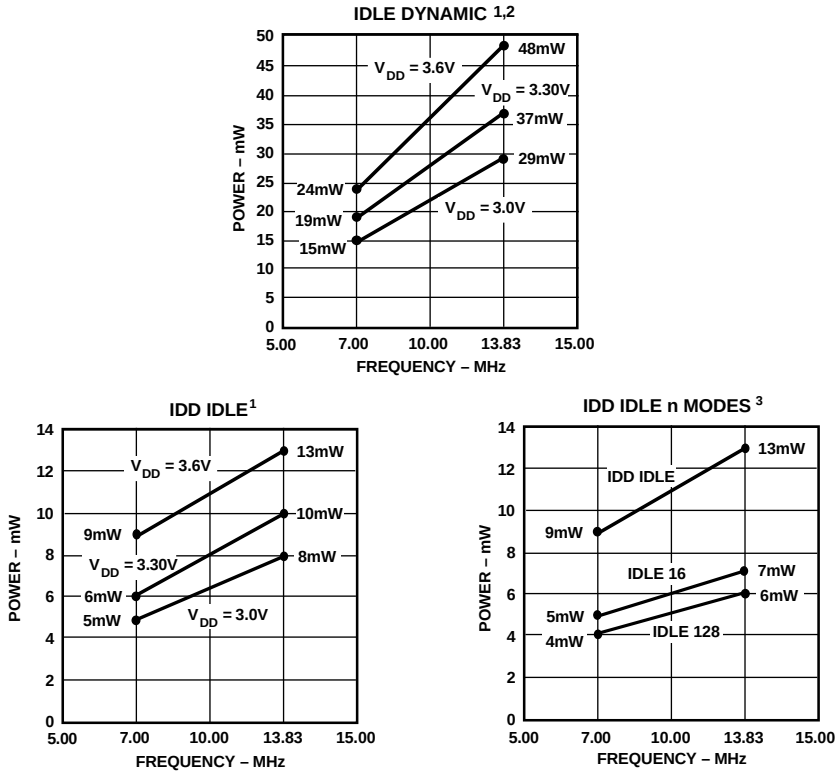
SPECIFICATIONS (ADSP-2103/2162/2164)

SUPPLY CURRENT & POWER (ADSP-2103/2162/2164)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 72.3 ns[2]		14	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 72.3 ns		4	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 23.



VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
3 MAXIMUM POWER DISSIPATION AT V_{DD} = 3.6V DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 23. ADSP-2103 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2103/2162/2164)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2103 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 100 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation (from Figure 23).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 10 MHz	= 8.71 mW
Data, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 5 MHz	= 4.90 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 5 MHz	= 0.55 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 10 MHz	= 1.09 mW
					15.25 mW

Total power dissipation for this example = P_{INT} + 15.25 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 24 and 25 show capacitive loading characteristics for the ADSP-2103, ADSP-2162, and ADSP-2164.

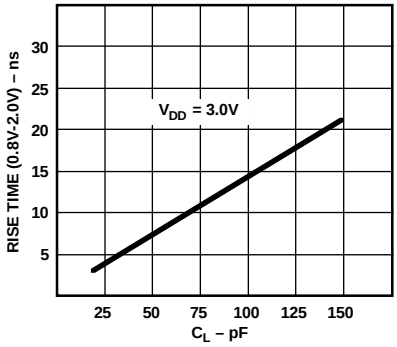


Figure 24. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

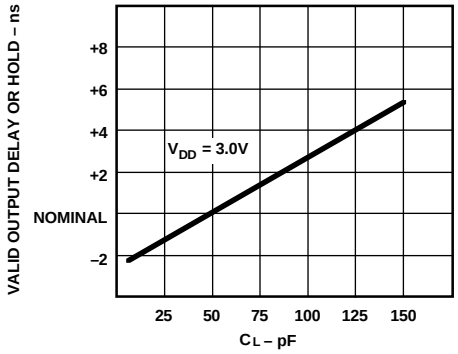


Figure 25. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Figure 26 shows voltage reference levels for ac measurements.

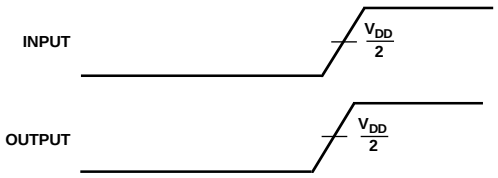


Figure 26. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 27. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 27. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

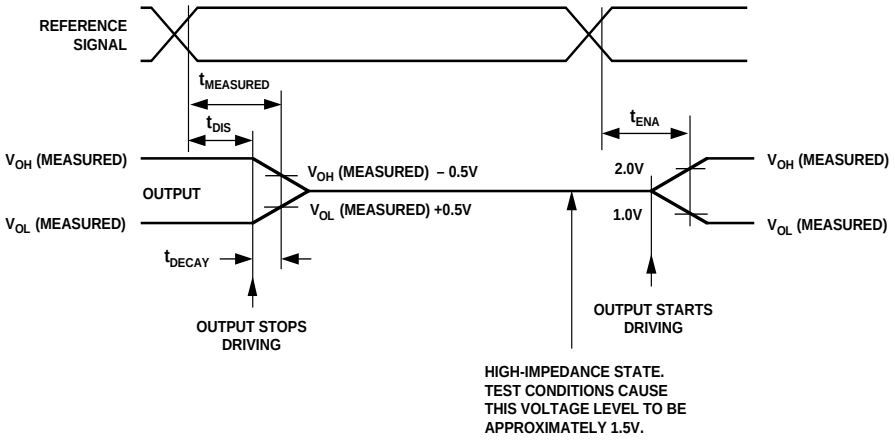


Figure 27. Output Enable/Disable

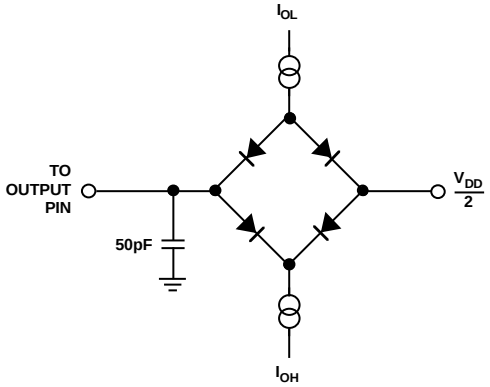


Figure 28. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Device Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

CLOCK SIGNALS & RESET

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{CK}	CLKIN Period	76.9	150	72.3	150	60	150	50	150	40	150			ns
t_{CKL}	CLKIN Width Low	20		20		20		20		15		20		ns
t_{CKH}	CLKIN Width High	20		20		20		20		15		20		ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	384.5		361.5		300		250		200		$5t_{CK}$[1]		ns
Switching Characteristic:														
t_{CPL}	CLKOUT Width Low	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	28.5		26.2		20		15		10		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	0	20	0	20	0	15			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

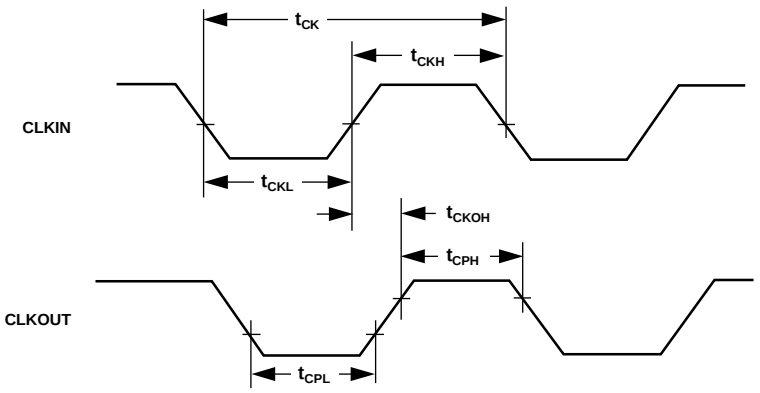


Figure 29. Clock Signals

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

INTERRUPTS & FLAGS

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:														
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	34.2		33.1		30		27.5		25		$0.25t_{CK}$ + 15[4]		ns
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low *(ADSP-2111)*[2, 3]	37.2		36.1		33		30.5		28		$0.25t_{CK}$ + 18[4]		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	19.2		18.1		15		12.5		10		$0.25t_{CK}$		ns
Switching Characteristic:														
t_{FOH}	FO Hold after CLKOUT High[5]	0		0		0		0		0		0		ns
t_{FOD}	FO Delay from CLKOUT High		15		15		15		15		12			ns

NOTES

[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.

[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)

[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

[4]t_{IFS} (min) = $0.25t_{CK}$ + 20 ns for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[5]t_{FOH} (min) = –5 ns for ADSP-2111TG-52 and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

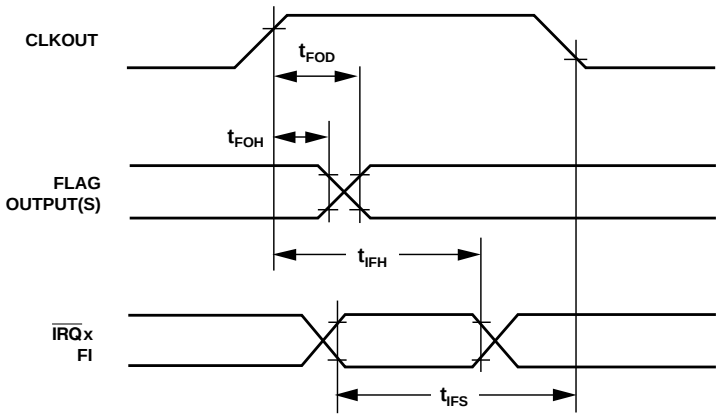


Figure 30. Interrupts & Flags

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

BUS REQUEST/GRANT

Parameter	13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:													
t_{BH} $\overline{BR}$ Hold after CLKOUT High[1]	24.2		23.1		20		17.5		15		$0.25t_{CK}$ + 5		ns
t_{BS} $\overline{BR}$ Setup before CLKOUT Low[1]	39.2		38.1		35		32.5		30		$0.25t_{CK}$ + 20		ns
Switching Characteristic:													
t_{SD} CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		39.2		38.1		35		32.5		30		$0.25t_{CK}$ + 20	ns
t_{SDB} $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		0		0		0		0		0		ns
t_{SE} $\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		0		0		0		0		0		ns
t_{SEC} $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	9.2		8.1		5		2.5		1.5[2]		$0.25t_{CK} - 10$[2]		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

[2]For 25 MHz only the minimum frequency dependency formula for $t_{SEC} = (0.25t_{CK} - 8.5)$.

Section 10.2.4, "Bus Request/Grant," on page 212 of the *ADSP-2100 Family User's Manual (1st Edition, 1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

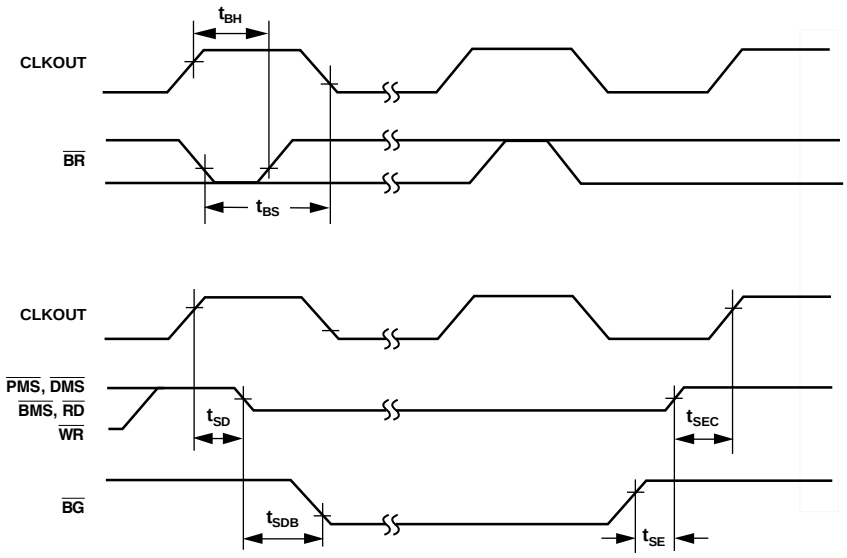


Figure 31. Bus Request/Grant

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY READ

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Unit
Timing Requirement:												
t_{RDD}	$\overline{RD}$ Low to Data Valid		23.5		23.2		17		12		7	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		37.7		36.2		27		19.5		12	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		0		0		0		0		ns
Switching Characteristic:												
t_{RP}	$\overline{RD}$ Pulse Width	33.5		28.2		22		17		12		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	14.2	29.2	13.1	28.1	10	25	7.5	22.5	5	20	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	9.2		8.1		5		2.5		1.5[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	10.2		9.1		6		3.5		1		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	33.5		31.2		25		20		15		ns

Parameter		Frequency Dependency (CLKIN ≤ 25 MHz) Min	Max	Unit
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 13 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 18 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 8 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 10$[1]		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 9$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

NOTES
[1]For 25 MHz only minimum frequency dependency formula for $t_{ASR} = (0.25t_{CK} - 8.5)$.
w = wait states × t_{CK}.

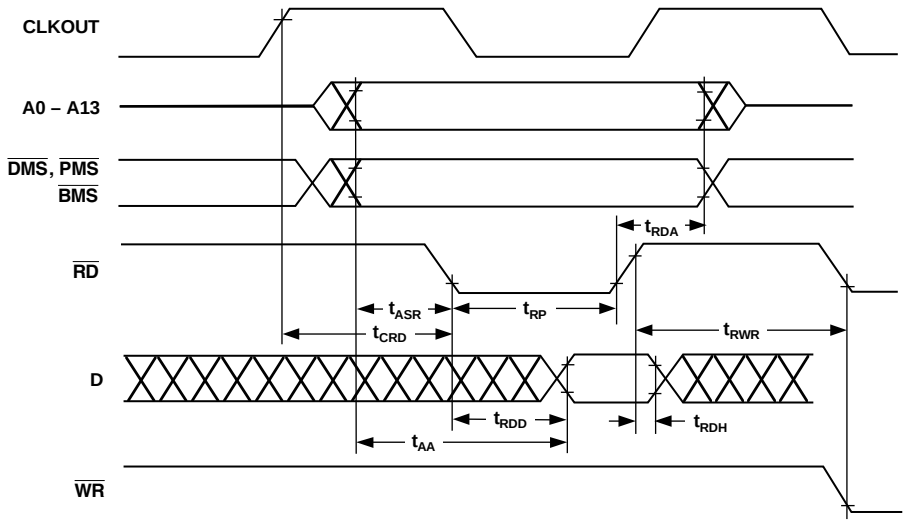


Figure 32. Memory Read

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY WRITE

Parameter		13 MHz Min	13 MHz Max	13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	Unit
Switching Characteristic:												
t_{DW}	Data Setup before $\overline{WR}$ High	25.5		23.2		17		12		7		ns
t_{DH}	Data Hold after $\overline{WR}$ High	9.2		8.1		5		2.5		0		ns
t_{WP}	$\overline{WR}$ Pulse Width	30.5		28.2		22		17		12		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		0		0		0		0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	9.2		8.1		5		2.5		1.5[1]		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	9.2		8.1		5		2.5		1.5[1]		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	14.2	29.2	13.1	28.1	10	25	7.5	22.5	5	20	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	35.7		32.2		23		15.5		8		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	10.2		9.1		6		3.5		1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	33.5		31.2		25		20		15		ns

Parameter		Frequency Dependency (CLKIN ≤ 25 MHz) Min	Frequency Dependency (CLKIN ≤ 25 MHz) Max	Unit
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 13 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 8 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 10$[1]		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$[1]		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 22 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 9$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

NOTES

[1]For 25 MHz only the minimum frequency dependency formula for t_{ASW} and t_{DDR} = $(0.25t_{CK} - 8.5)$.

w = wait states × t_{CK}.

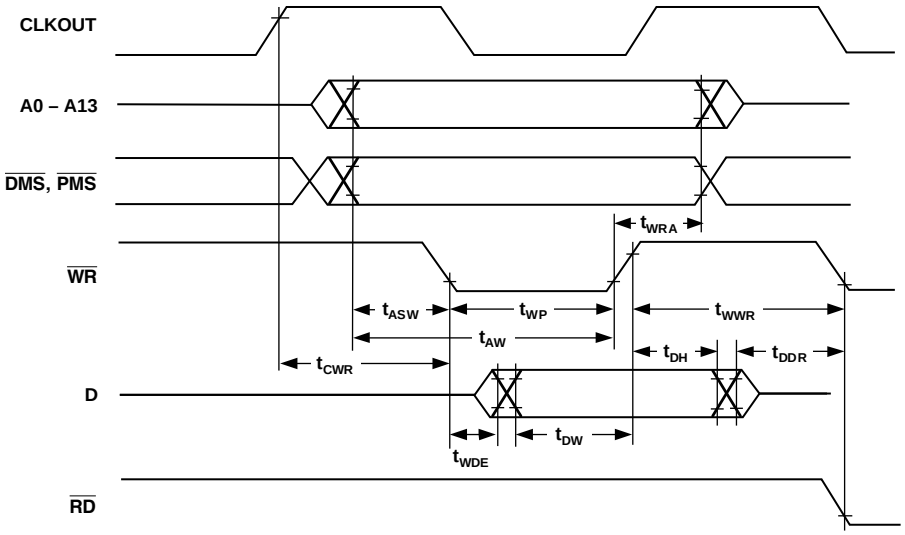


Figure 33. Memory Write

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

SERIAL PORTS

Parameter		12.5 MHz Min	12.5 MHz Max	13.0 MHz Min	13.0 MHz Max	13.824 MHz* Min	13.824 MHz* Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{SCK}	SCLK Period	80		76.9		72.3				ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		8		8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		10				ns
t_{SCP}	$SCLK_{IN}$ Width	30		28		28				ns
Switching Characteristic:										
t_{CC}	CLKOUT High to $SCLK_{OUT}$	20	35	19.2	34.2	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK}$ + 15ns	
t_{SCDE}	SCLK High to DT Enable	0		0		0				ns
t_{SCDV}	SCLK High to DT Valid		20		20		20			ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		0		0				ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20		20		20			ns
t_{SCDH}	DT Hold after SCLK High	0		0		0				ns
t_{TDE}	TFS (Alt) to DT Enable	0		0		0				ns
t_{TDV}	TFS (Alt) to DT Valid		18		18		18			ns
t_{SCDD}	SCLK High to DT Disable		25		25		25			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20		20		20			ns

*Maximum serial port operating frequency is 13.824 MHz for all processor speed grades except the 12.5 MHz ADSP-2101 and 13.0 MHz ADSP-2111.

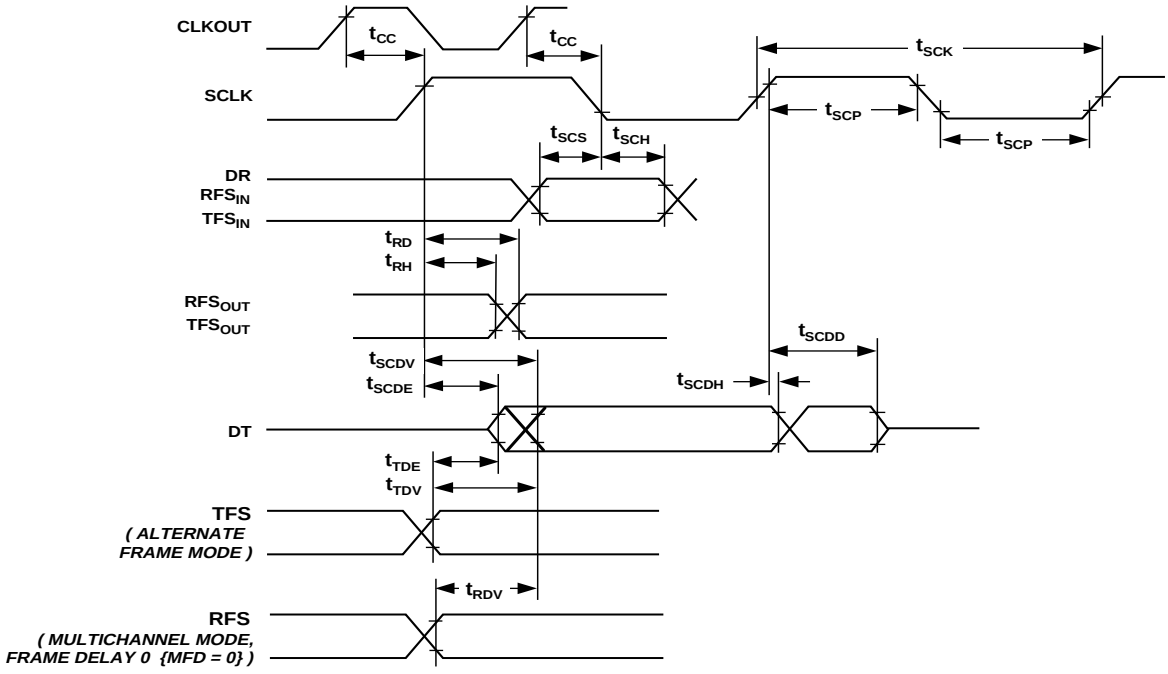


Figure 34. Serial Ports

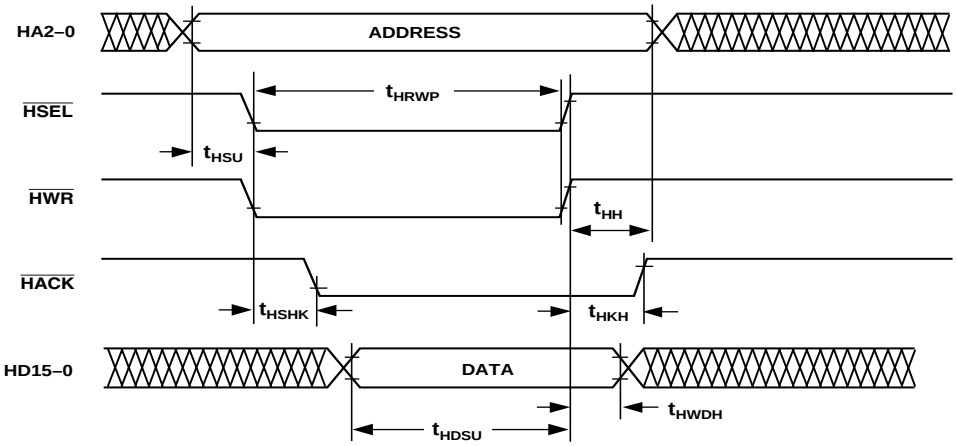
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0 Setup before Start of Write or Read[1, 2]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[3]	3		3		3			ns
t_{HH} HA2-0 Hold after End of Write or Read[3, 4]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]Start of Read = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low.
[3]End of Write = $\overline{\text{HWR}}$ High or $\overline{\text{HSEL}}$ High.
[4]End of Read = $\overline{\text{HRD}}$ High or $\overline{\text{HSEL}}$ High.
[5]Read Pulse Width = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low, Write Pulse Width = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

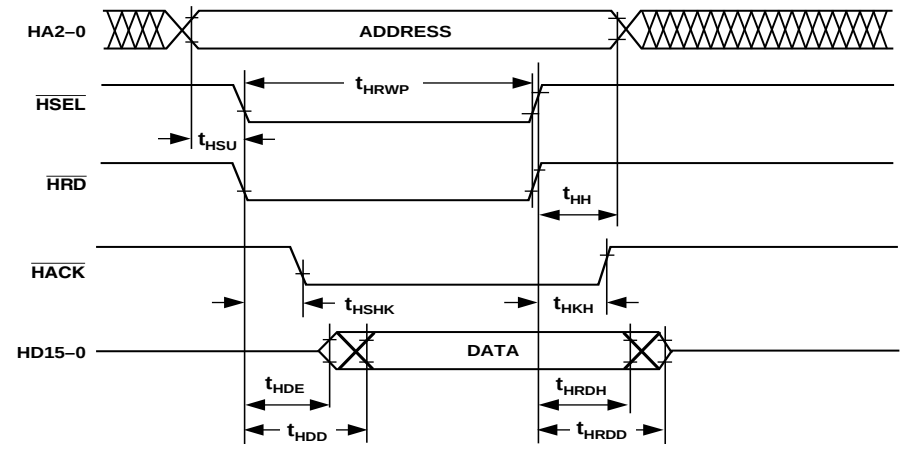


Figure 35. Host Interface Port (HMD1 = 0, HMD0 = 0)

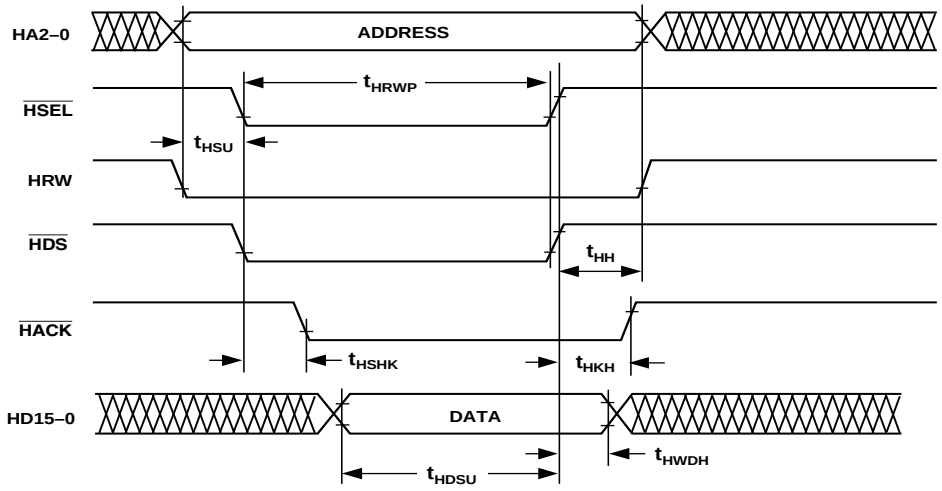
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0, HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[2]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HA2-0, HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

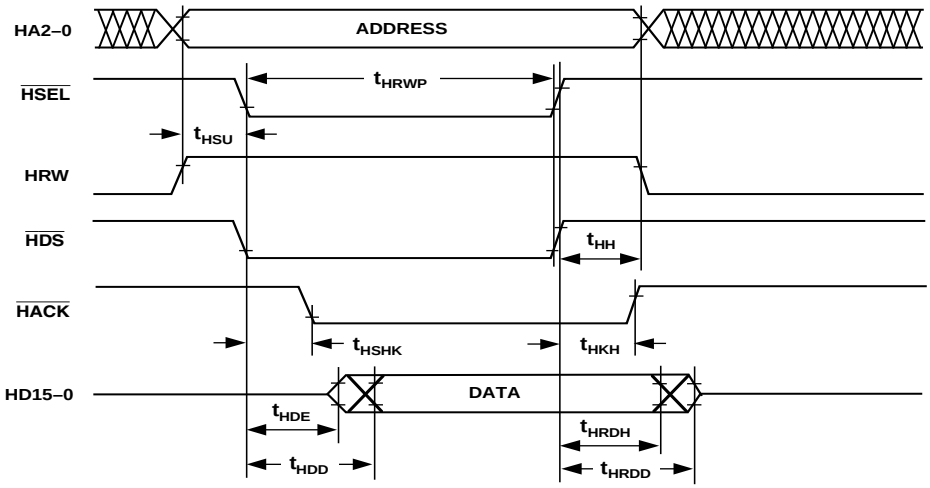


Figure 36. Host Interface Port (HMD1 = 0, HMD0 =1)

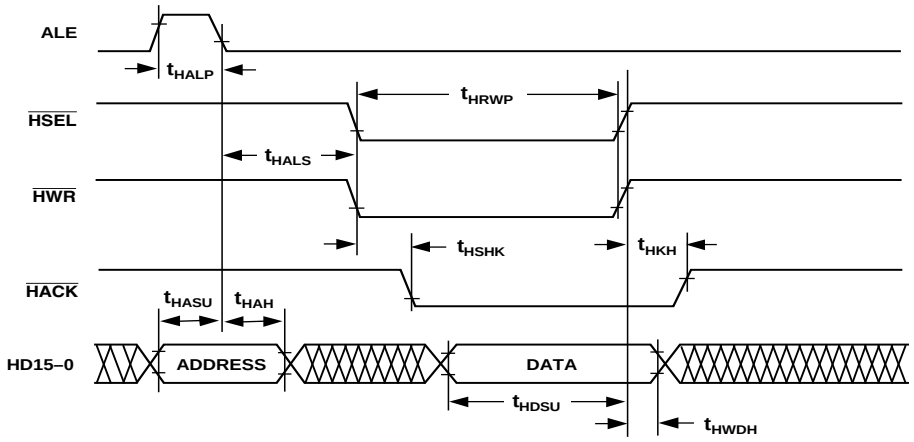
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1, 2]	15		15		15			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[3]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

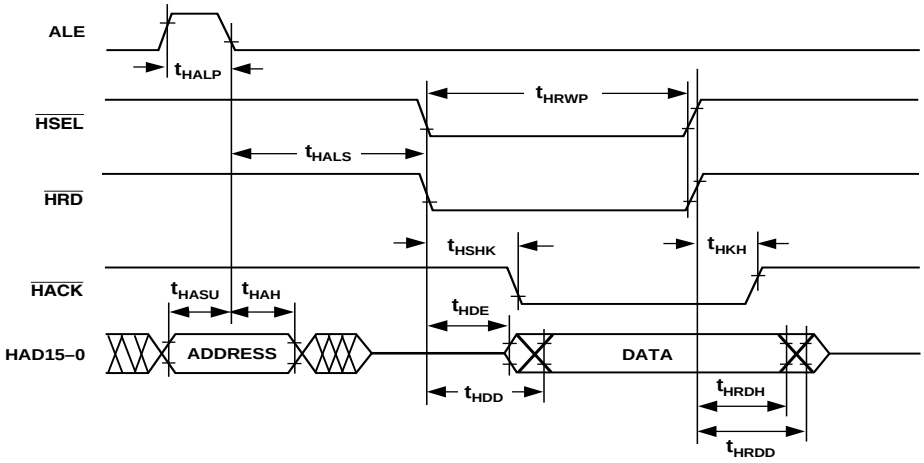


Figure 37. Host Interface Port (HMD1 = 1, HMD0 = 0)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1]	15		15		15			ns
t_{HSU} HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[2]	5		5		5			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle

Host Read Cycle

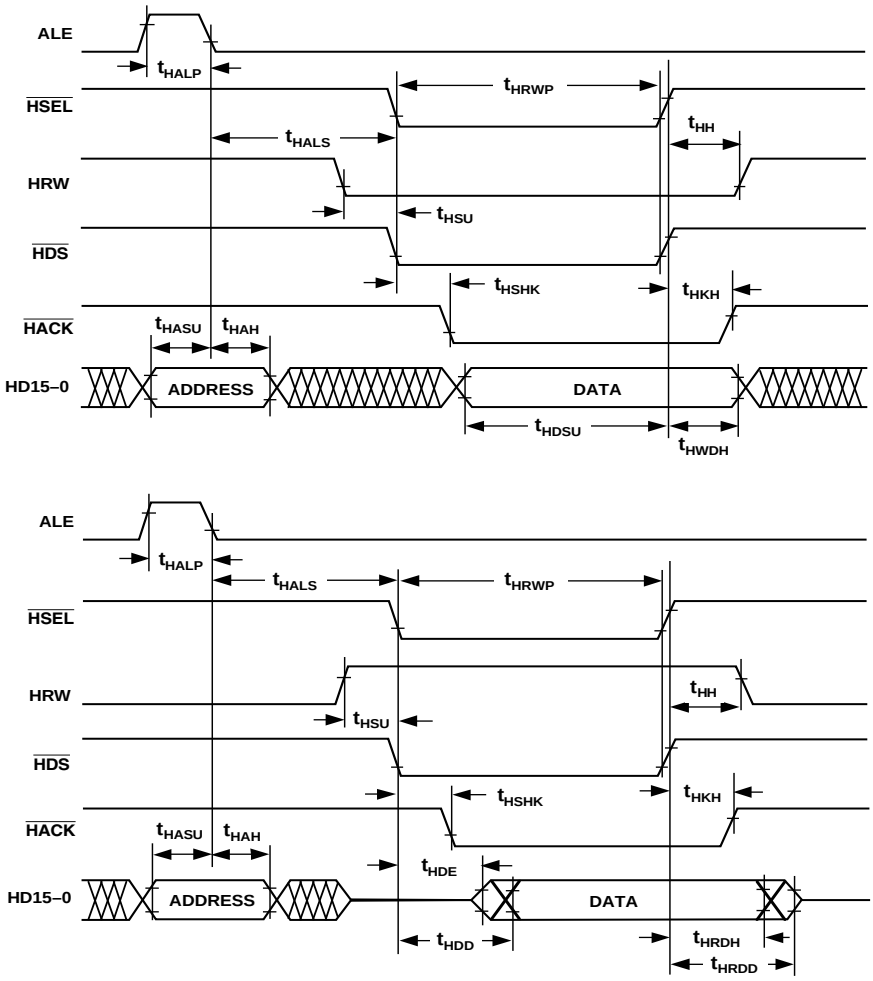


Figure 38. Host Interface Port (HMD1 = 1, HMD0 = 1)

TIMING PARAMETERS (ADSP-2103/2162/2164)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$ Hold after $\overline{\text{WR}}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
$\overline{\text{OE}}$ to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{DMS}}$, $\overline{\text{PMS}}$, $\overline{\text{BMS}}$ to Data Valid

TIMING PARAMETERS (ADSP-2103/2162/2164)

CLOCK SIGNALS & RESET

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{CK}	CLKIN Period	97.6	150			ns
t_{CKL}	CLKIN Width Low	20				ns
t_{CKH}	CLKIN Width High	20				ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	488		$5t_{CK}$[1]		ns
Switching Characteristic:						
t_{CPL}	CLKOUT Width Low	38.8		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	38.8		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator startup time).

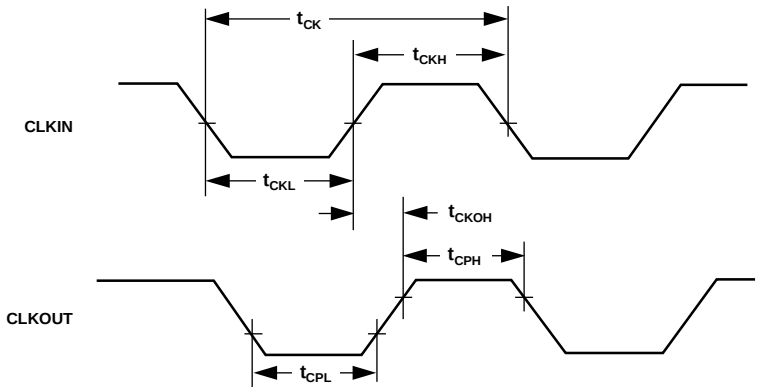


Figure 39. Clock Signals

TIMING PARAMETERS (ADSP-2103/2162/2164)

INTERRUPTS & FLAGS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	44.4		$0.25t_{CK}$ + 20		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	24.4		$0.25t_{CK}$		ns
Switching Characteristic:						
t_{FOH}	FO Hold after CLKOUT High	0				ns
t_{FOD}	FO Delay from CLKOUT High		15			ns

NOTES
[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

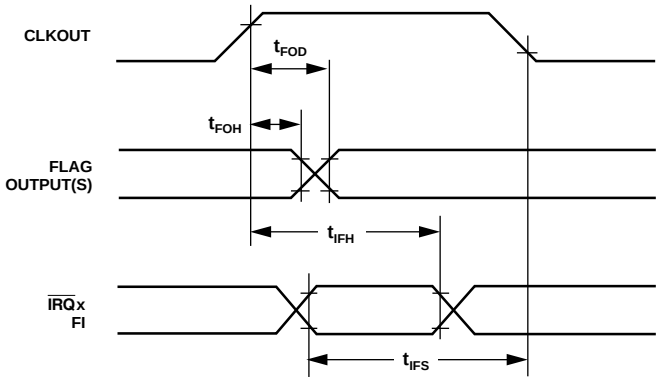


Figure 40. Interrupts & Flags

TIMING PARAMETERS (ADSP-2103/2162/2164)

BUS REQUEST/GRANT

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	29.4		$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	44.4		$0.25t_{CK}$ + 20		ns
Switching Characteristic:						
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		44.4		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0				ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0				ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	14.4		$0.25t_{CK}$ – 10		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

Section 10.2.4, "Bus Request/Grant," of the *ADSP-2100 Family User's Manual (1st Edition, ©1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

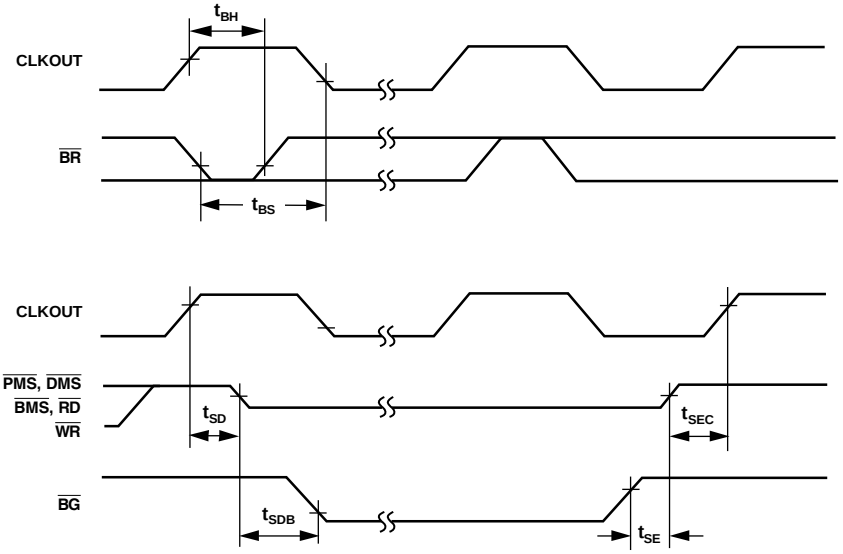


Figure 41. Bus Request/Grant

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY READ

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid		33.8		$0.5t_{CK} - 15 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		49.2		$0.75t_{CK} - 24 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0				ns
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

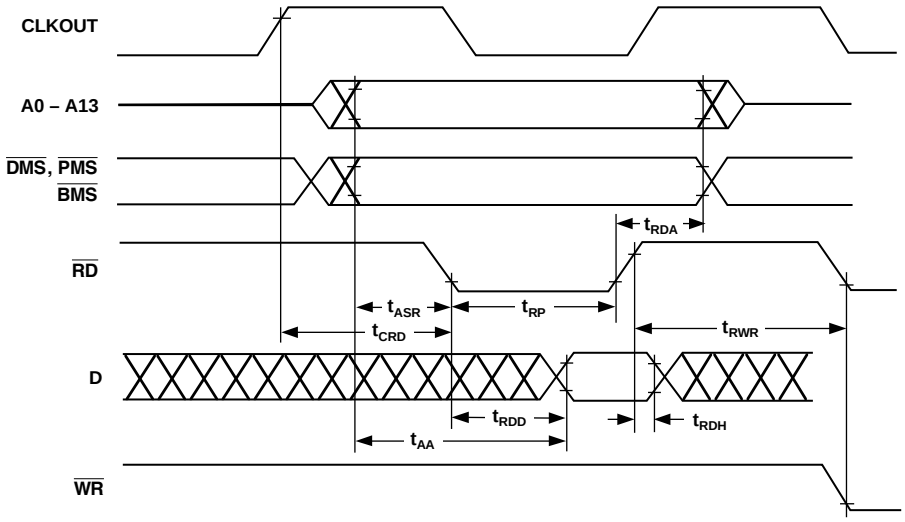


Figure 42. Memory Read

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY WRITE

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	38.8		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	14.4		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0				
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	14.4		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	58.2		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

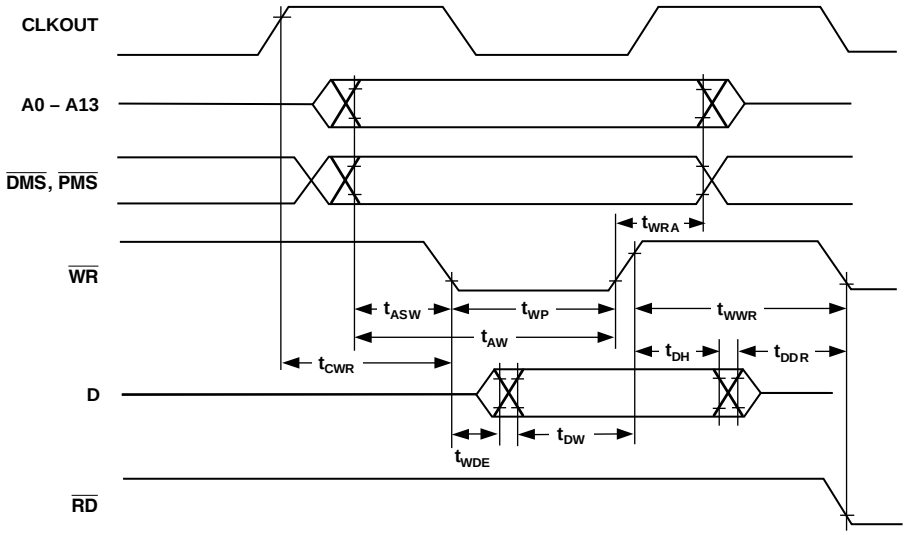


Figure 43. Memory Write

TIMING PARAMETERS (ADSP-2103/2162/2164)

SERIAL PORTS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		t_{CK}		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10				ns
t_{SCP}	$SCLK_{in}$ Width	28				ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	24.4	39.4	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0				ns
t_{SCDV}	SCLK High to DT Valid		28			ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0				ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		28			ns
t_{SCDH}	DT Hold after SCLK High	0				ns
t_{TDE}	TFS (alt) to DT Enable	0				ns
t_{TDV}	TFS (alt) to DT Valid		18			ns
t_{SCDD}	SCLK High to DT Disable		30			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20			ns

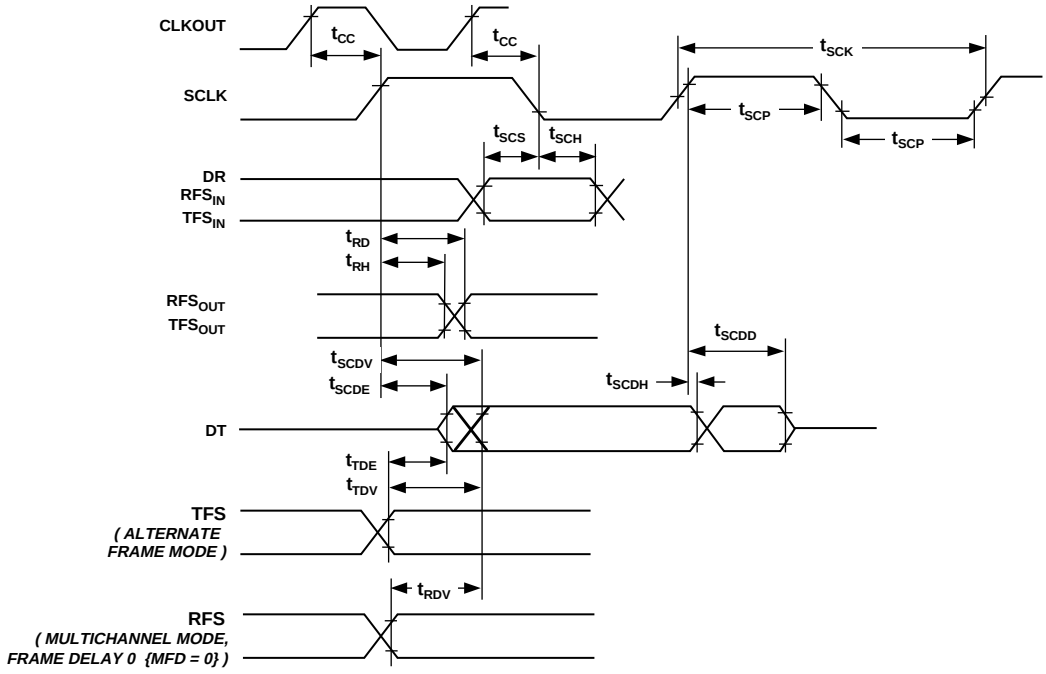
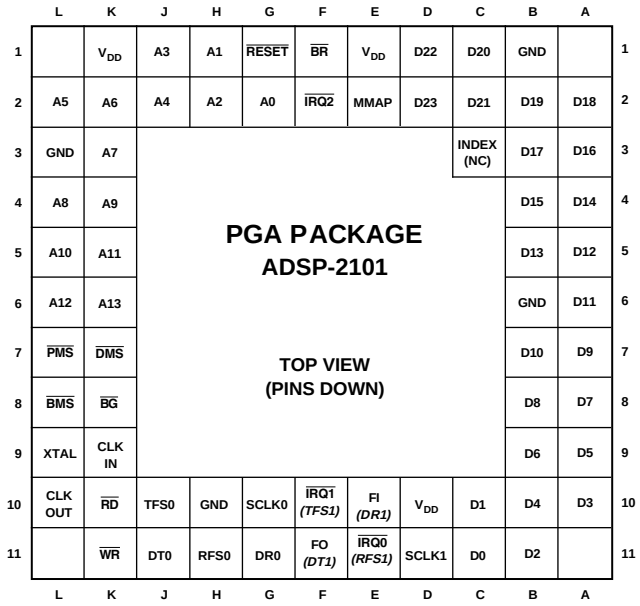
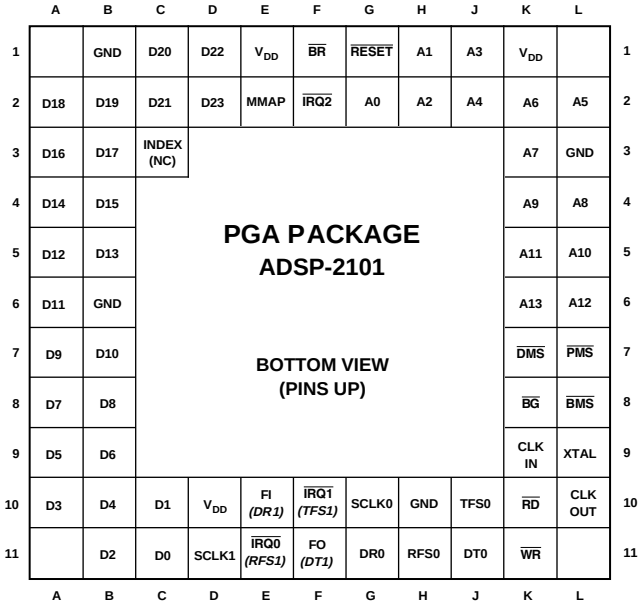


Figure 44. Serial Ports

PIN CONFIGURATIONS

68-Pin PGA





NC = NO CONNECT

PGA Number	Pin Name
K11	$\overline{WR}$
K10	$\overline{RD}$
J11	DT0
J10	TFS0
H11	RFS0
H10	GND
G11	DR0
G10	SCLK0
F11	FO *(DT1)*
F10	$\overline{IRQ1}$ *(TFS1)*
E11	$\overline{IRQ0}$ *(RFS1)*
E10	FI *(DR1)*
D11	SCLK1
D10	V_{DD}
C11	D0
C10	D1
B11	D2

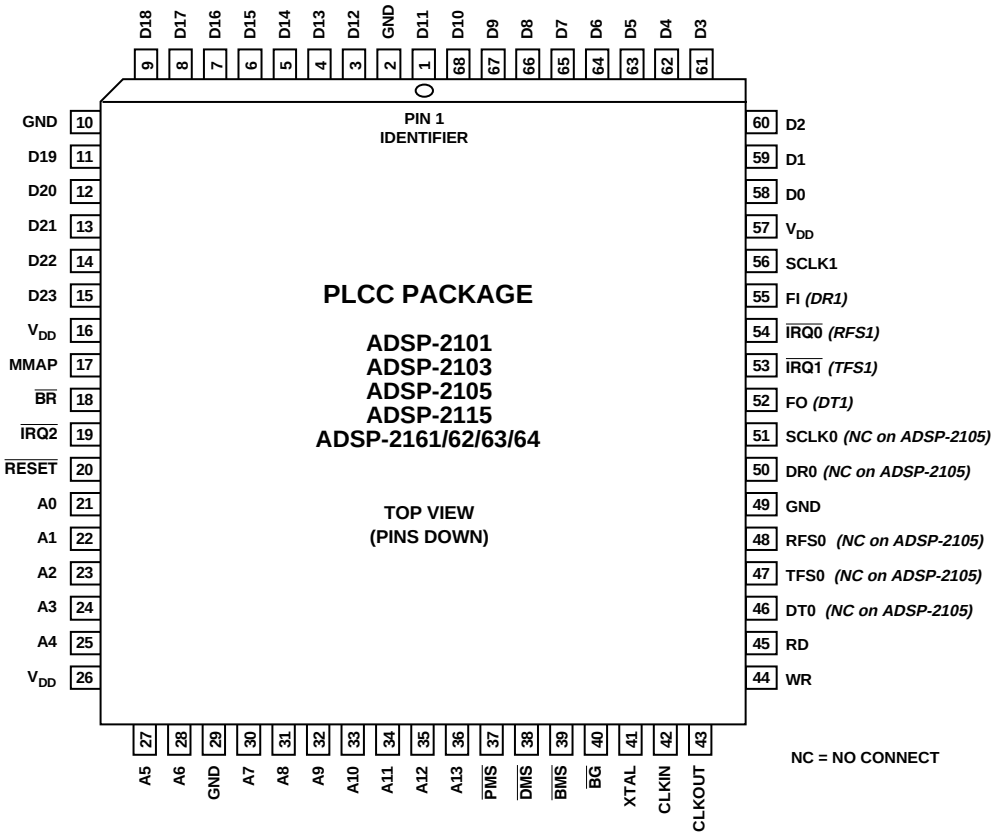
PGA Number	Pin Name
A10	D3
B10	D4
A9	D5
B9	D6
A8	D7
B8	D8
A7	D9
B7	D10
A6	D11
B6	GND
A5	D12
B5	D13
A4	D14
B4	D15
A3	D16
B3	D17
A2	D18

PGA Number	Pin Name
B1	GND
B2	D19
C1	D20
C2	D21
D1	D22
D2	D23
E1	V_{DD}
E2	MMAP
F1	$\overline{BR}$
F2	$\overline{IRQ2}$
G1	$\overline{RESET}$
G2	A0
H1	A1
H2	A2
J1	A3
J2	A4
K1	V_{DD}

PGA Number	Pin Name
L2	A5
K2	A6
L3	GND
K3	A7
L4	A8
K4	A9
L5	A10
K5	A11
L6	A12
K6	A13
L7	$\overline{PMS}$
K7	$\overline{DMS}$
L8	$\overline{BMS}$
K8	$\overline{BG}$
L9	XTAL
K9	CLKIN
L10	CLKOUT
C3	Index (NC)

PIN CONFIGURATIONS

68-Lead PLCC



PLCC Number	Pin Name
1	D11
2	GND
3	D12
4	D13
5	D14
6	D15
7	D16
8	D17
9	D18
10	GND
11	D19
12	D20
13	D21
14	D22
15	D23
16	V_{DD}
17	MMAP

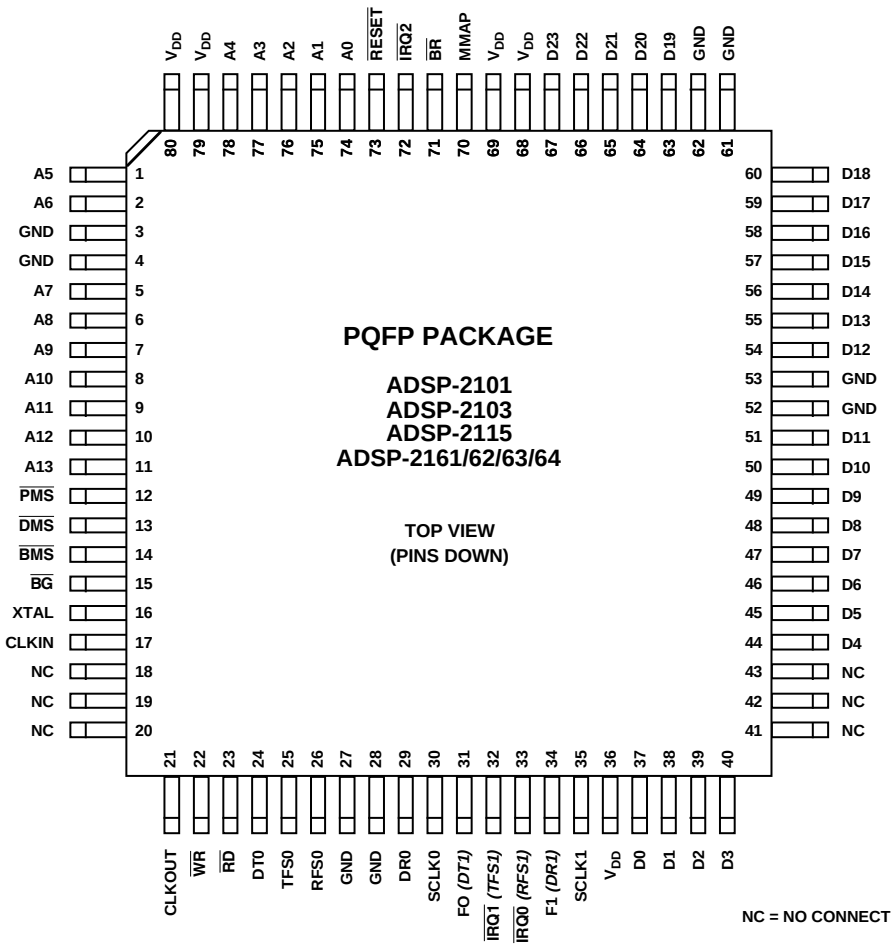
PLCC Number	Pin Name
18	$\overline{BR}$
19	$\overline{IRQ2}$
20	$\overline{RESET}$
21	A0
22	A1
23	A2
24	A3
25	A4
26	V_{DD}
27	A5
28	A6
29	GND
30	A7
31	A8
32	A9
33	A10
34	A11

PLCC Number	Pin Name
35	A12
36	A13
37	$\overline{PMS}$
38	$\overline{DMS}$
39	$\overline{BMS}$
40	$\overline{BG}$
41	XTAL
42	CLKIN
43	CLKOUT
44	$\overline{WR}$
45	$\overline{RD}$
46	DT0 *(NC on ADSP-2105)*
47	TFS0 *(NC on ADSP-2105)*
48	RFS0 *(NC on ADSP-2105)*
49	GND
50	DR0 *(NC on ADSP-2105)*
51	SCLK0 *(NC on ADSP-2105)*

PLCC Number	Pin Name
52	FO *(DT1)*
53	$\overline{IRQ1}$ *(TFS1)*
54	$\overline{IRQ0}$ *(RFS1)*
55	FI *(DR1)*
56	SCLK1
57	V_{DD}
58	D0
59	D1
60	D2
61	D3
62	D4
63	D5
64	D6
65	D7
66	D8
67	D9
68	D10

PIN CONFIGURATIONS

80-Lead PQFP
80-Lead TQFP



PQFP/ TQFP Number	Pin Name
1	A5
2	A6
3	GND
4	GND
5	A7
6	A8
7	A9
8	A10
9	A11
10	A12
11	A13
12	$\overline{PMS}$
13	$\overline{DMS}$
14	$\overline{BMS}$
15	$\overline{BG}$
16	XTAL
17	CLKIN
18	NC
19	NC
20	NC

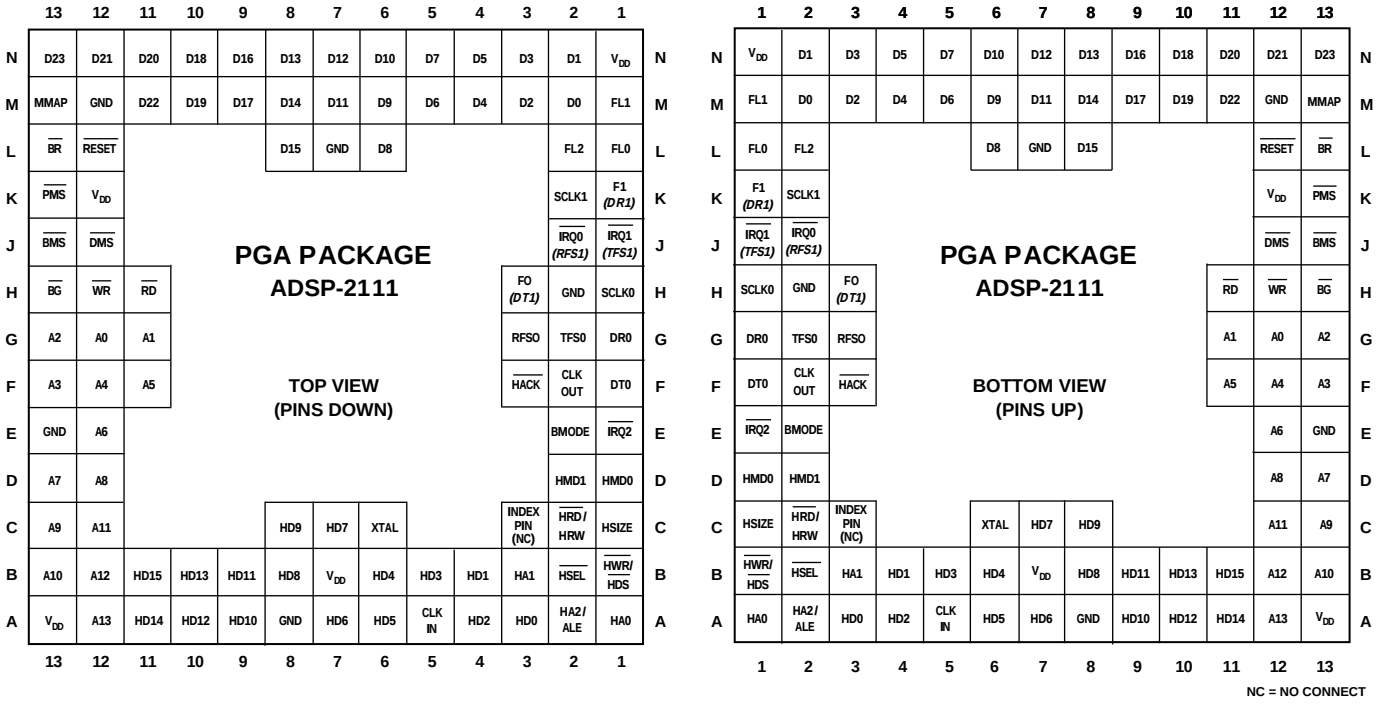
PQFP/ TQFP Number	Pin Name
21	CLKOUT
22	$\overline{WR}$
23	$\overline{RD}$
24	DT0
25	TFS0
26	RFS0
27	GND
28	GND
29	DR0
30	SCLK0
31	FO *(DT1)*
32	$\overline{IRQ1}$ *(TFS1)*
33	$\overline{IRQ0}$ *(RFS1)*
34	FI *(DR1)*
35	SCLK1
36	V_{DD}
37	D0
38	D1
39	D2
40	D3

PQFP/ TQFP Number	Pin Name
41	NC
42	NC
43	NC
44	D4
45	D5
46	D6
47	D7
48	D8
49	D9
50	D10
51	D11
52	GND
53	GND
54	D12
55	D13
56	D14
57	D15
58	D16
59	D17
60	D18

PQFP/ TQFP Number	Pin Name
61	GND
62	GND
63	D19
64	D20
65	D21
66	D22
67	D23
68	V_{DD}
69	V_{DD}
70	MMAP
71	$\overline{BR}$
72	$\overline{IRQ2}$
73	$\overline{RESET}$
74	A0
75	A1
76	A2
77	A3
78	A4
79	V_{DD}
80	V_{DD}

PIN CONFIGURATIONS

100-Pin PGA



PGA Number	Pin Name
N13	D23
N12	D21
M13	MMAP
M12	GND
L13	$\overline{BR}$
L12	$\overline{RESET}$
K13	$\overline{PMS}$
K12	V_{DD}
J13	$\overline{BMS}$
J12	$\overline{DMS}$
H13	$\overline{BG}$
H12	$\overline{WR}$
H11	$\overline{RD}$
G13	A2
G12	A0
G11	A1
F13	A3
F12	A4
F11	A5
E13	GND
E12	A6
D13	A7
D12	A8
C13	A9
C12	A11

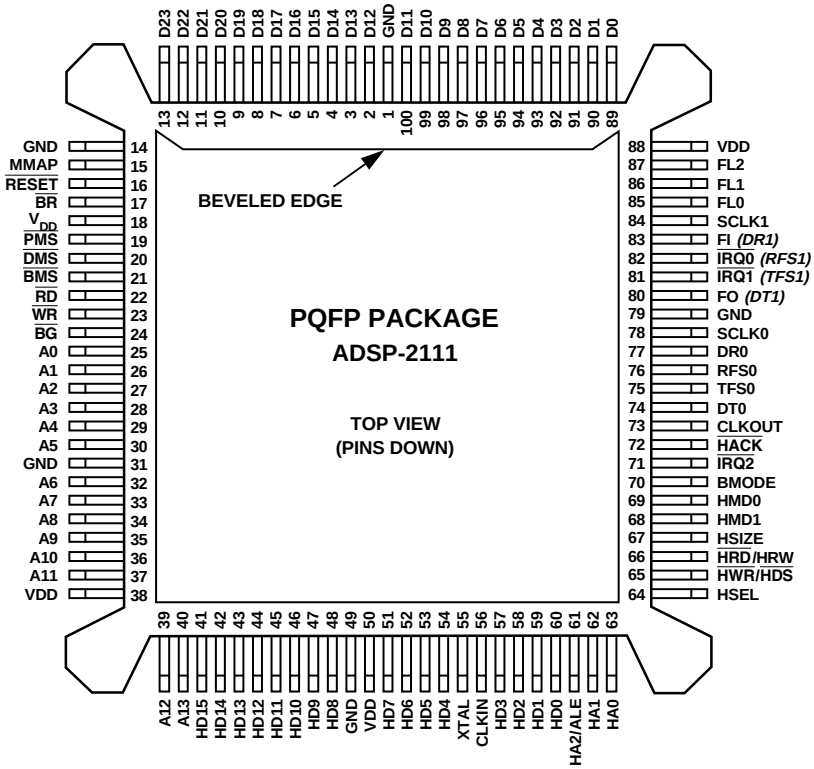
PGA Number	Pin Name
B13	A10
A13	V_{DD}
A12	A13
B12	A12
A11	HD14
B11	HD15
A10	HD12
B10	HD13
A9	HD10
B9	HD11
A8	GND
B8	HD8
C8	HD9
A7	HD6
B7	V_{DD}
C7	HD7
A6	HD5
B6	HD4
C6	XTAL
A5	CLKIN
B5	HD3
A4	HD2
B4	HD1
A3	HD0
B3	HA1

PGA Number	Pin Name
C3	Index (NC)
A2	HA2/ALE
A1	HA0
B1	$\overline{HWR}$/$\overline{HDS}$
B2	$\overline{HSEL}$
C1	HSIZE
C2	$\overline{HRD}$/HRW
D1	HMD0
D2	HMD1
E1	$\overline{IRQ2}$
E2	BMODE
F1	DT0
F2	CLKOUT
F3	$\overline{HACK}$
G1	DR0
G2	TFS0
G3	RFS0
H1	SCLK0
H2	GND
H3	FO *(DT1)*
J1	$\overline{IRQ1}$ *(TFS1)*
J2	$\overline{IRQ0}$ *(RFS1)*
K1	FI *(DR1)*
K2	SCLK1
L1	FL0

PGA Number	Pin Name
L2	FL2
M1	FL1
N1	V_{DD}
N2	D1
M2	D0
N3	D3
M3	D2
N4	D5
M4	D4
N5	D7
M5	D6
N6	D10
M6	D9
L6	D8
N7	D12
M7	D11
L7	GND
N8	D13
M8	D14
L8	D15
N9	D16
M9	D17
N10	D18
M10	D19
N11	D20
M11	D22

PIN CONFIGURATIONS

100-Lead Bumpered PQFP



NOTE: PIN 1 IS LOCATED AT THE CENTER OF THE BEVELED-EDGE SIDE OF THE PACKAGE.

PQFP Number	Pin Name
1	GND
2	D12
3	D13
4	D14
5	D15
6	D16
7	D17
8	D18
9	D19
10	D20
11	D21
12	D22
13	D23
14	GND
15	MMAP
16	$\overline{\text{RESET}}$
17	$\overline{\text{BR}}$
18	V_{DD}
19	$\overline{\text{PMS}}$
20	$\overline{\text{DMS}}$
21	$\overline{\text{BMS}}$
22	$\overline{\text{RD}}$
23	$\overline{\text{WR}}$
24	$\overline{\text{BG}}$
25	A0

PQFP Number	Pin Name
26	A1
27	A2
28	A3
29	A4
30	A5
31	GND
32	A6
33	A7
34	A8
35	A9
36	A10
37	A11
38	V_{DD}
39	A12
40	A13
41	HD15
42	HD14
43	HD13
44	HD12
45	HD11
46	HD10
47	HD9
48	HD8
49	GND
50	V_{DD}

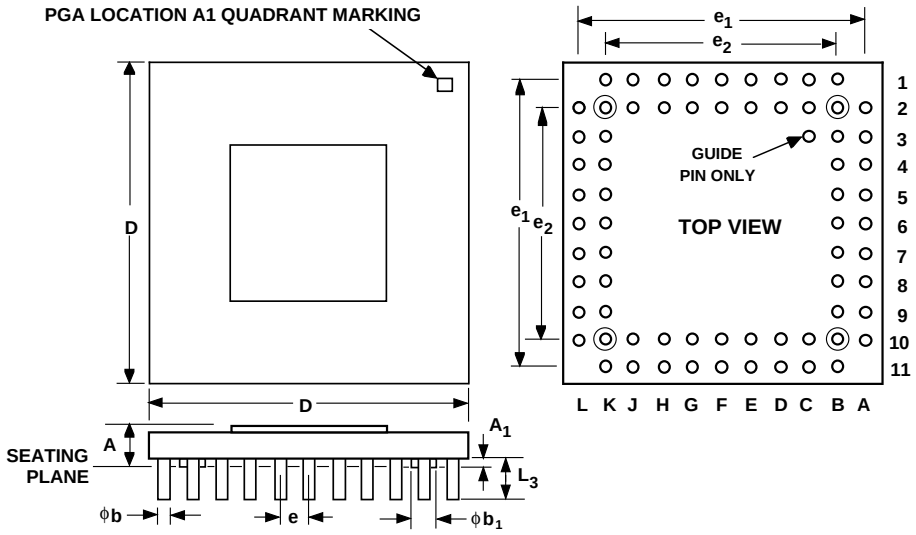
PQFP Number	Pin Name
51	HD7
52	HD6
53	HD5
54	HD4
55	XTAL
56	CLKIN
57	HD3
58	HD2
59	HD1
60	HD0
61	HA2/ALE
62	HA1
63	$\overline{\text{HA0}}$
64	$\overline{\text{HSEL}}$
65	$\overline{\text{HWR}}/\overline{\text{HDS}}$
66	$\overline{\text{HRD}}$/HRW
67	HSIZE
68	HMD1
69	HMD0
70	BMODE
71	$\overline{\text{IRQ2}}$
72	$\overline{\text{HACK}}$
73	CLKOUT
74	DT0
75	TFS0

PQFP Number	Pin Name
76	RFS0
77	DR0
78	SCLK0
79	GND
80	$\overline{\text{FO}}$ *(DT1)*
81	$\overline{\text{IRQ1}}$ *(TFS1)*
82	$\overline{\text{IRQ0}}$ *(RFS1)*
83	FI *(DR1)*
84	SCLK1
85	FL0
86	FL1
87	FL2
88	V_{DD}
89	D0
90	D1
91	D2
92	D3
93	D4
94	D5
95	D6
96	D7
97	D8
98	D9
99	D10
100	D11

OUTLINE DIMENSIONS

ADSP-2101

68-Pin Grid Array (PGA)

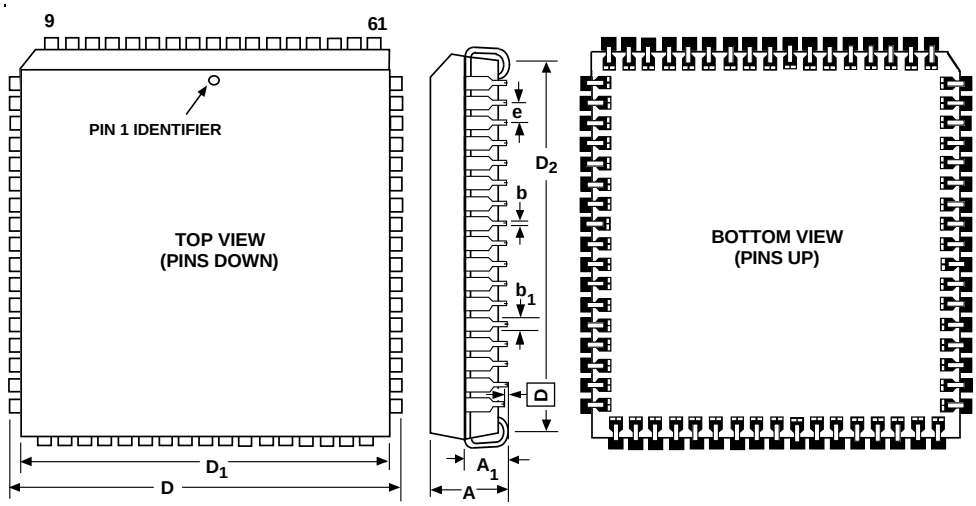


SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.164	3.12		4.17
A_1		0.50			1.27	
ϕb	0.016	0.018	0.020		0.46	
ϕb_1		0.050			1.27	
D	1.086		1.110	27.58		28.19
e_1	0.988		1.012	25.10		25.70
e_2	0.788		0.812	20.02		20.62
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-21xx

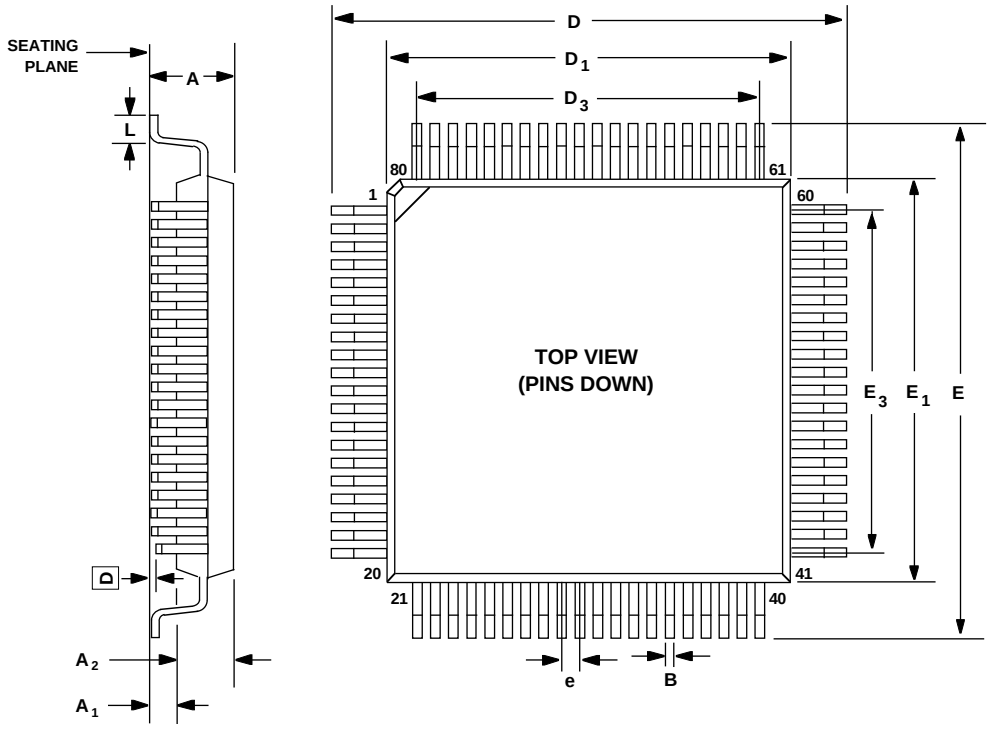
68-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.169	0.172	0.175	4.29	4.37	4.45
A_1		0.104			2.64	
b	0.017	0.018	0.019	0.43	0.46	0.48
b_1	0.027	0.028	0.029	0.69	0.71	0.74
D	0.985	0.990	0.995	25.02	25.15	25.27
D_1	0.950	0.952	0.954	24.13	24.18	24.23
D_2	0.895	0.910	0.925	22.73	23.11	23.50
e		0.050			1.27	
D			0.004			0.10

OUTLINE DIMENSIONS

ADSP-21xx
80-Lead Metric Plastic Quad Flatpack (PQFP)
80-Lead Metric Thin Quad Flatpack (TQFP)



PQFP

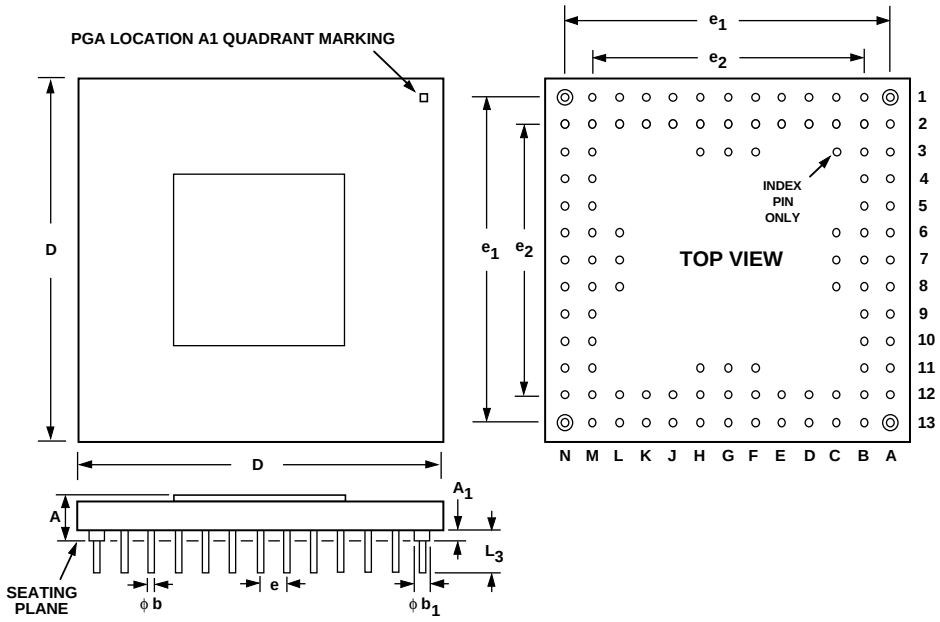
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.45			0.096
A_1	0.25			0.010		
A_2	1.90	2.00	2.10	0.075	0.079	0.083
D, E	16.95	17.20	17.45	0.667	0.678	0.690
D_1, E_1	13.90	14.00	14.10	0.547	0.551	0.555
D_3, E_3		12.35	12.43		0.486	0.490
L	0.65	0.80	0.95	0.026	0.031	0.037
e	0.57	0.65	0.73	0.023	0.026	0.029
B	0.22	0.30	0.38	0.009	0.012	0.015
a			0.10			0.004

TQFP

MILLIMETERS			INCHES		
MIN	TYP	MAX	MIN	TYP	MAX
		1.60			0.063
0.05		0.15	0.002		0.006
1.35	1.40	1.45	0.053	0.055	0.057
15.75	16.00	16.25	0.620	0.630	0.640
13.95	14.00	14.05	0.549	0.551	0.553
	12.35	12.43		0.486	0.490
0.50	0.60	0.75	0.020	0.024	0.030
0.57	0.65	0.73	0.022	0.026	0.029
0.25	0.30	0.35	0.010	0.012	0.014
		0.10			0.004

OUTLINE DIMENSIONS

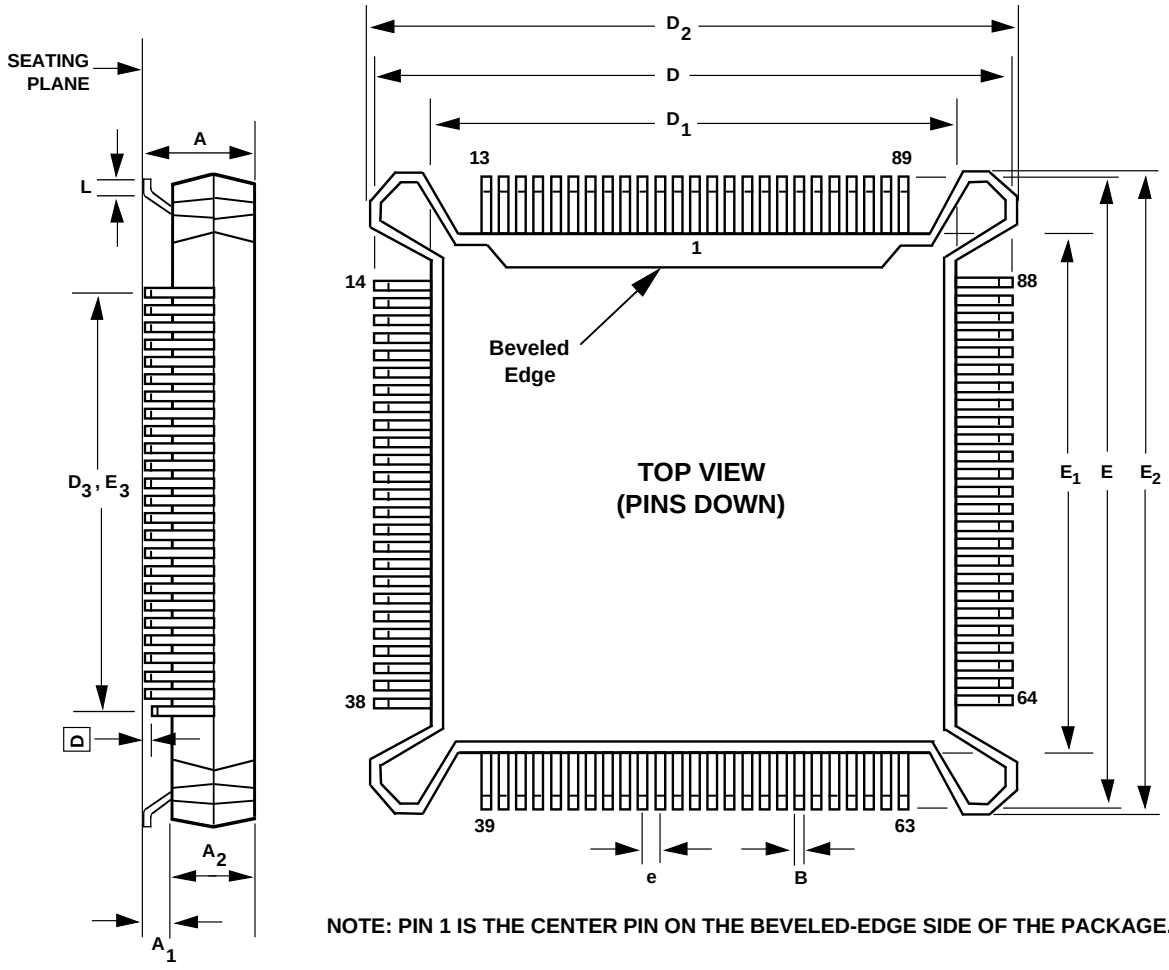
ADSP-2111
100-Pin Grid Array (PGA)



	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.169	3.12		4.29
A_1		0.050			1.27	
ϕb	0.016	0.018	0.020	0.41	0.46	0.51
ϕb_1		0.050			1.27	
D	1.308	1.32	1.342	33.22	33.53	34.09
e_1	1.188	1.20	1.212	30.18	30.48	30.78
e_2	0.988	1.00	1.012	25.10	25.4	25.70
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-2111
100-Lead Bumpered Plastic Quad Flatpack (PQFP)



NOTE: PIN 1 IS THE CENTER PIN ON THE BEVELED-EDGE SIDE OF THE PACKAGE.

	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A			0.180			4.572
A_1	0.020	0.030	0.040	0.508	0.762	1.016
A_2	0.130	0.140	0.150	3.302	3.556	3.810
D, E	0.875	0.880	0.885	22.225	22.352	22.479
D_1, E_1	0.747	0.750	0.753	18.974	19.050	19.126
D_2, E_2	0.897	0.900	0.903	22.784	22.860	22.936
D_3, E_3		0.600	0.603		15.240	15.316
L	0.036		0.046	0.914		1.168
e	0.022	0.025	0.028	0.559	0.635	0.711
B	0.008		0.012	0.203		0.305
D			0.004			0.102

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2101KG-66	0°C to +70°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101BG-66	–40°C to +85°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101KG-80	0°C to +70°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101BG-80	–40°C to +85°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101KP-100	0°C to +70°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101BP-100	–40°C to +85°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101KS-100	0°C to +70°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-100	–40°C to +85°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101KG-100	0°C to +70°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101BG-100	–40°C to +85°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101TG-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2103KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2103BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2105KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115KST-66	0°C to +70°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-66	–40°C to +85°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115KST-80	0°C to +70°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-80	–40°C to +85°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-100	0°C to +70°C	25.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-100	–40°C to +85°C	25.0 MHz	68-Lead PLCC	P-68A

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
ST = TQFP (Thin Quad Flatpack)

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2111KG-52	0°C to +70°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-52	–40°C to +85°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-52	0°C to +70°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-52	–40°C to +85°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-66	0°C to +70°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111BG-66	–40°C to +85°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111KS-66	0°C to +70°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-66	–40°C to +85°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-80	0°C to +70°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-80	–40°C to +85°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-80	0°C to +70°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-80	–40°C to +85°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111TG-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2161KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2161BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2162KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2162BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2163KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163KP-100[2]	0°C to +70°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-100[2]	–40°C to +85°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-100[2]	0°C to +70°C	25 MHz	80-Lead PQFP	S-80
ADSP-2163BS-100[2]	–40°C to +85°C	25 MHz	80-Lead PQFP	S-80
ADSP-2164KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2164BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
[2]Minimum order quantities required. Contact factory for further information.

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