EVALUATION KIT AVAILABLE

MAX77387

Dual-Phase Adaptive DC-DC Step-Up Converter With 2x 1000mA High-Side Current Regulators

General Description

The MAX77387 provides a high-efficiency solution for smartphone camera flash applications by integrating a dual-phase 2A PWM DC-DC step-up converter and two programmable 1A high side, low-dropout LED current regulators for flash and torch functions. An I²C interface provides flexible control of the step-up converter, torch, flash mode selection, and torch/flash safety timer duration settings.

The IC operates down to 2.5V, making it futureproof for new battery technologies. The step-up converter features an internal switching MOSFET and synchronous rectifier to improve efficiency and minimize external component count. Dual-phase operation ensures low output ripple and provides smallest possible solution size. The IC also includes dual high-side high-current regulators for supporting torch and flash modes. The high-current regulators can source up to 1A each in flash mode and up to 250mA each in torch mode. The high-current regulators can be combined to drive a single LED up to 2A in flash mode and up to 500mA in torch mode. The output voltage can be adaptively controlled, boosting only as high as necessary to support the required LED forward voltage. Adaptive mode can be used in either flash or torch mode and works with both DAC and/or PWM dimming control schemes. This approach reduces IC power dissipation by optimizing the boost ratio and by minimizing the losses in the current regulators.

The IC includes control for external NTC, dual Tx mask, flash strobe, and torch enable functions. This allows for flexible control of the IC.

Additionally, the IC includes MAXFLASH 2.0 function that adaptively reduces flash current during low battery conditions to help prevent system undervoltage lockup.

Other features include shorted LED detection, overvoltage and thermal shutdown protection, and low-power standby and shutdown modes. The IC is available in a 20-bump, 0.4mm pitch WLP package (2.1mm x 1.73mm).

Applications

Cell Phones and Smartphones

Tablets

**Patent protected PCT/US2008/075643.*

Benefits and Features

- **Input Supply of 2.5V to 5.5V with Full Functionality**
- **Dual-Phase Interleave Step-Up DC-DC Converter**
  - **True Shutdown Output**
  - **2A Guaranteed Output Current for V_{IN} > 2.7V and $V_{OUT} \leq$ 4.0V**
  - **Adaptive Output Voltage Regulation to Ensure Industry's Highest System Efficiency**
  - **Over 90% Peak Efficiency**
  - **3.125% Minimum Duty Cycle**
  - **Skip Mode Capable**
  - **On-Chip Power MOSFET and Synchronous Rectifier**
  - **Up to 4MHz PWM Switching Frequency per Phase**
  - **Small 0.47µH Inductor per Phase**
- **High-Side Torch/Flash LED Current Regulator**
  - **I²C Programmable Flash Output Current (15.625mA to 1000mA in 15.625mA Steps)**
  - **I²C Programmable Torch Output Current (3.91mA to 250mA in 3.91mA Steps for Non-PWM dimming) (125mA to 1000mA in 125mA Steps for PWM Dimming with Programmable Duty Cycle from 3.125% to 25% in 3.125% steps)**
  - **Low-Dropout Voltage (80mV typ) at 1000mA**
- **I²C-Programmable Flash Safety Timer**
- **I²C-Programmable Torch Safety Timer and Optional Disabled Torch Timer**
- **Dual Independent TX_MASK Inputs for Limiting Flash Current During Tx Events**
- **Open/Shorted LED Detection**
- **NTC Monitoring for LED Protection**
- **Overvoltage Protection**
- **MAXFLASH 2.0 Preventing System Undervoltage Lockup**
- **Thermal Shutdown Protection**
- **< 1µA Shutdown Current**
- **20-Bump, 0.4mm Pitch 2.1mm x 1.73mm WLP**

***Ordering Information* appears at end of data sheet.**

***Simplified Block Diagram* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX77387.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, IN, REG_IN to AGND ..... -0.3V to +6.0V
OUT_A, OUT_B to PGND_A, PGND_B ..... -0.3V to +6.0V
LX_A to PGND_A ..... -0.3V to V_{OUT} + 0.3V
LX_B to PGND_B ..... -0.3V to V_{OUT} + 0.3V
FLED1, FLED2 to AGND ..... -0.3V to V_{REG_IN} + 0.3v
TX1_MASK, TX2_MASK, TORCH_EN, NTC to AGND ..... -0.3V to V_{IN} + 0.3V
SDA, SCL, FLASH_STB to AGND ..... -0.3V to V_{IN} + 0.3V
AGND to PGND_A, PGND_B ..... -0.3V to +0.3V
I_{LX_A}, I_{LX_B} Current (rms) per Phase 2.0A
Continuous Power Dissipation (T_A = +70°C) (derate 21.7mW/°C above +70°C) 1736mW
Operating Temperature ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) (Note 1) ..... +260°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

WLP
Junction to Ambient Thermal Resistance (θ_{JA}) ..... 46°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C**,** unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN Operating Voltage Range			2.5		5.5	V
V_{DD} Operating Voltage Range			1.62		3.6	V
IN Undervoltage Lockout (IN_UVLO) Threshold	V_{IN} falling, 60mV (typ) hysteresis		2.10	2.20	2.30	V
V_{DD} Under voltage Lockout (VDD_UVLO) Threshold	V_{DD} falling		0.65	0.9	1.0	V
IN Shutdown Supply Current	V_{IN} = 5.5V, V_{DD} = 0V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
V_{DD} Standby Supply Current	V_{IN} = 5.5V, V_{DD} = V_{SDA} = V_{SCL} = 3.6V, DCDC_MODE = 00	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
IN Standby Supply Current	V_{IN} = 5.5V, V_{DD} = V_{SCL} = V_{SDA} = 3.6V, DCDC_MODE = 00, DC-DC converter and current regulators are off	T_A = -40°C to +85°C		1.5	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INTERFACE						
Logic Input High Voltage	V_{DD} = 1.62V to 3.6V	SDA, SCL, FLASH_STB	0.7 x V_{DD}		V_{DD} + 0.3V	V
	V_{IN} = 2.5V to 5.5V	TORCH_EN, TX1_MASK, TX2_MASK	1.25		V_{IN} + 0.3V	V
Logic Input Low Voltage	V_{DD} = 1.62V to 3.6V	SDA, SCL, FLASH_STB			0.4	V
	V_{IN} = 2.5V to 5.5V	TORCH_EN, TX1_MASK, TX2_MASK			0.4	
Pulldown Resistor	V_{DD} = 1.62V to 3.6V FLASH_STB_PD = 1	FLASH_STB	400	800	1600	kΩ
	V_{IN} = 2.5V to 5.5V TORCH_EN_PD = 1, TX1_MASK_PD = 1, TX2_MASK_PD = 1	TORCH_EN, TX1_MASK, TX2_MASK	400	800	1600	
Logic Input Current	V_{DD} = 1.62V to 3.6V, FLASH_STB_PD = 0	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		
	V_{IN} = 2.5V to 5.5V TORCH_EN_PD = 0, TX1_MASK_PD = 0, TX2_MASK_PD = 0	T_A = +25°C	-1	0.01	+1	
		T_A = +85°C		0.1		
LOGIC INTERFACE TIMING						
FLASH_STB Enable Delay in Active Mode ($t_{FLASH_EN_ACTIV}$)	See Figure 4, from FLASH_STB rising edge until start of current regulator ramp up (Note 4)			5		µs
TORCH_EN Enable Delay in Active Mode ($t_{TORCH_EN_ACTIV}$)	See Figure 4, from TORCH_EN rising edge until start of current regulator ramp up (Note 4)			5		µs
FLASH_STB Enable Delay in Standby Mode ($t_{FLASH_STB_STDBY}$)	See Figure 3, from FLASH_STB rising edge until start of precharge of the output (Note 4)			30		µs
TORCH_EN Enable Delay in Standby Mode ($t_{TORCH_EN_STDBY}$)	See Figure 3, from TORCH_EN rising edge until start of precharge of the output (Note 4)			30		µs
Precharging of Output (t_{OUT_PCHG})	See Figures 3–6, V_{IN} = 3.6, C_{OUT} = 10µF, charging the output from 0V until LX starts switching (Note 4)			600		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start Time Duration, (t_{DCDC_SS})	See Figures 3, 4, and 5 (Note 4)			DCDC_SS x 8		µs
TX_MASK Trigger to Reduced Output Current ($t_{TX_MASK_EN}$)	See Figures 9 and 10 From TX1_MASK, TX2_MASK triggered until output current is at reduced output current (Note 4)			7		µs
Standby to Active Mode ($t_{STDBY2ACTIV}$)	See Figures 5 and 6 Time to transition from standby to active mode (Note 4)			25		µs
I²C INTERFACE (Note 4)						
SDA Output Low Voltage	I_{SDA} = 3mA			0.03	0.4	V
I²C Clock Frequency					400	kHz
Bus-Free Time Between START and STOP	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}		0.6	0.1		µs
SCL Low Period	t_{LOW}		1.3	0.2		µs
SCL High Period	t_{HIGH}		0.6	0.2		µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6	0.1		µs
SDA Hold Time	t_{HD_DAT}		0	-0.01		µs
SDA Setup Time	t_{SU_DAT}		100	50		ns
Setup Time for STOP Condition	t_{SU_STO}		0.6	0.1		µs
STEP-UP DC-DC CONVERTER						
OUT Voltage Range	Adaptive controlled		2.3		5.2	V
Output Adaptive Regulation Step Size	Smallest step size when output voltage is in adaptive regulation $V_{ADPT_REG_STEP}$			6.25		mV
Digital Overvoltage Protection (OVP_D)	When operating in adaptive mode	OVP_TH = 00		0x140h (4.3V)		9-bit digital code
		OVP_TH = 01		0x170h (4.6V)		
		OVP_TH = 10		0x1A0h (4.9V)		
		OVP_TH = 11		0x1D0h (5.2V)		
Analog Overvoltage Protection	OVP_TH = 00		4.35	4.5	4.65	V
	OVP_TH = 01		4.65	4.8	4.95	
	OVP_TH = 10		4.95	5.1	5.25	
	OVP_TH = 11		5.25	5.4	5.55	
Output Threshold for Minimum Duty Cycle to Bypass Mode	V_{OUT_MIND} Output voltage where the DC-DC converter goes from operating at minimum duty cycle to dropout operation, during a disabling of the DC-DC converter, DCDC_MODE = 00			V_{IN} + 200mV		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Threshold for Dropout Operation to OFF Mode	V_{OUT_OFF} Output voltage where the DC-DC converter goes from operating in dropout mode to true shutdown, during a disabling of the DC-DC converter, DCDC_MODE = 00			V_{IN} + 150mV		V
Charge Mode Comparator Threshold	Output voltage where the DC-DC converter goes from operating at minimum duty cycle to soft start.			V_{IN} - 300mV		V
Adaptive Output Step Time	Time between sampling of adaptive regulation during soft-start (Note 5)			1		µs
	Time between sampling of adaptive regulation (Note 5)			8		
IN Supply Current	V_{OUT} = 4.5V, I_{OUT} = 0mA, switching 4MHz PWM mode dual-phase operation (Note 2)			14		mA
	V_{OUT} = 4.5V, I_{OUT} = 0mA, switching 2MHz PWM mode dual-phase operation (Note 2)			15		
	V_{OUT} = 4.5V, I_{OUT} = 0mA, no switching (skip mode)			450		µA
Low-Side Current Limit (Static Limits) (Phases A and B)	DCDC_ILIM = 00		1.11	1.25	1.37	A
	DCDC_ILIM = 01		1.35	1.5	1.65	
	DCDC_ILIM = 10		1.57	1.75	1.93	
	DCDC_ILIM = 11		1.80	2.0	2.20	
Current Sharing	Delta current between phase A and phase B (Note 4), excluding external components			0		%
Phase A Zero-Crossing Threshold (Static, Phases A and B)				120		mA
LX_ High-Side On-Resistance (Phases A and B)	LX_ to OUT_, $I_{LX_}$ = -200mA, V_{OUT} = 3.6V			130	185	mΩ
LX_ Low-Side On-Resistance (Phases A and B)	LX_ to PGND_, $I_{LX_}$ = 200mA, V_{OUT} = 3.6V			100	160	mΩ
Load Regulation	V_{IN} = 3.4V, V_{OUT} = 4.5V, enhanced mode (DCDC_GAIN = 1) (for adaptive mode only) (Note 4)			50		mV/A
	V_{IN} = 3.4V, V_{OUT} = 4.5V, enhanced mode (DCDC_GAIN = 1) (for program mode only) (Note 4)			100		mV/A
LX_ Leakage (Phase A, Phase B)	$V_{LX_}$ = 5.5V	T_A = +25°C		0.1	2	µA
		T_A = +85°C		0.1		
Operating Frequency (Phase A, Phase B)	DCDC_OPERATION[2:0] = 010	T_A = -40°C to +85°C	3.90	4.0	4.10	MHz
Maximum Duty Cycle (Phase A, Phase B)	DCDC_OPERATION[2:0] = 011		70			%
Minimum Duty Cycle	During non-skip mode (DCDC_OPERATION[2:0] = 011)			3.3		%
	During skip mode (Note 4)			0		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LED CURRENT SOURCE DRIVERS					
REG_IN Supply Current (FLED1, FLED2)	FLED_ enabled in torch mode with PWM dimming set to maximum current setting, supply current measured during off period of PWM cycle		100		µA
IN Supply Current (FLED1, FLED2)	FLED_ enabled in torch mode with PWM dimming set to maximum current setting, supply current measured during off period of PWM cycle		25		µA
LED Current Setting Range (FLED1, FLED2)	FLED_ enabled in flash mode, current range in 15.625mA steps	15.625		1000	mA
	FLED_ enabled in torch mode, with DAC mode active, current range in 3.91mA steps	3.91		250	
	FLED_ enabled in torch mode with PWM dimming active, current range in 125mA steps	125.0		1000	
PWM Dimming Duty Cycle Setting Range	FLED_ enabled in torch mode with PWM dimming active, duty cycle range in 3.125% steps (Note 5)	3.125		25	%
PWM Dimming Frequency Setting Range	FREQ_PWM[1:0] = 00 (Note 5)		7.8		kHz
	FREQ_PWM[1:0] = 01 (Note 5)		1.9		
	FREQ_PWM[1:0] = 10 (Note 5)		0.488		
	FREQ_PWM[1:0] = 11 (Note 5)		0.122		
LED Peak Current Overshoot	FLED_ enabled in torch mode with PWM dimming set to maximum current setting, maximum LED current overshoot during initial ramping up (Note 4)		10		%
LED Current Settling Time	FLED_ enabled in torch mode with PWM dimming set to maximum current setting. Time for LED current to settle to less than 10% from nominal setting (not including ramp time) (Note 4)		6		µs
LED Current Accuracy Flash Mode or Torch Mode with PWM Dimming (FLED1, FLED2)	625mA to 1000mA	-5		+5	%
	218.75mA to 609.375mA	-7		+7	
	62.5mA to 203.125mA	-10		+10	
	31.25mA to 46.875mA	-12		+12	
	15.625mA	-14		+14	
LED Current Accuracy Torch Mode (FLED1, FLED2)	156.25 to 250mA	-5		+5	%
	54.6875mA to 152.34375mA	-7		+7	
	15.625mA to 50.78125mA	-10		+10	
	7.8125mA to 11.71875mA	-12		+12	
	3.91mA	-14		+14	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LED Current Dropout Voltage Flash Mode or Torch Mode with PWM Dimming (FLED1, FLED2)	1000mA setting at -10%			80		mV
	1000mA setting at -1% (Note 4)			100		
LED Current Dropout Voltage Torch Mode (FLED1, FLED2)	250mA setting at -10%			80		mV
	250mA setting at -1% (Note 4)			100		
LED Adaptive Mode Threshold Voltage Setting Range (FLED1, FLED2)	FLED_ enabled in flash mode or torch mode	DCDC_ADPT_REG = 00		120		mV
		DCDC_ADPT_REG = 01		150		
		DCDC_ADPT_REG = 10		180		
		DCDC_ADPT_REG = 11		210		
LED Leakage Current	REG_IN = 5.5V, FLED_ = 0V	T_A = +25°C		0.1	2	µA
		T_A = +85°C		1		
REG_IN UVLO Voltage	Minimum voltage on REG_IN required before FLED_ current regulators are enabled		2.2	2.3	2.4	V
TIMERS						
Flash Duration Timer Range	In 0.256ms steps (Note 5)		0.128		0.896	ms
	In 0.512ms steps (Note 5)		0.896		2.944	
	In 1.024ms steps (Note 5)		2.944		11.136	
	In 2.048ms steps (Note 5)		11.136		43.904	
	In 4.096ms steps (Note 5)		43.904		437.12	
	In 8.192ms steps (Note 5)		437.12		699.264	
Torch Duration Timer Range TORCH_TMR0	In 131.072ms steps (Note 5)		122.88		561.1	ms
	In 262.144ms steps (Note 5)		561.1		1564.67	
	In 524.288ms steps (Note 5)		1564.67		5767.17	
	In 1048.576ms steps (Note 5)		5767.17		22536.19	
Torch and Flash Duration Timer Accuracy	T_A = 0°C to +85°C (Note 4)		-2.5	0	+2.5	ms
	T_A = -40°C to +85°C (Note 4)		-3	0	+3	
Flash Mode Ramp Rate Settings	LED current ramp-up time (Note 5)	Time it takes for current regulator to ramp from 0mA to full scale current	384		32896	µs
	LED current ramp-down time. (Note 5)	Time it takes for current regulator to ramp from full scale current to 0mA	384		32896	µs
Torch Mode Ramp Rate Settings	LED current ramp-up time (Note 5)	Time it takes for current regulator to ramp from 0mA to full scale current	16.392		2097	ms
	LED current ramp-down time (Note 5)	Time it takes for current regulator to ramp from full scale current to 0mA	16.392		2097	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DIE PROTECTION					
Shorted LED detection Threshold FLED1, FLED2				1	V
Short Debounce timer FLED1, FLED2	From LED short detected until LED current regulator is disabled (Note 5)		1.024		ms
OVP_A Debounce Timer	Time where adaptive regulation threshold is set at OVP_A threshold until current regulator is disabled (Note 5)		1.024		ms
OVP_D Debounce Timer	Time where adaptive regulation threshold is set at OVP_D threshold until current regulator is disabled (Note 5)		384		µs
IN_UVLO/THERM Debounce Timer	Either time where V_{IN} is less than IN_UVLO threshold or thermal threshold is exceeded until the current regulator is disabled (Note 5)		0.512		ms
Thermal Shutdown Hysteresis	(Note 4)		20		°C
Thermal Shutdown	T_J = rising (Note 4)		+160		°C
NTC THERMAL PROTECTION					
NTC Bias	NTC_BIAS_25C T_A = +25°C	194	200	206	µA
NTC Bias Temperature Coefficient	NTC_T_COMP (Note 4)		0.020		µA/°C
NTC Bias On-Time ($t_{NTC_TORCH_ON}$)	Time NTC bias is enabled before temperature measurement is performed in torch mode (Note 5)		0.512		ms
NTC Bias On Interval ($_{NTC_TORCH_OFF}$)	Time between enabling of NTC bias in torch mode (Note 5)		131		ms
NTC Over Temperature Detection Threshold Range	In 50mV steps, NTC falling	200		550	mV
NTC Over Temperature Threshold Hysteresis			50		mV
NTC Over Temperature Threshold Accuracy	For NTC_TH at the 200mV setting	-2		+2	%
NTC Short Detection Threshold		55	70	120	mV
MAXFLASH					
Low Battery Detect Threshold Range	In 33mV steps, V_{IN} falling	2.4		3.4	V
Low Battery Voltage Threshold Accuracy			±2.5		%
Low Battery Voltage Hysteresis Programmable Range	In 50mV steps	50		350	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{DD} = 1.8V, V_{PGND_A} = V_{PGND_B} = V_{AGND} = 0V, V_{TX1_MASK} = V_{TX2_MASK} = V_{TORCH_EN} = V_{FLASH_STB} = 0V, f_{SW} = 4MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Battery Inhibit Timer	Falling in 256µs steps (Note 5)	256		2048	µs
	Rising in 256µs steps (Note 5)	256		2048	
Low Battery Inhibit Time Accuracy	(Note 4)	-3		+3	%

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

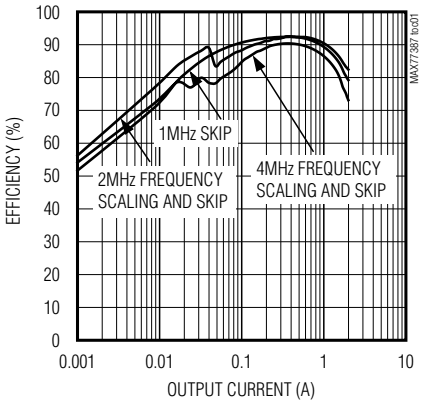
Note 4: Parameter not production tested. Parameter guaranteed by design through characterization.

Note 5: Parameter production tested through scan. Parameter guaranteed by design through characterization.

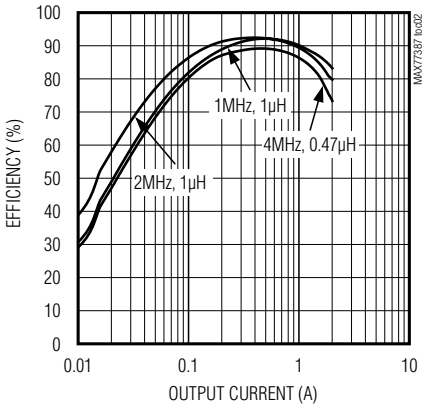
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

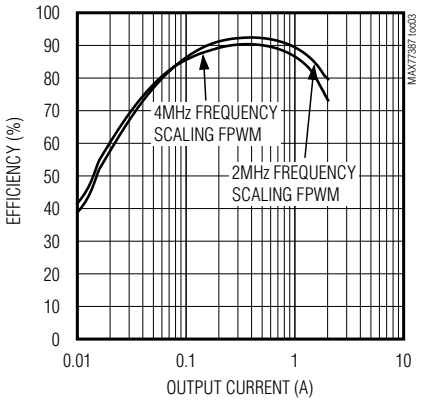
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 2.5V, V_{OUT} = 4V) 1µH



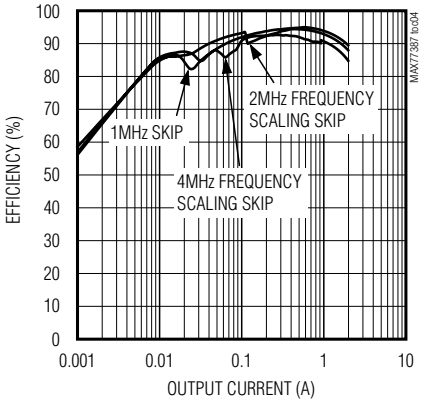
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 2.5V, V_{OUT} = 4V, FPWM)



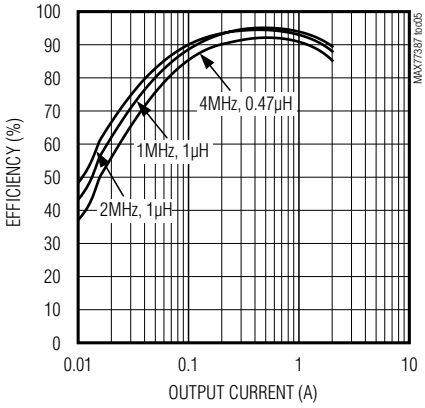
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 2.5V, V_{OUT} = 4V) 1µH



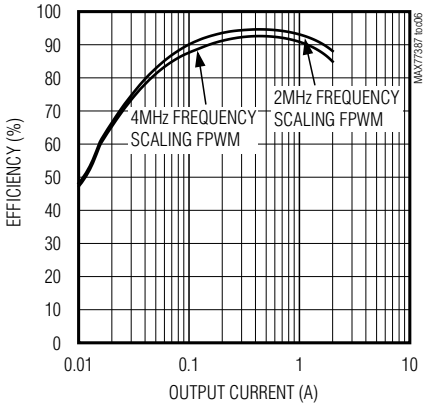
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.2V, V_{OUT} = 4V) 1µH



DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.2V, V_{OUT} = 4V, FPWM)



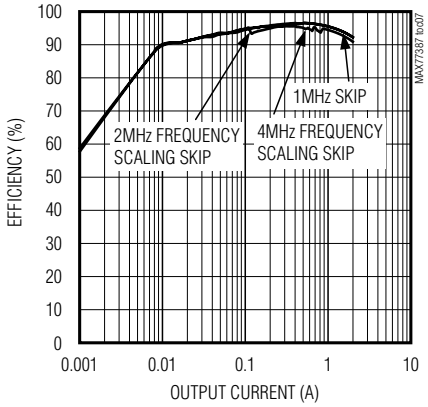
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.2V, V_{OUT} = 4V) 1µH



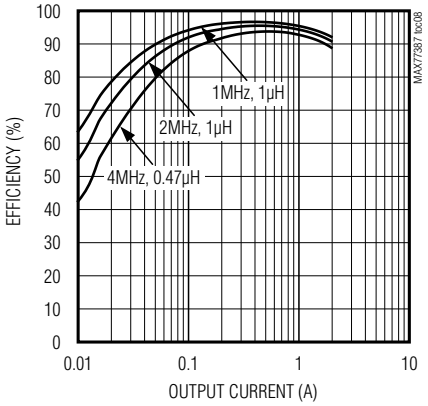
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

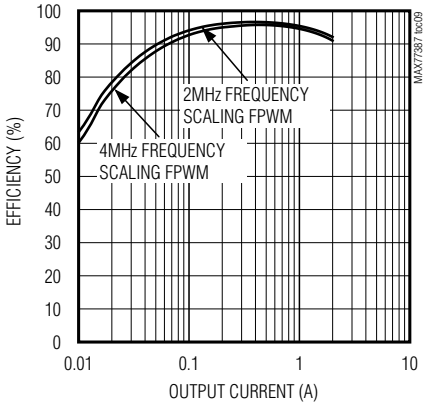
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.7V, V_{OUT} = 4V) 1µH



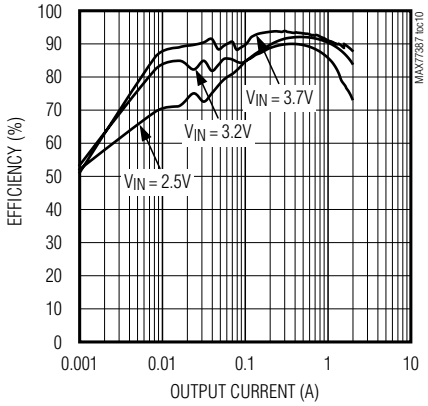
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.7V, V_{OUT} = 4V, FPWM)



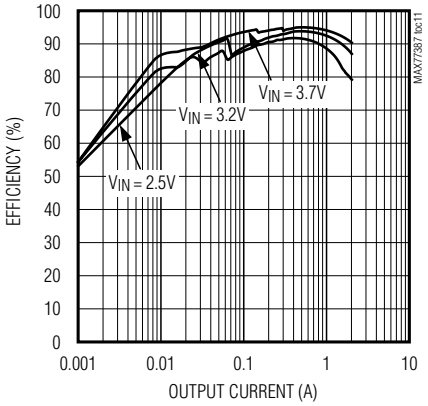
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.7V, V_{OUT} = 4V) 1µH



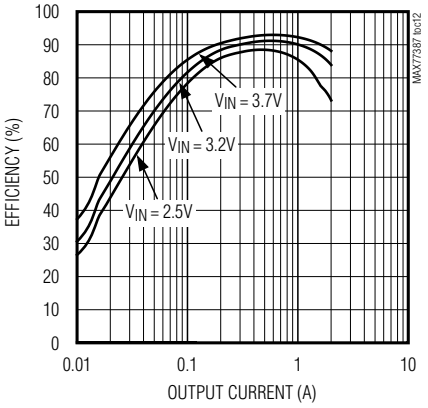
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT, V_{OUT} = 4.5V 4MHz FREQUENCY SCALING AND SKIP 1µH



DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT, V_{OUT} = 4.5V 2MHz FREQUENCY SCALING AND SKIP 1µH



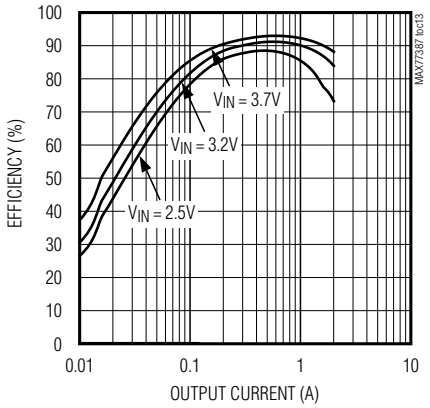
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 4V, 4MHz FPWM, 0.47µH)



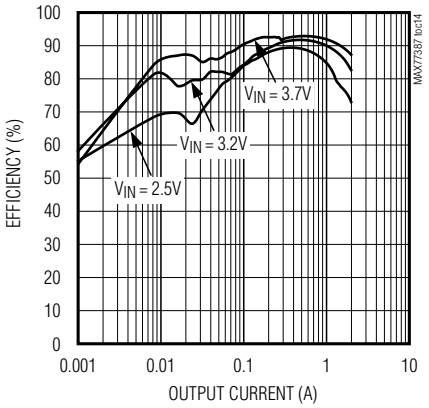
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

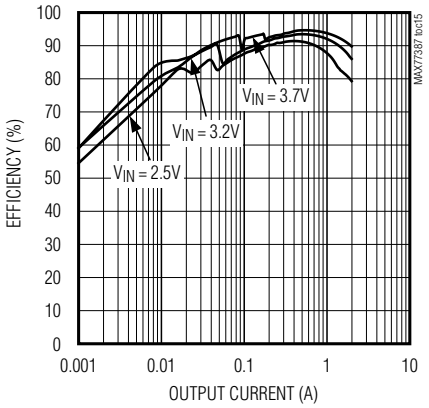
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT, V_{OUT} = 4.5V 2MHz FPWM 1µH



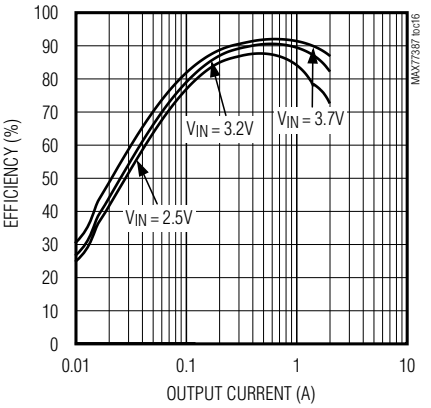
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRRENT, V_{OUT} = 5V 4MHz FREQUENCY SCALING AND SKIP 1µH



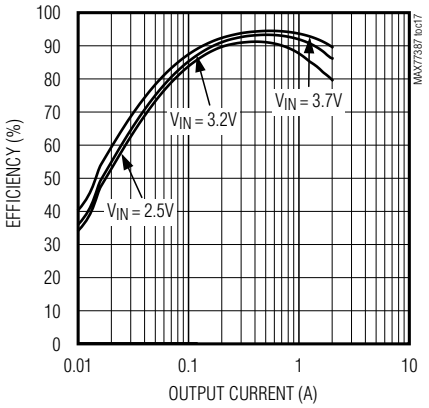
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRRENT, V_{OUT} = 5V 2MHz FREQUENCY SCALING AND SKIP 1µH



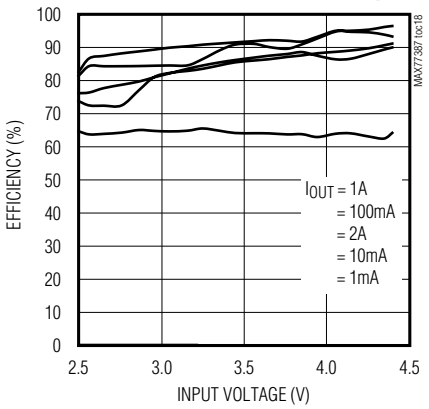
DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V, 4MHz FPWM, 0.47µH)



DC-DC CONVERTER EFFICIENCY vs. LOAD CURRENT, V_{OUT} = 5V 2MHz FPWM 1µH



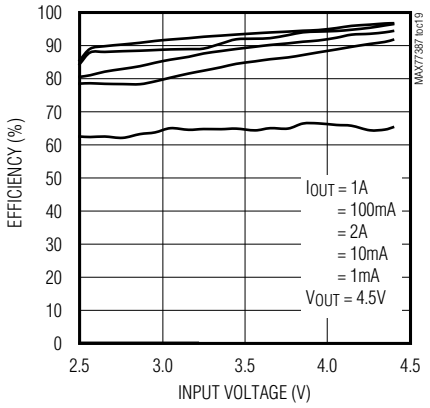
DC-DC CONVERTER EFFICIENCY vs. V_{IN}, V_{OUT} = 4.5V, 4MHz FREQUENCY SCALING AND SKIP 1µH



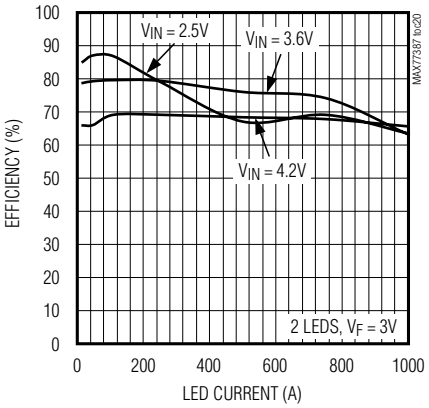
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

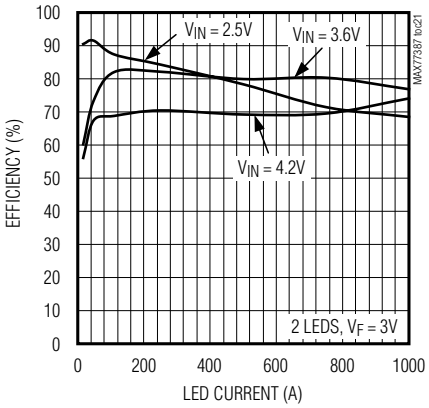
DC-DC CONVERTER EFFICIENCY vs. V_{IN}, 2MHz FREQUENCY SCALING AND SKIP 1µH



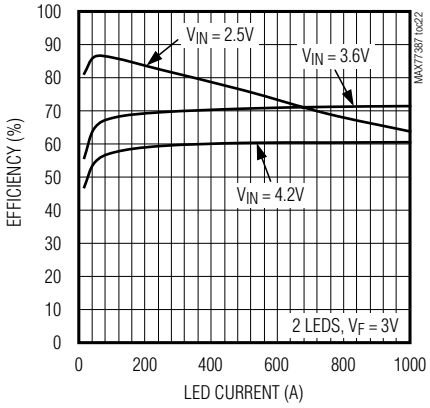
LED EFFICIENCY vs. LED CURRENT (4MHz, FREQUENCY SCALING, SKIP ALLOWED)



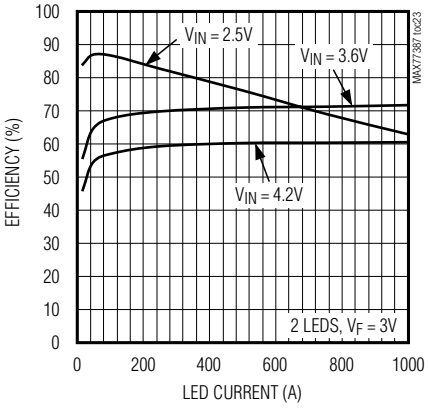
LED EFFICIENCY vs. LED CURRENT (2MHz, FREQUENCY SCALING, SKIP ALLOWED)



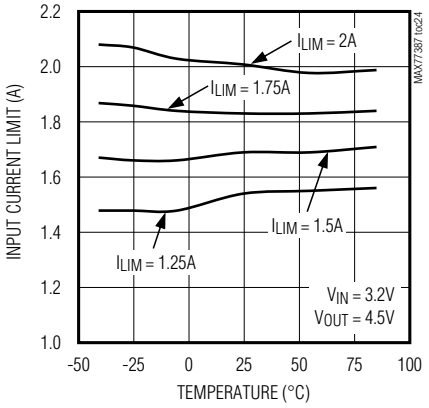
LED EFFICIENCY vs. LED CURRENT (4MHz, FPWM)



LED EFFICIENCY vs. LED CURRENT (2MHz, FPWM)



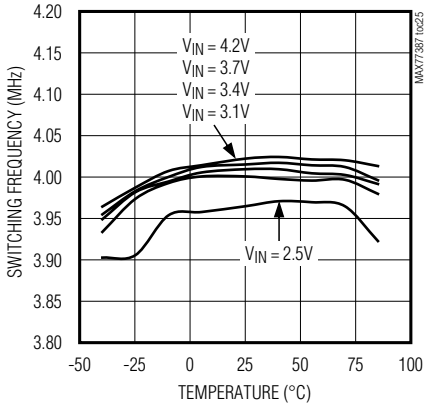
INPUT CURRENT LIMIT vs. TEMPERATURE



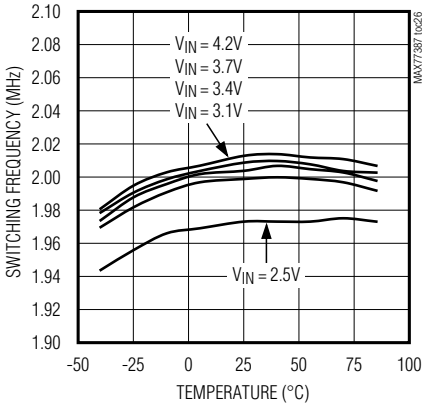
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

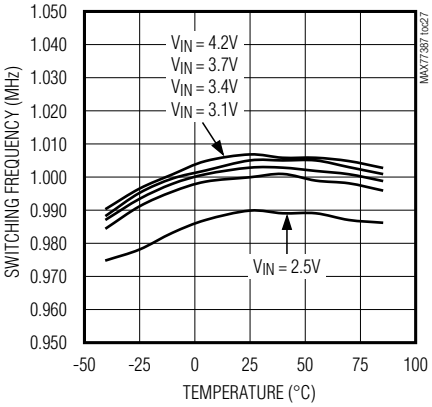
SWITCHING FREQUENCY vs. TEMPERATURE (4MHz FPWM)



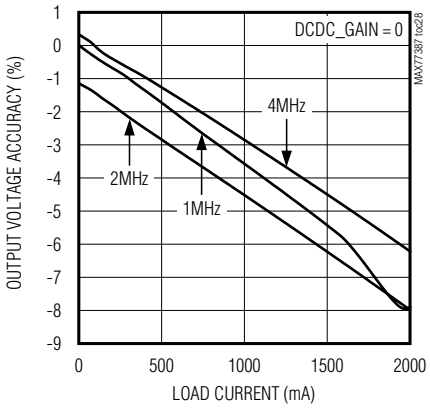
SWITCHING FREQUENCY vs. TEMPERATURE (2MHz FPWM)



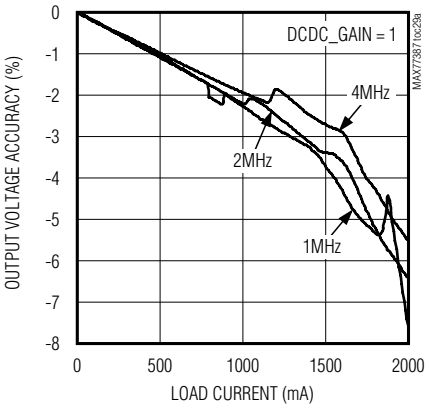
SWITCHING FREQUENCY vs. TEMPERATURE (1MHz FPWM)



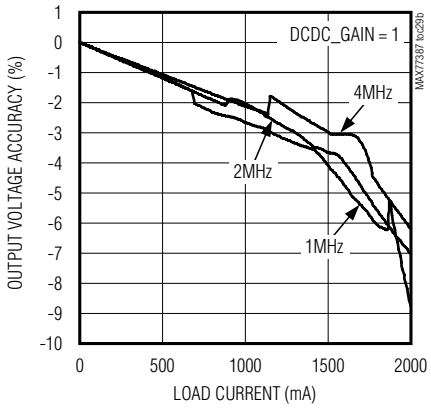
OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT (V_{IN} = 3.6V V_{OUT} = 5V FPWM)



OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT (V_{IN} = 3.6V, V_{OUT} = 5V FPWM)



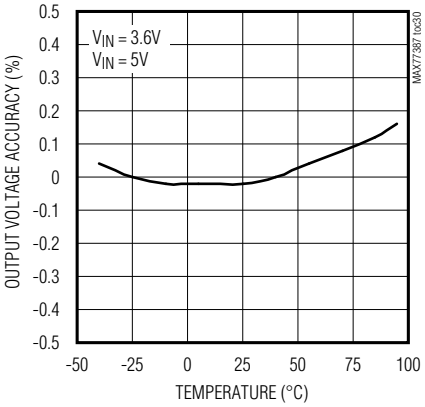
OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT (V_{IN} = 3.6V, V_{OUT} = 5V FPWM)



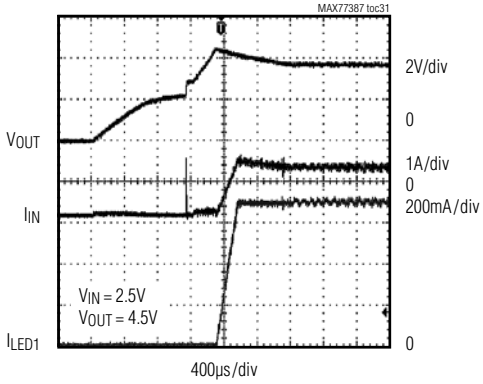
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

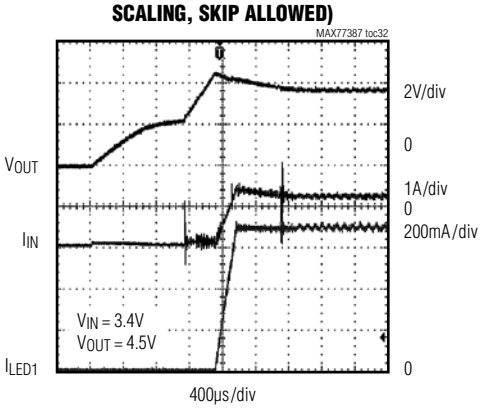
OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE



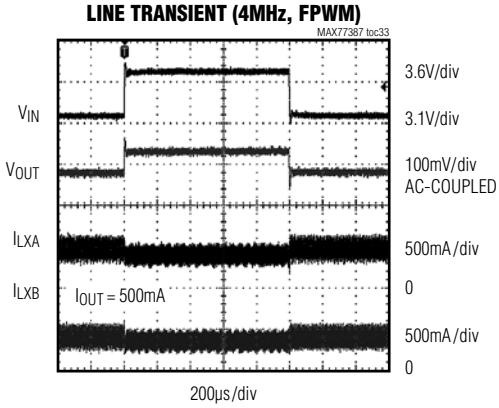
SOFT-START (4MHz, FPWM)



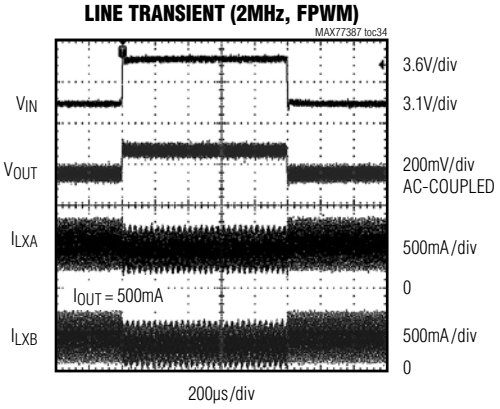
SOFT-START (4MHz, FREQUENCY SCALING, SKIP ALLOWED)



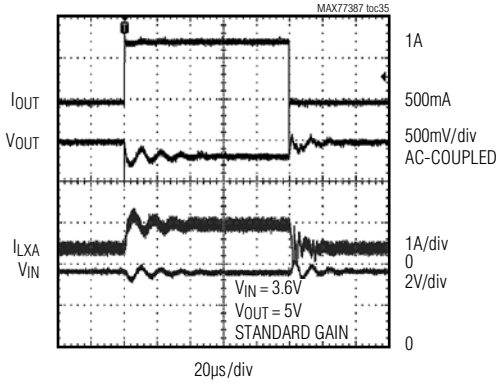
LINE TRANSIENT (4MHz, FPWM)



LINE TRANSIENT (2MHz, FPWM)



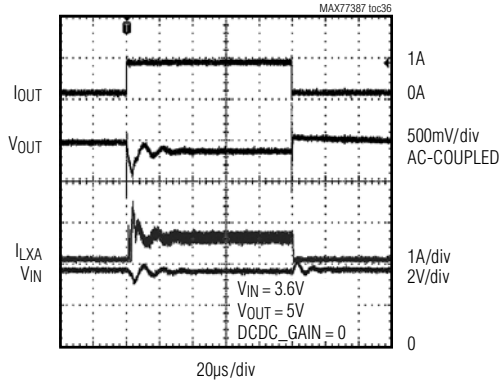
LOAD TRANSIENT (500mA-1A-500mA) 4MHz, FREQUENCY SCALING, SKIP ALLOWED



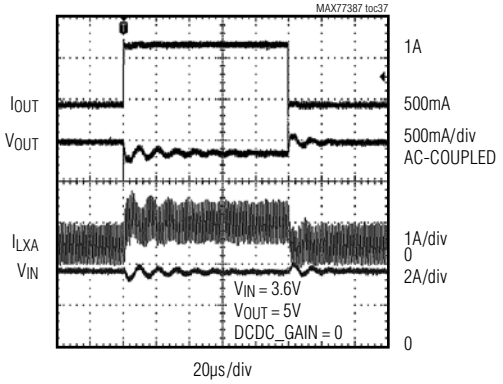
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

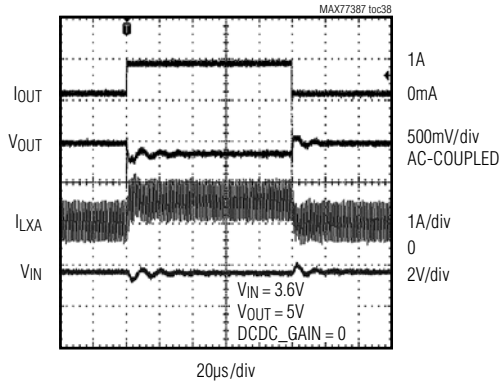
LOAD TRANSIENT (0A-1A-0A) 4MHz, FREQUENCY SCALING, SKIP ALLOWED



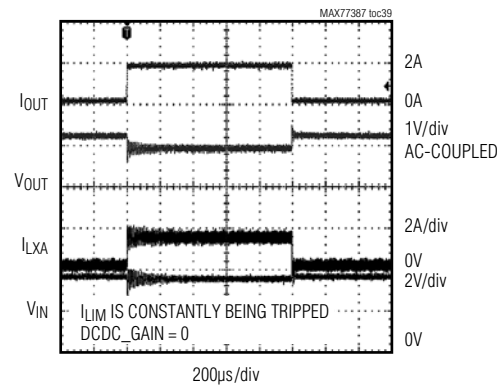
LOAD TRANSIENT (500mA-1A-500mA) 2MHz FPWM



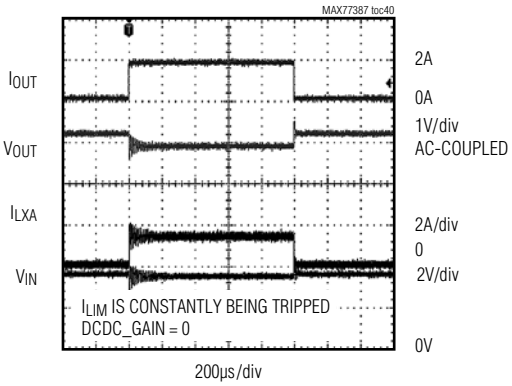
LOAD TRANSIENT (1mA-1A-1mA) 2MHz FPWM



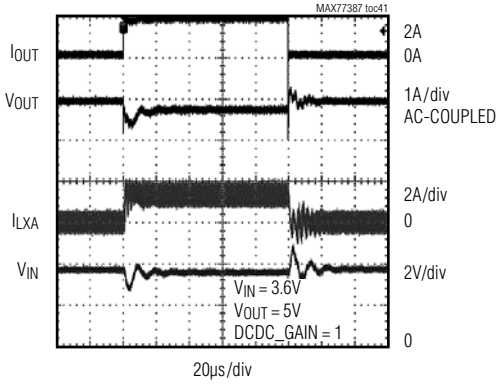
LOAD TRANSIENT (1mA-2A-1mA) 2MHz FPWM



LOAD TRANSIENT (1mA-2A-1mA) 4MHz FPWM



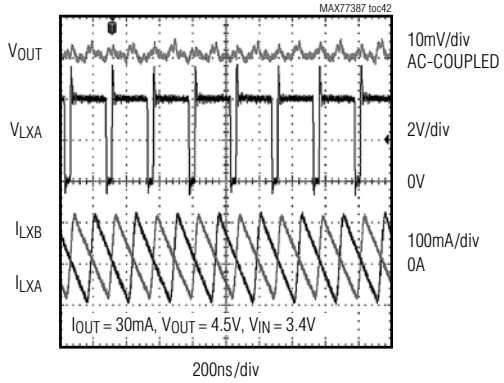
LOAD TRANSIENT (1mA-2A-1mA) 2MHz FPWM



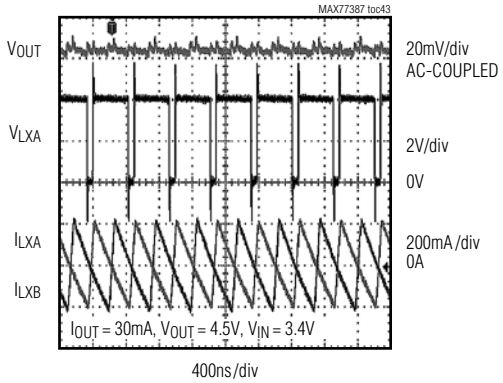
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

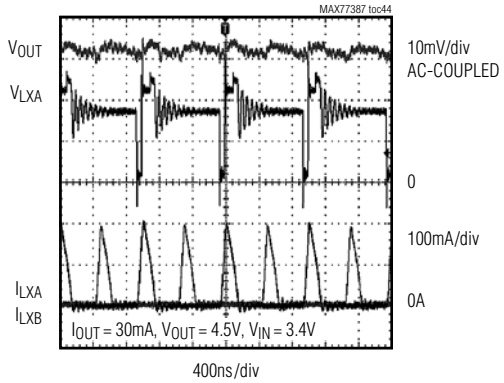
LIGHT-LOAD SWITCHING WAVEFORMS (4MHz FPWM)



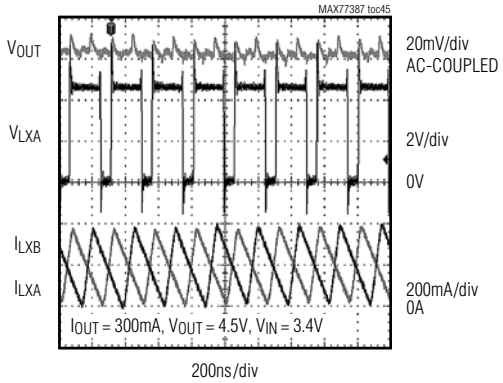
LIGHT-LOAD SWITCHING WAVEFORMS (2MHz FPWM)



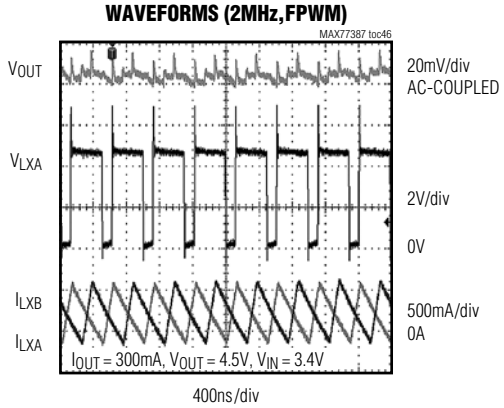
LIGHT-LOAD SWITCHING WAVEFORMS (4MHz, FREQUENCY SCALING, SKIP ALLOWED)



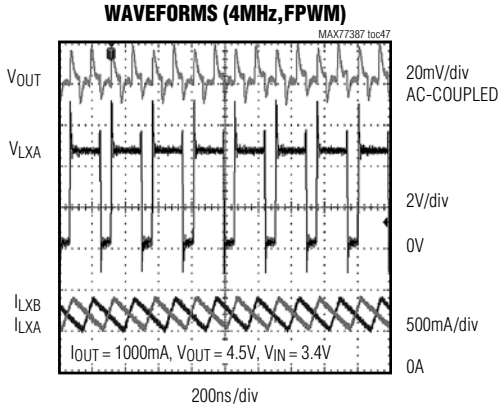
MODERATE-LOAD SWITCHING WAVEFORMS (4MHz,FPWM)



MODERATE-LOAD SWITCHING WAVEFORMS (2MHz,FPWM)



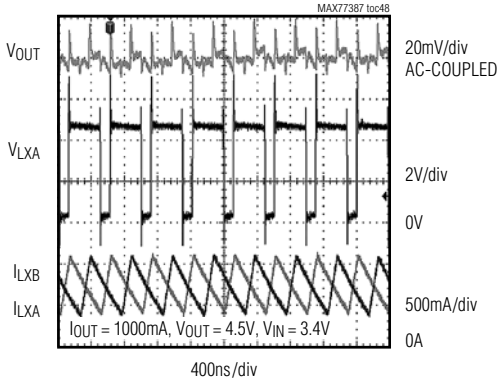
HEAVY-LOAD SWITCHING WAVEFORMS (4MHz,FPWM)



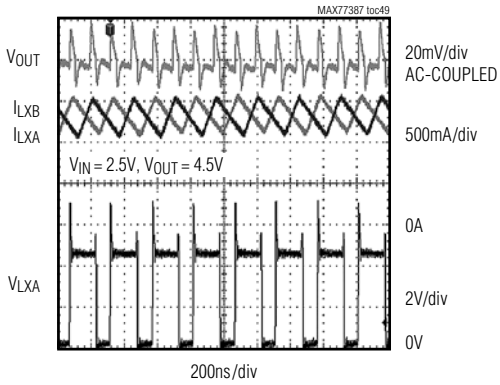
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

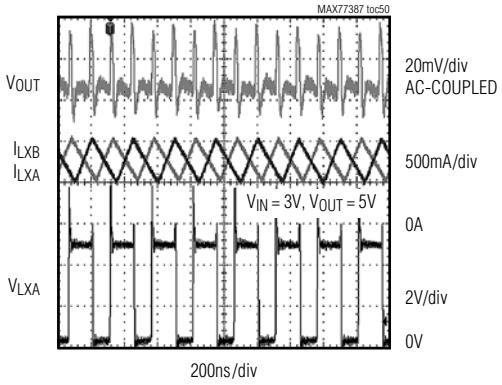
HEAVY-LOAD SWITCHING WAVEFORMS (2MHz,FPWM)



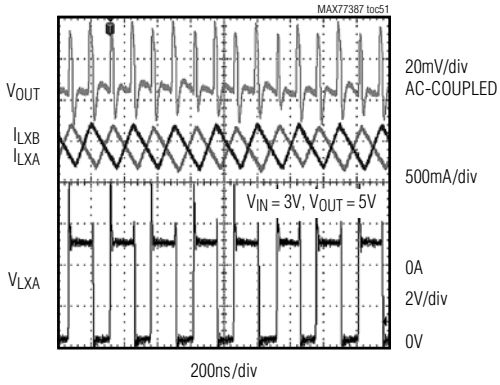
1.25A CURRENT LIMIT



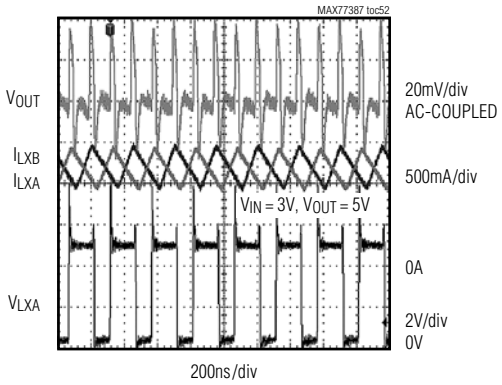
1.5A CURRENT LIMIT



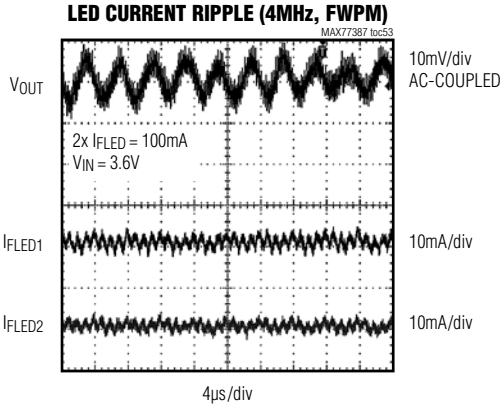
1.75A CURRENT LIMIT



2A CURRENT LIMIT



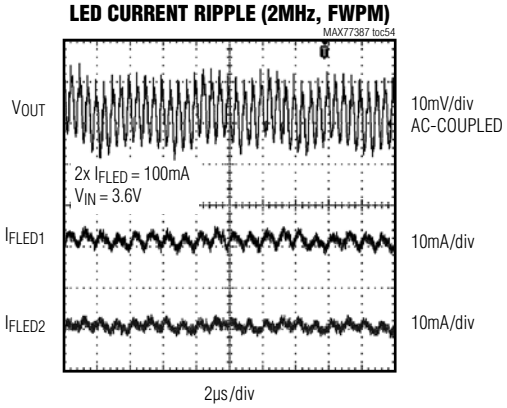
LED CURRENT RIPPLE (4MHz, FWPM)



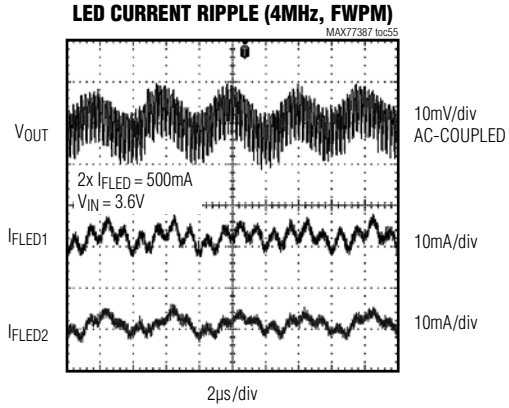
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

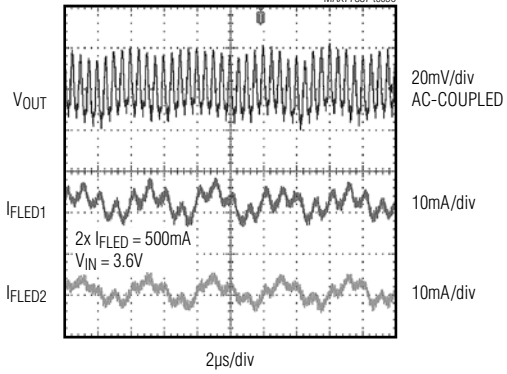
LED CURRENT RIPPLE (2MHz, FWPM)



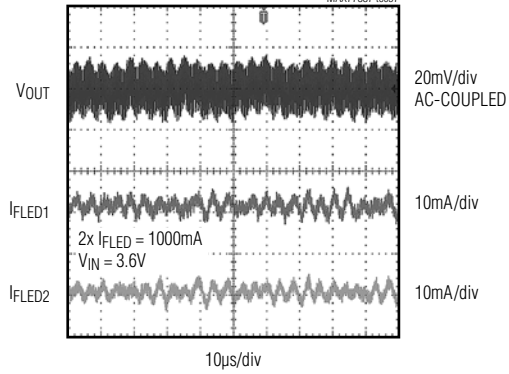
LED CURRENT RIPPLE (4MHz, FWPM)



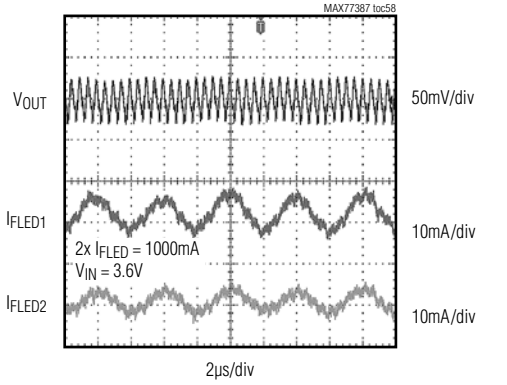
LED CURRENT RIPPLE (2MHz, FWPM)



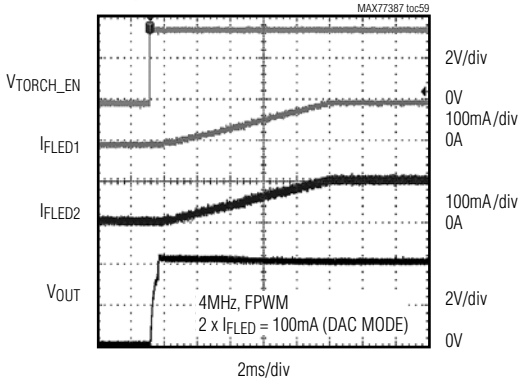
LED CURRENT RIPPLE (4MHz, FWPM)



LED CURRENT RIPPLE (2MHz, FWPM)



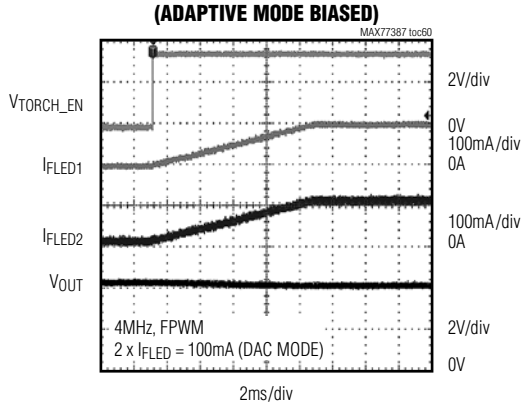
TORCH ENABLED BY TORCH_EN (ADAPTIVE MODE NO PREBIAS)



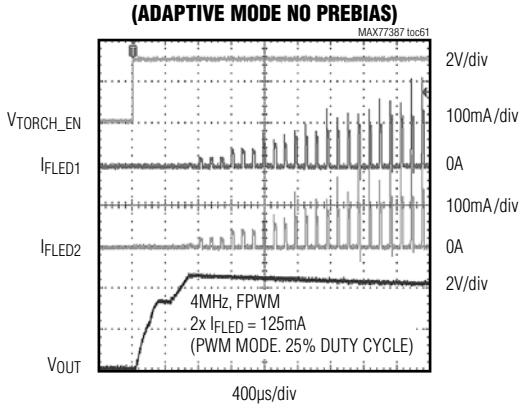
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

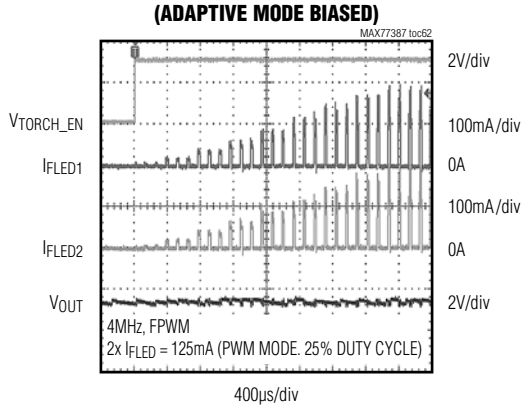
TORCH ENABLED BY TORCH_EN (ADAPTIVE MODE BIASED)



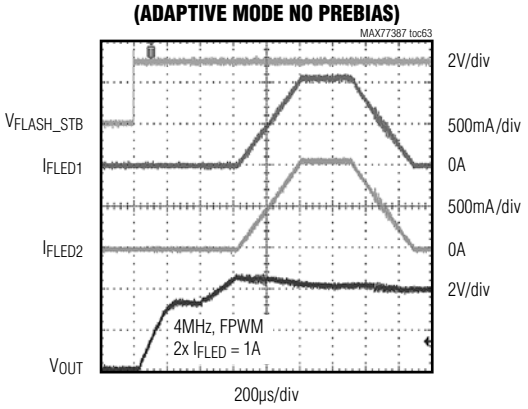
TORCH ENABLED BY TORCH_EN (ADAPTIVE MODE NO PREBIAS)



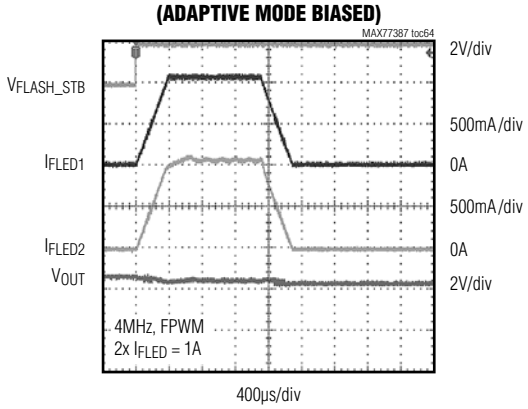
TORCH ENABLED BY TORCH_EN (ADAPTIVE MODE BIASED)



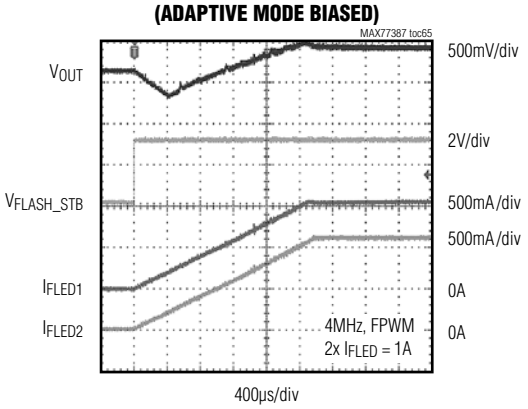
FLASH ENABLED BY FLASH_STB (ADAPTIVE MODE NO PREBIAS)



FLASH ENABLED BY FLASH_STB (ADAPTIVE MODE BIASED)



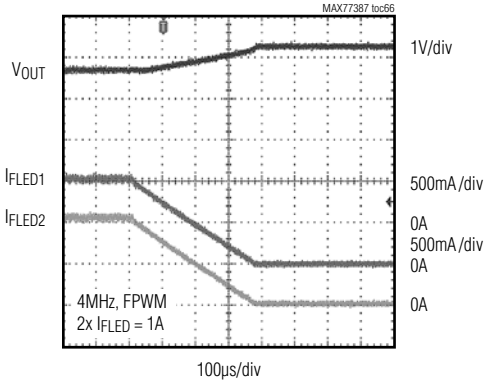
FLASH ENABLED BY FLASH_STB (ADAPTIVE MODE BIASED)



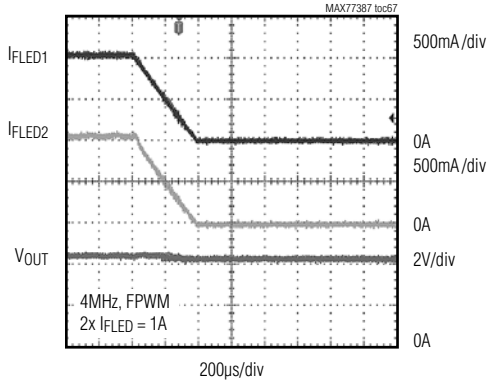
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

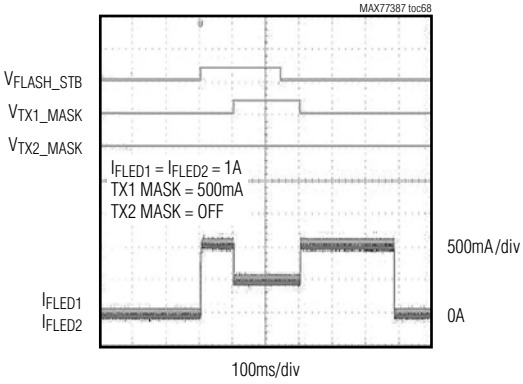
FLASH RAMP DOWN



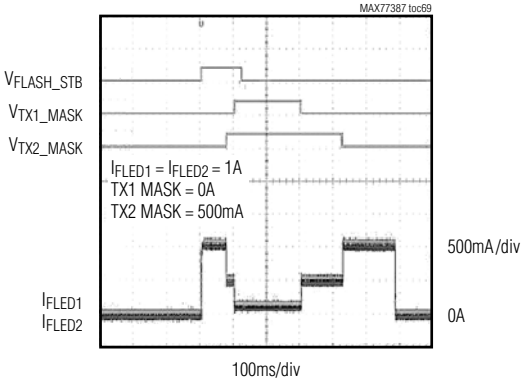
FLASH RAMP DOWN



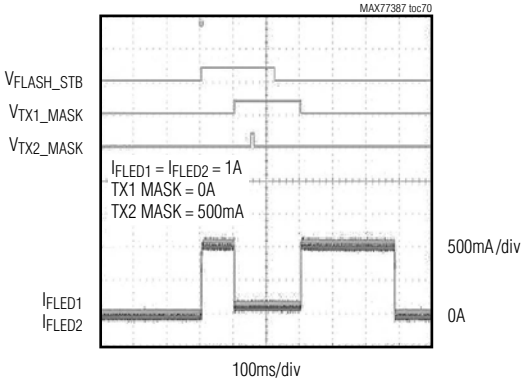
TX1 MASK (RISING EDGE)



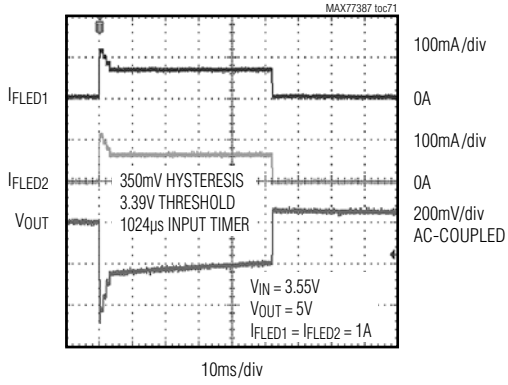
TX1 AND TX2 MASKS



TX1 AND TX2 MASKS



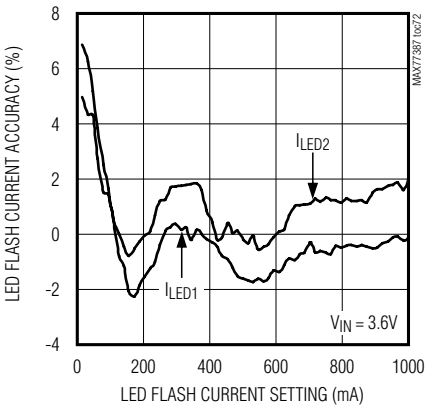
MAXFLASH



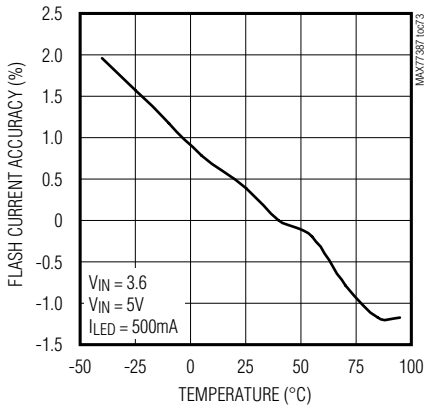
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

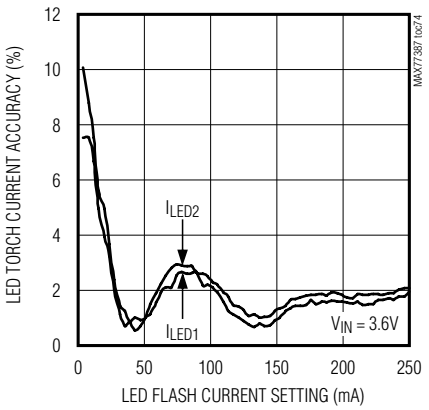
LED FLASH CURRENT ACCURACY vs. LOAD CURRENT



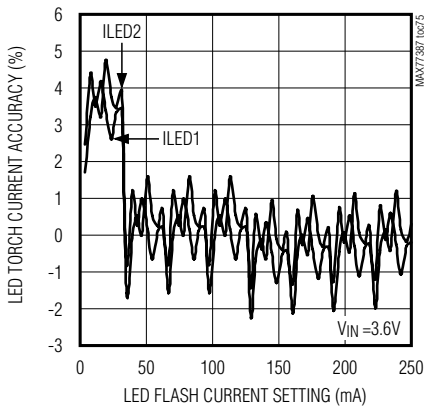
FLASH CURRENT ACCURACY vs. TEMPERATURE



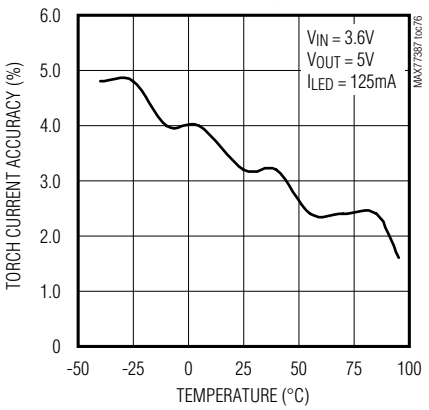
LED TORCH CURRENT ACCURACY vs. LOAD CURRENT (DAC MODE)



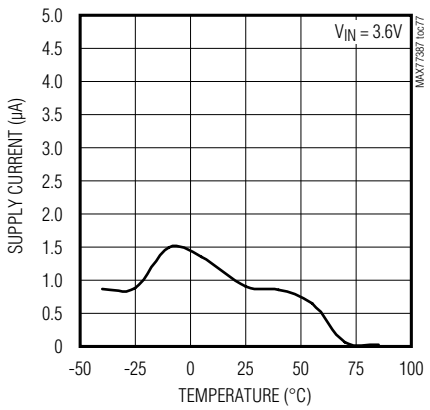
LED TORCH CURRENT ACCURACY vs. LOAD CURRENT (PWM MODE)



TORCH CURRENT ACCURACY vs. TEMPERATURE (DAC MODE)



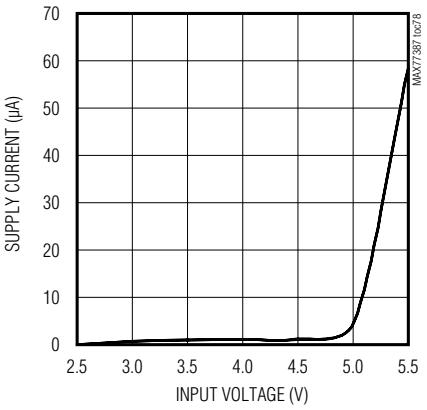
SHUTDOWN CURRENT vs. TEMPERATURE



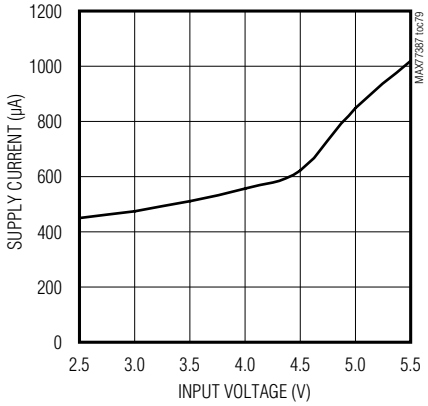
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

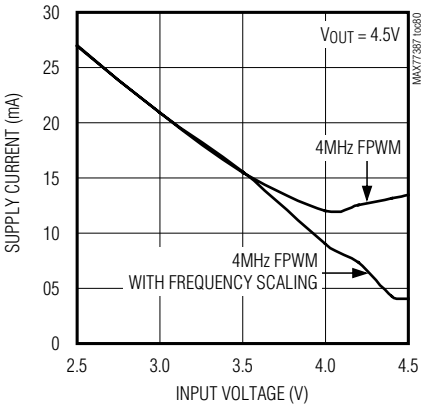
SHUTDOWN CURRENT vs. INPUT VOLTAGE



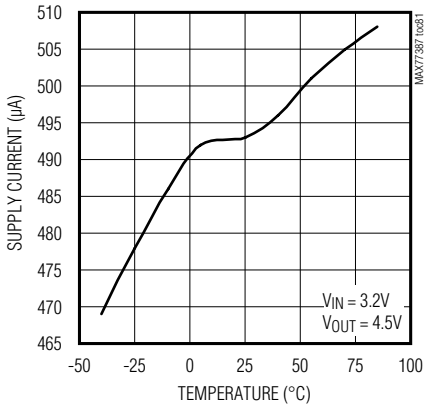
SUPPLY CURRENT vs. INPUT VOLTAGE (4MHz, FREQUENCY SCALING, SKIP ALLOWED)



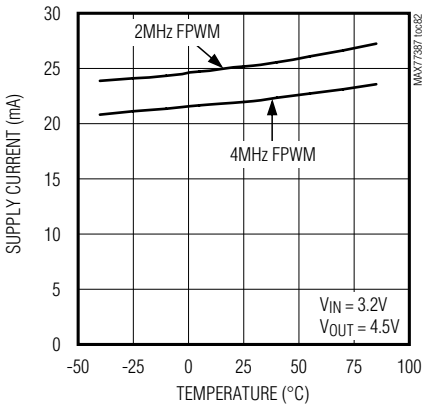
SUPPLY CURRENT vs. INPUT VOLTAGE (4MHz FPWM WITH FREQUENCY SCALING)



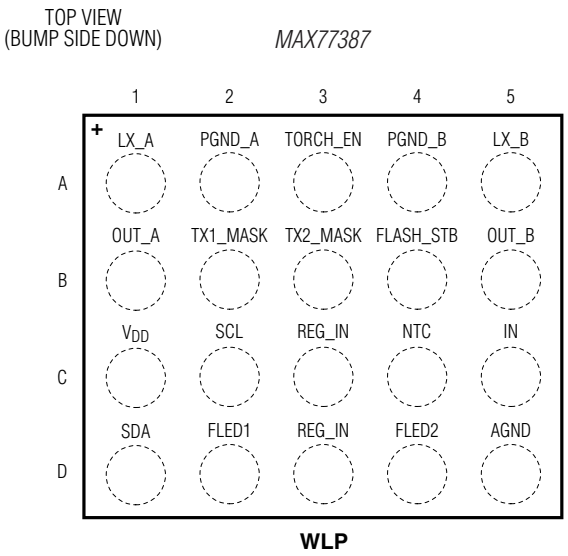
SUPPLY CURRENT vs. TEMPERATURE (4MHz, FREQUENCY SCALING, SKIP ALLOWED)



SUPPLY CURRENT vs. TEMPERATURE (2MHz FPWM, 4MHz FPWM)



Bump Configuration



WLP

Bump Description

PIN	NAME	FUNCTION
A1	LX_A	Inductor Connection for Phase A. Connect LX_A to the switched side of the inductor and to the phase A synchronous rectifier. LX_A is internally connected to the drain of the internal low-side MOSFET.
A2	PGND_A	Power Ground for DC-DC Converter Phase A. Connect to PGND (A2 and A4 together) as close as possible to the IC. Make a star connection between input and output capacitors to ensure a short ground loop. Connect to the common ground plane of the application.
A3	TORCH_EN	Logic Input. Used to enable torch/flash mode (I^2C programmable). TORCH_EN input has an optional 800kΩ pulldown resistor to AGND.
A4	PGND_B	Power Ground for DC-DC Converter Phase B. Connect to PGND (A2 and A4 together) as close as possible to the IC. Make a star connection between input and output capacitors to ensure a short ground loop. Connect to the common ground plane of the application.
A5	LX_B	Inductor Connection for Phase B. Connect LX_B to the switched side of the inductor and to the phase B synchronous rectifier. LX_B is internally connected to the drain of the internal low-side MOSFET.

Pin Description (continued)

PIN	NAME	FUNCTION
B1	OUT_A	DC-DC Step-Up Converter Output Voltage for Phase A. Bypass this output using a ceramic capacitor. See the *Output Capacitor Selection* section. Ensure that (B1) is directly connected to the output capacitor and not to the REG_IN bumps (C3 or D3). This ensures lowest output ripple current of the FLED current regulators. During shutdown OUT_A is high impedance.
B2	TX1_MASK	Logic Input. TX1_MASK input has an optional 800kΩ pulldown resistor to AGND.
B3	TX2_MASK	Logic Input. TX2_MASK input has an optional 800kΩ pulldown resistor to AGND.
B4	FLASH_STB	Logic Input. Used to enable flash/torch mode (I^2C programmable). FLASH_STB input has an optional 800kΩ pulldown resistor to AGND.
B5	OUT_B	DC-DC Step-Up Converter Output Voltage for Phase B. Bypass this output using a ceramic capacitor. See the *Output Capacitor Selection* section. Ensure that (B5) is directly connected to the output capacitor and not to the REG_IN bumps (C3 or D3). This ensures the lowest output ripple current of the FLED current regulators. During shutdown OUT_B is high impedance.
C1	V_{DD}	Voltage for SDA/SCL Logic Levels. The I^2C registers are reset when V_{DD} is low.
C2	SCL	I^2C Clock Input. Data is read on the rising edge of SCL.
C3, D3	REG_IN	Input Supply for Current Regulators. Connect directly to the output capacitors. Make sure not to share the trace between OUT_ and the capacitor since this results in increased output ripple current on the LED output.
C4	NTC	NTC Bias Output. NTC provides 200µA to bias the NTC thermistor. The NTC voltage is compared to the trip threshold programmed by the NTC_CNTL register. NTC is high impedance during shutdown. Connect NTC to IN if not used.
C5	IN	Input supply. Connect input bypass capacitor close to this input and AGND. This input is used for low noise supply for internal bias as well as for the MAXFLASH function.
D1	SDA	I^2C Data Input. Data is read on the rising edge of SCL and data is clocked out on the falling edge of SCL.
D2	FLED1	Flash LED1. High-side current regulator output. Current flowing out of FLED1 is based on I^2C register settings. Connect FLED1 to the anode of a flash LED or LED module. Optionally connect FLED1 and FLED2 together for driving a single LED module. Connect FLED1 to REG_IN if not used. FLED1 is high impedance during shutdown.
D4	FLED2	Flash LED2. High-side current regulator output. Current flowing out of FLED2 is based on I^2C register settings. Connect FLED2 to the anode of a flash LED or LED module. Optionally connect FLED1 and FLED2 together for driving a single LED module. Connect FLED2 to REG_IN if not used. FLED2 is high impedance during shutdown.
D5	AGND	Analog Ground. Connect to common ground plane of the application.

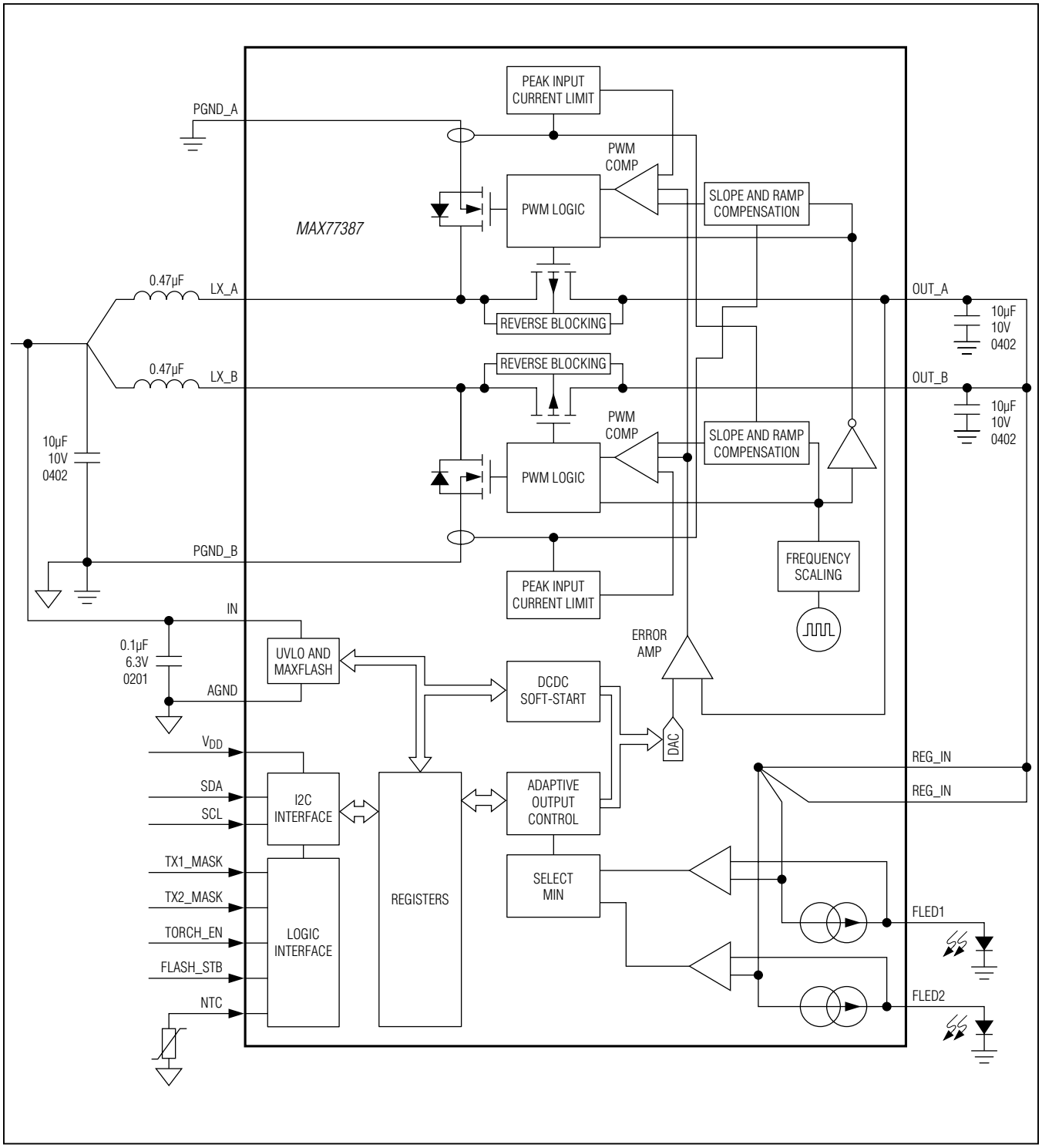


Figure 1. Detailed Block Diagram and Typical Application Circuit

Detailed Description

The MAX77387 flash driver IC integrates a dual-phase 2.0A adaptive PWM step-up DC-DC converter and two high-side 1A current regulators for LED camera flash and torch applications. All aspects of the device for torch and flash can be controlled through an I²C interface.

Modes of Operation

The IC has five modes of operation. See Figure 2.

Shutdown Mode

In shutdown mode, only the V_{DD} input is active.

The IC enters shutdown mode when V_{DD} is reduced below the V_{DD_UVLO}. When the IC enters shutdown mode, all I²C registers are reset.

If V_{DD} increases above the V_{DD_UVLO} threshold, the IC exits shutdown mode and enters standby mode.

Standby Mode

In standby mode, the I²C interface is active and trigger inputs are also active if defined by I²C register (TORCH_EN and FLASH_STB).

The IC enters standby mode from active mode when the DC-DC converter is disabled or in the case where the input voltage is below the IN_UVLO.

If the current regulators are enabled (torch or flash mode) or the DC-DC converter is enabled (in either normal mode, dropout mode), then the IC enters active mode. The input voltage must also be above IN_UVLO for the transition from standby to active mode to occur. If the IN is below the IN_UVLO, the IC remains in standby mode.

Active Mode

In active mode, the DC-DC converter is enabled and operating in the boost mode set by the DCDC_MODE bits. The current regulators are disabled.

While in active mode, if either current regulator is enabled, then the IC enters torch or flash mode.

Torch Mode

In torch mode, the current regulator is enabled according to the torch settings.

The IC continues to operate in torch mode when the torch current regulator is enabled and the flash current regulator is not enabled.

If flash mode is enabled for a current regulator, that regulator mode enters flash mode since flash mode has a higher priority.

If the current regulator is disabled, then the IC returns to active mode.

Flash Mode

In flash mode, the current regulator is enabled according to the flash settings.

Once the flash event ends, the IC can either enter torch mode or active mode depending on the torch settings.

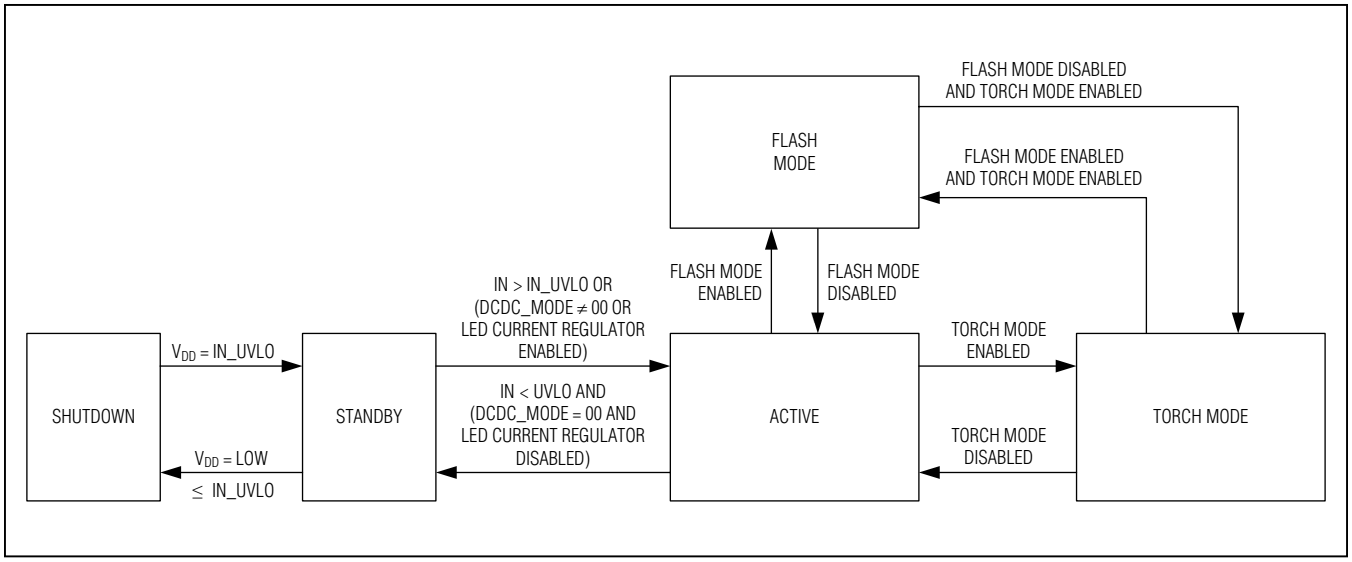


Figure 2. Modes of Operation

Adaptive Output Voltage Regulation

The IC uses an adaptive voltage scheme to optimize system efficiency based on the forward voltage of the populated LED. To ensure that the DC-DC converter is operating in a stable condition and that the current regulators are providing the correct output current levels, the voltages across the current regulators are sampled to determine whether the output voltage of the DC-DC converter needs to be increased or decreased.

The adaptive control loop controls an internal 9-bit DAC that sets the output voltage of the DC-DC converter. During a torch or flash event, the DC-DC converter continuously adapts its output voltage up or down by one DAC LSB (VADPT_REG_STEP) every 1µs during soft-start, and every 8µs during normal operation.

During the torch or flash event, the DC-DC converter output voltage is logged and then stored in both the DCDC_OUT and DCDC_OUT_MAX registers.

The DCDC_OUT register is used to store the value of the DC-DC converter output voltage just before the current regulator is disabled. The DCDC_OUT_MAX register is used to store the maximum value of the DC-DC converter output voltage that occurred during the torch or flash event. The information stored in these two registers allows the user to predict the forward voltage of the LED for diagnostics.

In certain cases, the adaptive control loop operation is limited. During minimum duty cycle operation, the DC-DC converter output voltage is only allowed to increase to ensure correct operation. During the time when the DC-DC converter is operating at the peak input current limit, the DC-DC converter output voltage is only allowed to decrease since increasing the output voltage would require a greater input current than is allowed.

If the adaptive control loop attempts to increase the DC-DC converter output voltage above the OVP_D voltage level, then the output voltage is maintained at this level for the duration of the OVP_D debounce time. If the adaptive control loop continues to attempt to increase the output voltage above the OVP_D voltage level after the OVP_D debounce timer expires, then this is an indication that the LED forward voltage is too high for the IC or the LED is not correctly installed.

Current Regulator Voltage Headroom

The current regulator headroom is selectable between +120mV to +210mV in 30mV steps. This allows the user to optimize for either efficiency or accuracy.

Lowering the voltage headroom of the current regulator reduces the accuracy and the PSRR of the current regulator while improving the system efficiency.

Increasing the voltage headroom of the current regulator improves the accuracy and the PSRR of the current regulator while reducing the system efficiency.

Step-Up Converter

The IC includes a dual-phase PWM step-up converter that supplies power to the flash LEDs. The output voltage can be adaptively controlled based on the forward voltage of the installed LEDs. The step-up converter switches an internal power MOSFET at frequencies up to 4MHz (per phase), resulting in a maximum output ripple frequency of 8MHz, with a duty cycle that can vary from 3.125% to 75% to maintain constant output voltage as V_{IN} and load vary. Internal circuitry prevents any unwanted subharmonic switching by forcing a minimum duty-cycle. Alternatively, the converter can be programmed to enter skip mode for light load conditions to ensure high efficiency for low output current operation.

Dual-Phase Operation

The advantage of the IC dual-phase control architecture is that the effective switching frequency is doubled. This provides a significant reduction in the output voltage ripple, hence reducing stress on the output capacitor. Lowering the output voltage ripple also lowers the output current ripple of the current regulator, resulting in lower EMI for the system.

For high-current applications such as LED flash, the dual phase scheme also helps reduce the inductor size. For example, a traditional single-phase architecture requiring an input current of 3A and an inductor saturation current of 3A would require and inductor sized approximately 5mm x 5mm with a height of 1mm. By going to a dual-phase architecture the 5x5mm inductor can be replaced by two 1.8mm x 1.0mm inductors to significantly reduce the total solution size. In addition, the second advantage is inductor saturation current (per phase) could be lowered to 1.8A.

Skip Mode

In PWM operation, the DC-DC converter switches cycles continuously. When SKIP mode is enabled, the DC-DC converter can disable a switching cycle if the output voltage is sufficiently high. When this condition is detected, the next switching cycle is skipped. The peak inductor current value is chosen to be high enough so that sufficient energy is transferred to the output in a burst of

switching-cycles that occur less frequently to improve the overall efficiency. However, the output voltage ripple in this mode increases.

Noise-sensitive applications that cannot tolerate the increased output voltage ripple can disable skip mode to force continuous PWM operation. See the DCDC_CNTL2 register.

Current Sharing

For multiphase converters one of the critical parameters is current sharing. If good balance between the phases is not ensured, then one phase could potentially be forced to handle a disproportionate amount of the total output current, resulting in overheating and loss of efficiency.

The IC uses a common peak current mode control scheme that inherently provides current balancing between the phases.

Switching Frequency Selection

The DC-DC converter can be programmed to operate at several different fixed switching frequencies. Alternatively, the DC-DC converter can be programmed to automatically select the optimal switching frequency based on the operating duty cycle. Optimized frequency selection allows the DC-DC converter to operate at the highest available switching frequency for the lowest required duty cycle. See the DCDC_CNTL2 register.

Overvoltage Protection

The IC provides two overvoltage protection mechanisms. The primary protection mechanism (OVP_D), which is part of the adaptive regulation control, limits the DCDC converter output voltage to the OVP_D threshold for a time duration of t_{OVP_D} before the DC-DC converter and current regulators are disabled.

A secondary protection mechanism (OVP_A) limits the DC-DC converter output voltage to the OVP_A threshold that is set higher than the OVP_D threshold, but has a much reduced time duration. If the DC-DC converter output voltage rises above the OVP_A threshold, the DC-DC converter and current regulators are disabled with minimum time delay.

True Shutdown

When the IC is in standby mode, the DC-DC converter is disabled where both the high side and low side switches are turned off. In addition, the high-side switch's rectifier is reversed biased putting the DC-DC converter output into a high-impedance state, allowing the output to discharge to ground.

Soft-Start

When the input supply is initially applied to the IC, the output is in true shutdown mode, meaning that the output DC-DC converter remains at high impedance. Upon entering active mode the following steps are implemented to ensure a controlled soft-starting of the DC-DC converter output.

The soft-start steps are:

1) Precharge

   When entering precharge, the output voltage is unknown since it was in high impedance. If the high-side switch is simply forced on, this can result in a large inrush of current. To avoid this, the high-side switch switches at a 25% duty cycle resulting in a controlled precharge of the output.

   The precharge is completed once the output voltage reaches V_{IN} - 300mV.

   If the load on the output exceeds 10mA while precharging, the DC-DC converter remains in precharge mode and the output is unable to reach V_{IN} - 300mV.

2) Ramping of the output voltage

   In this mode, the output is ramped to DCDC_SS level. The output is ramped at a rate of 1LSB per 1µs, resulting in 6.25mV/µs ramp rate.

For DCDC_MODE = 00 (low-power adaptive mode), the output does not soft-start before the trigger event. When a torch or flash event is triggered the DC-DC converter first performs step 1, followed by step 2. After the DC-DC converter output is ramped to the DCDC_SS level, the current regulator is then ramped according to the programmed ramp values.

For DCDC_MODE = 01 (prebiased adaptive mode), when setting this mode, the DC-DC converter first performs step 1, followed by step 2. Once step 2 is completed the DC-DC converter continues to regulate the output at DCDC_SS level.

Once a torch or flash event is triggered, the current regulator is enabled with minimum delay since the output is already precharged. The output current ramps according to the programmed ramp values. Once the current regulator is disabled the output continues to regulate at the DCDC_OUT level. Upon a new torch or flash event the output continues from this DCDC_OUT level.

For DCDC_MODE = 10 (fixed voltage mode), when setting this mode, the DC-DC converter first performs step 1, followed by step 2. Once step 2 is completed the DC-DC converter continues to regulate the output at the DCDC_SS level, regardless of status of torch and flash modes.

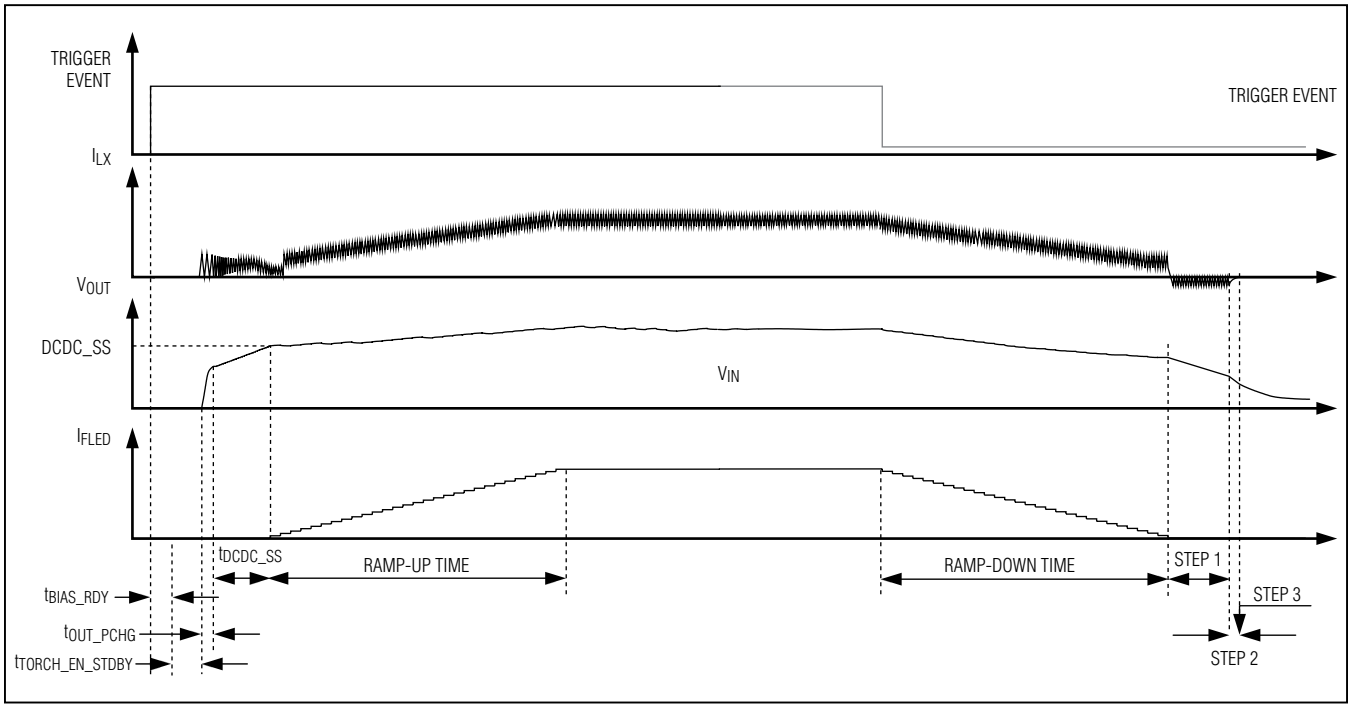


Figure 3. DC-DC Converter Soft-Start for DCDC_MODE = 00

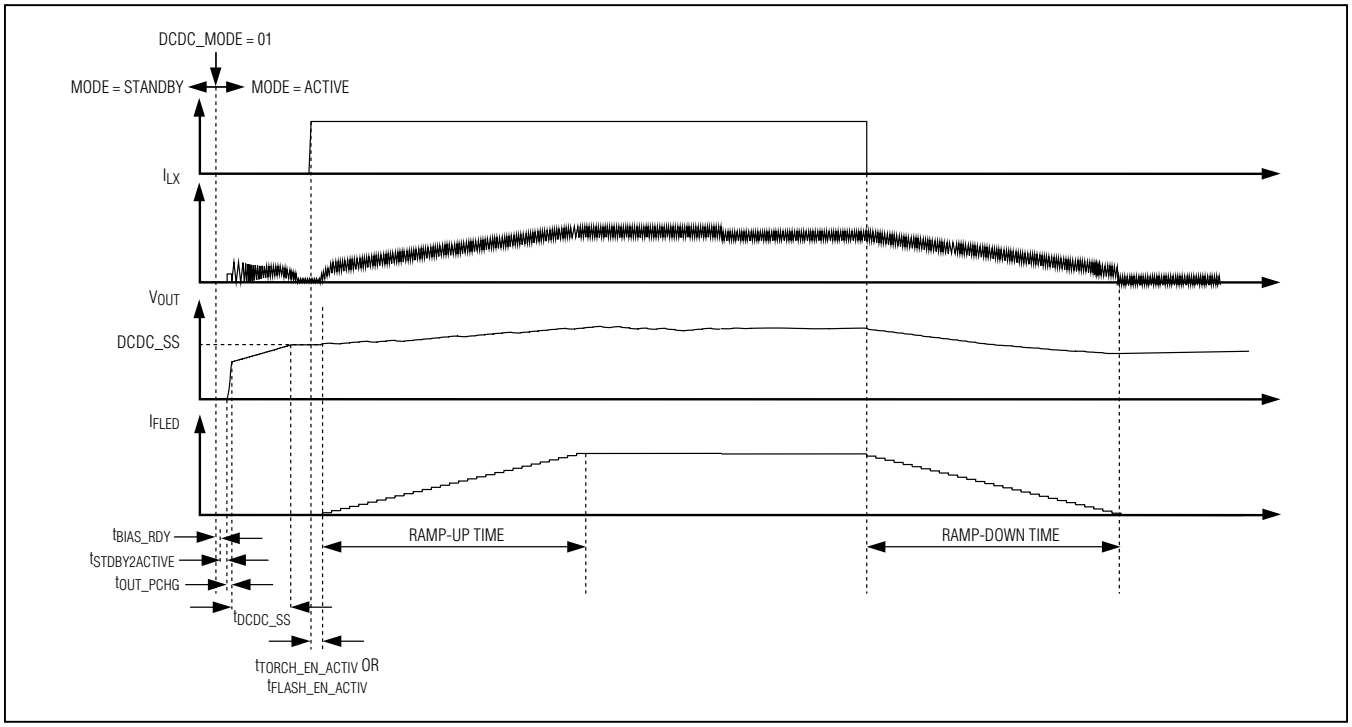


Figure 4. DC-DC Converter Soft-Start for DCDC_MODE = 01

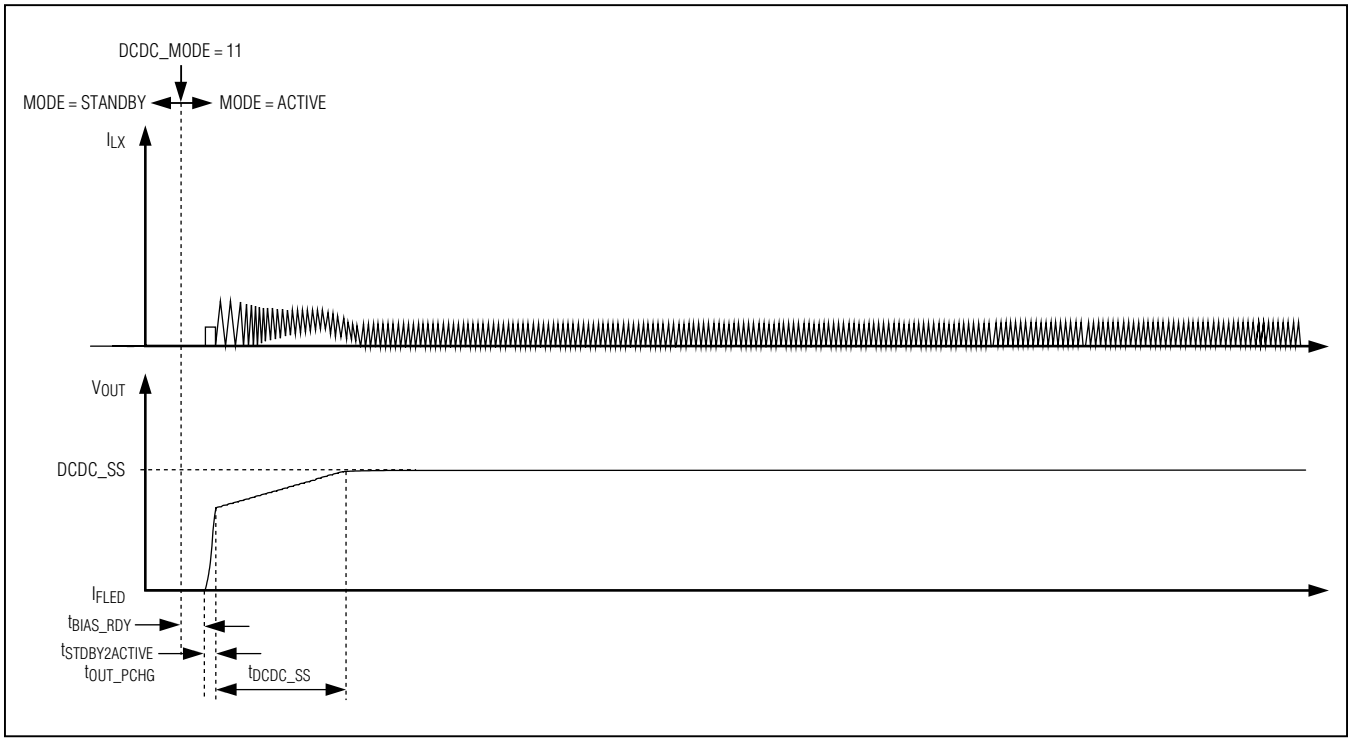


Figure 5 DC-DC Converter Soft-Start for DCDC_MODE = 10

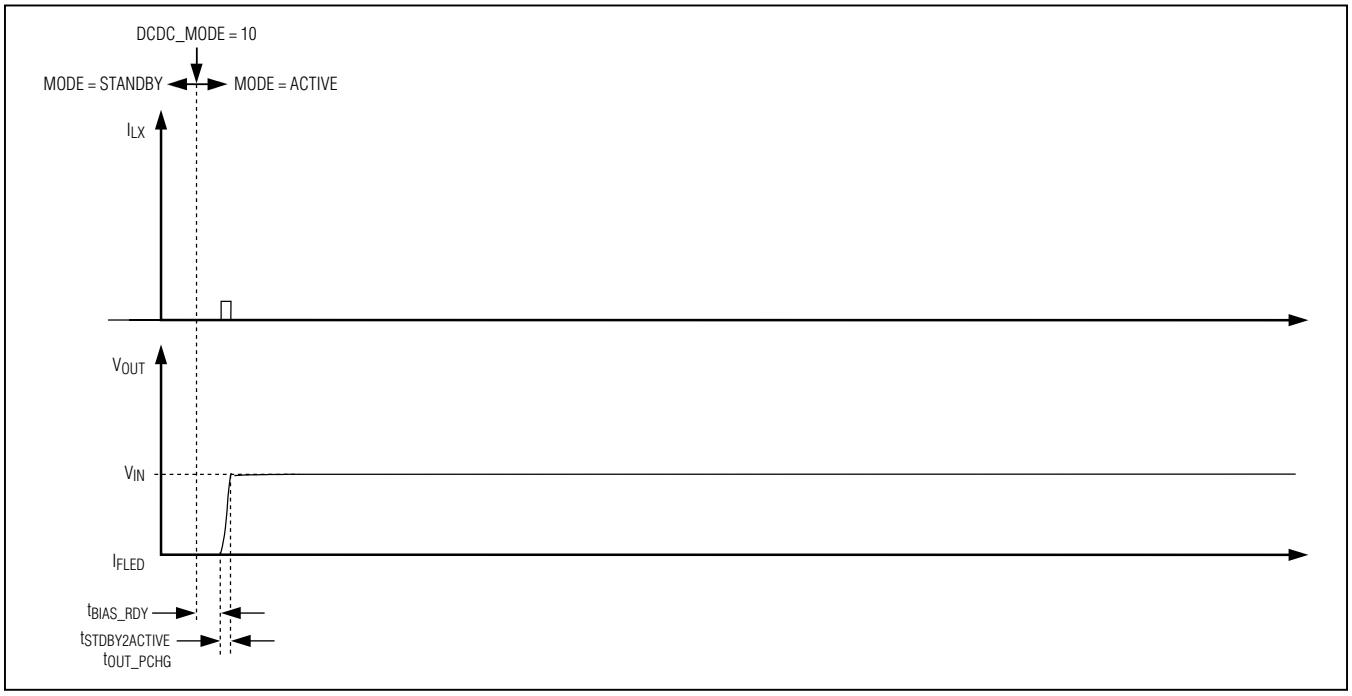


Figure 6. DC-DC Converter Soft-Start for DCDC_MODE = 11

For DCDC_MODE = 11 (dropout mode), when setting this mode, the DC-DC converter first performs step 1, after which, the high-side switch is turned on 100%, regardless of the status of torch and flash modes.

The time it takes from triggering torch or flash mode until the current is at final value depends on the following conditions:

- If the time spent in standby mode is shorter than the internal bias, t_{BIAS_RDY}, then the bias needs to come up before anything happens.
- The time duration of the soft-start is dependent on the input voltage and initial charge of the output capacitor, t_{OUT_PCHG}.
- The higher the programmed voltage level results in a longer start time (t_{DCDC_SS}). The output is ramped at a rate of 1LSB per 1µs, resulting in a 6.25mV/µs ramp rate.
- The regulator output current is ramped according to the programmed ramp rate in flash or torch mode. Therefore, the final value of the output current impacts the time duration it takes to ramp the current from 0mA to the final value.

End of Trigger Event

When the DC-DC converter is disabled, the setting of the DCDC_MODE determines the method to discharge the output.

The discharge steps are:

1) The DC-DC converter continues switching the high-side switch at 25% duty cycle allowing for the output to be a controlled discharge. During this step, the energy in the output capacitor is gradually transferred from the output capacitor back to the input capacitor, ensuring that the energy is conserved. Step 1 is completed once the output voltage reaches V_{IN} + 200mV.
2) The DC-DC converter high-side switch goes from 25% switching to 100% (dropout mode). This allows the output to be discharged to within V_{IN} + 150mV.
3) The DC-DC converter transitions from operating in dropout mode to true shutdown mode. In true shutdown mode, the output is high impedance.

For DCDC_MODE = 00, the DCDC converter goes through all three steps listed above. This ensures that the output is discharged to within V_{IN} +150mV.

For DCDC_MODE = 01, 10, or 11, the DC-DC converter is not disabled therefore the output is not discharged. To disable the DC-DC converter, set DCDC_MODE = 00.

The following describes the end of trigger event when coming from the different modes 01, 10, or 11 to 00.

Coming from DCDC_MODE = 01 or 10 to 00, the DC-DC converter goes through all three steps listed above. This ensures that the output is discharged to within V_{IN} + 150mV.

Coming from DCDC_MODE = 11 to 00, the DC-DC converter enters true shutdown mode since the output is equal or lower than the input voltage.

Gain Selection

The gain of the error amplifier of the DC-DC converter determines the load regulation performance as well as setting the minimum output capacitor value required for stable regulation. Lowering the gain results in larger load regulation and a decreased output capacitor value requirement.

The following DCDC_GAIN settings are available:

- DCDC_GAIN = 0 sets the lowest gain.
- DCDC_GAIN = 1 sets the highest gain.

For output capacitor values, see the *Output Capacitor Selection* section.

Low-Side Current Limit

The IC provides a programmable current limit for the low-side switch. This current limit functions as an input current limit, and is critical for the application since this is the function that determines the maximum current that can be drawn from the input supply. The low side current limit is also important for the choice of inductor since this determines the minimum saturation current.

If the input current limit is reached during operation, the low-side switch terminates the cycle and turns on the high-side switch. When minimum t_{ON} condition is reached the duty cycle is limited and the LX peak current might exceed the current limit setting slightly. This results in a drop of the output voltage. The DC-DC converter can operate in continuous input current limit condition. However, due to the drop in output voltage the current regulator parameters cannot be guaranteed in this mode of operation.

Current Regulator LED

The IC has two high-side regulators that can be used for torch and flash modes with the settings:

- Flash mode from 15.625mA to 2000mA (1000mA for each current regulator) in 15.625mA steps total

- Torch mode with DAC mode enabled from 3.91mA to 500mA (250mA for each current regulator) in 3.91mA steps total
- Torch mode with PWM mode enabled from 125mA to 1000mA in 125mA steps for PWM dimming with programmable duty cycle from 3.125% to 25% in 3.125% steps.

The regulator sources current out of the FLED output, and is always powered from REG_IN.

If both torch and flash are enabled for LED current regulator, flash mode always has the highest priority.

Each current setting is controlled by I²C interface.

For applications requiring higher output current, the two current regulators can be connected in parallel, doubling the output current capability. The total current flowing though the LED is the sum of the programmed FLED1 and FLED2 current. The ramp rate is doubled compared to the dual LED application. If one of the LED current levels is set higher than the other the ramp rate, decrease to 1x as soon as the lower LED current regulator has completed its ramp function. It is therefore recommended that the current settings for FLED1 and FLED2 are set to the same rate of maximum of 1LSB in difference. It is not recommended to use PWM dimming when FLED1 and FLED2 are connected since the LED current regulators are not synchronized together.

When FLED1 and FLED2 are connected together, the adaptive control monitors the voltage headroom for each of the current regulators. Since the two FLED pins are connected together, the required output voltage of the FLED1/FLED2 is the same. The adaptive control scheme regulates the voltage across the current regulator to be the preset value. In this case, the required V_{OUT} for FLED1 and FLED2 are the same.

DAC and PWM Dimming

Dimming control of the current regulators can be achieved using DAC control, PWM control or a combination of both.

DAC Control

When DAC control is used, the current regulators are set to a constant preprogrammed value.

PWM Control

When PWM control is used, the current regulators are enabled/disabled at a predetermined frequency, FREQ_PWM[1:0]. The ratio between the on and off times determines the percentage of full-scale current that each current regulator outputs.

Using PWM dimming with high frequency and low duty cycle increases the output error due to rise and fall time and becomes a significant part of the total on time. It is therefore not recommended to operate at high frequency and low duty cycle.

DAC and PWM Control

DAC and PWM control can be used at the same time. For example, in torch mode the full-scale current can be set with the DAC, and then PWM control used to establish a much lower average current. Typically, this is done to eliminate the color shift seen when using a high-current LED at a low DC current setting.

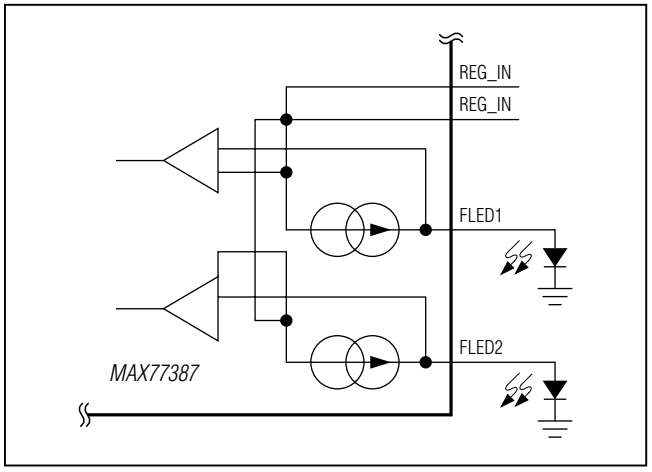


Figure 7. Driving Two LED Configuration

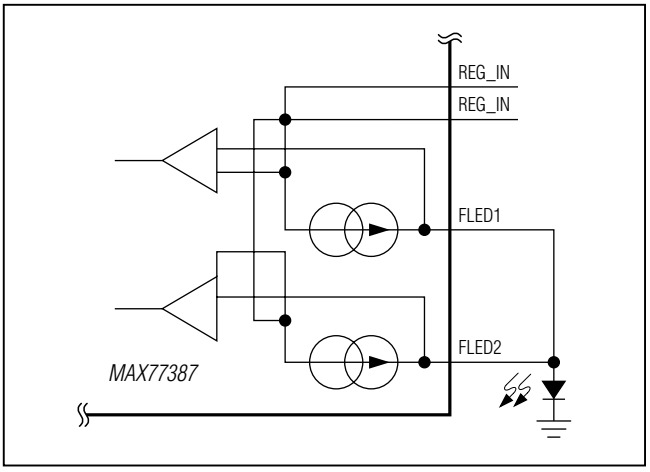


Figure 8. Driving a Single LED Configuration

Ramp Control

Each current regulator has a ramp function that is engaged every time the current regulator is enabled/disabled or the output current level is changed. This is done to control the EMI of the current regulator output.

The ramping of the current regulator is done by ramping one LSB step of the current regulator per the internal clock, providing a staircase ramp of the output current.

For flash mode, the output current increases in 15.625mA steps from 15.625mA until the final value.

For torch mode the output current increases in 3.91mA steps from 3.91mA until final value.

The actual time used for ramping up and down are determined by the following equations.

For flash mode:

$$t_{FLASH_UP} = \frac{FLASH_RU}{IFLASH_MAX}(IFLASH)$$

$$t_{FLASH_DOWN} = \frac{FLASH_RD}{IFLASH_MAX}(IFLASH)$$

where:

FLASH_RU is the total ramp-up time.

FLASH_RD is the total ramp-down time.

I_{FLASH} is the programmed flash current.

I_{FLASH_MAX} is the maximum programmable flash current (1000mA).

For torch mode in DAC mode:

$$t_{TORCH_DAC_UP} = \frac{TORCH_RU}{ITORCH_DAC_MAX}(ITORCH_DAC)$$

$$t_{TORCH_DAC_DOWN} = \frac{TORCH_RD}{ITORCH_DAC_MAX}(ITORCH_DAC)$$

where:

TORCH_RU is the total ramp-up time.

TORCH_RD is the total ramp-down time.

I_{TORCH_DAC} is the programmed DAC mode torch current.

$I_{TORCH_DAC_MAX}$ is the maximum programmable DAC mode torch current (250mA).

For torch mode in PWM mode:

$$t_{TORCH_PWM_UP} = \frac{TORCH_RU}{ITORCH_PWM_MAX}(ITORCH_PWM)$$

$$t_{TORCH__PWM_DOWN} = \frac{TORCH_RD}{ITORCH_PWM_MAX}(ITORCH_PWM)$$

where:

TORCH_RU is the total ramp-up time.

TORCH_RD is the total ramp-down time.

I_{TORCH_PWM} is the programmed PWM mode torch current.

$I_{TORCH_PWM_MAX}$ is the maximum programmable PWM mode torch current (1000mA).

Torch and Flash Safety Timer

The torch/flash safety timers are activated any time torch/flash mode is respectively enabled.

The torch safety timer, programmable from 122.9ms to 22s through I²C, limits the duration of the torch mode in case the torch mode is not disabled through logic control or I²C within the programmed torch safety timer duration.

The flash safety timer, programmable from 0.256msec to 699.392ms through I²C, limits the duration of the flash mode in case the flash is not disabled through logic control or I²C within the programmed flash safety timer duration.

The flash mode timers operate in either one-shot time mode or maximum duration timer mode or PWM timer mode.

The torch mode timers operate only in one-shot time mode. There is a torch mode register setting to disable the timer potentially allowing for indefinite torch mode duration. See Figure 11. See the TORCH_TMR_CNTL[7] register. In maximum flash mode, the trigger input is level triggered, and the timer is only ensuring that the maximum duration of the flash is limited to the preprogrammed threshold.

Time duration includes current ramp-up time, but not ramp down time.

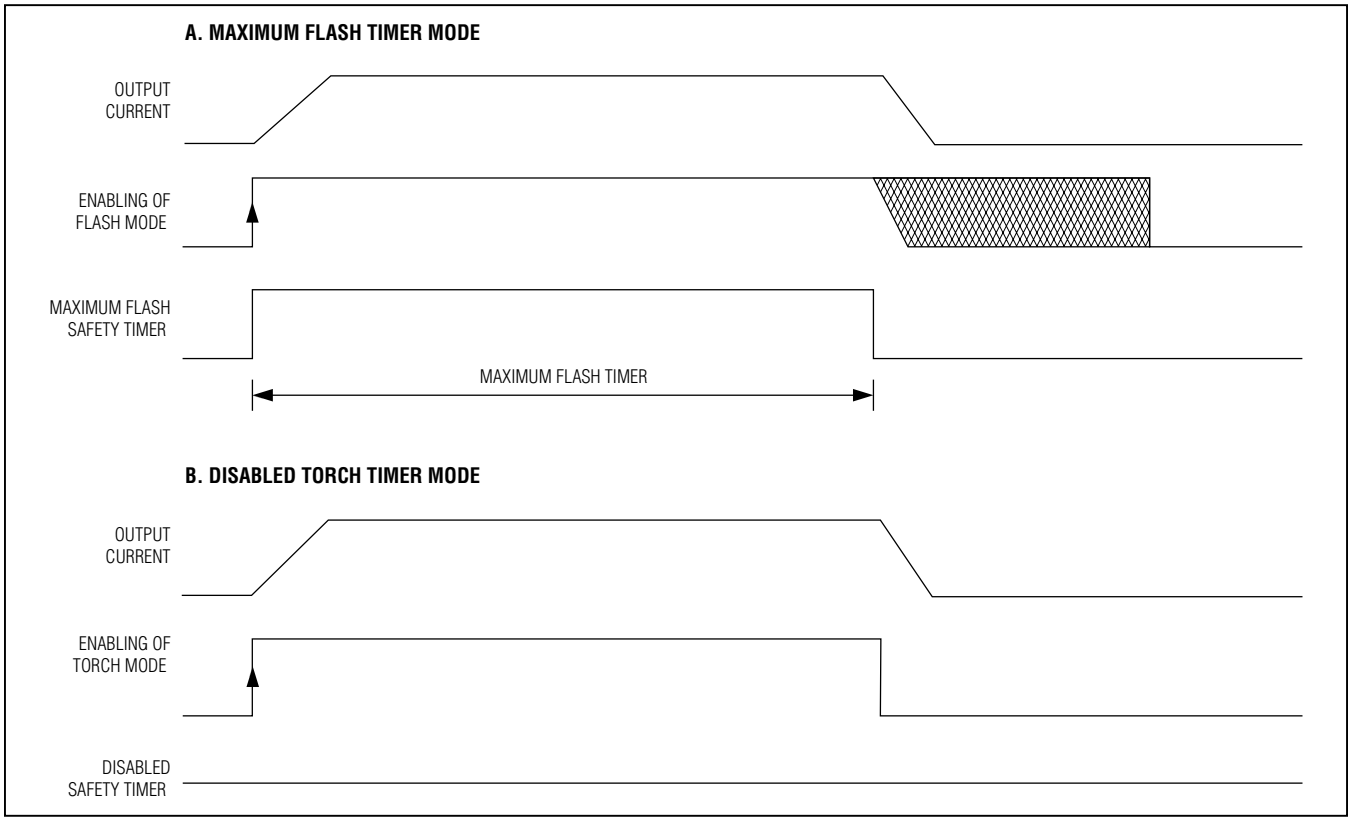


Figure 9. Maximum Flash Timer Mode/Disabled Torch Timer Mode

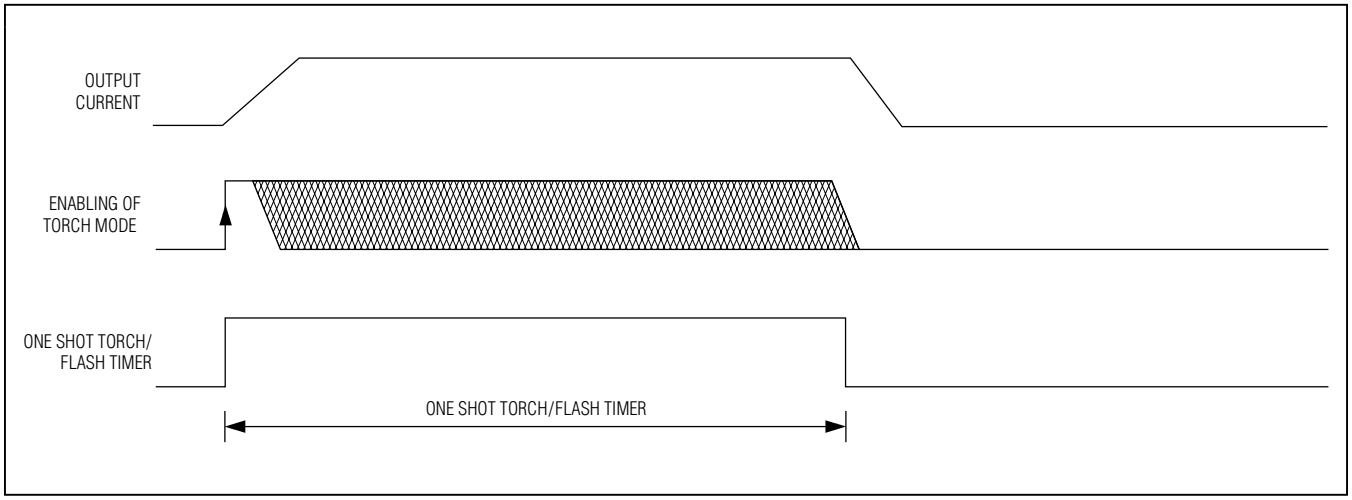


Figure 10. One-Shot Torch/Flash Timer Mode

MAXFLASH Function

During high load currents on a battery cell, the battery voltage momentarily drops due to internal ESR of the battery in series with impedance between the battery and the load.

For equipment requiring a minimum voltage for stable operation, the ESR of the battery needs to be calculated to estimate the maximum current that can be drawn from the battery without making the cell voltage drop below this critical minimum system voltage level.

If the system is not able to accurately predict the true ESR and impedance of the system, the minimum operational battery voltage has to be increased to guard band for tolerances and operating conditions.

In addition, a smartphone includes multiple applications that are operating asynchronously with the camera flash application. Therefore, it is difficult to predict the load current on the battery at any given time that would require additional guard banding of the battery voltage to insure that a sufficient system voltage is provided during worst case conditions.

The MAXFLASH 2.0 function eliminates the requirement for predicting the battery voltage during flash events. The MAXFLASH 2.0 monitors the input voltage while comparing it against a user defined voltage threshold. If the input voltage drops below this user defined threshold, referred to as MAXFLASH_TH, the current regulator output current is reduced by one step. After a given time, referred to as LB_TMR_F, the input voltage is compared against the MAXFLASH_TH threshold again. If the input voltage is still below the MAXFLASH_TH threshold, the current regulator output current is once again reduced by one step to ensure that the minimum operational voltage is available for the rest of the system. However, if the input voltage is near the MAXFLASH_TH threshold plus a user defined hysteresis, referred to as MAXFLASH_HYS, the current regulator output current is increased by one step, but only if the current regulator out¬put current is less than the user defined output current setting. In the event that MAXFLASH_HYS is set to 000, the flash current can only be reduced as a result of a low system battery voltage regardless of whether or not the system voltage recovers. This continues for the entire duration of the flash/torch event, ensuring that the current regulator output current is always maximized for the specific operational conditions.

If the MAXFLASH 2.0 function is triggered during a torch or flash event, the MAXFLASH bit in the STATUS2 register is set. In the case of a MAXFLASH event, the MAX77387 logs the lowest current setting reached for each current regulator during the torch or flash event. This information is stored in both the MAXFLASH3 and MAXFLASH4 registers. This information can be used to determine whether the reduction in LED light has been sufficient or if the picture quality has been compromised.

TX_MASK

In the typical application there are several other applications that can draw large peak currents from the battery that are also supplying the flash driver.

Since the current from the battery has to be limited to protect the battery from getting damaged, the IC has two logic inputs that can be used to limit the flash current during high current events, such as GSM Tx or WCDMA Tx.

The TX1_MASK and TX2_MASK can be used to limit the maximum current for the LED by setting the maximum allowed flash current during Tx event. If TX1_MASK and TX2_MASK are triggered at the same time, the current is limited by the TX1_MASK. Once the TX1_MASK event is no longer present, output current is limited by TX2_MASK if this event is still valid.

Once a TX_MASK event is triggered the output current is reduced within the $t_{TX_MASK_EN}$ to ensure that the current draw from the battery does not exceed the maximum allowed for the battery.

Once the TX_MASK event is no longer present the output current is ramped from the reduced value to normal flash current level according to the ramp up for flash mode.

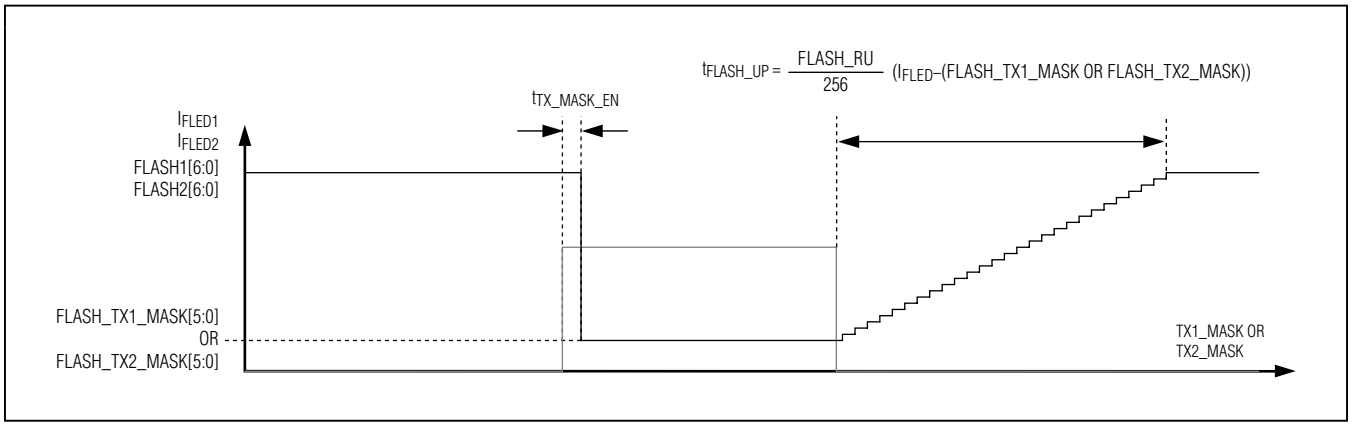


Figure 11. TX1_MASK or TX2_MASK During Flash Mode

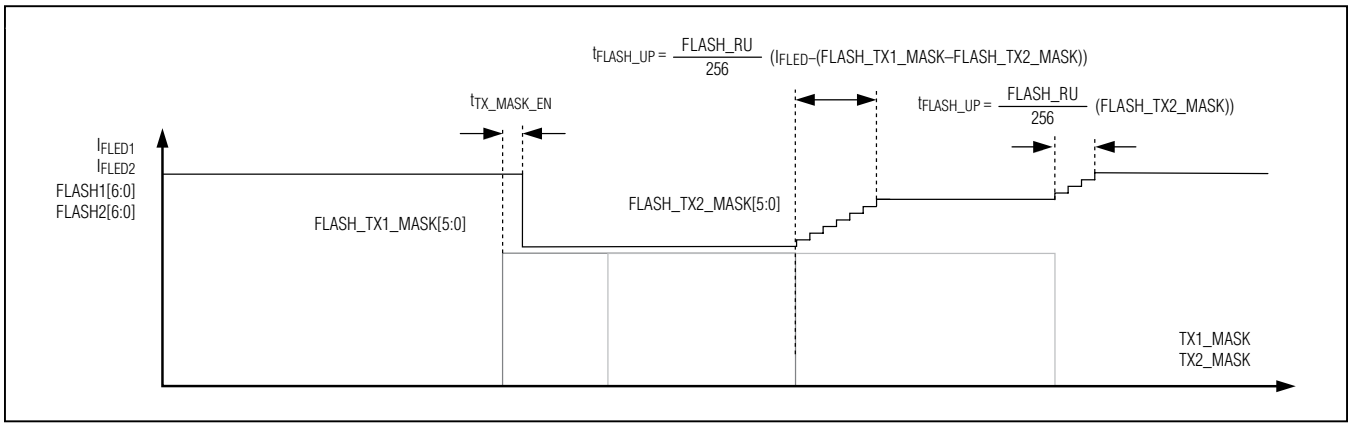


Figure 12. TX1_MASK and TX2_MASK Occurring at Same Time

NTC Control

An NTC input is provided for the (optional) finger-burn protection feature. To use this feature, connect a negative temperature thermistor (NTC) between NTC and AGND.

In flash mode, the IC sources 200µA current out of the NTC pin, and the voltage established by this current and the NTC resistance is compared internally to a voltage threshold in the range of 200mV to 550mV, programmed through bits NTC_TH_FLASH[2:0]. If the voltage on the NTC pin falls below the programmed threshold during a flash event, the flash cycle is immediately terminated, and an indication is latched into the Status 2 register. To disable this function, clear NTC_EN bit in the NTC Control registers.

In torch mode, the IC pulses a 200µA current out of the NTC pin, and the voltage established by this current and the NTC resistance is compared internally to a voltage threshold in the range of 200mV to 550mV, programmed through bits NTC_TH_TORCH[2:0]. If the voltage on the NTC pin falls below the programmed threshold during a torch event, the torch cycle is immediately terminated, and an indication is latched into the Status 2 register. To disable this function, clear NTC_EN bit in the NTC Control registers.

The NTC pulse time is defined by $t_{NTC_TORCH_ON}$ and $t_{NTC_TORCH_OFF}$. The NTC biased current is pulsed in torch mode to ensure low power dissipation of the NTC resistor as well as saving current.

Due to self-heating of the IC, the NTC bias current changes. This can be compensated for by calculating what the expected temperature is for the IC, and therefore, what the exact NTC bias current is. Doing this provides a higher accuracy for the thermal sensing:

$$T_J = T_A + \theta_{JA} x (V_{OUT} x I_{OUT} x \eta)$$

where:

T_A is the ambient temperature.

θ_{JA} is 46°C/W (determined by the package type).

V_{OUT} is the expected output voltage for given setting.

I_{OUT} is the programmed output current for the given setting.

η is the system (DCDC converter + current regulator) efficiency.

Once the T_J is calculated then the correct NTC bias current level can be calculated:

NTC_BIAS = NTC_BIAS_25C + NTC_T_COM x(Tj-25)

where:

NTC_BIAS is the output bias current for given junction temperature.

NTC_BIAS_25C is the bias current at T_A = +25°C.

NTC_T_COM is the temperature compensation factor.

Short and Open LED Detection

The IC includes a comparator that detects if the LED output is shorted. If the voltage across the LED is less than 1V, then bit[7:6] in STATUS1 is set after the debounce time expires, LED1_SHORT, LED2_SHORT. When the IC detects the short, only that current regulator is disabled.

If an LED becomes open-circuit during adaptive loop control operation, then V_{REG_IN} increases until the OVP_D threshold is reached. The OVP_D event is logged in STATUS1 after the debounce timer expires. When an OVP_D condition exists the regulator and DC-DC converter is disabled

Thermal Shutdown

Thermal shutdown limits total power dissipation in the IC. When the junction temperature exceeds +160°C (typ), the device turns off, allowing the IC to cool. See STATUS1 register.

When a thermal shutdown condition exists the regulator and DC-DC converter is disabled.

I²C Serial Interface

An I²C-compatible, 2-wire serial interface controls the step-up converter output voltage, flash and torch current settings, flash duration, and other parameters. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The IC is a slave-only device, relying upon a master to generate a clock signal. The master initiates data transfer to and from the IC and generates SCL to synchronize the data transfer (Figure 13).

I²C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to assure proper device operation. A bus master initiates communication with the IC as a slave device by issuing a START condition followed by the IC's address. The IC's address byte consists of 7 address bits and a read/write bit (R/W). After receiving the proper address, the IC issues an acknowledge bit by pulling SDA low during the ninth clock cycle.

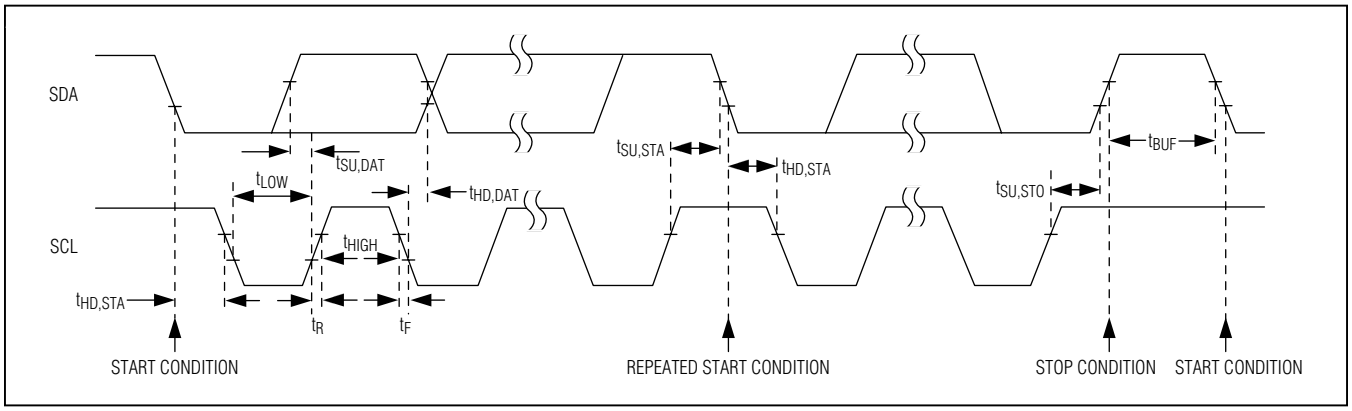


Figure 13. 2-Wire Serial Interface Timing Detail

I²C Slave Address

The IC acts as a slave transmitter/receiver. Its slave address is 0x94h for write operations and 0x95h for read operations.

I²C Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock (Figure 14).

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the IC, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 15). Both START and STOP conditions are generated by the bus master.

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data Figure 16. After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse so that the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the IC, it releases the SDA line and the IC takes the control of the SDA line and generates the acknowledge bit. When SDA remains

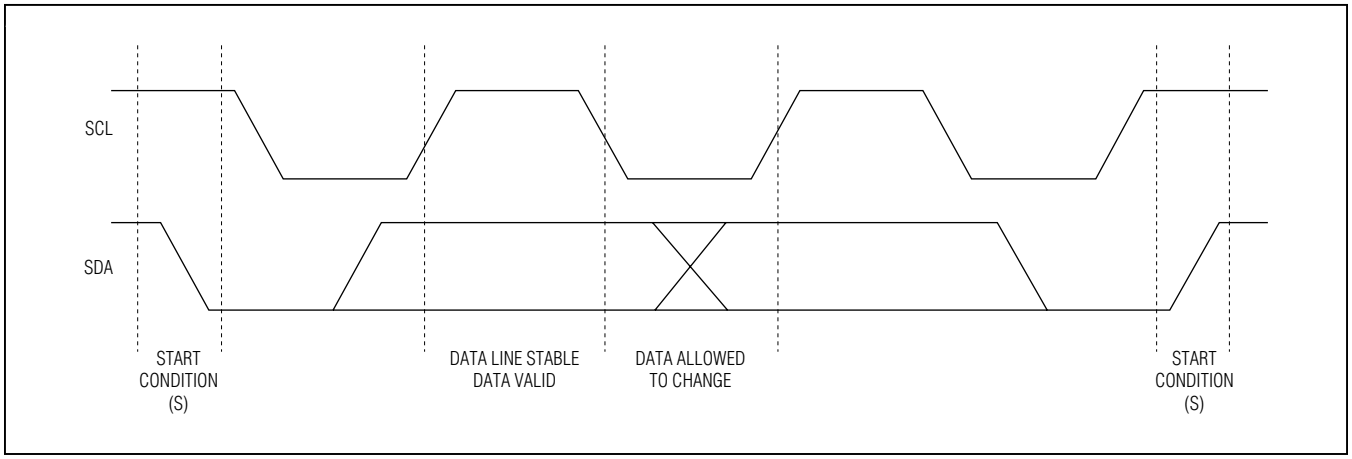


Figure 14. Bit Transfer

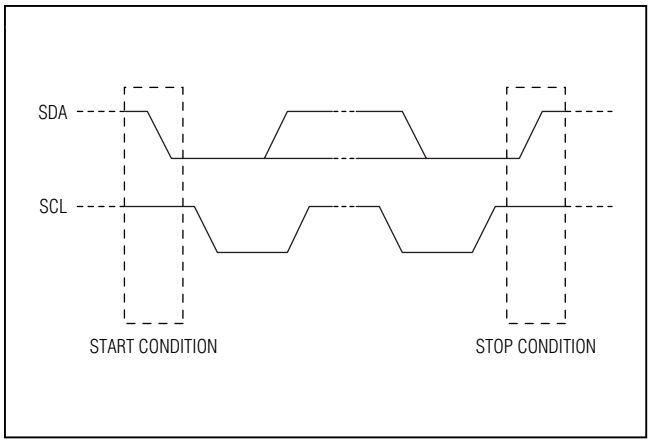


Figure 15. START and STOP Conditions

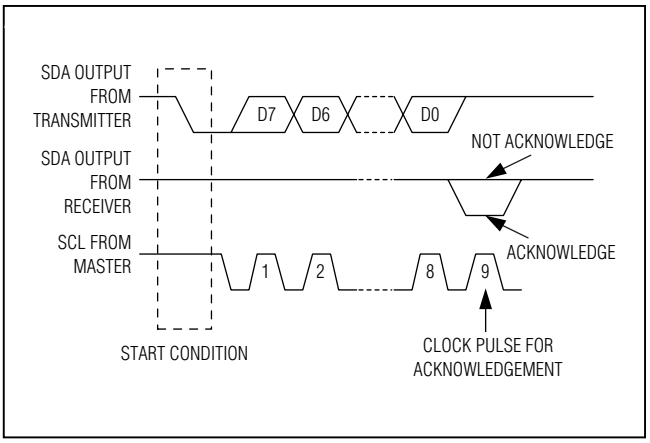


Figure 16. Acknowledge

high during this 9th clock pulse, this is defined as the not acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

Write Operations

The IC recognizes the write byte protocol as defined in the SMBus specification and shown in section A of Figure 17. The write byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write byte protocol requires a register pointer address for the subsequent write. The IC acknowledges any register pointer even though only a subset of those registers actually exists in the device.

The write byte protocol is as follows:

1. The master sends a start command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an acknowledge by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges the data byte.
9. The master sends a STOP condition.

In addition to the write-byte protocol, the IC can write to multiple registers as shown in section B of Figure 17. This protocol allows the I²C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1. The master sends a start command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an acknowledge by pulling SDA low.
4. The master sends the 8-bit register pointer of the first register to write.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges the data byte.

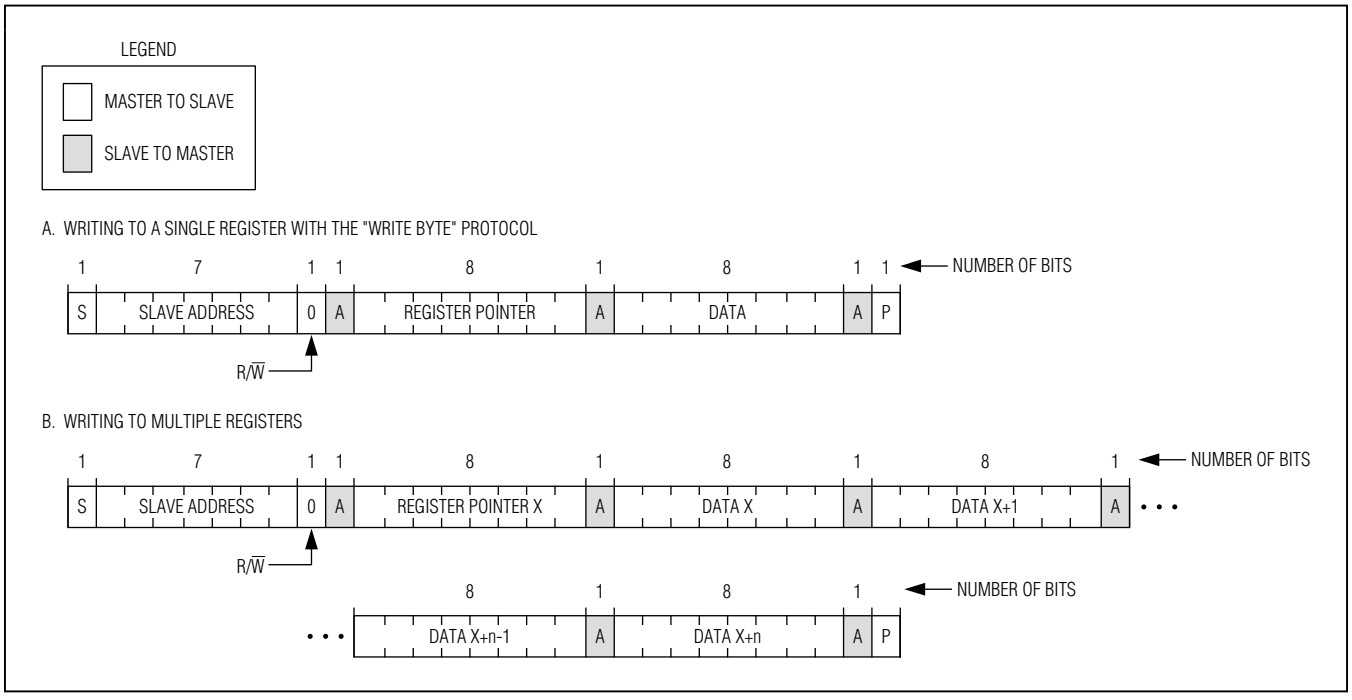


Figure 17. Write to the IC

9. Steps 6 to 8 are repeated for as many registers in the block with the register pointer automatically incremented each time.
10. The master sends a STOP condition.

Read Operations

The method for reading a single register (byte) is shown in section A of Figure 18. To read a single register:

1. The master sends a start command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an acknowledge by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated START condition.
7. The master sends the 7-bit slave address followed by a read bit.
8. The slave assets an acknowledge by pulling SDA low.
9. The slave sends the 8-bit data (contents of the register).
10. The master assets an acknowledge by pulling SDA low.
11. The master sends a STOP condition.

In addition, the IC can read a block of multiple sequential registers as shown in section B of Figure 18. Use the following procedure to read a sequential block of registers:

1. The master sends a start command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an acknowledge by pulling SDA low.
4. The master sends an 8-bit register pointer of the first register in the block.
5. The slave acknowledges the register pointer.
6. The master sends a repeated START condition.
7. The master sends the 7-bit slave address followed by a read bit.
8. The slave assets an acknowledge by pulling SDA low.
9. The slave sends the 8-bit data (contents of the register).
10. The master assets an acknowledge by pulling SDA low.
11. Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12. The master sends a STOP condition.

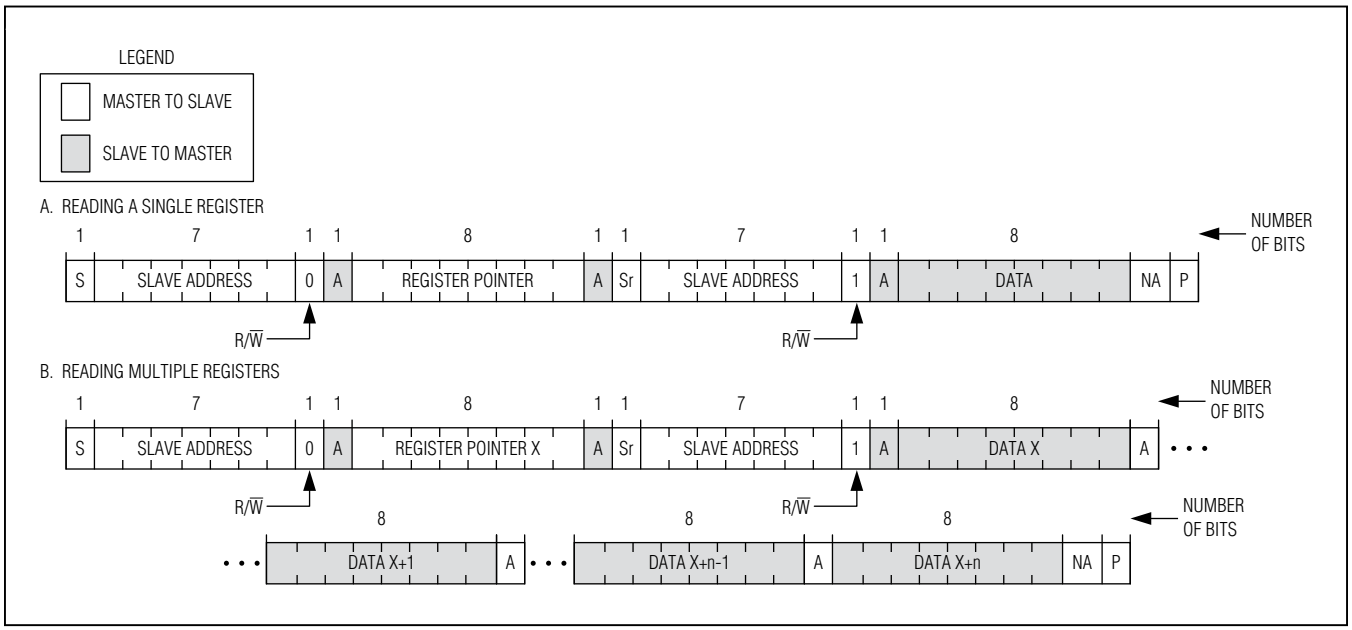


Figure 18. Read from the IC

Table 1. I²C Register Map

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x00	CHIP_ID1	DIE_TYPE[7:4]				DIE_TYPE[3:0]			
0x01	CHIP_ID2	DIE_DASH[3:0]				DIE_REV[3:0]			
0x02	STATUS1	LED1_SHORT	LED2_SHORT	REG_IN_UVLO	IN_UVLO_THERM	NTC_THERM	NTC_SHORT	OVP_A	OVP_D
0x03	STATUS2	MAXFLASH	DONE	TX1_MASK	TX2_MASK	FLASH_TMR	TORCH_TMR	ILIM	nRESET
0x04	IFLASH1	FLASH1_EN		FLASH1[5:0]					
0x05	IFLASH2	FLASH2_EN		FLASH2[5:0]					
0x06	ITORCH1	TORCH1_EN	TORCH1_5:0]						TORCH1_DIM
0x07	ITORCH2	TORCH2_EN	TORCH2_5:0]						TORCH2_DIM
0x08	MODE_SEL	TORCH_EN_PD	FLASH_STB_PD	TORCH_MODE[2:0]			FLASH_MODE[2:0]		
0x09	TX1_MASK	TX1_MASK_EN	TX1_MASK_PD	FLASH_TX1_MASK[5:0]					
0x0A	TX2_MASK	TX2_MASK_EN	TX2_MASK_PD	FLASH_TX2_MASK[5:0]					
0x0B	FLASH_RAMP_SEL		FLASH_RU[2:0]				FLASH_RD[2:0]		
0x0C	TORCH_RAMPSEL		TORCH_RU[2:0]				TORCH_RD[2:0]		
0x0D	FLASH_TMR_CNTL	FLASH_TMR_CNTL	FLASH_TMR[6:0]						
0x0E	TORCH_TMR_CNTL	TORCH_TMR_CNTL	TORCH_TMR[4:0]						
0x10	MAXFLASH1	MAXFLASH_HYS[2:0]			MAXFLASH_TH[4:0]				
0x11	MAXFLASH2	LB_TMR_R[3:0]				LB_TMR_F[3:0]			
0x12	MAXFLASH3	MAX_FLASH1_IMIN[7:0]							
0x13	MAXFLASH4	MAX_FLASH2_IMIN[7:0]							
0x14	NTC	NTC_EN	NTC_TH_FLASH[2:0]			NTC_TH_TORCH[2:0]			
0x15	DCDC_CNTL1	OVP_TH[1:0]				FREQ_PWM[1:0]		DCDC_MODE[1:0]	
0x16	DCDC_CNTL2	DCDC_ADPT_REG[1:0]		DCDC_GAIN	DCDC_OPERATION[2:0]			F_SCALE [1:0]	
0x17	DCDC_ILIM	DCDC_ILIM[1:0]			DCDC_SS[5:0]				
0x18	DCDC_OUT	DCDC_OUT[7:0]							
0x19	DCDC_OUT_MAX	DCDC_OUT_MAX[7:0]							

Table 2. CHIP_ID1

Register Name	CHIP_ID1
Address	0x00h
Reset Value	0x91
Type	Read only
Reset Conditions	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DIE_TYPE[7:4]	BCD character 9	1001
B6			
B5			
B4			
B3	DIE_TYPE[3:0]	BCD character 1	0001
B2			
B1			
B0 LSB			

This register contains manufacture die type information.

Table 3. CHIP_ID2

Register Name	CHIP_ID2
Address	0x01h
Reset Value	N/A
Type	Read only
Reset Conditions	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DIE_DASH[3:0]	BCD character representing dash number	N/A
B6			
B5			
B4			
B3	DIE_REV[3:0]	BCD character representing silicon revision	N/A
B2			
B1			
B0 LSB			

This register contains version control.

Table 4. STATUS1

Register Name	STATUS1
Address	0x02h
Reset Value	0x00h
Type	Read only
Reset Conditions	Reset upon read operation and on $V_{DD} < V_{DD_UVLO}$. Fault conditions must be cleared before new event can take place.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	LED1_SHORT	**LED1 Current Regulator Output Status** 0 = No shorted LED detected. 1 = Shorted LED detected.	0
B6	LED2_SHORT	**LED2 Current Regulator Output Status** 0 = No shorted LED detected. 1 = Shorted LED detected.	0
B5	REG_IN_UVLO	**Indication if REG_IN Input Support is Valid** 0 = Valid power at REG_IN. 1 = No valid power at REG_IN.	0
B4	IN_UVLO_THERM	**Indication if IN is Valid or Internal Die Temperature is Fault** 0 = Valid power at IN and No temperature fault has occurred. 1 = No valid power at IN or temperature fault has occurred.	0
B3	NTC_THERM	**Indication of Status of NTC Resistor** 0 = NTC within normal operating range. 1 = NTC over temperature detected.	0
B2	NTC_SHORT	**Indication of Status of NTC** 0 = NTC not shorted to ground. 1 = NTC shorted to ground detected.	0
B1	OVP_A	**Overvoltage Condition Caused by Analog Control Loop** 0 = No OVP_A detected. 1 = OVP_A detected.	0
B0 LSB	OVP_D	**Overvoltage Condition Caused by Digital Control Loop** 0 = No OVP_D detected. 1 = OVP_D detected.	0

This register contains status of IC.

Table 5. STATUS2

Register Name	STATUS2
Address	0x03h
Reset Value	0x01h
Type	Read only
Reset Conditions	Reset upon read operation and on $V_{DD} < V_{DD_UVLO}$ or new flash/torch event triggered.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	MAXFLASH	**Indication of Status of MAXFLASH** 0 = MAXFLASH has not occurred during last FLASH event. 1 = MAXFLASH has occurred during last FLASH event.	0
B6	DONE	**This is a Simple Indication Where or Not Torch/Flash Event is Done or Not** 0 = Torch/flash event in progress. 1 = Torch/flash event is completed.	0
B5	TX1_MASK	**Indication of TX1_MASK** 0 = TX1_MASK has not occurred during last FLASH event. 1 = TX1_MASK has occurred during last FLASH event.	0
B4	TX2_MASK	**Indication of TX2_MASK** 0 = TX2_MASK has not occurred during last FLASH event. 1 = TX2_MASK has occurred during last FLASH event.	0
B3	FLASH_TMR	**Indication of Flash Timer** **(Only Valid When Operating in Maximum Timer Mode)** 0 = Flash timer did not expire during last Flash sequence. 1 = Flash timer expired during last flash sequence.	0
B2	TORCH_TMR	**Indication of Torch Timer** **(Only Valid When Operating in Maximum Timer Mode)** 0 = Torch timer did not expire during last torch sequence. 1 = Torch timer expired during last torch sequence.	0
B1	ILIM	**Inductor Current Limit Status** 0 = Inductor peak current limit not reached. 1 = Inductor peak current limit reached.	0
B0 LSB	nRESET	**Indication if Register has been Reset Since Last Operation** 0 = I^2C registers not reset. 1 = I^2C registers reset. Reset upon read.	1

This register contains status of IC.

Table 6. IFLASH1

Register Name	IFLASH1
Address	0x04h
Reset Value	0x29h
Type	Read/write
Reset Conditions	FLASH1_EN is reset upon UVLO, $V_{DD} < V_{DD_UVLO}$, or LED1 fault for flash mode.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	FLASH1_EN	**Enable of Flash Mode for FLED1 Current Regulator** 0 = FLED1 disabled in flash mode. 1 = FLED1 enabled in flash mode.	0
B6	—	—	0
B5	FLASH1[5:0]	**Setting Flash Current** 000000 = 15.625mA 000001 = 31.25mA … 111110 = 984.375mA 111111 = 1000mA	101001
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control output current for flash mode.

Table 7. IFLASH2

Register Name	IFLASH2
Address	0x05h
Reset Value	0x29h
Type	Read/Write
Reset Conditions	FLASH2_EN is reset upon UVLO, $V_{DD} < V_{DD_UVLO}$, or LED2 fault for flash mode.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	FLASH2_EN	**Enabling Flash Mode for FLED2 Current Regulator** 0 = FLED2 disabled in flash mode. 1 = FLED2 enabled in flash mode.	0
B6	—	—	0
B5	FLASH2[5:0]	**Setting Flash Current** 000000 = 15.625mA 000001 = 31.25mA … 111110 = 984.375mA 111111 = 1000mA	101001
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control output current for flash mode.

Table 8. ITORCH1

Register Name	ITORCH1
Address	0x06h
Reset Value	0x00h
Type	Read/write
Reset Conditions	TORCH1_EN is reset upon UVLO, $V_{DD} < V_{DD_UVLO}$, or LED1 fault for torch mode.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TORCH1_EN	**Enabling Torch Mode for FLED1 Current Regulator** 0 = FLED1 disabled in torch mode. 1 = FLED1 enabled in torch mode.	0
B6 B5 B4 B3 B2 B1	TORCH1[5:0]	**Setting TORCH1 Current** **DAC Mode** 000000 = 3.91mA 000001 = 7.8125mA … 111110 = 246.1mA 111111 = 250.0mA **PWM Mode** Output current XXX000 = 125mA duty cycle XXX001 = 250mA duty cycle … XXX110 = 875mA duty cycle XXX111 = 1000.00mA duty cycle **Duty Cycle** 000XXX = 3.125% duty cycle 001XXX = 6.25% duty cycle … 110XXX = 21.875% duty cycle 111XXX = 25.000% duty cycle	000000
B0 LSB	TORCH1_DIM	**Select DAC or PWM Dimming for Torch** 0 = DAC 1 = PWM	0

This register contains output current for torch mode.

Table 9. ITORCH2

Register Name	ITORCH2
Address	0x07h
Reset Value	0x00h
Type	Read/write
Reset Conditions	TORCH2_EN is reset upon UVLO, $V_{DD} < V_{DD_UVLO}$, or LED2 fault for torch mode

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TORCH2_EN	**Enabling Torch Mode for FLED2 Current Regulator** 0 = FLED2 disabled in torch mode. 1 = FLED2 enabled in torch mode.	1
B6 B5 B4 B3 B2 B1	TORCH2[5:0]	**Setting TORCH2 Current** **DAC Mode** 000000 = 3.91mA 000001 = 7.8125mA … 111110 = 246.1mA 111111 = 250.0mA **PWM Mode** Output current XXX000 = 125mA duty cycle XXX001 = 250mA duty cycle … XXX110 = 875mA duty cycle XXX111 = 1000.00mA duty cycle **Duty Cycle** 000XXX = 3.125% duty cycle 001XXX = 6.25% duty cycle … 110XXX = 21.875% duty cycle 111XXX = 25.000% duty cycle	000000
B0 LSB	TORCH2_DIM	**Select DAC or PWM Dimming for Torch** 0 = DAC 1 = PWM	0

This register contains output current for torch mode.

Table 10. MODE_SEL

Register Name	MODE_SEL
Address	0x08h
Reset Value	0xC0h
Type	Read/write
Reset Conditions	TORCH_MODE, FLASH_MODE is reset upon UVLO, $V_{DD} < V_{DD_UVLO}$, THERM fault, or OVP fault

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TORCH_EN_PD	**On/Off Control for Pulldown Resistor of TORCH_EN Input** 0 = Not enabled. 1 = Enabled.	1
B6	FLASH_STB_PD	**On/Off Control for Pulldown Resistor of FLASH_STB Input** 0 = Not enabled. 1 = Enabled.	1
B5 B4 B3	TORCH_MODE[2:0]	000 = Torch mode disabled. 001 = Torch mode enabled using TORCH_EN 010 = Torch mode enabled using FLASH_STB 011 = Torch mode enabled using TORCH_EN or FLASH_STB 100 = Torch mode enabled using TORCH_EN and FLASH_STB 101 = Torch mode enabled regardless of logic inputs 110 = Torch mode enabled regardless of logic inputs 111 = Torch mode enabled regardless of logic inputs	001
B2 B1 B0 LSB	FLASH_MODE[2:0]	000 = Flash mode disabled. 001 = Flash mode enabled using TORCH_EN 010 = Flash mode enabled using FLASH_STB 011 = Flash mode enabled using TORCH_EN or FLASH_STB 100 = Flash mode enabled using TORCH_EN and FLASH_STB 101 = Flash mode enabled regardless of logic inputs 110 = Flash mode enabled regardless of logic inputs 111 = Flash mode enabled regardless of logic inputs	010

This register control the mode of operation.

Table 11. TX1_MASK

Register Name	TX1_MASK
Address	0x09h
Reset Value	0xC0h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TX1_MASK_EN	**On/Off Control for TX1_MASK** 0 = Not enabled. 1 = Enabled.	1
B6	TX1_MASK_PD	**Enable/Disable Pulldown Resistor for TX1_MASK** 0 = Not enabled. 1 = Enabled.	1
B5 B4 B3 B2 B1 B0 LSB	FLASH_TX1_MASK[5:0]	**Setting Maximum Flash Current During TX1_MASK Event** 000000 = 15.625mA 000001 = 31.25mA … 111110 = 984.375mA 111111 = 1000mA	000000

This register contains control output current for flash mode.

Table 12. TX2_MASK

Register Name	TX2_MASK
Address	0x0Ah
Reset Value	0xC0h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TX2_MASK_EN	**On/Off Control for TX2_MASK** 0 = Not enabled. 1 = Enabled.	1
B6	TX2_MASK_PD	**Enable/Disable Pulldown Resistor for TX2_MASK** 0 = Not enabled. 1 = Enabled.	1
B5	FLASH_TX2_MASK[5:0]	**Setting Maximum Flash Current During TX2_MASK Event** 000000 = 15.625mA 000001 = 31.25mA … 111110 = 984.375mA 111111 = 1000mA	000000
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control output current for flash mode.

Table 13. FLASH_RAMP_SEL

Register Name	FLASH_RAMP_SEL
Address	0x0Bh
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	—	0
B6 B5 B4	FLASH_RU[2:0]	**Selection of Flash Ramp-Up Rate** 000 = 384µs 001 = 640µs 010 = 1152µs 011 = 2176µs 100 = 4224µs 101 = 8.320µs 110 = 16.512ms 111 = 32.896ms	000
B3	—	—	0
B2 B1 B0 LSB	FLASH_RD[2:0]	**Selection of Flash Ramp-Down Rate** 000 = 384µs 001 = 640µs 010 = 1152µs 011 = 2176µs 100 = 4224µs 101 = 8.320µs 110 = 16.512ms 111 = 32.896ms	000

This register controls the ramping.

Table 14. TORCH_RAMP_SEL

Register Name	TORCH_RAMP_SEL
Address	0x0Ch
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—		0
B6	TORCH_RU[1:0]	**Selection of Torch Ramp-Up Rate** 000 = 16.392ms 001 = 32.776ms 010 = 65.544ms 011 = 131.08ms 100 = 262.152ms 101 = 524.296ms 110 = 1.048s 111 = 2.097s	000
B5			
B4			
B3	—	—	0
B2	TORCH_RD[1:0]	**Selection of Torch Ramp-Down Rate** 000 = 16.392ms 001 = 32.776ms 010 = 65.544ms 011 = 131.08ms 100 = 262.152ms 101 = 524.296ms 110 = 1.048s 111 = 2.097s	000
B1			
B0 LSB			

This register controls the ramping.

Table 15. FLASH_TMR_CNTL

Register Name	FLASH_TMR_CNTL
Address	0x0Dh
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	FLASH_TMR_CNTL	**Select Timer Mode for Flash Timer** 0 = One-shot timer mode 1 = Maximum timer mode	0
B6 B5 B4 B3 B2 B1 B0 LSB	FLASH_TMR[6:0]	**Selecting for Flash Timer** 0000000 = 0.128ms 0000001 = 0.384ms 0000010 = 0.640ms 0000011 = 0.896ms 0000100 = 1.41ms 0000101 = 1.92ms 0000101 = 1.92ms 0001110 = 2.43ms 0000111 = 2.94ms 0001000 = 3.97ms 0001001 = 4.99ms … (1.024ms step size) 0001110 = 10.11ms 0001111 = 11.14ms 0010000 = 13.18ms 0010001 = 15.23ms … (2.048ms step size) 0011110 = 41.86ms 0011111 = 43.90ms 0100000 = 48.00ms 0100001 = 52.09ms … (4.096ms step size) 0111110 = 170.88ms 0111111 = 174.98ms 1000000 = 183.17ms 1000001 = 191.36ms … (8.192ms step size) 1111110 = 691.07ms 1111111 = 699.26ms	0000000

This register contains control information for flash timer.

Table 16. TORCH_TMR_CNTL

Register Name	TORCH_TMR_CNTL
Address	0x0Eh
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	TORCH_TMR_CNTL	**Select Timer Mode for Torch Timer** 0 = One-shot timer mode. 1 = Timer mode disabled.	0
B6 B5 B4 B3 B2	TORCH_TMR[4:0]	**Selecting for Torch Timer** 00000 = 122.88ms … (131.072ms step size) 00011 = 516.096ms … (262.144 step size) 00100 = 778.24ms 00111 = 1564.67ms … (262.144 step size) 01000 = 2088.96ms 01111 = 5758.976ms … (524.288ms step size) 10000 = 6807.552ms 11110 = 21487.616ms 11111 = 22536.192ms … (1048.576ms step size)	00000
B1	—	—	0
B0 LSB	—	—	0

This register contains control information for torch timer.

Table 17. MAXFLASH1

Register Name	MAXFLASH1
Address	0x10h
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	MAXFLASH_HYS[2:0]	**Selects Hysteresis for MAXFLASH** 000 = Off, LED current only allowed to decrease 001 = 50mV 010 = 100mV 110 = 300mV 111 = 350mV	000
B6			
B5			
B4	MAXFLASH_TH[4:0]	**Selects MAXFLASH Threshold** 00000 = Off, MAXFLASH disabled. 00001 = 2.40V 00010 = 2.433V … 11110 = 3.366V 11111 = 3.40V	000000
B3			
B2			
B1			
B0 LSB			

This register contains control information for MAXFLASH.

Table 18. MAXFLASH2

Register Name	MAXFLASH2
Address	0x11h
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	LB_TMR_R[3:0]	**Selects MAXFLASH Timer for Rising Input Voltage** 0000 = 256µs 0001 = 512µs … 1110 = 1792µs 1111 = 2048µs	0000
B6			
B5			
B4			
B3	LB_TMR_F[3:0]	**Selects MAXFLASH Timer for Falling Input Voltage** 0000 = 256µs 0001 = 512µs … 1110 = 1792µs 1111 = 2048µs	0000
B2			
B1			
B0 LSB			

This register contains control information for MAXFLASH.

Table 19. MAXFLASH3

Register Name	MAXFLASH3
Address	0x12h
Reset Value	0x3Fh
Type	Read only
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	MAX_FLASH1_IMIN[7:0]	Minimum output current logged for LED (FLED1) during a MAXFLASH event	00111111
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control information for MAXFLASH.

Table 20. MAXFLASH4

Register Name	MAXFLASH4
Address	0x13h
Reset Value	0x3Fh
Type	Read only
Reset Conditions	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	MAX_FLASH2_IMIN[7:0]	Minimum output current logged for LED (FLED2) during a MAXFLASH event	00111111
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control information for MAXFLASH

Table 21. NTC

Register Name	NTC
Address	0x14h
Reset Value	0x00h
Type	Read/Write
Reset Conditions	NTC_EN bit is cleared on NTC_SHORT detected. Reset upon $V_{DD} < V_{DD_UVLO}$.

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	NTC_EN	**On/Off Control of NTC Input** 0 = Disabled. 1 = Enabled.	0
B6	NTC_TH_FLASH[2:0]	**Selects Threshold for Hot for Flash Mode** 000 = 200mV 001 = 250mV … 110 = 500mV 111 = 550mV	000
B5			
B4			
B3	NTC_TH_TORCH[2:0]	**Selects Threshold for Hot for Torch Mode** 000 = 200mV 001 = 250mV … 110 = 500mV 111 = 550mV	000
B2			
B1			
B0 LSB			0

This register contains control information for NTC function.

Table 22. DCDC_CNTL1

Register Name	DCDC_CNTL1
Address	0x15h
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB B6	OVP_TH[1:0]	**Selects Overvoltage Threshold for the DC-DC Converter Output Voltage** 00 = 4.50V 01 = 4.80V 10 = 5.10V 11 = 5.40V	00
B5	—	—	0
B4	—	—	0
B3 B2	FREQ_PWM[1:0]	**Selection of Frequency for PWM of Current Regulators** 00 = 7.8kHz 01 = 1.9kHz 10 = 488Hz 11 = 122Hz	00
B1 B0 LSB	DCDC_MODE	00 = Adaptive mode. DCDC is enabled together with current regulators. 01 = Prebiased adaptive mode. Output is prebiased and DC-DC is enabled together with current regulators. 10 = Forced active mode with output regulating at DCDC_SS. 11 = Dropout mode.	00

This register contains control information for DC-DC converter.

Table 23. DCDC_CNTL2

Register Name	DCDC_CNTL2
Address	0x16h
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td>B7
MSB</td><td rowspan="2">DCDC_ADPT_REG[1:0]</td><td colspan="4">Sets the Adaptive Regulation Threshold for the DC-DC Converter
00 = 120mV
01 = 150mV
10 = 180mV
11 = 210mV</td><td rowspan="2">00</td></tr>
<tr><td>B6</td></tr>
<tr><td>B5</td><td>DCDC_GAIN</td><td colspan="4">0 = Standard
1 = Enhancement</td><td>0</td></tr>
<tr><td>B4</td><td rowspan="9">DCDC_OPERATION[2:0]</td><td colspan="4">Mode for DC-DC Converter</td><td rowspan="9">000</td></tr>
<tr><td>B4, B3, B2</td><td>Mode</td><td>Frequency</td><td>DC Min (%)</td></tr>
<tr><td rowspan="3">B3</td><td>000</td><td>SKIP</td><td>1MHz Fixed</td><td>3.125</td></tr>
<tr><td>001</td><td>SKIP</td><td>4MHz Auto Adjust</td><td>3.125</td></tr>
<tr><td>010</td><td>FPWM</td><td>4MHz Fixed</td><td>12.50</td></tr>
<tr><td>011</td><td>FPWM</td><td>4MHz Auto Adjust</td><td>3.125</td></tr>
<tr><td rowspan="3">B2</td><td>100</td><td>FPWM</td><td>1MHz Fixed</td><td>3.125</td></tr>
<tr><td>101</td><td>FPWM</td><td>2MHz Fixed</td><td>12.50</td></tr>
<tr><td>110</td><td>FPWM</td><td>2MHz Auto Adjust</td><td>3.125</td></tr>
<tr><td>111</td><td>SKIP</td><td>2MHz Auto Adjust</td><td>3.125</td></tr>
<tr><td>B1</td><td rowspan="2">—</td><td colspan="4" rowspan="2">—</td><td rowspan="2">00</td></tr>
<tr><td>B0
LSB</td></tr>
</table>

This register contains control information for DC-DC converter.

Table 24. DCDC_LIM

Register Name	DCDC_LIM
Address	0x17h
Reset Value	0x00h
Type	Read/write
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_ILIM[1:0]	**Selects Current Limit for Low-Side Switch (per phase)** 00 = 1.25 01 = 1.5 10 = 1.75 11 = 2.0	00
B6			
B5	DCDC_SS[5:0]	**Set the Soft-Start Threshold for the DC-DC Converter** 000000 = 2.3V 000001 = 2.35V … 111110 = 5.15V 111111 = 5.2V	000000
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control information for DC-DC converter.

Table 25. DCDC_OUT

Register Name	DCDC_OUT
Address	0x18h
Reset Value	0x00h
Type	Read only
Reset Conditions	Reset upon $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_OUT[7:0]	**Readback Information Regarding Adaptive Regulation Output Voltage** 00000000 = 2.3V 00000001 = 2.3125V … 11111110 = 5.1875V 11111111 = 5.2V	00000000
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control information about the actual regulation threshold for the DCD converter during adaptive regulation.

Table 26. DCDC_OUT_MAX

Register Name	DCDC_OUT_MAX
Address	0x19h
Reset Value	0x00h
Type	Read only
Reset Conditions	Reset upon triggering torch or flash mode and $V_{DD} < V_{DD_UVLO}$

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_OUT_MAX[7:0]	**Readback Information Regarding Adaptive Regulation Output Voltage** 00000000 = 2.3V 00000001 = 2.3125V … 11111110 = 5.1875V 11111111 = 5.2V	00000000
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

This register contains control information about the maximum regulation threshold for the DCD converter during adaptive regulation.

Applications Information

Programming the I²C Registers

It is critical to program the IC in the correct sequence to ensure proper operation.

Changing any register values other than the DCDC_MODE bits in the DCDC_CNTL1 register during a flash or torch event is not advised. Poll the STATUS2 register to wait for the DONE bit to be asserted before changing values.

Sequencing can be divided in to three groups flash and torch mode and DC-DC output voltage.

For flash mode, the following sequence is recommended:

1. Clear any pending fault status by reading the STATUS1 register. Failing to do this can result in incorrect values written is some of the registers. For example, failing to clear a FLED1 or FLED2 fault clears the FLED1_EN or FLED2_EN, respectively, disabling the current regulators remain disabled until the FLED_ fault is cleared in the STATUS1 register.
2. Ensure that flash mode is not enabled, by setting the FLASH_MODE bits to 000 in the MODE_SEL register. Ensure the DCDC_MODE bits are 00 in the DCDC_CNTL1 register.
3. If the TX_MASK function is required for flash operation, write the appropriate values into the TX1_MASK and TX2_MASK register. This register does not need to be updated if current values are already set.
4. Select the ramp rate in the FLASH_RAMP_SEL register for ramping up/down the FLED current. These registers do not need to be updated if current values are already set.
5. Select the flash timer and mode of operation by writing to the FLASH_TMR_CNTL register. This register does not need to be updated if current values are already set.
6. If the MAXFLASH function is required for flash operation, write the appropriate values into the MAXFLASH1 and MAXFLASH2 registers. These registers do not need to be updated if current values are already set.
7. If the NTC function is required for flash operation, write the appropriate values into the NTC register. This register does not have to be updated if current values are already set.
8. Select the settings for the DC-DC converter by writing to the DCDC_CNTL2 and DCDC_ILIM registers. These registers do not need to be updated if current values are already set.
9. Select the settings for the flash mode by writing to the FLASH1 and FLASH2 registers. These registers do not need to be updated if current values are already set.
10. Select the settings for the DCDC_CNTL1 register.
11. Select the trigger mode for flash event by writing to the FLASH_MODE bits in the MODE_SEL register. This register does not need to be updated if current values are already set.

Now the flash event is ready to be triggered based on the value set for the FLASH_MODE setting.

For hardware triggering, set FLASH_MODE = 001, 010, 011, or 100. Flash event is retriggered based on logic input. No update to I²C registers is required.

For software triggering, set FLASH_MODE = 101, 110, or 111. Flash event is triggered once FLASH_MODE changes from an external trigger to a software trigger. If an additional flash event is required through a software trigger, the FLASH_MODE needs to be set to 000 first before writing to the software value (101, 110, or 111) to retrigger a new flash event.

For torch mode, the following sequence is recommended:

1. Clear any pending fault status by reading the STATUS1 register. Failing to do this can result in incorrect values written to some of the registers. For example, failing to clear a FLED1 or FLED2 fault clears the FLED1_EN or FLED2_EN, respectively, disabling the current regulators that remain disabled until the FLED_ fault is cleared in the STATUS1 register. When the FLED_ fault is cleared, the TORCH_EN can be set.
2. Ensure that torch mode is not enabled by setting the TORCH_MODE to 000 in the MODE_SEL register. Ensure the DCDC_MODE bits are 00 in the DCDC_CNTL1 register.
3. Select the ramp rate in the TORCH_RAMP_SEL register for ramping up/down the torch FLED current. This register does not need to be updated if current values are already set.
4. Select the torch timer and mode of operation by writing to the TORCH_TMR_CNTL register. This register does not need to be updated if current values are already set.

5. If the MAXFLASH function is required for torch operation, write the appropriate values into the MAXFLASH1 and MAXFLASH2 registers. These registers do not need to be updated if current values are already set.
6. If the NTC function is required for torch operation, write the appropriate values into the NTC register. This register does not need to be updated if current values are already set.
7. Select the settings for the DC-DC converter by writing to the DCDC_CNTL2 and DCDC_ILIM registers. These registers do not need to be updated if current values are already set.
8. Select the settings for the torch mode by writing to the TORCH1 and TORCH2 registers. These registers do not need to be updated if current values are already set.
9. Select the settings for the DCDC_CNTL1 register.
10. Select the trigger mode for the torch event by writing to the TORCH_MODE bits in the MODE_SEL register. This register does not need to be updated if current values are already set.

Now the torch event is ready to be triggered based on the value set for the TORCH_MODE setting.

For hardware triggering set TORCH_MODE = 001, 010, 011, or 100. A torch event is retriggered based on logic input. No update to I²C registers is required.

For software triggering, set TORCH_MODE = 101, 110, or 111. A torch event is triggered once TORCH_MODE changes from an external trigger to a software trigger. If an additional torch event is required through a software trigger, the TORCH_MODE needs to be set to 000 first before writing to the software value (101, 110, or 111) to retrigger a new torch event.

For DC-DC fixed voltage mode and dropout output voltage, the following sequence is recommended:

1. Clear any pending fault status by reading the STATUS1 register. Failing to do this can result in incorrect values written is some of the registers.
2. Ensure the DCDC_MODE bits are 00 in the DCDC_CNTL1 register.
3. For fixed output voltage mode, select the settings for the DC-DC converter by writing to the DCDC_CNTL2 and DCDC_ILIM registers. These registers do not have to be updated if current values are already set.
4. Select the settings for DCDC_CNTL1 register including the DCDC_MODE bits. Writing anything other than 00 to the DCDC_MODE bits enables the DC-DC converter.

During a torch or flash event, the following optional registers can be read:

The DCDC_OUT register contains current information regarding the output voltage settings. The actual output voltage is slightly lower due to the load regulation of the DC-DC converter. It is not required to read this register during a torch or flash event.

STATUS1 register contains current information if any fault condition occurs during the torch or flash event. It is optional to read this register during torch or flash event.

The STATUS2 register contains information regarding any events that might have happened during a torch or flash event.

After a torch or flash event the following optional register can be read:

The DCDC_OUT_MAX register contains the last adaptive output voltage to which the converter has regulated the output. This information can be used to adjust the DCDC_SS setting.

The STATUS1 register contains information regarding any fault condition that might have occurred during a torch or flash event.

The STATUS2 register contains information regarding any events that might have happened during a torch or flash event.

If the MAXFLASH is enabled, the MAXFLASH3 and MAXFLASH4 registers contain the minimum current setting that the current regulators where regulating to during the MAXFLASH event. The STATUS2 register contains a MAXFLASH bit indicating if the MAXFLASH was active during the torch or flash event.

It should be note that during fixed output voltage mode, the output is regulated to the DCDC_SS value that was set during the enabling of the converter. The DCDC_SS value can be updated when the converter is enabled, but this does not impact the output voltage.

To change the output voltage, first power down the DC-DC converter (DCD_MODE = 00), then update the DCDC_SS value, and then power it up again (DCDC_MODE = 10).

Output Voltage Operating Range

The capability of the DC-DC converter of the IC is depending on following parameters:

- Input voltage
- Output voltage
- Efficiency for given range of operation
- Inductor value
- Switching frequency
- Peak input current limit of the IC

The following tables give examples of different operating conditions with the respective input and output voltage limitations.

Table 27. Maximum Output Voltage for 2A Output Current as a Function of V_{IN} and I_{PEAK}

I_{PEAK} (PER PHASE)				
	1.25A	1.50A	1.75A	2.00A
V_{IN}	V_{OUT} max support for 2A output current			
2.50V	2.50V	2.69V	3.19V	3.69V
2.60V	2.60V	2.82V	3.34V	3.87V
2.70V	2.70V	2.95V	3.50V	4.05V
2.80V	2.80V	3.08V	3.66V	4.24V
2.90V	2.90V	3.21V	3.82V	4.43V
3.00V	3.00V	3.35V	3.98V	4.62V
3.10V	3.10V	3.48V	4.15V	4.82V
3.20V	3.20V	3.62V	4.32V	5.00V
3.30V	3.30V	3.76V	4.48V	5.00V
3.40V	3.40V	3.90V	4.65V	5.00V
3.50V	3.50V	4.04V	4.82V	5.00V
3.60V	3.60V	4.13V	4.94V	5.00V
3.70V	3.70V	4.22V	5.00V	5.00V
3.80V	3.80V	4.32V	5.00V	5.00V
3.90V	3.90V	4.41V	5.00V	5.00V
4.00V	4.00V	4.50V	5.00V	5.00V
4.10V	4.10V	4.59V	5.00V	5.00V
4.20V	4.20V	4.68V	5.00V	5.00V
4.30V	4.30V	4.76V	5.00V	5.00V
4.40V	4.40V	4.85V	5.00V	5.00V
4.50V	4.50V	4.94V	5.00V	5.00V

Note: *For f_{SW} = 4MHz, L = 0.5µH.*

Table 28. Maximum Output Voltage for 1.5A Output Current as a Function of V_{IN} and I_{PEAK}

I_{PEAK} (PER PHASE)				
	1.25A	1.50A	1.75A	2.00A
V_{IN}	V_{OUT} max support for 1.5A output current			
2.50V	2.92V	3.58V	4.25V	4.92V
2.60V	3.05V	3.76V	4.46V	5.00V
2.70V	3.19V	3.93V	4.67V	5.00V
2.80V	3.33V	4.11V	4.88V	5.00V
2.90V	3.47V	4.28V	5.00V	5.00V
3.00V	3.61V	4.46V	5.00V	5.00V
3.10V	3.75V	4.64V	5.00V	5.00V
3.20V	3.90V	4.83V	5.00V	5.00V
3.30V	4.04V	5.00V	5.00V	5.00V
3.40V	4.19V	5.00V	5.00V	5.00V
3.50V	4.33V	5.00V	5.00V	5.00V
3.60V	4.43V	5.00V	5.00V	5.00V
3.70V	4.52V	5.00V	5.00V	5.00V
3.80V	4.62V	5.00V	5.00V	5.00V
3.90V	4.71V	5.00V	5.00V	5.00V
4.00V	4.80V	5.00V	5.00V	5.00V
4.10V	4.89V	5.00V	5.00V	5.00V
4.20V	4.98V	5.00V	5.00V	5.00V
4.30V	5.00V	5.00V	5.00V	5.00V
4.40V	5.00V	5.00V	5.00V	5.00V
4.50V	5.00V	5.00V	5.00V	5.00V

Note: *For f_{SW} = 4MHz, L = 0.5µH.*

Table 29. Maximum Output Voltage for 1.0A Output Current as a Function of V_{IN} and I_{PEAK}

I_{PEAK} (PER PHASE)				
	1.25A	1.50A	1.75A	2.00A
V_{IN}	V_{OUT} max support for 1.0A output current			
2.50V	4.38V	5.00V	5.00V	5.00V
2.60V	4.58V	5.00V	5.00V	5.00V
2.70V	4.79V	5.00V	5.00V	5.00V
2.80V	5.00V	5.00V	5.00V	5.00V
2.90V	5.00V	5.00V	5.00V	5.00V
3.00V	5.00V	5.00V	5.00V	5.00V
3.10V	5.00V	5.00V	5.00V	5.00V
3.20V	5.00V	5.00V	5.00V	5.00V
3.30V	5.00V	5.00V	5.00V	5.00V
3.40V	5.00V	5.00V	5.00V	5.00V
3.50V	5.00V	5.00V	5.00V	5.00V
3.60V	5.00V	5.00V	5.00V	5.00V
3.70V	5.00V	5.00V	5.00V	5.00V
3.80V	5.00V	5.00V	5.00V	5.00V
3.90V	5.00V	5.00V	5.00V	5.00V
4.00V	5.00V	5.00V	5.00V	5.00V
4.10V	5.00V	5.00V	5.00V	5.00V
4.20V	5.00V	5.00V	5.00V	5.00V
4.30V	5.00V	5.00V	5.00V	5.00V
4.40V	5.00V	5.00V	5.00V	5.00V
4.50V	5.00V	5.00V	5.00V	5.00V

Note: *For f_{SW} = 4MHz, L = 0.5µH.*

For conditions other than those specified in the tables above the maximum output voltage that can be supported by the IC can be calculated using following formula:

$$V_{OUT} = \frac{2\left(I_{PEAK} - \frac{V_{IN(MIN)}}{2 \times L \times f_{SW}}\right)\eta \times V_{IN(MIN)}}{I_{OUT(MAX)}}$$

V_{OUT} cannot exceed OVP_D minus load regulation.

Inductor Selection

The IC is designed to use a 0.47µH to 1.0µH inductor per phase. Selecting a higher inductance value increases efficiency by reducing inductor peak-to-peak current with the trade-off in solution size.

To prevent core saturation, ensure that the inductor-saturation current rating exceeds the peak inductor current for the application. Calculate the worst-case peak inductor current with the following formula:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT(MAX)}}{2 \times \eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times L \times f_{SW}}$$

where:

L is the inductance chosen.

f_{SW} is the actual switching frequency for the IC.

η is the DC-DC converter efficiency. See the appropriate typical operating curve.

Table 30. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX}) (mm)
RECOMMENDED INDUCTORS FOR THE I_{LIM} 1.25A SETTING					
Coilcraft	PFL1610	0.47	85	1.8	1.8 x 1.0 x 1.0
	XPL2010	0.50 0.68 0.82 1.00	40 57 68 89	2.35 1.95 1.65 1.60	2.0 x 1.9 x 1.0
SEMCO	CIG21LR47MNE	0.47	96	1.35	2.0 x 1.25 x 1.0
	CIG22L1R0MNE	1.0	60	1.6	2.5 x 2.0 x 1.0
TOKO	MDT2012-CR	0.56	65	1.5	2.0 x 1.25 x 1.0
TDK	VLS2012	0.47	54	1.85	2.0 x 1.6 x 0.95
		0.68	72	1.65	
Cyntec	PSB1210T	0.33	68	2.1	1.25 x 1.0 x 1.0
		0.5	85	1.48	
	PIFE20161B	0.47 1.0	30 60	3.6 2.4	2.0 x 1.6 x 1.2

Table 30. Suggested Inductors (continued)

MANUFACTURER	SERIES	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX}) (mm)
RECOMMENDED INDUCTORS FOR THE I_{LIM} 1.5A SETTING					
Coilcraft	PFL1610	0.47	85	1.8	1.8 x 1.0 x 1.0
	XPL2010	0.50 0.68	40 57	2.35 1.95	2.0 x 1.9 x 1.0
TOKO	MDT2012-CR	0.56	65	1.5	2.0 x 1.25 x 1.0
	DEM2812C	1.0	66	1.6	3.2 x 3.0 x 1.2
SEMCO	CIG2MWR47MNE	0.47	75	1.8	2.0 x 1.25 x 1.0
TDK	VLS2012	0.47	54	1.85	2.0 x 1.6 x 0.95
		0.68	72	1.65	
Cyntec	PSI2520	0.47	40	2.3	2.5 x 2.0 x 1.0
	PIFE2520T	0.47 1.0	34 54	4.5 3.5	2.5 x 2.0 x 1.0
	PIFE20161B	0.47 1.0	30 60	3.6 2.4	2.0 x 1.6 x 1.2
	PSB1210T	0.33	68	2.1	1.25 x 1.0 x 1.0
RECOMMENDED INDUCTORS FOR THE I_{LIM} 1.75A SETTING					
Coilcraft	PFL2010	0.47	60	1.8	2.0 x 1.46 x 1.0
	XPL2010	0.50	40	2.35	2.0 x 1.9 x 1.0
TDK	VLS2012	0.47	54	1.85	2. 0x 1.6 x 0.95
SEMCO	CIG22HR47	0.47	52	3.8	2.5 x 2.0 x 1.0
Cyntec	PSI2520	0.47	40	2.3	2.5 x 2.0 x 1.0
	PSB1210T	0.33	68	2.1	2.5 x 2.0 x 1.0
	PIFE2520T	0.47 1.0	34 54	4.5 3.5	2.5 x 2.0 x 1.0
	PIFE20161B	0.47 1.0	30 60	3.6 2.4	2.0 x 1.6 x 1.2
RECOMMENDED INDUCTORS FOR THE I_{LIM} 2.0A SETTING					
CoilCraft	XPL2010	0.50	40	2.35	2.0 x 1.9 x 1.0
SEMCO	CIG22HR47	0.47	52	3.8	2.5 x 2.0 x 1.0
TDK	VLF3025	1.0	33	2.0	3.0 x 2.5 x 1.0
Cyntec	PSI2520	0.47	40	2.3	2.5 x 2.0 x 1.0
	PSB1210T	0.33	68	2.1	1.25 x 1.0 x 1.0
	PIFE2520T	0.47 1.0	34 54	4.5 3.5	2.5 x 2.0 x 1.0
	PIFE20161B	0.47 1.0	30 60	3.6 2.4	2.0 x 1.6 x 1.2

Input Capacitor Selection

The input capacitor required consists of two capacitors. One capacitor is used for decoupling the input to IN. The other is for decoupling the inductors to reduce input ripple.

The IN should be decoupled using a minimum capacitance of 0.08µF. This capacitor is required to ensure a low noise input to IN and is critical for MAXFLASH and adaptive regulation quality.

The input capacitor for the inductor is required to support the ripple current from the DC-DC converter switching. The input capacitor needs to have a minimum capacitance of 4µF. Ensure that with voltage derating that the value of the capacitor is sufficient to ensure stability of the converter. Since capacitors can derate as much as 40% to 60%, a 10µF capacitor is recommended. See Table 31 below for recommended capacitors.

Another critical parameter for the input capacitor is that the impedance at 8MHz is as low as possible. Since the ripple frequency of the converter is 2x 4MHZ, choosing an input capacitor with high impedance at this frequency results in increased input ripple, reducing the performance of the IC.

Output Capacitor Selection

The output capacitor is one of the critical items in determining the output ripple current of the FLED output. The current regulator output ripple current is generated from the voltage ripple existing on the OUT capacitor due to DC-DC step up converter switching.

The voltage ripple on OUT capacitor is mainly due to the following two factors:

ESR of the output capacitor.

ΔV across the output capacitor caused by the charge and discharge cycle.

Therefore, the choice of output capacitor has a large impact on the output ripple of the current regulators. In order to ensure low output ripple current, the following steps should be taken:

1. Select an output capacitor with a low ESR.
2. Select an output capacitor with low impedance at the switching frequency.
3. In the PCB layout careful routing between the IC and output capacitors can reduce ripple current. By routing to the output capacitor as a star connection the ripple that is injected into the current regulator is reduced by $I_{LX_}xR_{TRACE1}$. Even though this is a small reduction in ripple, it still aids in producing a low output ripple current.
4. (Optional) A capacitor at REG_IN can even further reduce the output ripple current. The additional capacitor at REG_IN reduces the overall ESR of the output capacitor by having more capacitors in parallel. Also the connection between the output capacitor and the capacitor at REG_IN acts at a high-frequency filter since the trace acts like an inductor forming a LC filter. This is especial effective in filtering away the switching edges of the DC-DC converter.

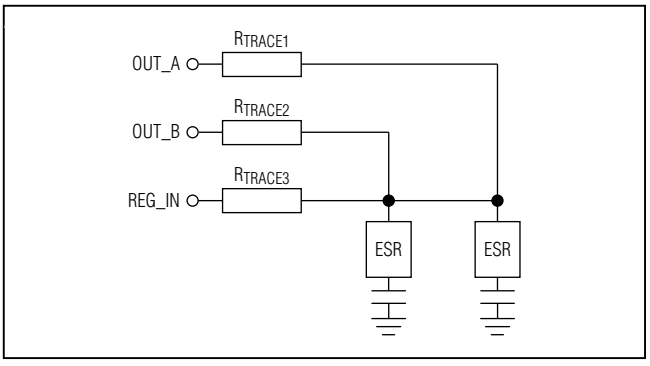


Figure 19. Output Capacitor Start Connection

Table 31. Suggested Input Capacitors

MANUFACTURER	SERIES	CAPACITANCE (µF)	ESR (mΩ at 4HMz)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX}) (mm)
Samsung	CL05A106MP5NUNC	10	9	1.0 x 0.5 x 0.5
Murata	GRM188R60J106ME84	10	10	1.6 x 0.6 x 0.085
Samsung	CL05A104KA5NNNC	0.1	4.6	1.0 x 0.5 x 0.5
Taiyo Yuden	TMK105BJ1040KV	0.1	20	1.0 x 0.5 x 0.5
Murata	GRM155R61E104KA87	0.1	15	1.0 x 0.5 x 0.5

Table 32. Suggested Output Capacitors

MANUFACTURER	SERIES	CAPACITANCE (µF)	ESR (mΩ at 4HMz)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX} = VOLUME) (mm)
Samsung	CL05A106MP5NUNC	10	9	1.0 x 0.5 x 0.5
Murata	GRM188R60J106ME84	10	10	1.6 x 0.6 x 0.085
Samsung	CL05A475KP5NRNC	4.7	5	1.0 x 0.5 x 0.5

The output capacitors needs to have a minimum capacitance of 6µF for DCDC_GAIN = 0 and a minimum capacitance of 12µF for DCDC_GAIN = 1 and operating in non adaptive mode. Ensure that with voltage derating that the value of the capacitor is sufficient to ensure stability of the converter. Since capacitors can derate as much as 40% to 60%, a 10µF capacitor for each output is recommended for DCDC_GAIN of 0. With DCDC_GAIN of 1 either a 20µF capacitor or 2x 10µF capacitors at each output is recommended.

An optional capacitor at REG_IN of 4.7µF can help increase the performance of the current regulator.

See Table 32 for recommended capacitors.

PCB Layout

Layout is critical for the performance of the IC. Proper layout ensures good thermal conditions for the IC as well as minimizing EMI disturbances and most important good current sharing between the two phases.

Bypass IN to AGND with a ceramic capacitor. Ceramic capacitors with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over a wide temperature ranges. Place the capacitor as close as possible to the IN input bump with a value recommended in the input capacitor selection section. Place an additional capacitor from IN to PGND,close to the inductor (shared for both phases) with a recommended value give in the input capacitor selection section.

Bypass OUT_ to PGND_ with a ceramic capacitor. Ceramic capacitors with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over a wide temperature ranges. Place the capacitor as close as possible to the IC. Ensure that the routing form IC to output capacitor is as identical for each phase as possible since this yields the best efficiency. The minimum required output capacitor value is given in output capacitor selection section. Ensure that OUT_A and OUT_B are routed directly to the output capacitor before routed to REG_IN. Doing this minimizes the output ripple current on the LED due to voltage ripple on the output capacitor. For enhanced performance of the current regulator, an additional capacitor can be paced at REG_IN_. This reduces the output ripple current of the current regulator and overall enhances the performance of the current regulator.

Keep the ground loop among the input, output and the IC as short as possible since this ground plane is carrying the full load current.

Keep the connection between the LX_ and inductor as short as possible. Keep the LX_ trace away from noise sensitive traces.

Ensure that the layout for each of the phases is as symmetrical as possible since this yields the best current sharing between the two phases.

The trace from FLED_ to the anode of the FLED_ can be longer, but keeping this trace low impedance is critical for the efficiency of the applications as well as getting heat transferred away from the IC.

Place as much ground as possible around the IC since this enhances the thermal properties of the device.

Chip Information

PROCESS: BiCMOS

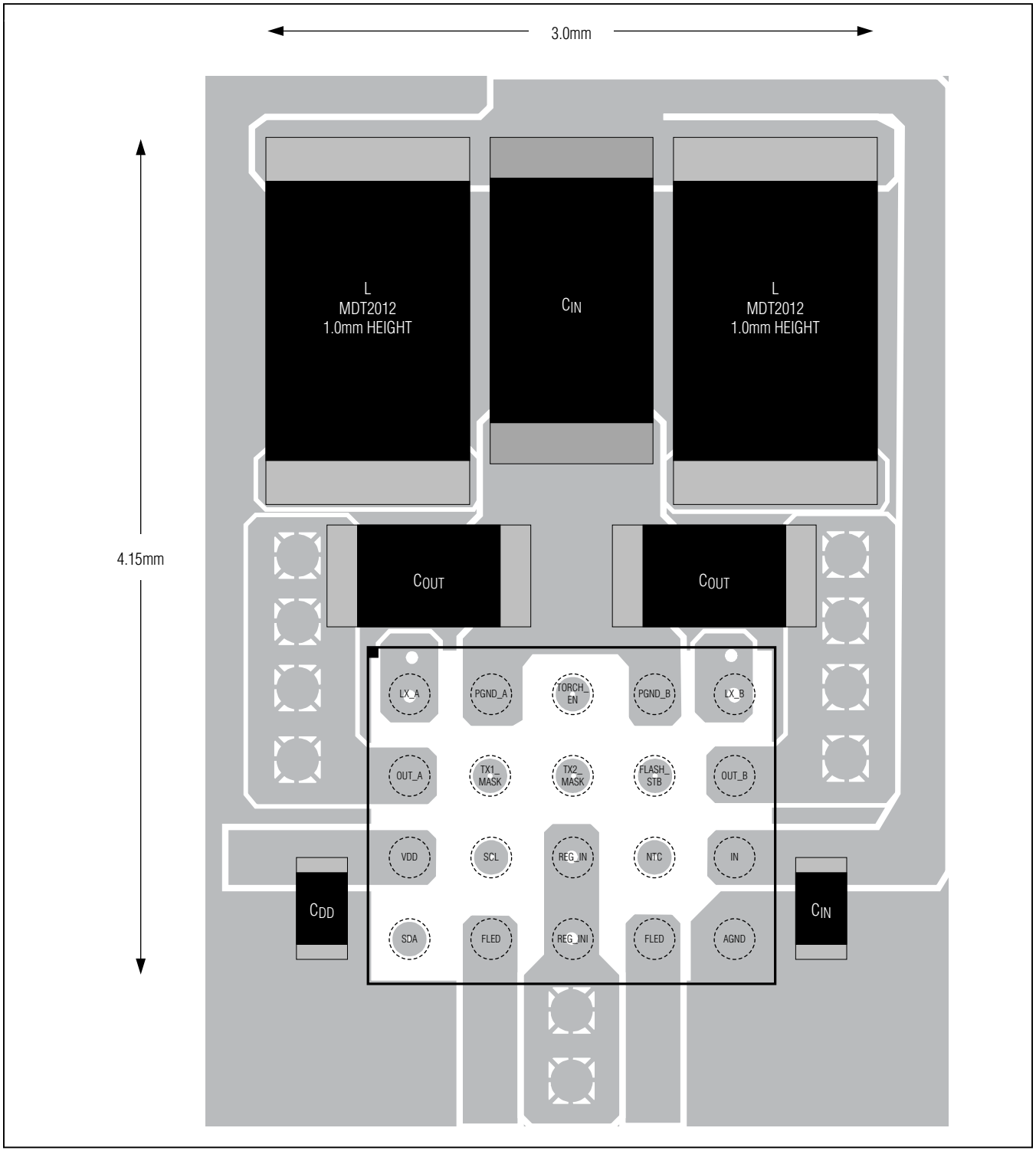
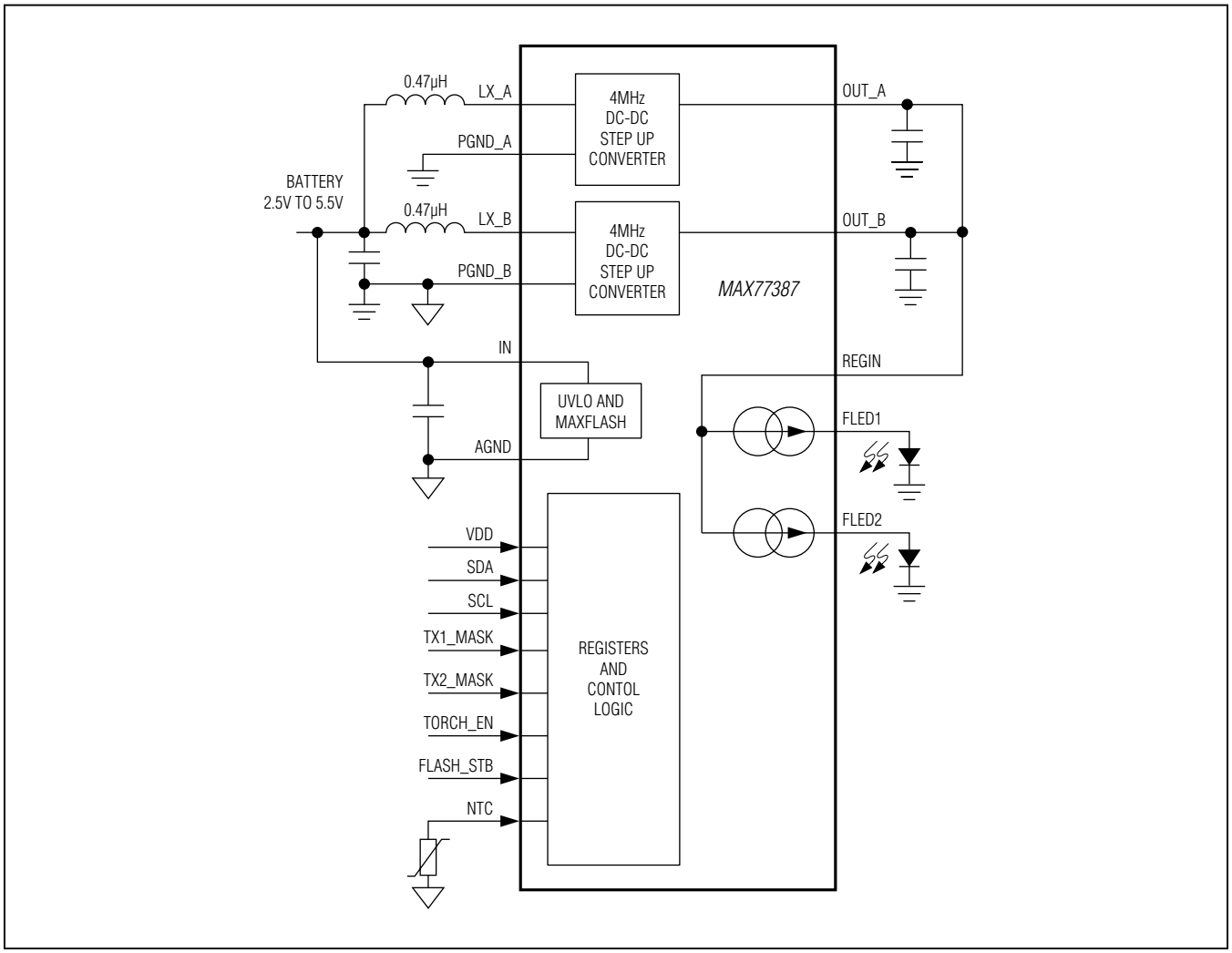


Figure 20. 20-Bump WLP Recommended Layout for 2x1.5A Input Current Limit

Dual-Phase Adaptive DC-DC Step-Up Converter With 2x 1000mA High-Side Current Regulators

Simplified Block Diagram



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77387EWP+T	-40°C to +85°C	20 WLP
MAX77387EWP+	-40°C to +85°C	20 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W201D2+1	21-0544	Refer to Application Note 1891

Dual-Phase Adaptive DC-DC Step-Up Converter With 2x 1000mA High-Side Current Regulators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—

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