INTEGRATED CIRCUITS
UNITRODE

UC1727
UC2727
UC3727

Isolated High Side IGBT Driver

FEATURES

- Receives Power and Signal from Single Isolation Transformer
- Generates Split Rail for 4A Peak Bipolar Gate Drive
- 16V High Level Gate Drive
- Low Level Gate Drive more Negative than -5V
- Undervoltage Lockout
- Desaturation Detection and Fault Processing
- Separate Output Enable Input
- Programmable Stepped Gate Drive for Soft Turn On
- Programmable Stepped Gate Drive for Soft Fault

DESCRIPTION

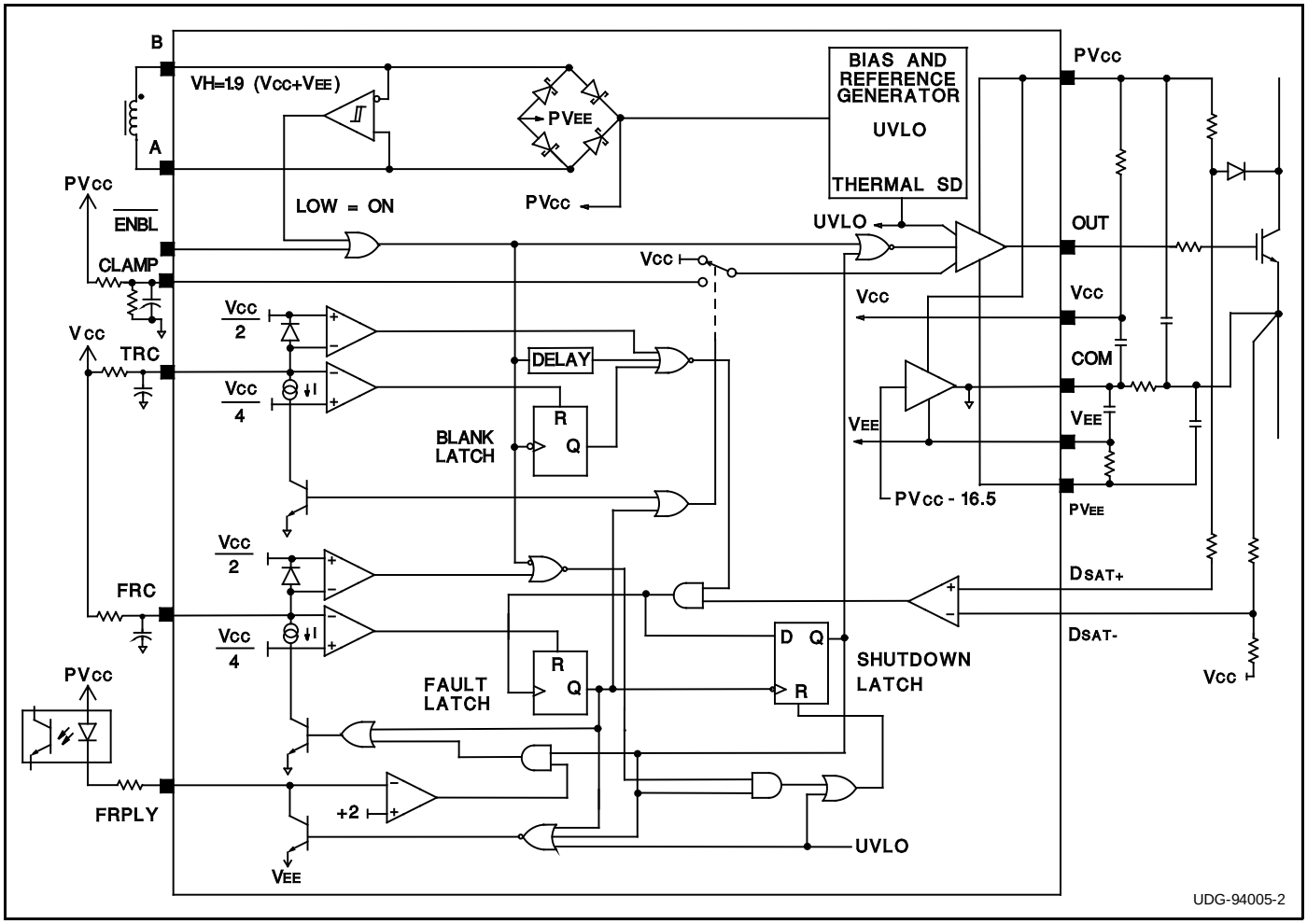
The UC1727 and its companion chip, the UC1726, provide all the necessary features to drive an isolated IGBT transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signal across an isolation boundary with a minimum of external components.

Protection features include under voltage lockout and desaturation detection. High level gate drive signals are typically 16V. Intermediate high drive levels can be programmed for various periods of time to limit surge current at turn on and in the event of desaturation due to a short circuit.

The chip generates a bipolar supply so that the gate can be driven to a negative voltage insuring the IGBT remains off in the presence of high common mode slew rates.

Uses include isolated off-line full bridge and half bridge drives for motors, switches, and any other load requiring full electrical isolation.

BLOCK DIAGRAM



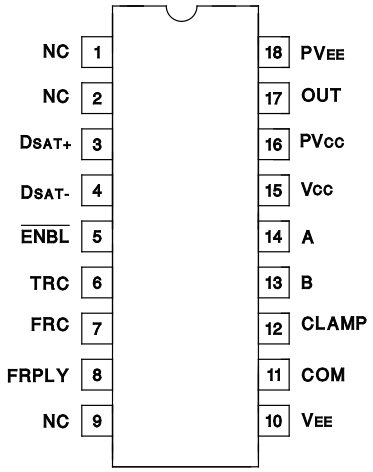
ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC} - V_{EE}) 40V
Power Inputs (|A - B|) 45V
Analog Input Voltage ($\overline{ENBL}$, CLAMP) . . . . . -0.3 To Vcc+0.3
Analog Input Voltage (D_{SAT+}, D_{SAT-}) . . . . . V_{EE}-0.3 to V_{CC}+0.3
Analog Input Current (D_{SAT+}, D_{SAT-}) . . . . . -10 to 10mA
Output Current, |(OUT)|
DC 0.8A
Pulse (0.5µs) 4A
FRPLY Output Current 30mA

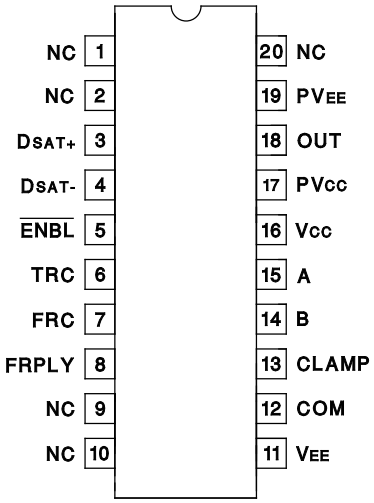
Note: All voltages are with respect to COM. Currents are positive into the specified terminal.

CONNECTION DIAGRAMS

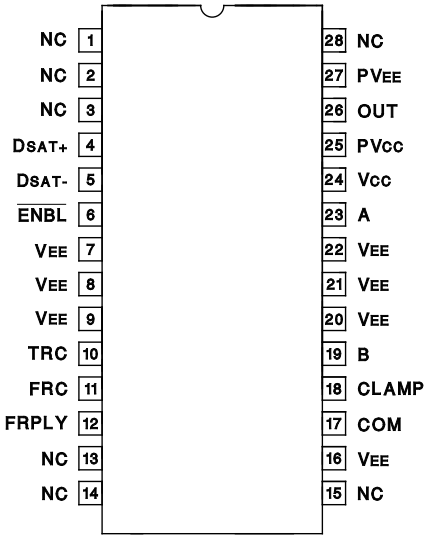
DIL-18 (Top View)
J Package



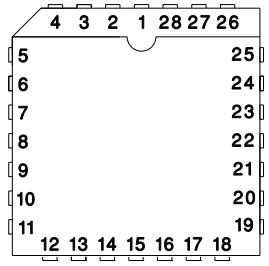
DIL-20 (Top View)
N Package



SOIC-28 (Top View)
DWP Package

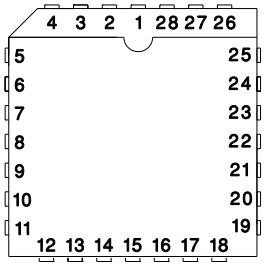


PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
PV_{EE}	12-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26
N/C	27
N/C	28

LCC-28 (Top View)
LP Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
N/C	12-13
PV_{EE}	14
N/C	15-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26-28

See Application Note U-143A "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

A, B: Signal and power input pins. Connect these pins to the secondary of the transformer driven by UC1726.

CLAMP: Analog programming pin for intermediate drive level to be used at turn on or in response to a desaturation event. Requires a bypass capacitor to COM.

COM: Self generated common for bipolar supply. This pin will be 16.5V below PVCC.

DSAT+, DSAT-: Inputs to the desaturation comparator. Desaturation is detected when DSAT+ is greater than DSAT-.

$\overline{\text{ENBL}}$: Negative true enable input. Tie to VCC to disable the chip. Connect to COM to enable the chip. If the $\overline{\text{ENBL}}$ pin is used as the primary input to the chip, connect B to VCC and A to VEE.

FRC: Fault Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential during a desaturation event before it is driven fully low. Also sets the period of time that OUT will be held low before allowing it to be driven high again.

FRPLY: Fault Reply pin. Open collector output. Normally connected to VEE. When desaturation is detected, the pin opens.

OUT: Gate drive output. Connect to gate of IGBT with a series damping resistor greater than 3 ohms.

TRC: Timing Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential and the period of time the desaturation comparator will be ignored during the rising edge.

VCC: Positive supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

VEE: Negative supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

PVEE: Output driver negative supply. Connect to VEE with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

PVCC: Output driver positive supply. Connect to VCC with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, V_{CC} - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Input Receivers					
Forward Diode Drop	I_F = 50mA		0.5	0.65	V
	I_F = 500mA		1.2	2	V
VCC Regulator					
VCC	25 ≤ (VCC - VEE) ≤ 36V, |I(COM)| ≤ 15mA	15.5	16.5	17.5	V
Hysteresis Comparator					
Input Open Circuit Voltage	(Measured with respect to VEE)		12		V
Input Impedance			100		kΩ
Hysteresis		44	47	50	V
Enable Input					
High Level Input Voltage		12			V
Low Level Input Voltage				5	V
Input Bias Current	$\overline{\text{ENBL}}$ = COM		–460	–900	µA
Output Driver					
Saturation to VCC	I(OUT) = -20mA		1.7	2.3	V
Saturation to VCC	I(OUT) = -500mA		2	2.5	V
Saturation to VEE	I(OUT) = 20mA		2	3	V
Saturation to VEE	I(OUT) = 500mA		2.4	3.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, V_{CC} - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Driver (cont.)					
Turn on Clamp Voltage	I(OUT) = -100mA	7	9	11	V
Fault Clamp Voltage	|I(OUT)| = 100mA	8	10	12.5	V
UVLO Saturation to V_{EE}	I(OUT) = 20mA,V_{CC} no connection		2	3	V
Rise and Fall Times	Cl = 1n, CLAMP = V_{CC}, R_{OUT} = 3Ω (Note 1)		75	150	ns
Turn On Sequence Timer					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Blanking Time	(Note 1)	3	5	7	µs
Fault Manager					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Fault Lock Off Time	(Note 1)	15	25	35	µs
FRPLY Saturation	I(FRPLY) = 10mA		1.8	3	V
FRPLY Leakage	FRPLY = V_{CC}		0	10	µA
Desaturation Detection Comparator					
Input Offset Voltage (|vio|)	V_{CM} = V_{EE}+2, V_{CM} = V_{CC}-2		0	20	mV
Input Bias Current			–1.5	10	µA
Delay to Output	C(FRC) = 0 (Note 1)		150		ns
Undervoltage Lock Out					
V_{CC} Threshold		14	15.5	17	V
V_{CC} Hysteresis			0.35		V
V_{EE} Threshold		–4.5	–5.5	–6.5	V
V_{EE} Hysteresis		0.5	1	1.5	V
Thermal Shutdown					
Threshold	Not tested		175		°C
Hysteresis	Not tested		45		°C
Total Standby Current					
I(V_{CC})			24	30	mA

Note 1: Guaranteed by design, but not 100% tested in production.

APPLICATION INFORMATION

Figure 1 shows the rectification and detection scheme used in the UC1727 to derive both power and signal information from the input waveform. V_{CC}-V_{EE} is generated by peak detecting the input signal via the internal bridge rectifier and storing it on external capacitors. COM is generated by an internal amplifier that maintains PV_{CC}-COM = 16.5V.

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (or resetting) the comparator only if the input signal exceeds 0.95 $|V_{CC}-V_{EE}|$. In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator as shown in Figure 3.

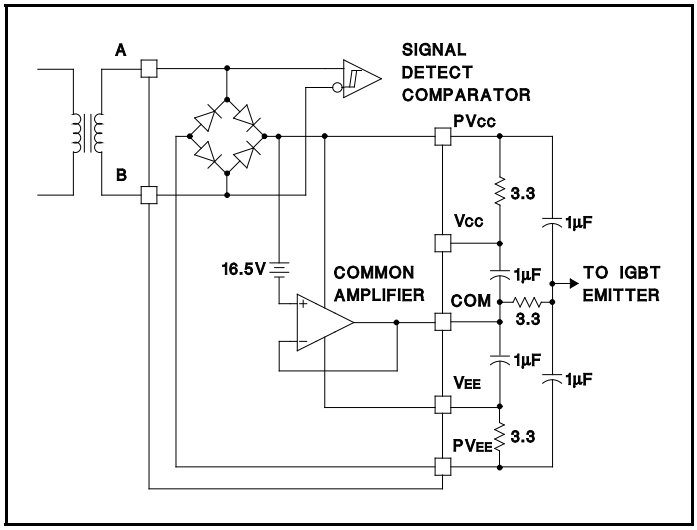


Figure 1. Input Stage & Bipolar Supply

APPLICATION INFORMATION (cont.)

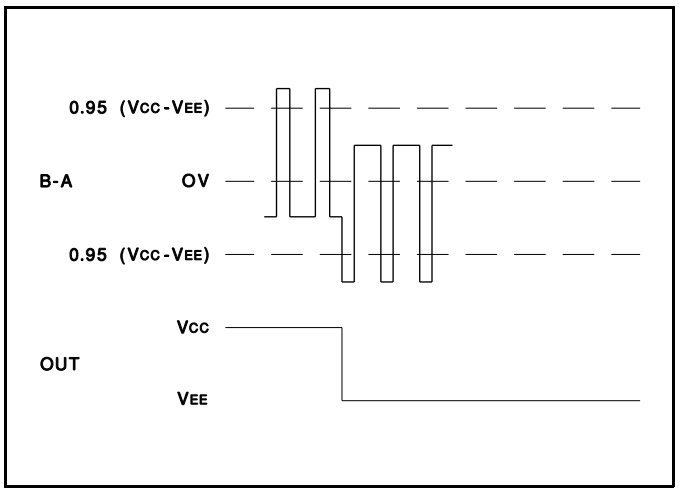


Figure 2. Input Waveform

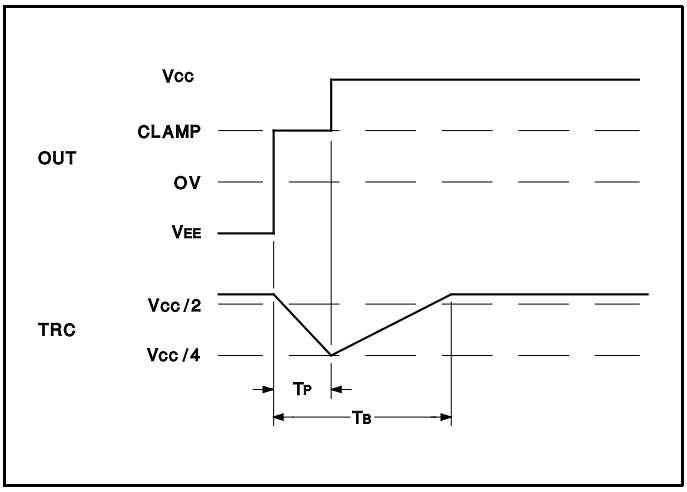


Figure 4. Rising Edge Waveform

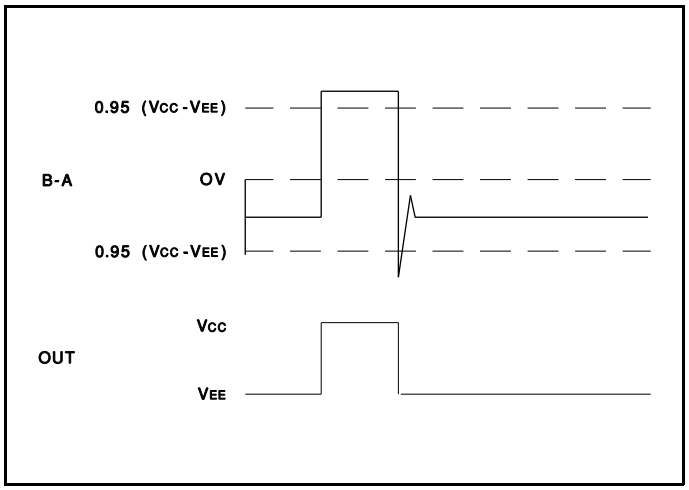


Figure 3. Output Pulsing Caused By Transformer Ringing

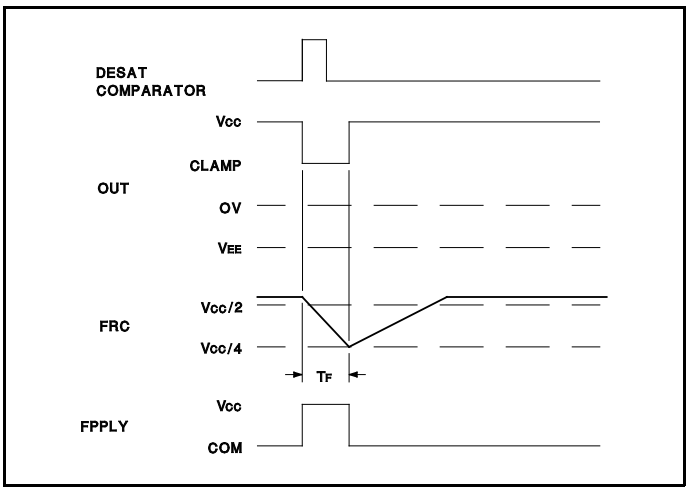


Figure 5. Transient Desaturation Response

GATE DRIVE WAVEFORM

The rising edge of OUT can be programmed for a two step sequence as shown in Figure 4. The plateau voltage is programmed by a resistive divider from VCC to COM applied at CLAMP. CLAMP must be bypassed to COM. The plateau voltage is approximately OUT = CLAMP. The plateau time is set by a resistor from TRC to VCC and a capacitor to COM as:

$$Tp = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

TRC also programs a blanking time during which the chip ignores the desaturation comparator. The blanking time is:

$$Tb = Tp + 0.4RC.$$

In the event that desaturation is detected outside the blanking interval, OUT will be driven back to the CLAMP plateau for a fault time set by a resistor from FRC to VCC and a capacitor to COM as:

$$Tf = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

If the event is transient, OUT will return high at the end of Tf as shown in Figure 5. During Tf, FRPLY is open. After Tf, FRPLY is connected to COM.

Desaturation shown in Figure 6 that persists longer than Tf will cause OUT to be driven low. The chip will not accept a command to drive OUT high for a delay period of

$$Td = 0.4RC$$

FRPLY will be open during this entire period.

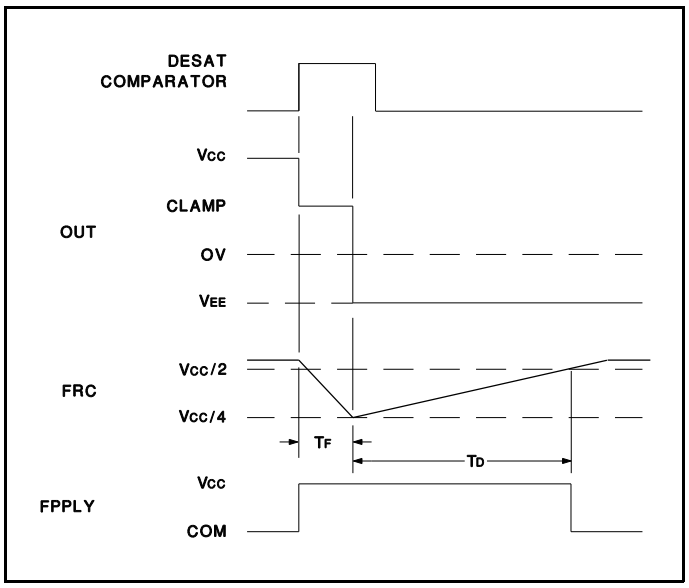


Figure 6. Desaturation Response

ENABLE

$\overline{\text{ENBL}}$ provides an alternate means of controlling the output. If $\overline{\text{ENBL}}$ is used as the primary input, B must be connected to VCC and A to VEE. $\overline{\text{ENBL}}$ can be driven by the output of an optoisolator from $\overline{\text{ENBL}}$ to COM as shown in Figure 7. If $\overline{\text{ENBL}}$ is not used, it should be connected to COM.

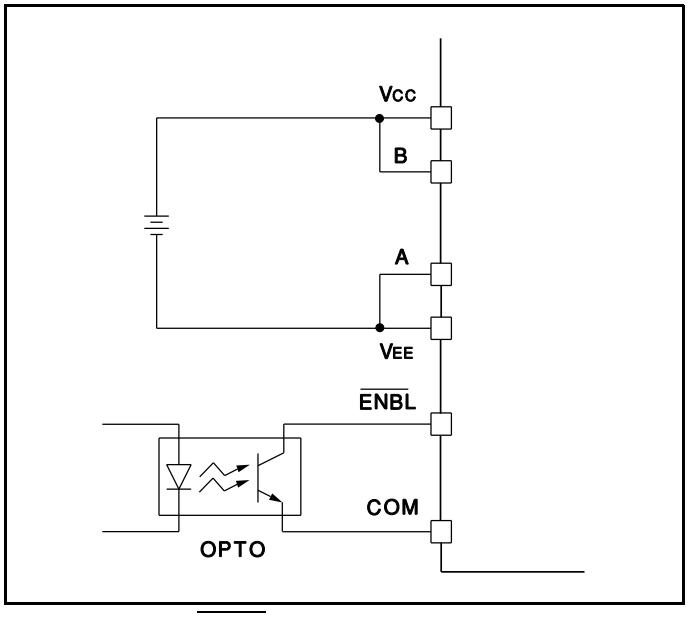


Figure 7. Using $\overline{\text{ENBL}}$ as Primary Input

EXTERNAL BIPOLAR SUPPLIES

If it is desired to drive an emitter grounded IGBT from external supplies, the configuration in Figure 8 should be used. COM should never be connected to ground. VCC must be ≥ 12V and VCC-VEE must be ≥ 23.5V.

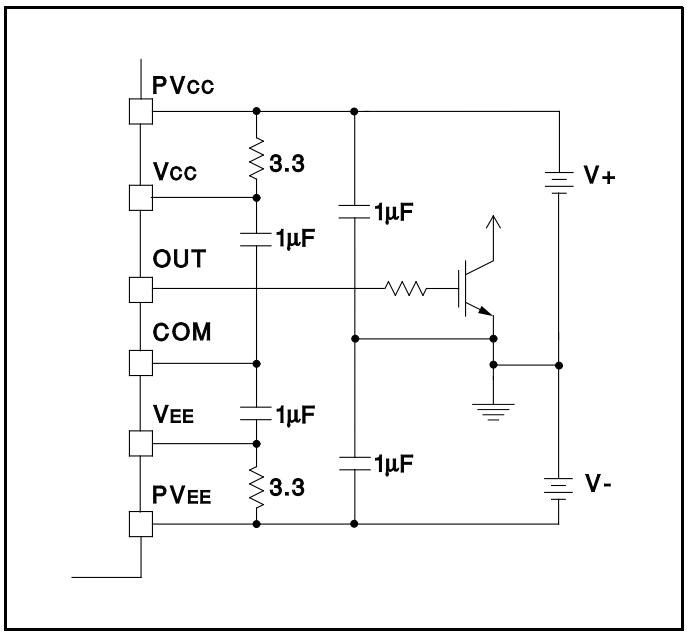


Figure 8. Using External Supplies

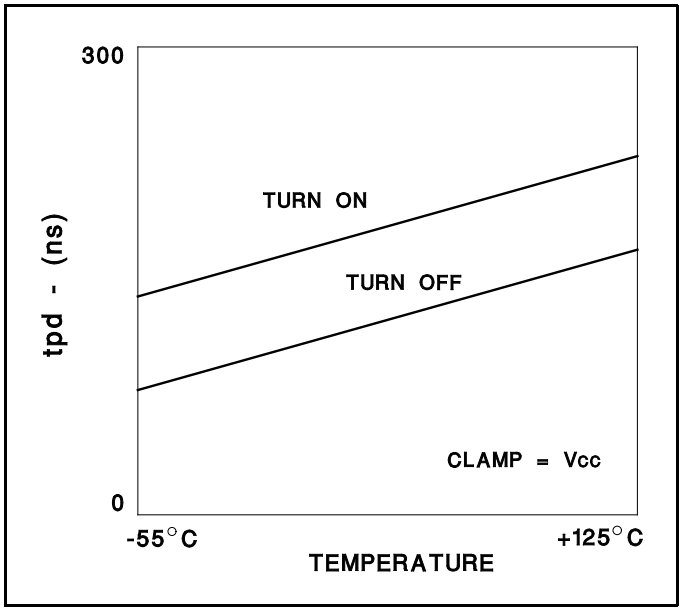


Figure 9. Input to Output Delay

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