

CD4069UB Types

CMOS Hex Inverter

High-Voltage Types (20-Volt Rating)

■ CD4069UB types consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

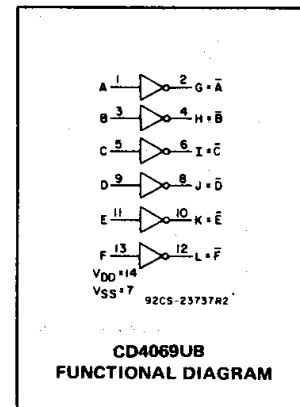
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation— $t_{PHL}, t_{PLH} = 30$ ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	 -0.5V to +20V
Voltages referenced to V_{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	 -0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	 ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	 500 mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	 Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	 100 mW
OPERATING-TEMPERATURE RANGE (T_A)	 -55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	 -65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 $\pm$ 0.79 mm) from case for 10s max	 $+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20$ ns,

$C_L = 50$ pF, $R_L = 200$ K Ω

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
		V _{DD} V			
			Typ.	Max.	
Propagation Delay Time; t _{PLH} , t _{PHL}		5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time; t _{THL} , t _{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance; C _{IN}		Any Input	10	15	pF

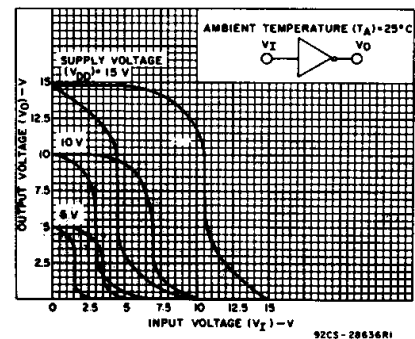


Fig. 1 — Minimum and maximum voltage transfer characteristics.

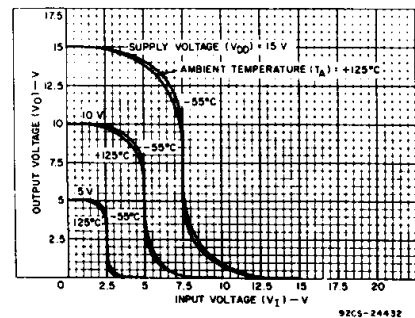


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

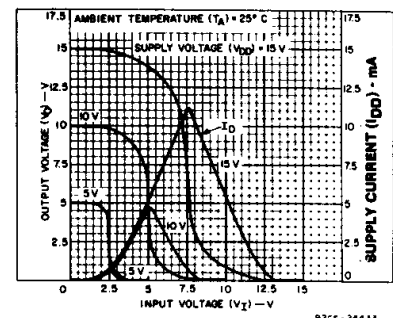


Fig. 3 — Typical current and voltage transfer characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0,15	15	1	1	30	30	—	0.01	1	
	—	0,20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	5	5	0.05				—	0	0.05	V
	—	10	10	0.05				—	0	0.05	
	—	15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0	5	4.95				4.95	5	—	V
	—	0	10	9.95				9.95	10	—	
	—	0	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	4.5	—	5	1				—	—	1	V
	9	—	10	2				—	—	2	
	13.5	—	15	2.5				—	—	2.5	
Input High Voltage, V _{IH} Min.	0.5	—	5	4				4	—	—	V
	1	—	10	8				8	—	—	
	1.5	—	15	12.5				12.5	—	—	
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

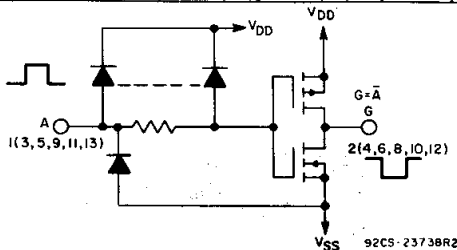


Fig. 6 – Schematic diagram of one of six identical inverters.

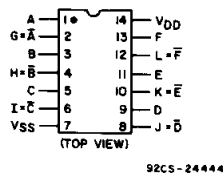


Fig. 7 – CD4069UB terminal assignment.

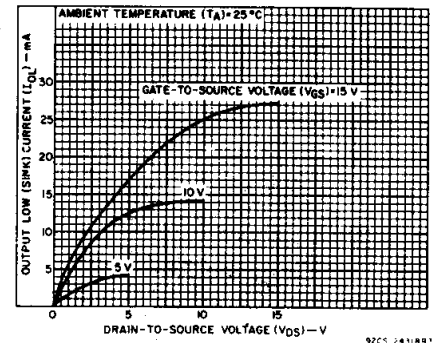


Fig. 4 – Typical output low (sink) current characteristics.

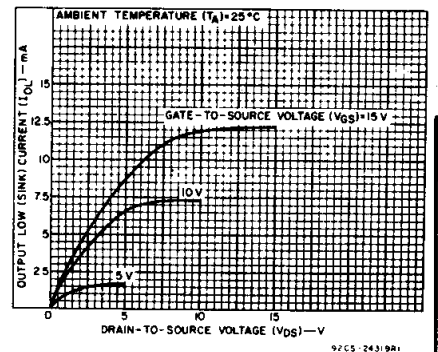


Fig. 5 – Minimum output low (sink) current characteristics.

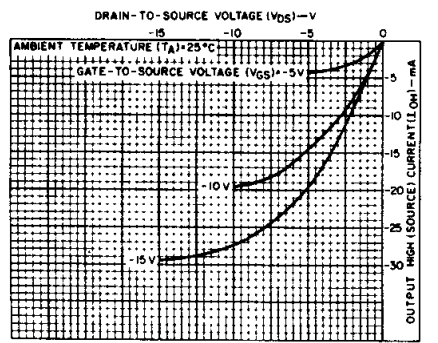


Fig. 8 – Typical output high (source) current characteristics.

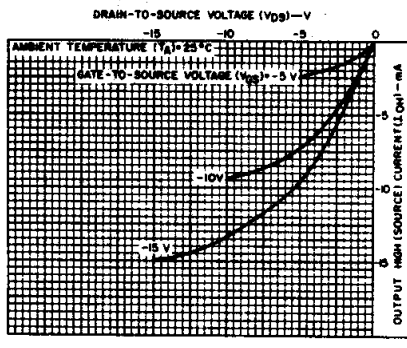


Fig. 9 – Minimum output high (source) current characteristics.

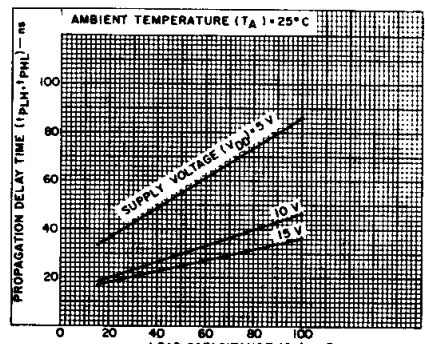


Fig. 10 – Typical propagation delay time vs. load capacitance.

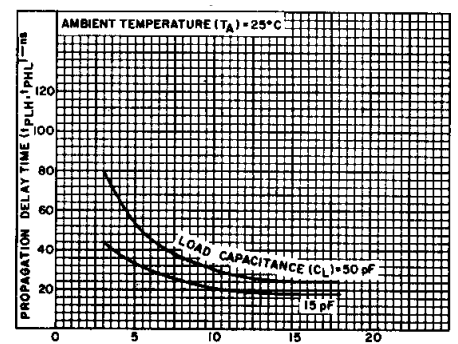


Fig. 11 – Typical propagation delay time vs. supply voltage.

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HIGH VOLTAGE ICs

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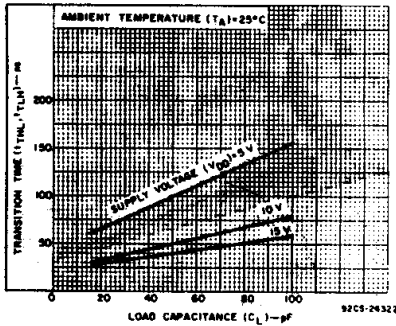


Fig. 12 - Typical transition time vs. load capacitance.

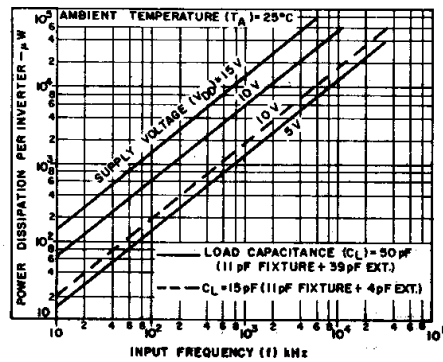


Fig. 13 - Typical dynamic power dissipation vs. frequency.

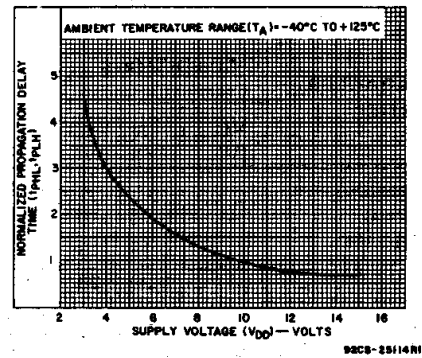


Fig. 14 - Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

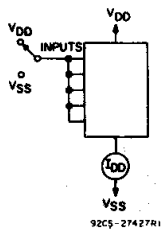


Fig. 15 - Quiescent device current test circuit.

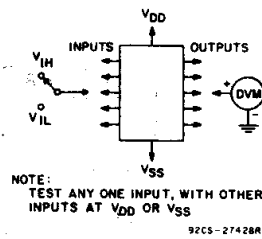


Fig. 16 - Noise immunity test circuit.

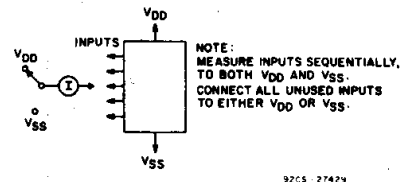


Fig. 17 - Input leakage current test circuit.

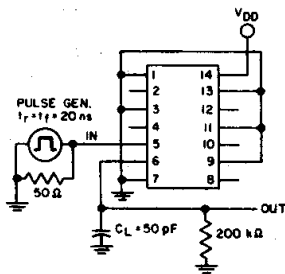


Fig. 18 - Dynamic electrical characteristics test circuit and waveforms.

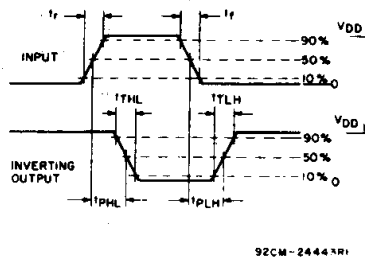


Fig. 19 - Typical crystal oscillator circuit.

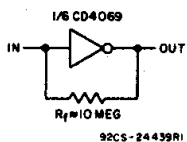


Fig. 20 - High-input impedance amplifier.

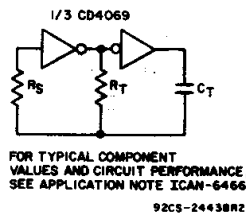


Fig. 21 - Typical RC oscillator circuit.

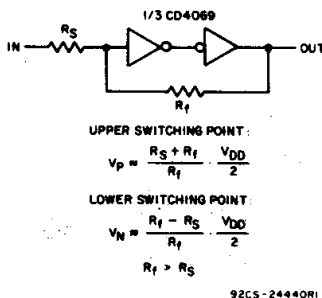


Fig. 22 - Input pulse shaping circuit (Schmitt trigger).

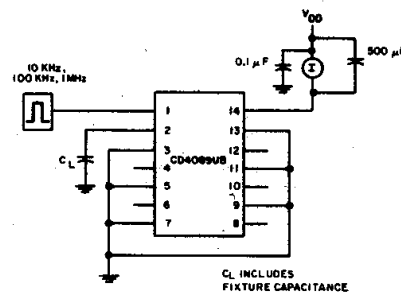
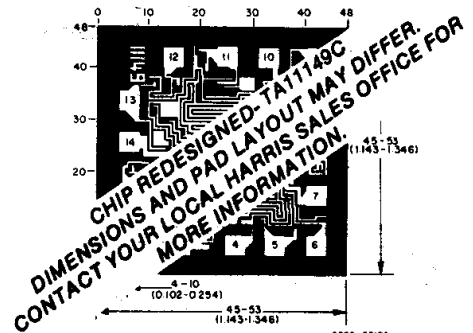


Fig. 23 - Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4069UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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