19-4973; Rev 2; 4/12

EVALUATION KIT AVAILABLE

8.5Gbps Quad Equalizer and Preemphasis Driver

MAX3987

General Description

The MAX3987 is a 4-channel receive and transmit equalizer (EQ). It compensates for transmission medium losses encountered with FR4 stripline/microstrip and/or high-speed cable. The device can be used at the beginning, middle, or end of a channel. The input equalization requires no setting, and the output preemphasis (PE) is programmable.

For each channel, the preemphasis level, output drive level, output polarity, and powering down of unused outputs are programmable through an I²C serial interface. It can also be configured globally through pins.

The device operates from a 2.5V or 3.3V supply, and is packaged in a 7mm x 7mm, 48-pin TQFN.

Applications

Preemphasis and Receive Equalization

Redrive

FR4 and Cable Equalization

XAUI and XAUI2, Fibre Channel, Interlaken, InfiniBand™/SM, SAS-2 and SATA Revision 3 OOB

PCIe® Compatible

InfiniBand is a trademark/service mark of InfiniBand Trade Association.

PCIe is a registered trademark of PCI-SIG Corp.

Features

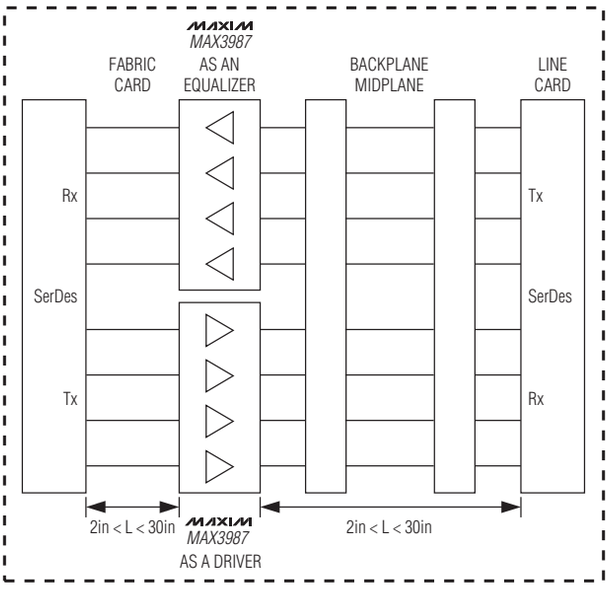
- **Up to 8.5Gbps NRZ Data Speed**
- **Receive Equalization Up to 30in FR4**
- **Preemphasis Drive Up to 30in FR4**
- **Global and Individual Programming of Preemphasis, Output Drive Levels, Polarity Inversion, and Offset Cancellation**
- **Signal Detect and Internal Output Squelch**
- **Compliant with SAS-2 and SATA Revision 3 OOB**
- **Coding Independent, 8B/10B, 64B/66B, Scrambled, and Others**
- **Differential CML Data-Output Drive**
- **I²C Serial Interface and Pin Programmable**
- **Software Power-Down of Unused Outputs**
- **0.5W Typical Power Dissipation for Drive Level 1 at V_{CC} = 2.5V**
- **High-Performance, Lead-Free, 7mm x 7mm, 48-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3987ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Application Circuit



8.5Gbps Quad Equalizer and Preemphasis Drive

ABSOLUTE MAXIMUM RATINGS

Termination Supply Voltage Range .....-0.5V to +3.9V
Signal Voltage Range on Any One Signal Wire (TTL) ..... -0.5V to (V_{CC} + 0.3V)
Signal Voltage Range on Any One Signal Wire (CML) ..... -0.5V to (V_{CC} + 0.3V)
CML Output Loading (Shorted to Ground).....90mA
Operating Ambient Temperature Range ..... -40°C to +85°C
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 27.8mW/°C above +70°C).....2.22W
Storage Ambient Temperature Range ..... -65°C to +150°C
ESD Human Body Model, Any Pin..... ±2000V
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATION TABLES

(Typical values measured at V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified.)

OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	2.5V supply	2.375	2.5	2.625	V
	3.3V supply	2.97	3.3	3.63	
Operating Ambient Temperature	2.5V supply	0	+25	+85	°C
	3.3V supply	-40	+25	+85	
Supply Noise Tolerance	100kHz ≤ f < 200MHz		50		mV_{P-P}
AC Common-Mode Noise at the Input	2MHz ≤ f < 200MHz			150	mV_{P-P}
Bit Rate	NRZ data (Note 2)			8.5	Gbps
CID	Consecutive identical digits (bits)			100	Bits
Time to Reach 50% Mark/Space Ratio	For continuous traffic			1	µs
DC-Blocking Capacitor	For bursty traffic such as SAS/SATA			12	nF

SUPPLY CHARACTERISTICS: 2.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		-5%	2.5	+5%	V
Supply Current	I_{CC}	Four outputs in level 3 drive; squelch turned on		320	385	mA
		Four outputs in level 3 drive; squelch turned off		306	365	
		Four outputs in level 2 drive; squelch turned on		286	340	
		Four outputs in level 2 drive; squelch turned off		271	325	
		Four outputs in level 1 drive; squelch turned on		235	280	
		Four outputs in level 1 drive; squelch turned off		221	265	
Inrush Current	ΔI_{CC}	(Note 3)			+10	%
Power-On Delay	$t_{POWERON}$	(Note 3)			100	ms

SUPPLY CHARACTERISTICS: 3.3V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		-10%	3.3	+10%	V
Supply Current	I_{CC}	Four outputs in level 3 drive; squelch turned on		370	445	mA
		Four outputs in level 3 drive; squelch turned off		354	430	
		Four outputs in level 2 drive; squelch turned on		334	405	
		Four outputs in level 2 drive; squelch turned off		318	390	
		Four outputs in level 1 drive; squelch turned on		272	330	
		Four outputs in level 1 drive; squelch turned off		257	315	
Inrush Current	ΔI_{CC}	(Note 3)			+10	%
Power-On Delay	$t_{POWERON}$	(Note 3)			100	ms

LVCMOS INPUT

(ADDR[4:1], I2C_EN, SDSF, SQ, OC_EN, TX_EN, TX_LV0, TX_LV1, TX_PE0, TX_PE1, RESET, TEST.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage High	V_{IH}	V_{CC} = 2.5V ±5%, 3.3V ±10%	0.7 x V_{CC}		V_{CC} + 0.3	V
Input-Voltage Low	V_{IL}	V_{CC} = 2.5V ±5%, 3.3V ±10%	-0.3		0.3 x V_{CC}	V
Input Current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or GND	-200		+200	µA

HIGH-SPEED INPUTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Any Input to Any Output	t_{PD}	Output at level 3		250		ps
Output Channel-to-Channel Delay Skew	t_{SKEW}	Output at level 3 (Note 4)		20	40	ps
Input Sensitivity at the Device Pin (Note 5)	$V_{SENSITIVITY}$ (Point B in Figure 2)	Offset cancellation off			75	mV_{P-P}
		Offset cancellation on			50	
Residual Deterministic Jitter: 6.5Gbps (Notes 6, 7, 9)	DJ_{RX}	Less than 2in FR4 at the output; max reach 24in FR4; Maxim stress pattern (Note 8)		0.1	0.2	UI
		Less than 2in FR4 at the output; max reach 30in FR4; PRBS7 pattern		0.07		

8.5Gbps Quad Equalizer and Preemphasis Drive

HIGH-SPEED INPUTS (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Residual Deterministic Jitter: 7.5Gbps (Notes 6, 7, 9)	DJ_{RX}	Less than 2in FR4 at the output; max reach 24in FR4; Maxim stress pattern (Note 8)		0.12	0.26	UI
		Less than 2in FR4 at the output; max reach 24in FR4; PRBS7 pattern		0.07		
Residual Deterministic Jitter: 8.5Gbps (Notes 6, 7, 9)	DJ_{RX}	Less than 2in FR4 at the output; max reach 20in FR4; Maxim stress pattern (Note 8)		0.10	0.22	UI
		Less than 2in FR4 at the output; max reach 20in FR4; PRBS7 pattern		0.1		
Squelch-Deassert Voltage for Slow Response Signal Detect (Notes 8 to 11)	$V_{SQ\_DEAS\_S}$	SDL = 0			120	mV_{P-P}
		SDL = 1 (default state)			170	
Squelch-Deassert Voltage for Fast Response Signal Detect (Notes 9, 11, 12, 13)	$V_{SQ\_DEAS\_F}$	SDL = 0			155	mV_{P-P}
		SDL = 1 (default state)			220	
Squelch-Assert Voltage for Slow Response Signal Detect (Notes 8 to 11)	$V_{SQ\_AS\_S}$	SDL = 0	50			mV_{P-P}
		SDL = 1 (default state)	100			
Squelch-Assert Voltage for Fast Response Signal Detect (Notes 9, 11, 12)	$V_{SQ\_AS\_F}$	SDL = 0	65			mV_{P-P}
		SDL = 1 (default state)	120			
Signal Detect and Squelch Delay (Note 14)	t_{SD_SQ}	Slow-signal detect and squelch is enabled (Note 8)		200		ns
		Fast-signal detect and squelch is enabled (Note 12)		2.5	5.4	
Voltage Input Swing Launched Differentially at the Source (Point A in Figure 2 before the signal encountering any loss)	V_{LAUNCH}	Offset cancellation off	400		1800	mV_{P-P}
		Offset cancellation on	200		1800	
Input Resistance	R_{IN}	Between signal and V_{CC}		50		Ω
Differential Input Return Loss	SDD11	TQFN, 100MHz to 4.25GHz		17		dB

HIGH-SPEED OUTPUTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Residual Deterministic Jitter: 6.5Gbps (Notes 6, 8, 9, 15, 16, 17)	DJ_{TX}	PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 18in FR4; PE = 11, up to 30in FR4; Maxim stress pattern		0.15	0.20	UI
		PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 18in FR4; PE = 11, up to 30in FR4; PRBS7 pattern		0.09		
Residual Deterministic Jitter: 7.5Gbps (Notes 6, 8, 9, 15, 16, 17)	DJ_{TX}	PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 16in FR4; PE = 11, up to 24in FR4; Maxim stress pattern		0.15	0.23	UI
		PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 16in FR4; PE = 11, up to 24in FR4; PRBS7 pattern		0.12		
Residual Deterministic Jitter: 8.5Gbps (Notes 6, 8, 9, 15, 16, 17)	DJ_{TX}	PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 18in FR4; PE = 11, up to 24in FR4; Maxim stress pattern		0.10	0.15	UI
		PE = 00, up to 2in FR4; PE = 01, up to 10in FR4; PE = 10, up to 18in FR4; PE = 11, up to 24in FR4; PRBS7 pattern		0.06		
Serial-Data Output Rise and Fall Time	t_R/t_F	20% to 80% of settled value; level 3 drive (Note 4)	30		50	ps
Differential Output Swing: Level 1 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 2.5V ±5% (Notes 4, 10)	530	600	660	mV_{P-P}
Differential Output Swing: Level 2 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 2.5V ±5% (Notes 4, 10)	740	840	930	mV_{P-P}
Differential Output Swing: Level 3 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 2.5V ±5% (Notes 4, 10)	900	1000	1150	mV_{P-P}
Differential Output Swing: Level 1 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 3.3V ±10% (Notes 4, 10)	530	630	730	mV_{P-P}
Differential Output Swing: Level 2 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 3.3V ±10% (Notes 4, 10)	750	900	1050	mV_{P-P}
Differential Output Swing: Level 3 Drive	V_{AC_OUT}	When output is enabled; PE = 00; V_{CC} = 3.3V ±10% (Notes 4, 10)	900	1100	1250	mV_{P-P}
Differential Output Swing: AC Output Disabled	V_{AC_OUT}	When output is powered down; input at 7.5Gbps with D24.3 pattern			50	mV_{P-P}
AC Common-Mode Voltage Change	V_{AC_COM}	(Note 18)			40	mV_{P-P}
DC Common-Mode Voltage Change	V_{DC_COM}	(Note 19)	-25		+25	mV_{P-P}

8.5Gbps Quad Equalizer and Preemphasis Drive

HIGH-SPEED OUTPUTS (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Average DC Offset Voltage Change	ΔV_{OFFSET}	(Note 20)	-25		+25	mV_{P-P}
Output Resistance	R_{OUT}	Between signal and V_{CC}		50		Ω
Differential Output Return Loss	SD22	100MHz to 4.25GHz; output on; PE = 11, LV = 10		17		dB
Random Jitter	t_{RJ}	(Note 21)			1	ps_{RMS}
Channel Isolation	SDD_{ISO}	Up to 5GHz (Note 22)		38		dB

I²C CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		-0.5		0.3 x V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.5	V
Low-Level Output Voltage	V_{OL1}	At I_{OL} = 3mA sink current	0		0.4	V
		I_{OL} = 6mA	0		0.6	
SDATA Leakage Current	$I_{LEAKAGE}$	I²C output high	0		10	µA
Output Fall Time V_{IHMAX} to V_{ILMAX}	t_{OF}		60		250	ns
Input Current Each I/O Pin	I_I	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		+10	µA
SCLK Clock Frequency	f_{SCL}				400	kHz

Note 1: 2.5V covers 0°C to +85°C, and 3.3V covers -40°C to +85°C.

Note 2: With offset cancellation off, the minimum data rate is limited by the DC-blocking capacitor value; with offset cancellation on, the minimum data rate is limited above 1Gbps.

Note 3: Supply voltage ramp-up time of less than 200µs. Power-on delay interval measured from the 50% level of the final voltage at the device side of filter to 50% of final current. See Figure 1 for a typical supply filter.

Note 4: Guaranteed by design and characterization with a K28.7 pattern at 7.5Gbps, PE = 00.

Note 5: Minimum input amplitude to generate full output swing (PE = 00, squelch disabled). Guaranteed by design and characterization with 1010 clock pattern at 6Gbps. Input sensitivity can be frequency dependent because of the input equalization network. Outputs reach within 90% of settled value at level 3 drive.

Note 6: Difference in deterministic jitter between reference data source and equalizer output. Residual DJ = Output DJ - Source DJ. The deterministic jitter at the output of the transmission line must be from media-induced loss and not from clock source modulation.

Note 7: Input signal at point A in Figure 2. No more than 2in FR4 at the output. PE setting = 00, output drive at level 3, offset cancellation off. Signal is applied differentially at input to a 6-mil wide, loosely coupled microstrip up to 30in.

Note 8: Maxim stress pattern is 464 bits: PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.

Note 9: All four channels are populated with traffic of the same data pattern to the channel under test with outputs set at level 3.

Note 10: Guaranteed by test at 7.5Gbps.

Note 11: Less than 2in FR4 at the input and less than 2in FR4 at the output.

Note 12: Guaranteed at 1.5Gbps and 3Gbps.

Note 13: Tested with ALIGN (0) pattern at 6.0Gbps.

Note 14: For the channel under test, time from the input differential peak-to-peak level rising above the squelch-deassert voltage (dropping below the squelch-assert voltage) to the output data reaching 90% of maximum differential peak-to-peak level for input transition from idle to active (10% of maximum differential peak-to-peak level for inputs transition from active to idle). Squelch of individual output is completed (see Figure 3).

Note 15: No more than 2in FR4 at the input. Output drive is applied differentially to a 6-mil wide, loosely coupled differential microstrip up to 30in. Output measured at the point C in Figure 4. Input level = $100mV_{P-P}$.

Note 16: The output PE level is defined as the ratio of peak-to-peak voltage of a transition bit to the peak-to-peak voltage of a non-transition bit.

Note 17: For lowest (level 1) drive, Tx DJ spec must be met for PE = 00 and 01 only.

Note 18: PE = maximum preemphasis, load is 50Ω ±1% at each side, output is configured for level 3 drive. The pattern is 11001100 (50% edge density) at 7.5Gbps. AC common-mode output is computed as:

$$V_{AC\_COM} = ((V_P + V_N)/2 - V_{DC\_COM})$$

where:

V_P = time-domain voltage measured at true terminal

V_N = time-domain voltage measured at complementary terminal

V_{DC_COM} = DC common-mode voltage $(V_P + V_N)/2$

Note 19: The maximum difference in the average DC voltage (V_{DC_COM} - DC common-mode voltage $(V_P + V_N)/2$) component between data present and output on, and data absent and output squelched. PE = lowest preemphasis, load is 50Ω ±1% at each side, output is configured for level 3 drive.

Note 20: The maximum difference in the average differential voltage (DC offset) component between data present and output on, and data absent and output squelched. PE = lowest preemphasis, load is 50Ω ±1% at each side, output is configured for level 3 drive.

Note 21: Guaranteed by design and characterization with a K28.7 pattern at 7.5Gbps with 100mV_{P-P} input swing. Output set at level 3 drive, offset cancellation off.

Note 22: Measured using a vector-network analyzer (VNA). The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω. The obtained value excludes the forward gain of the victim amplifier.

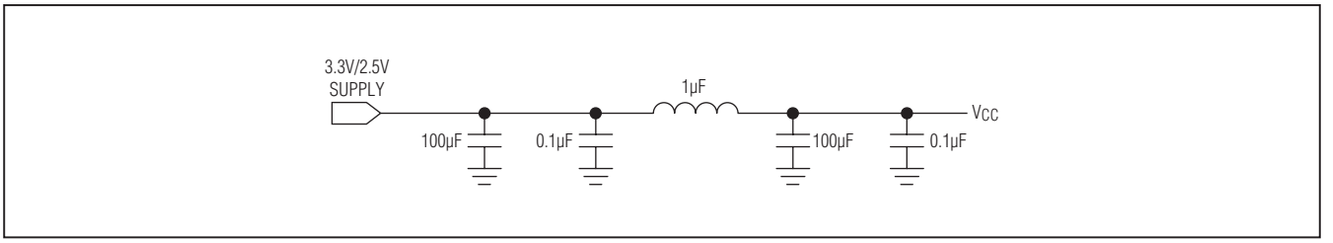


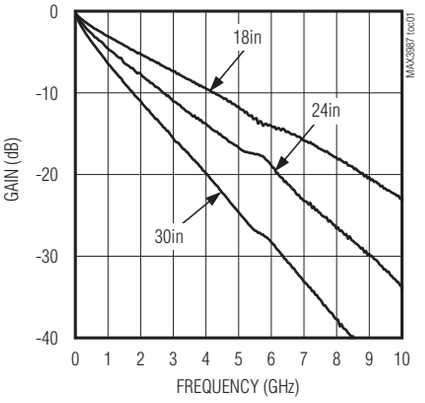
Figure 1. Recommended Supply Filtering

8.5Gbps Quad Equalizer and Preemphasis Drive

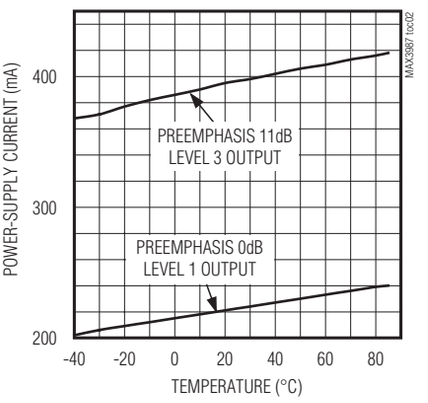
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

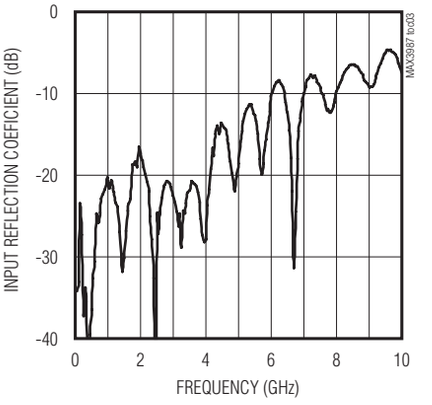
LOSS MEASUREMENT OF TRACE BOARDS (INPUT POWER OF 0dBm)



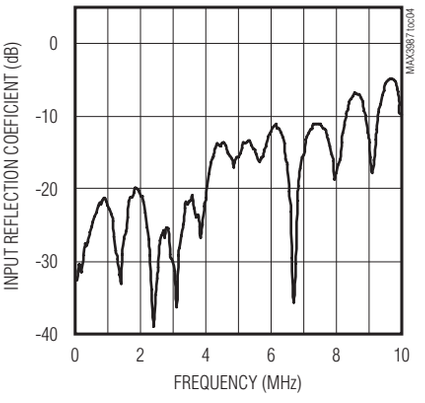
POWER-SUPPLY CURRENT vs. TEMPERATURE (V_{CC} = 3.3V)



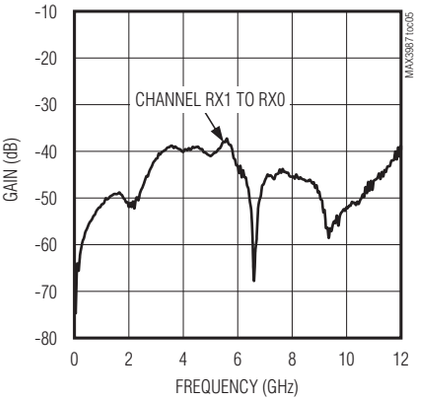
INPUT RETURN GAIN (SDD11) (INPUT POWER OF -40dBm)



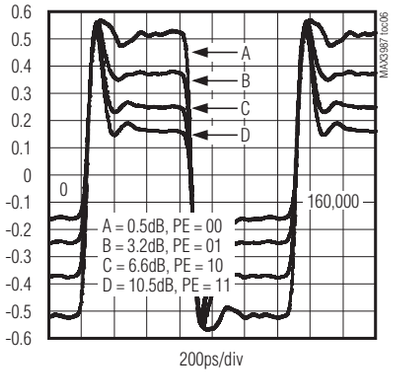
INPUT RETURN GAIN (SDD22) (INPUT POWER OF -40dBm)



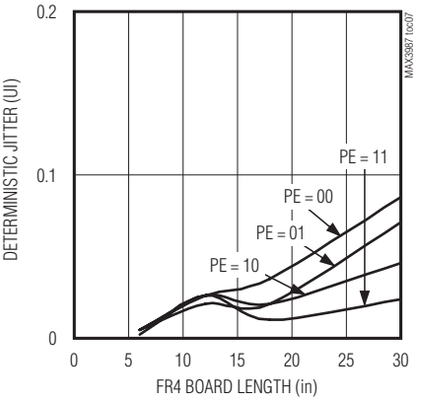
INPUT CHANNEL-TO-CHANNEL ISOLATION (INPUT POWER OF 0dBm, PART ENABLED)



TRANSIENT RESPONSE (3.125Gbps 1010 PATTERN, LV = 10)



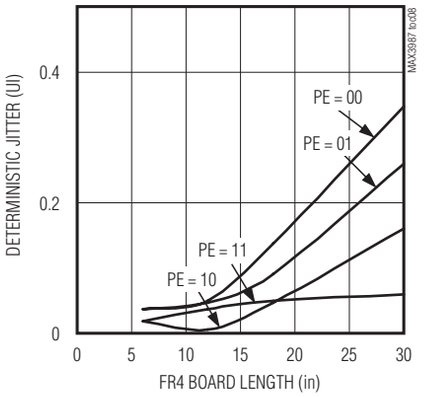
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 200mV$_{P-P}$, MAXIM STRESS PATTERN, DATA RATE = 1.25Gbps)



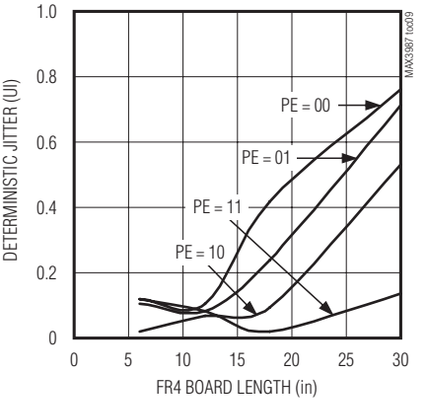
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

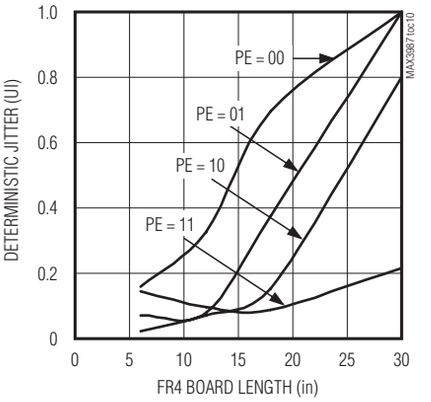
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 200mV$_{P-P}$, MAXIM STRESS PATTERN, DATA RATE = 3.25Gbps)



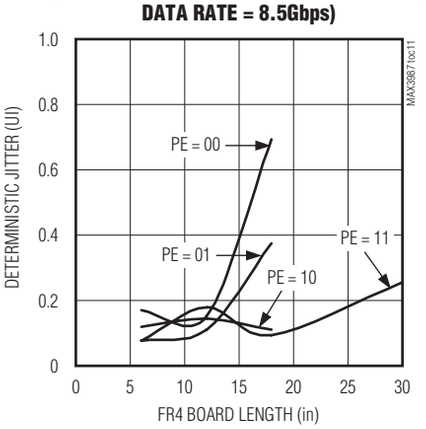
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 200mV$_{P-P}$, MAXIM STRESS PATTERN, DATA RATE = 6.25Gbps)



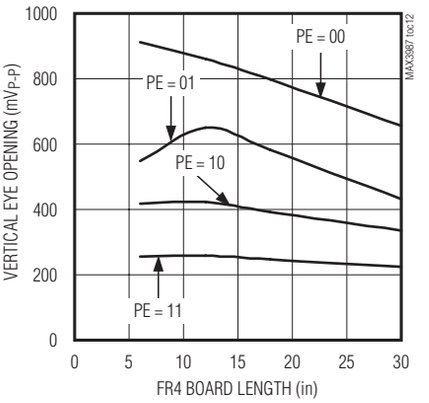
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 200mV$_{P-P}$, MAXIM STRESS PATTERN, DATA RATE = 7.5Gbps)



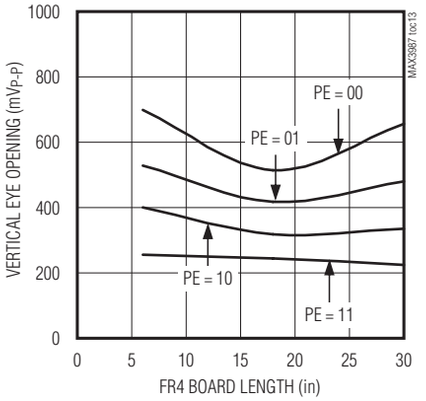
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 200mV$_{P-P}$, MAXIM STRESS PATTERN, DATA RATE = 8.5Gbps)



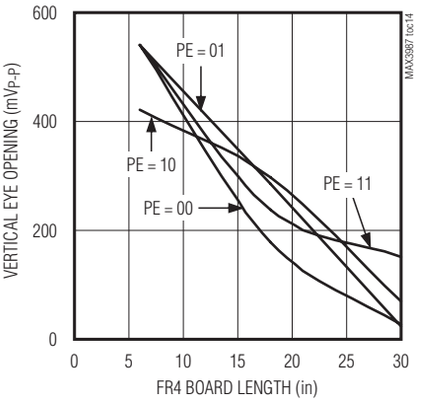
VERTICAL EYE OPENING vs. LENGTH (V_{IN} = 200mV$_{P-P}$, FR4 BOARD, MAXIM STRESS PATTERN, DATA RATE = 1.25Gbps)



VERTICAL EYE OPENING vs. LENGTH (V_{IN} = 200mV$_{P-P}$, FR4 BOARD, MAXIM STRESS PATTERN, DATA RATE = 3.25Gbps)



VERTICAL EYE OPENING vs. LENGTH (V_{IN} = 200mV$_{P-P}$, FR4 BOARD, STRESS PATTERN, DATA RATE = 6.25Gbps)

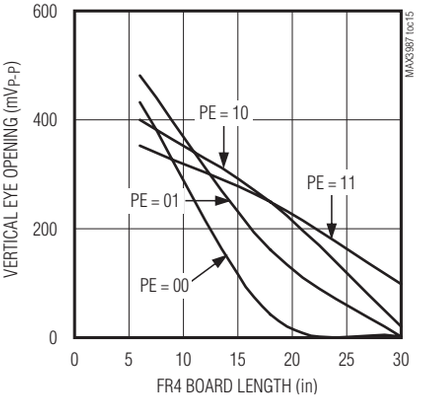


8.5Gbps Quad Equalizer and Preemphasis Drive

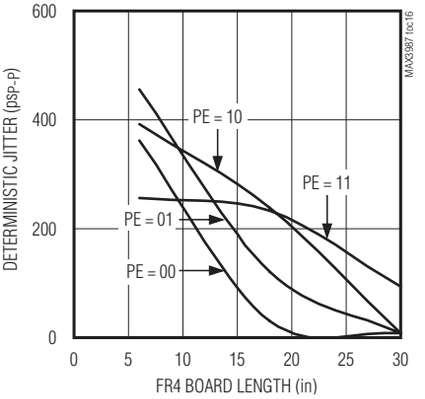
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

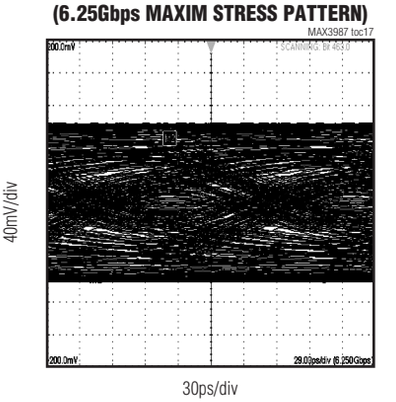
VERTICAL EYE OPENING vs. LENGTH (V_{IN} = 200mV$_{P-P}$, FR4 BOARD, STRESS PATTERN, DATA RATE = 7.5Gbps)



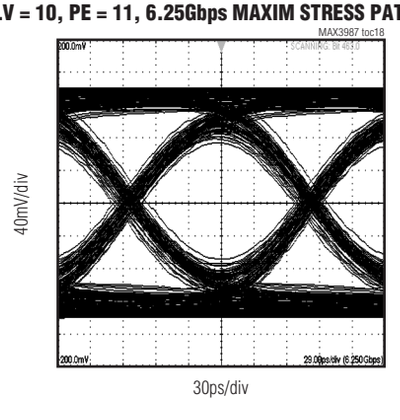
VERTICAL EYE OPENING vs. LENGTH (V_{IN} = 200mV$_{P-P}$, FR4 BOARD, STRESS PATTERN, DATA RATE = 8.5Gbps)



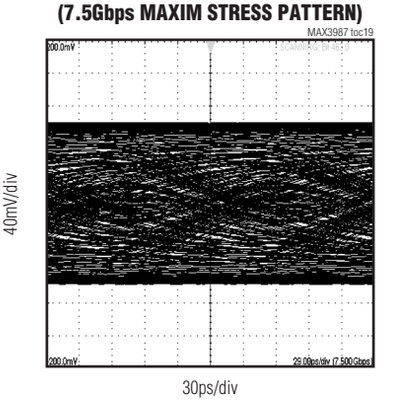
OUTPUT OF 30in FR4 WITHOUT PREEMPHASIS (6.25Gbps MAXIM STRESS PATTERN)



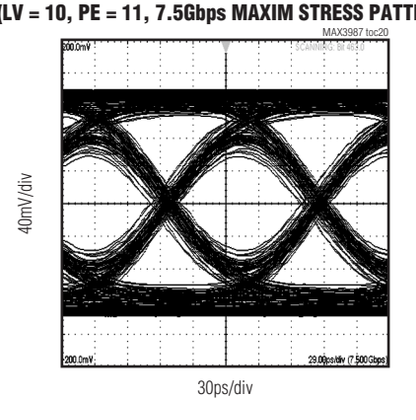
OUTPUT OF 30in FR4 DRIVEN BY MAX3987 (LV = 10, PE = 11, 6.25Gbps MAXIM STRESS PATTERN)



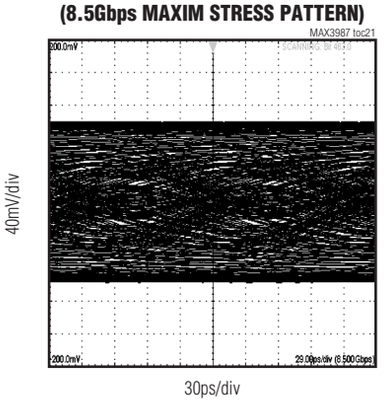
OUTPUT OF 30in FR4 WITHOUT PREEMPHASIS (7.5Gbps MAXIM STRESS PATTERN)



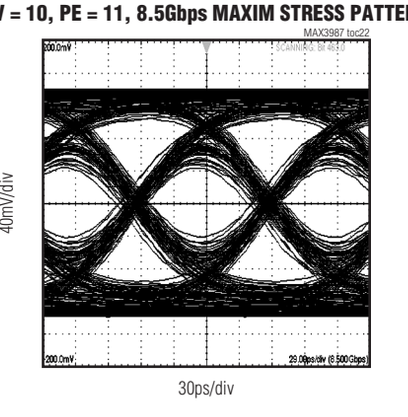
OUTPUT OF 30in FR4 DRIVEN BY MAX3987 (LV = 10, PE = 11, 7.5Gbps MAXIM STRESS PATTERN)



OUTPUT OF 30in FR4 WITHOUT PREEMPHASIS (8.5Gbps MAXIM STRESS PATTERN)



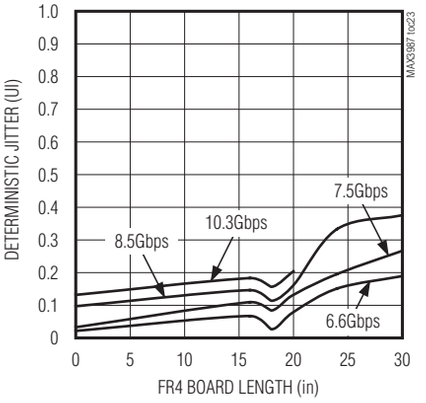
OUTPUT OF 30in FR4 DRIVEN BY MAX3987 (LV = 10, PE = 11, 8.5Gbps MAXIM STRESS PATTERN)



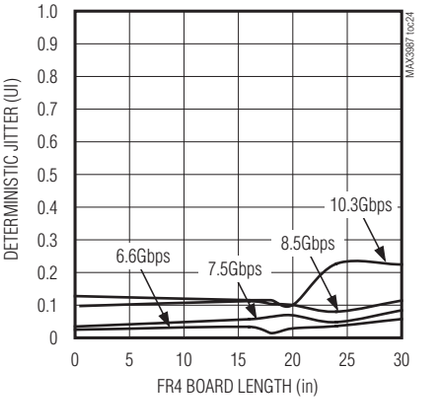
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

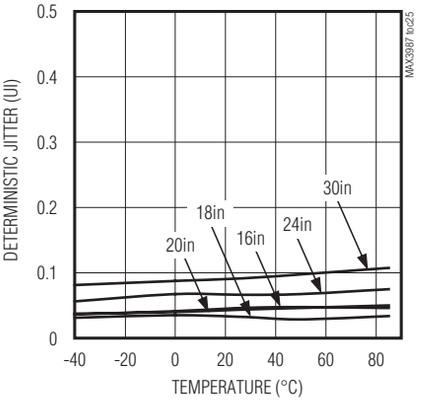
RECEIVER DETERMINISTIC JITTER vs. LENGTH (INPUT SIGNAL = 400mVP-P, MAXIM STRESS PATTERN, TA = +27°C)



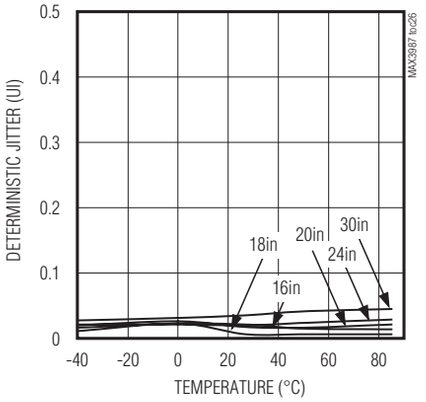
RECEIVER DETERMINISTIC JITTER vs. LENGTH (INPUT SIGNAL = 400mVP-P, PRBS7, TA = +27°C)



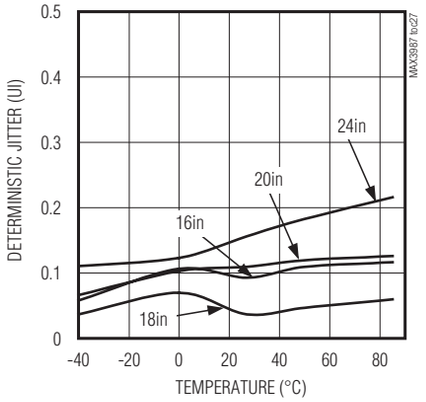
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, MAXIM STRESS PATTERN, 3.125Gbps)



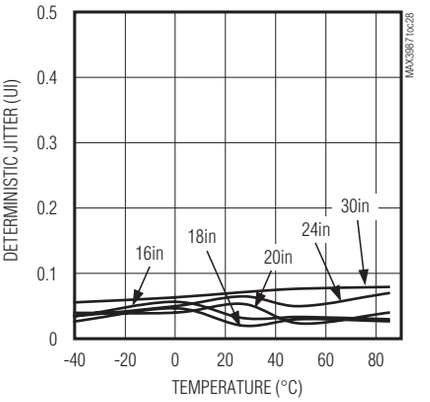
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, PRBS7, 3.125Gbps)



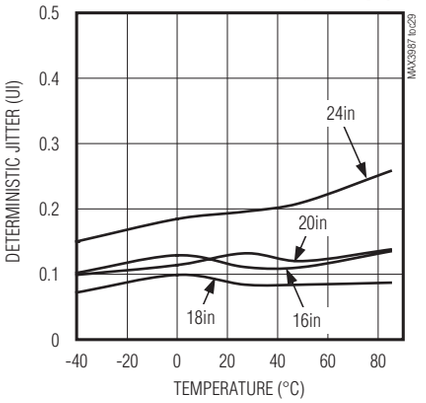
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, STRESS PATTERN, 6.6Gbps)



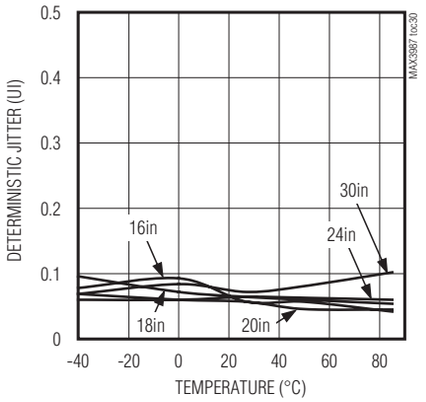
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, PRBS7, 6.6Gbps)



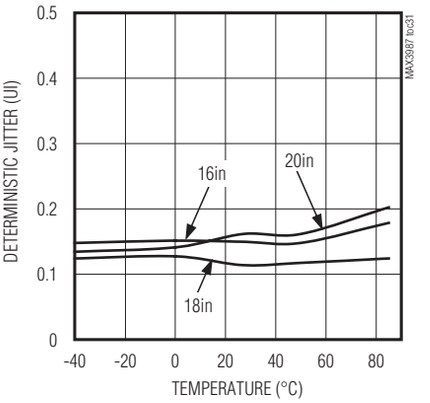
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (VIN = 400mVP-P, MAXIM STRESS PATTERN, 7.5Gbps)



RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, PRBS7, 7.5Gbps)



RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (VIN = 400mVP-P, STRESS PATTERN, 8.5Gbps)

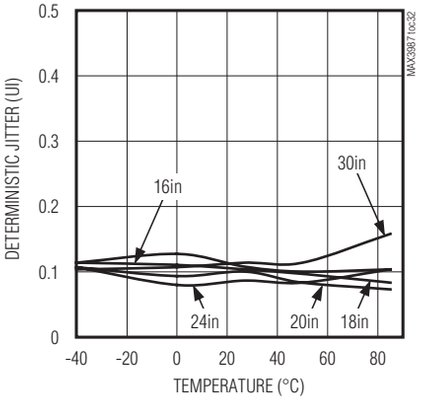


8.5Gbps Quad Equalizer and Preemphasis Drive

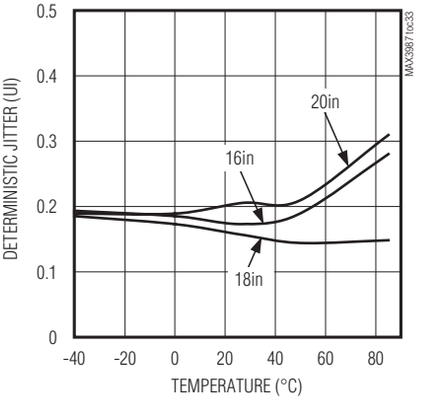
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

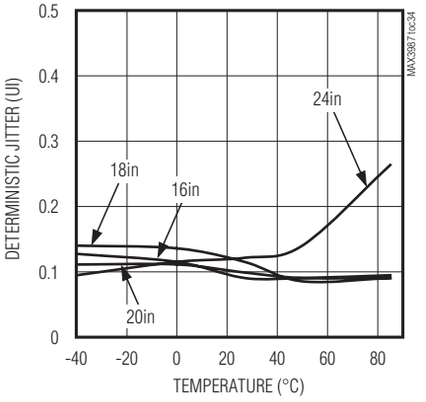
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, PRBS7, 8.5Gbps)



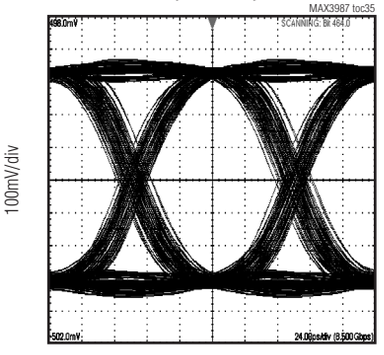
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (INPUT SIGNAL = 400mVP-P, MAXIM STRESS PATTERN, 10.3Gbps)



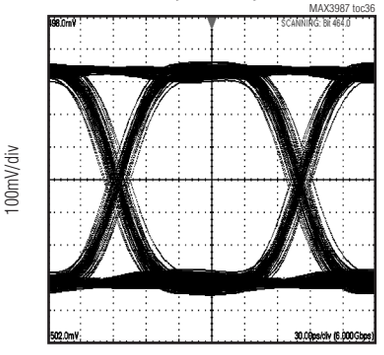
RECEIVER DETERMINISTIC JITTER vs. TEMPERATURE (V_{IN} = 400mVP-P, PRBS7, 10.3Gbps)



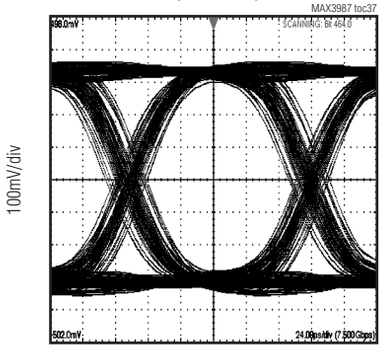
20in INPUT FR4, 8.5Gbps, MAXIM STRESS PATTERN, PE = 00, LV = 00



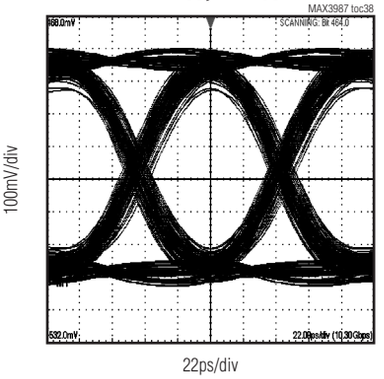
24in INPUT FR4, 6Gbps, MAXIM STRESS PATTERN, PE = 00, LV = 00



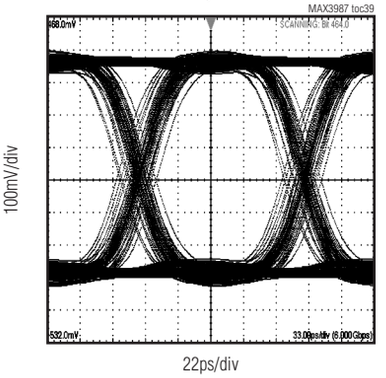
24in INPUT FR4, 7.5Gbps, MAXIM STRESS PATTERN, PE = 00, LV = 00



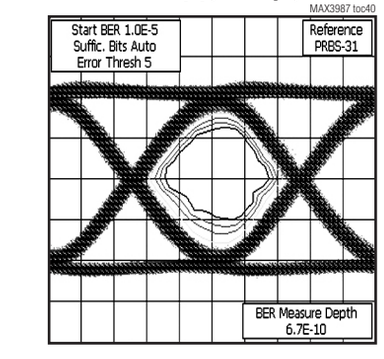
24in INPUT FR4, 10.3Gbps, PRBS7 PATTERN, PE = 00, LV = 00



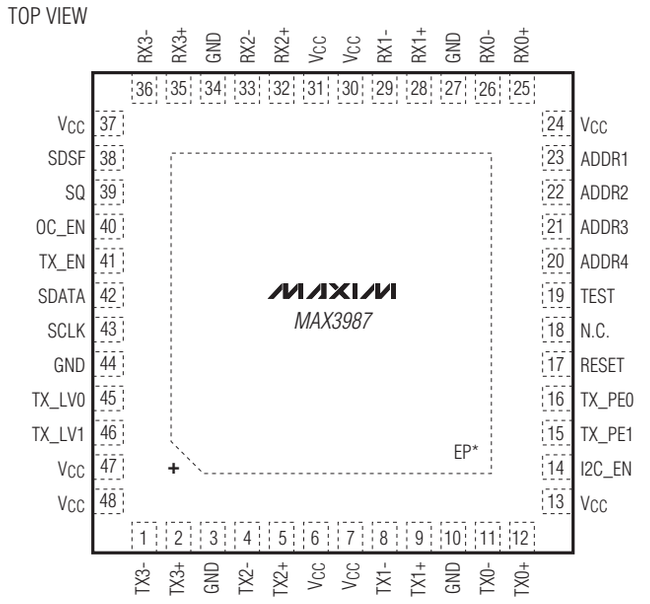
30in INPUT FR4, 7.5Gbps, PRBS7 PATTERN, PE = 00, LV = 00



BER MEASUREMENT (BER < 1e-12) 18in INPUT AND OUTPUT FR4, INPUT SIGNAL: 400mVP-P, 7.5Gbps, PRBS31



Pin Configuration



*EXPOSED PAD.

Pin Description

PIN	NAME	FUNCTION
1	TX3-	Negative CML Output Signal
2	TX3+	Positive CML Output Signal
3, 10, 27, 34, 44	GND	Negative Power Supply (Ground)
4	TX2-	Negative CML Output Signal
5	TX2+	Positive CML Output Signal
6, 7, 13, 24, 30, 31, 37, 47, 48	V_{CC}	Positive Power Supply. All pins should be set at 3.3V or 2.5V.
8	TX1-	Negative CML Output Signal
9	TX1+	Positive CML Output Signal
11	TX0-	Negative CML Output Signal
12	TX0+	Positive CML Output Signal
14	I2C_EN	LVCMOS Signal to Enable/Disable I^2C Programming Interface
15	TX_PE1	LVCMOS Signal to Set Output Preemphasis Levels
16	TX_PE0	LVCMOS Signal to Set Output Preemphasis Levels
17	RESET	LVCMOS Signal to Reset the Device to Default Configuration When High
18	N.C.	No Connection. Leave this pin unconnected.

8.5Gbps Quad Equalizer and Preemphasis Drive

Pin Description (continued)

PIN	NAME	FUNCTION
19	TEST	Reserved for Manufacturing Test. Connect to ground.
20–23	ADDR[4:1]	LVCMOS Signal for I²C Serial Interface Address
25	RX0+	Positive CML Differential Data Input Signal
26	RX0-	Negative CML Differential Data Input Signal
28	RX1+	Positive CML Differential Data Input Signal
29	RX1-	Negative CML Differential Data Input Signal
32	RX2+	Positive CML Differential Data Input Signal
33	RX2-	Negative CML Differential Data Input Signal
35	RX3+	Positive CML Differential Data Input Signal
36	RX3-	Negative CML Differential Data Input Signal
38	SDSF	LVCMOS Signal to Select Signal Detect Type
39	SQ	LVCMOS Signal to Enable/Disable Output Squelch and Signal Detect
40	OC_EN	LVCMOS Signal to Enable/Disable Offset Cancellation
41	TX_EN	LVCMOS Signal to Power On/Off Transmitter
42	SDATA	Analog I²C Serial Interface Data Input and Output
43	SCLK	Analog I²C Serial Interface Clock Input
45	TX_LV0	LVCMOS Signal to Set Output Amplitude
46	TX_LV1	LVCMOS Signal to Set Output Amplitude
—	EP	Exposed Pad. Signal and supply common. For optimal thermal conductivity and supply return (GND), this pad must be soldered to circuit board ground.

Detailed Description

The MAX3987 is a 4-channel equalizer and preemphasis driver that accepts CML differential signals whose data rates vary from 1Gbps to 8.5Gbps. Each channel has a fixed equalization network and programmable preemphasis driver. All controls for preemphasis, output swing level, signal detect/squelch, offset cancellation, output enable/disable, output polarity, etc., are programmed through the I²C interface. These functions are implemented through a programming block on-chip where control bits can be received through a serial bus or through control pins at the edge of the chip. A block diagram is shown in Figure 5.

Power-On Reset

The MAX3987 has a built-in power-on reset function. After the power-on reset, or when RESET is asserted, all 4 channels are configured to a “default” state. Table 1 describes the functions that are controlled and the default state on reset if all the control pins are not connected.

Global and Individual Channel Programming

The MAX3987 supports global programming through hardware pins (only applicable to EQ/PE) and individual channel programming through I²C. Table 1 describes the control pins and their function.

Table 1. Function Table

PIN NAME	INTERNAL DEFAULT*	PIN VALUE, X = 0	PIN VALUE, X = 1
I2C_EN	0	Selects the pin configuration mode (TX_EN, TX_LV0, TX_LV1, TX_PE0, TX_PE1, SDSF, SQ, OC_EN). In this mode, I²C read of pin settings is supported.	Selects the I²C serial interface for programming. Registers can be read and write for full configuration.
SDSF	0	See Table 2.	
SQ	1	See Table 2.	
OC_EN	0	Offset cancellation turned off.	Offset cancellation turned on.
TX_EN	1	All outputs powered off.	All outputs powered on.
TX_LV0	0	See Table 4.	
TX_LV1	1		
TX_PE0	1	Global output preemphasis control. See Table 3.	
TX_PE1	0		
SDATA, SCLK	—	See the *Device Power-Up and Reset and I²C Programming* section.	
RESET	0	The device is in normal operation mode.	The device is reset. After releasing reset (upon the falling edge of RESET), the MAX3987 acquires a startup configuration depending on whether it is an EQ/PE or a crosspoint, independent of the I2C_EN signal status.
ADDR4	0	I²C address bit = 0	I²C address bit = 1
ADDR3	0	I²C address bit = 0	I²C address bit = 1
ADDR2	0	I²C address bit = 0	I²C address bit = 1
ADDR1	0	I²C address bit = 0	I²C address bit = 1

**Default is set by internal pullup or pulldown resistors of 40kΩ.*

Software Power-Down of Individual Output

With the software power-down feature, unused outputs can be turned off by programming a hardware pin or through I²C. It is recommended that any change in programming that affects power be executed only as part of an initialization sequence.

Signal Detect and Internal Squelch

Signal detect and internal squelch suit several applications like Fibre Channel, PCIe, and SAS/SATA.

Signal detect can be enabled and disabled for each individual input by sensing the presence of a valid input signal. Signal detect controls the squelch of the corresponding output (see Table 2).

Squelch can be enabled and disabled independently for each individual output that is controlled by a specific input. The output power-down overrides squelch. When an output is squelched, both terminals of the differential output are set to the common-mode DC voltage (differential zero voltage).

Table 2. Signal Detect and Squelch Pin Programming

PIN VALUE	SIGNAL DETECT AND SQUELCH SELECTION
SDSF = 0	Select slow-response signal detect (SD1).
SDSF = 1	Select fast-response signal detect (SD2).
SQ = 0	Signal detect and output squelch disabled.
SQ = 1	Signal detect and output squelch enabled.

Signal detect and internal squelch have one setting for fast-response applications such as SAS/SATA and PCIe, and another setting for slow-response applications such as XAUI, Fibre Channel, and InfiniBand cable applications. They are controllable through the I²C serial programming interface or hardware pin.

8.5Gbps Quad Equalizer and Preemphasis Drive

Signal-detect status of each input can be monitored through the I2C interface.

Signal detect assert/deassert has two programmable levels for each individual channel. They are accessible only through the I2C interface. The default threshold level for signal detect is high.

Input Equalization

One fixed, universal input equalization level of approximately 15dB compensates any length up to 30in, 6-mil-wide FR4 microstrip up to 8.5Gbps. The device can also compensate up to 8m to 10m 24 AWG twin axial cable.

Input Offset Cancellation

Each input path has an option to enable and disable offset cancellation for high-sensitivity applications. It is programmable through pin or I2C interface. It typically requires signal detect and squelch turned off to realize its full benefits.

When offset cancellation is on, the minimum data rate is 1Gbps. It is suggested that offset cancellation be turned off for SAS/SATA or PCIe bursty applications.

Output Preemphasis

Four different levels of preemphasis at the driver output are selectable to compensate for driving different lengths of PCB routing or cables. The PE levels are 0dB, 3dB, 7dB, and 11dB. The PE level can be set either for all the outputs globally or for each output individually. See Table 3.

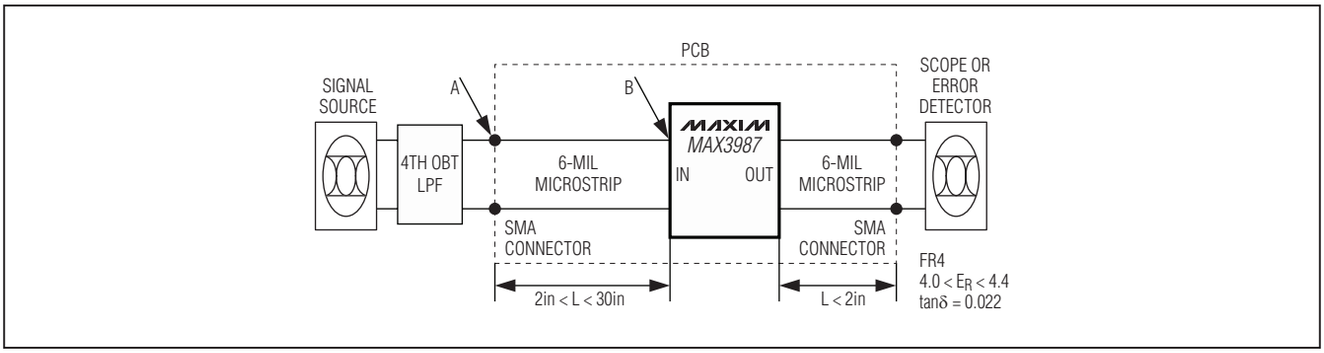


Figure 2. Receive Equalizer Test Setup. The points labeled A and B are referenced for AC parameter test conditions. The filter is a lowpass fourth-order Bessel-Thompson or equivalent (BW = 0.75 x bit rate ±10%).

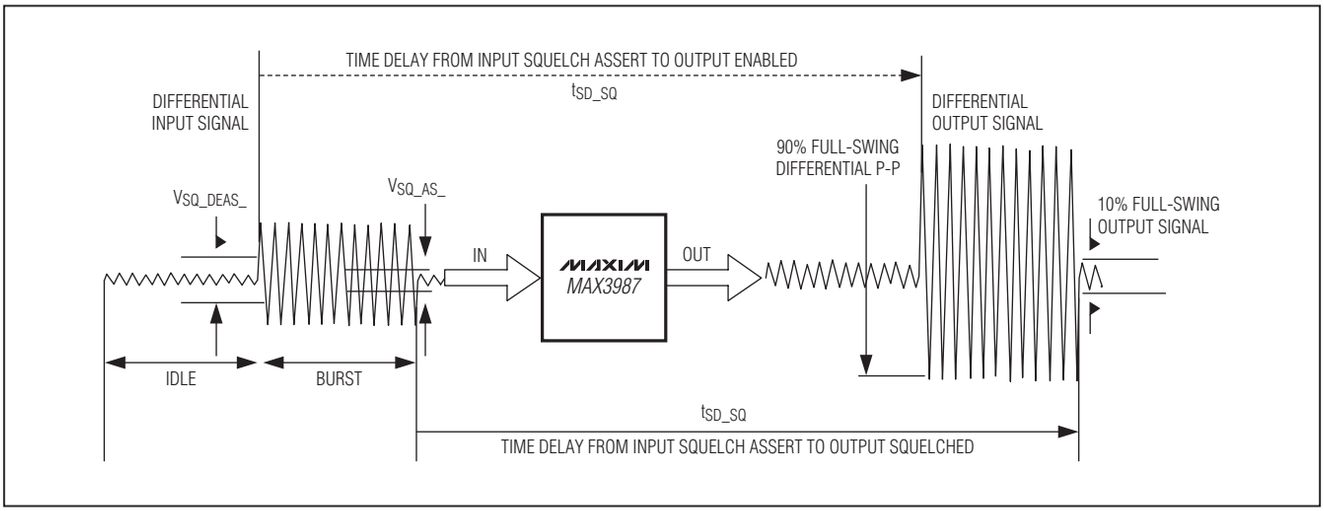


Figure 3. Input Signal Detect and Output Squelch and Its Timing Definition

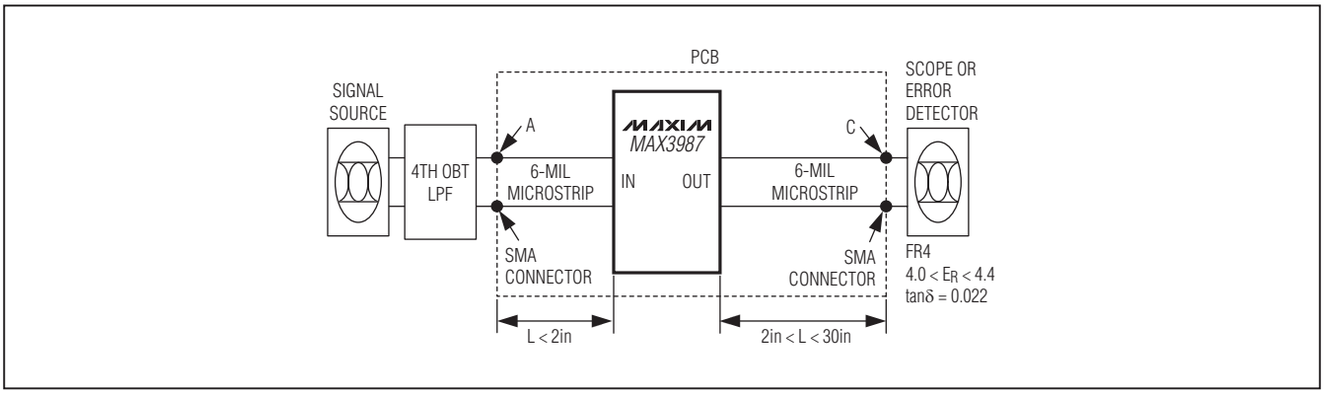


Figure 4. Preemphasis Test Setup. The points labeled A and C are referenced for AC parameter test conditions. The filter is a low-pass fourth-order Bessel-Thompson or equivalent (BW = 0.75 x bit rate ±10%).

Output Level

Three different output levels can be programmed for all outputs. The nominal level 1 output drive is approximately 600mV$_{P-P}$ when level setting LV = 00. The level 2 drive is approximately 850mV$_{P-P}$ when level setting LV = 01, and the level 3 drive is approximately 1050mV$_{P-P}$ when level setting LV = 10. This control can be programmed globally or individually. See Table 4.

Programming Interface

An I^{2}C serial interface is provided to support global and individual programming. Hardware pins (TX_EN, TX_LV0, TX_LV1, TX_PE0, TX_PE1, SDSF, SQ, OC_EN) are also provided to support global programming including output drive level, PE level, signal detect/squelch selection, outputs on/off, and offset cancellation.

Register Maps

Table 5 details the register map showing the address, name, and function. The detailed registers are shown in Tables 6 to 11.

Input and Output Coupling

All data input and output connections are AC-coupled with typical 100nF for continuous traffic, and 12nF maximum for bursty traffic such as SAS/SATA.

Table 3. PE Pin Programming

PIN VALUE		PE	PREEMPHASIS VALUE (dB)
TX_PE1 = 0	TX_PE0 = 0	00	0
TX_PE1 = 0	TX_PE0 = 1	01	3
TX_PE1 = 1	TX_PE0 = 0	10	7
TX_PE1 = 1	TX_PE0 = 1	11	11

Table 4. Drive Level Pin Programming

PIN VALUE		LV	OUTPUT DRIVE LEVEL
TX_LV1 = 0	TX_LV0 = 0	00	Level 1 Drive (minimum)
TX_LV1 = 0	TX_LV0 = 1	01	Level 2 Drive
TX_LV1 = 1	TX_LV0 = 0	10	Level 3 Drive (maximum)
TX_LV1 = 1	TX_LV0 = 1	—	Do not use this mode.

8.5Gbps Quad Equalizer and Preemphasis Drive

Table 5. Register Map

ADDRESS	NAME	REGISTER	BITS	R/W
1	XPE	TX PE	8	R/W
2	XLV	TX Level	8	R/W
3	XOP	TX ON and Polarity	8	R/W
4	SDM	Signal-Detect Mode	8	R/W
5	OCS	Offset Cancellation and Squelch	8	R/W
6	SDS	Signal-Detect Status	8	R

Table 6. Register 1: TX PE (XPE)

Bit	7	6	5	4	3	2	1	0
Function	TX3 PE SELECT 1	TX3 PE SELECT 0	TX2 PE SELECT 1	TX2 PE SELECT 0	TX1 PE SELECT 1	TX1 PE SELECT 0	TX0 PE SELECT 1	TX0 PE SELECT 0
Default	TXPE1	TXPE0	TXPE1	TXPE0	TXPE1	TXPE0	TXPE1	TXPE0

PE SELECT FUNCTION	
BIT[1:0]	**FUNCTION (dB)**
00	≈ 0
01	≈ 3
10	≈ 7
11	≈ 11

Table 7. Register 2: TX Level (XLV)

Bit	7	6	5	4	3	2	1	0
Function	TX3 LEVEL SELECT 1	TX3 LEVEL SELECT 0	TX2 LEVEL SELECT 1	TX2 LEVEL SELECT 0	TX1 LEVEL SELECT 1	TX1 LEVEL SELECT 0	TX0 LEVEL SELECT 1	TX0 LEVEL SELECT 0
Default	TXLV1	TXLV0	TXLV1	TXLV0	TXLV1	TXLV0	TXLV1	TXLV0

TX LEVEL SELECT FUNCTION	
BIT[1:0]	**FUNCTION (mV)**
00	≈ 600
01	≈ 850
10	≈ 1050
11	Do not use

Table 8. Register 3: TX ON and Polarity (XOP)

Bit	7	6	5	4	3	2	1	0
Function	TX3 ON	TX2 ON	TX1 ON	TX0 ON	TX3 POL	TX2 POL	TX1 POL	TX0 POL
Default	TXEN	TXEN	TXEN	TXEN	0	0	0	0

If TXEN is zero, the output signal for that channel is off. If TX[3:0] POL is zero, there is no polarity inversion for that channel.

Table 9. Register 4: Signal-Detect Mode (SDM)

Bit	7	6	5	4	3	2	1	0
Function	SQ3	SQ2	SQ1	SQ0	SF3	SF2	SF1	SF0
Default	SQ	SQ	SQ	SQ	SF	SF	SF	SF

SF function: 0 = slow, 1 = fast. A zero selects slow-response signal detect; a one selects fast signal detect.

SQ function: 0 disables the squelch; 1 enables squelch.

Table 10. Register 5: Offset Cancellation and Squelch (OCS)

Bit	7	6	5	4	3	2	1	0
Function	OC3	OC2	OC1	OC0	SDL3	SDL2	SDL1	SDL0
Default	OCEN	OCEN	OCEN	OCEN	1	1	1	1

If OCEN = 1, offset cancellation is enabled; if OCEN = 0, offset cancellation is off.

If the SDL bit = 0, the signal-detect threshold level is low. If the SDL bit = 1, the signal-detect threshold level is high.

Table 11. Register 6: Signal-Detect Status (SDS)

Bit	7	6	5	4	3	2	1	0
Function	—	—	—	—	SD3	SD2	SD1	SD0
Default	—	—	—	—	—	—	—	—

If the SD bit = 0, the signal is present in the corresponding channel.

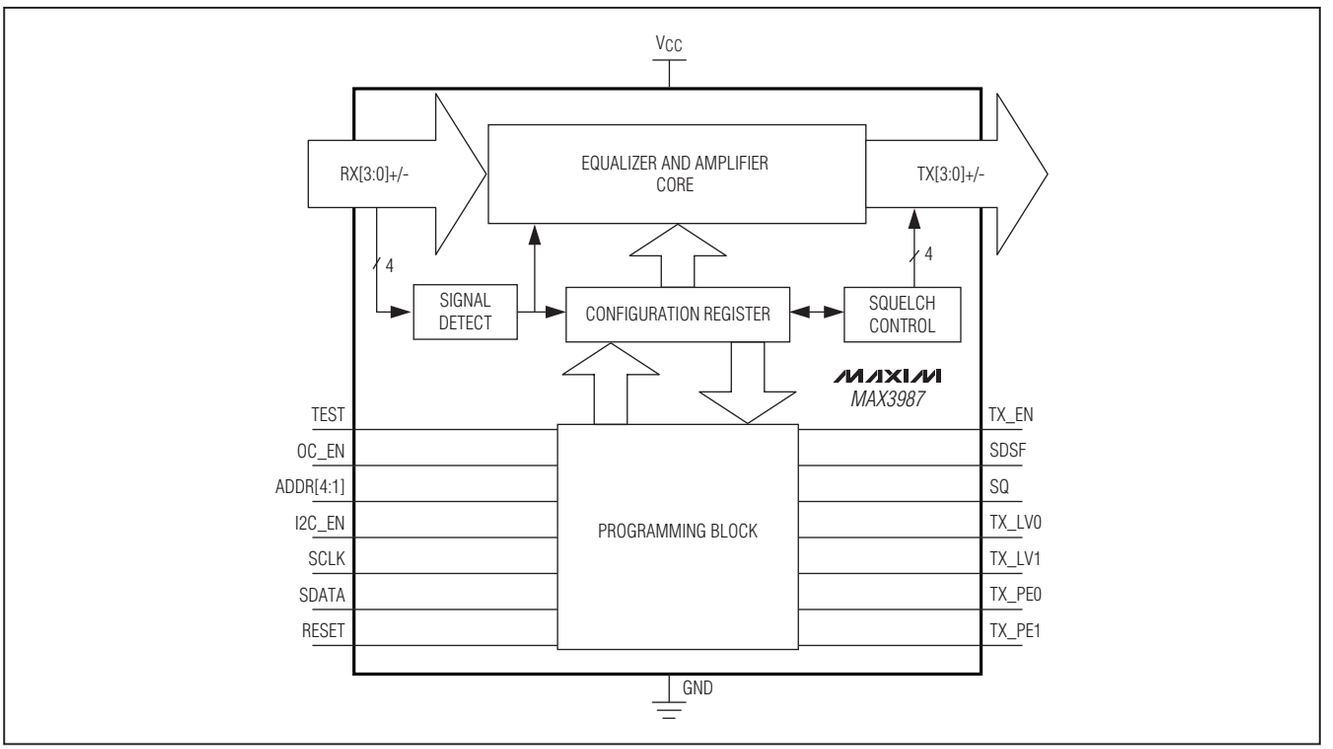


Figure 5. Functional Diagram

8.5Gbps Quad Equalizer and Preemphasis Drive

Device Power-Up and Reset and I²C Programming

Power-Up and Reset Default Condition

The MAX3987 enters the default condition on power-up or on assertion of the RESET signal. The RESET signal is active high. When RESET is deasserted, the power-up sequence disables the MAX3987 for 100ms, during which the MAX3987 does not respond to the I²C port.

At the end of the 100ms timeout, the MAX3987 samples the control pins and programs the control registers according to the register map.

After power-up the MAX3987 listens to the I²C bus and can be accessed for read or write at any time if the I2C_EN pin is asserted, or for read access only if the I2C_EN pin is not asserted.

I²C Control

The MAX3987 can be configured through the control pins or the I²C interface. When I2C_EN is asserted, the control pin's only role is to set the default value of the control registers during power-on reset. Other than during power-on reset, the control pins do not control the functionality of the chip. The I²C interface can write and read the control registers.

When I2C_EN is not asserted, the MAX3987 is in pin control mode. The control pins affect the functionality of the chip, and each control pin controls all the channels. The I²C interface can only read the control registers, and only channel 0 bits are valid and apply to all channels. All other bits are zero.

I²C Programming

The MAX3987 I²C function implements only the mandatory fast-mode slave functions. Implemented features are START condition, STOP condition, acknowledge, and 7-bit address.

The I²C address comprises a fixed address, which is 100, and 4 bits of programmable address. During the first I²C cycle the fixed address should match data in bits [7:5] and the programmable address should match bits [4:1]. Bit 0 is the I²C R/$\overline{W}$ bit.

A power-on reset or assertion of the RESET signal, or an I²C START or STOP condition, always resets the register address to zero. If I2C_EN is asserted, write and read access to the registers is enabled. If I2C_EN is not asserted, only read access is enabled, and the MAX3987 acknowledges a write cycle, but does not write into any register.

Each I²C access starts with the address and read/write byte. The first access always addresses register 0, which is the XPE register. For each subsequent access, the MAX3987 autoincrements the register addresses. The register address does not increment above address 6. If there are more than six consecutive read cycles, the MAX3987 acknowledges and provides zero data. If there are more than five consecutive write cycles, the MAX3987 acknowledges and does not write into any register.

The MAX3987 internal registers change at the end of the write cycle, when all 8 bits are written. The control function changes approximately 200ns after the rising edge of SCLK, which samples the I²C LSB.

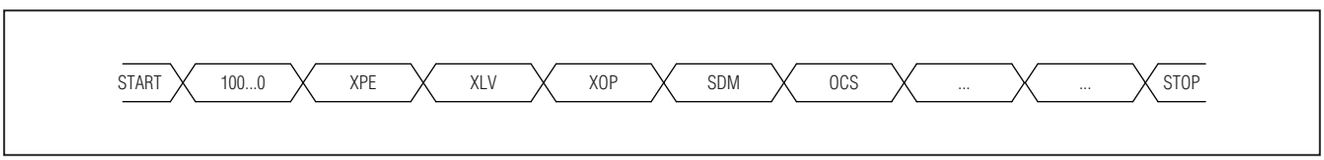


Figure 6. EQ I²C Write Sequence

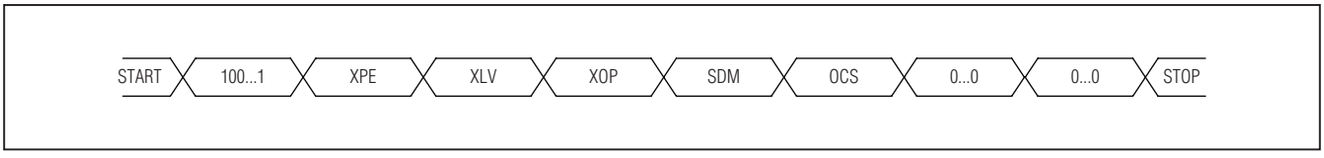


Figure 7. EQ I²C Read Sequence

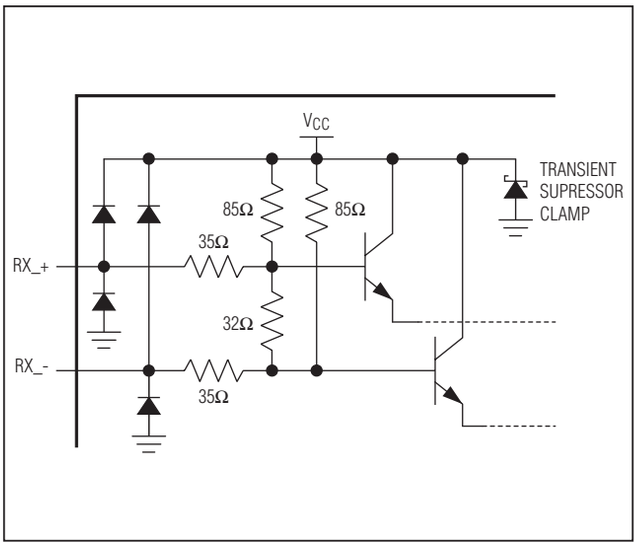


Figure 8. Simplified Input Circuit

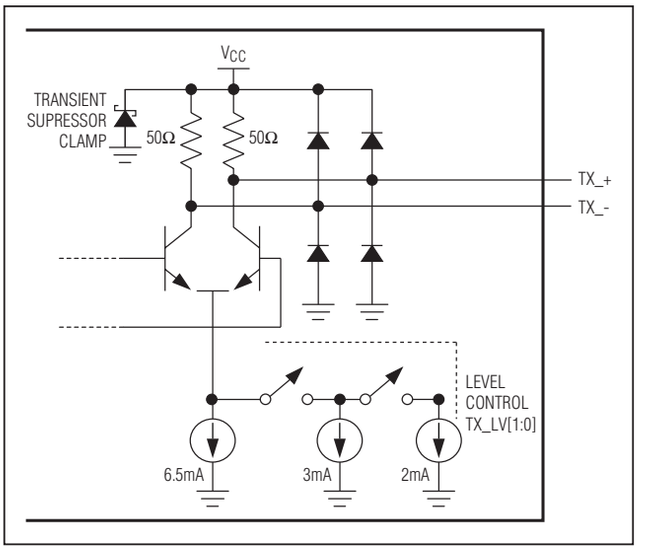


Figure 9. Standard Output Circuit

Input and Output Buffers

The input buffers and the output drivers are current-mode logic (CML). The input buffers consist of a 50Ω load resistor connected to V_{CC} and the input connected to a differential equalizer as shown in Figure 8. The output circuit is shown in Figure 9. The ESD protection for both the input and output circuitry consists of diodes connected to a transient voltage suppressor clamp shown as a Schottky diode. For more information about the function of the suppressor clamp, refer to the *Detailed Description* section of the MAX3208E IC data sheet.

Using the MAX3987 in PCIe Applications

The MAX3987 does not support presence detection. However, it passes low-frequency beacon signals and has signal detect and output squelch compatibility with the electrical idle state requirements.

Package and Exposed Pad

The exposed-pad, 48-pin thin QFN package incorporates features that provide a very low-thermal resistance path for heat removal from the IC. The exposed pad on the MAX3987 must be soldered to the circuit board for proper thermal performance and correct electrical grounding. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

8.5Gbps Quad Equalizer and Preemphasis Drive

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/09	Initial release	—
1	1/10	Corrected the naming convention for SAS, SATA in the *Applications* and *Features* sections	1
		Added the soldering temperature line to the *Absolute Maximum Ratings* section	2
		Added the EP description to the *Pin Description* table	14
		Added the *Using the MAX3987 in PCIe Applications* section	21
2	4/12	Corrected the storage ambient temperature range in the *Absolute Maximum Ratings* section	2