

74AHC125; 74AHCT125

Quad buffer/line driver; 3-state

Rev. 5 — 12 June 2020

Product data sheet

1. General description

The 74AHC125; 74AHCT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($\overline{nOE}$). A HIGH on $\overline{nOE}$ causes the outputs to assume a high impedance OFF-state. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

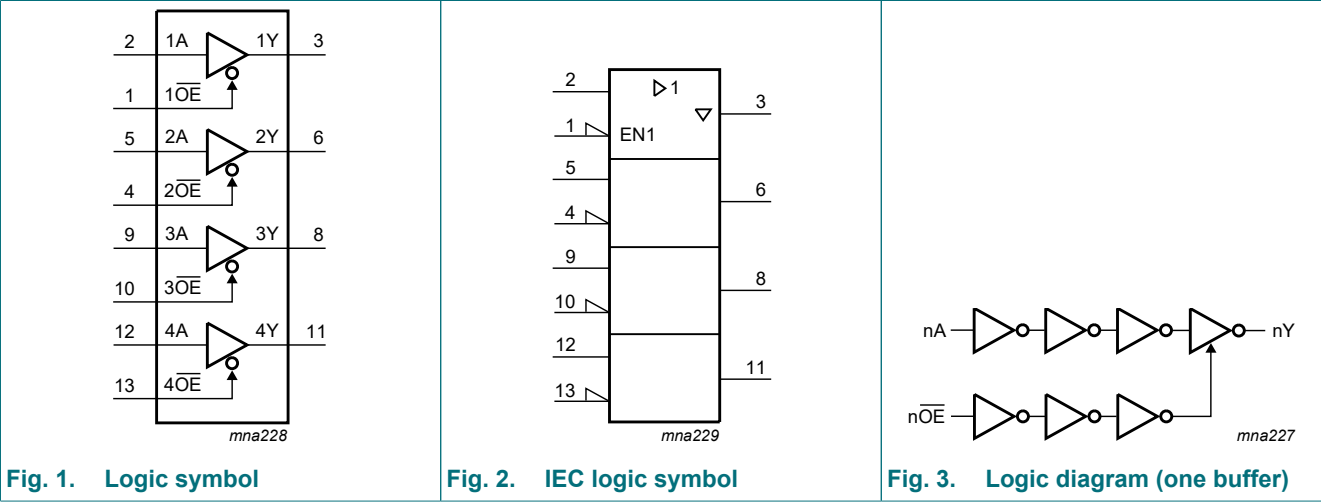
- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Input levels:
 - For 74AHC125: CMOS level
 - For 74AHCT125: TTL level
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

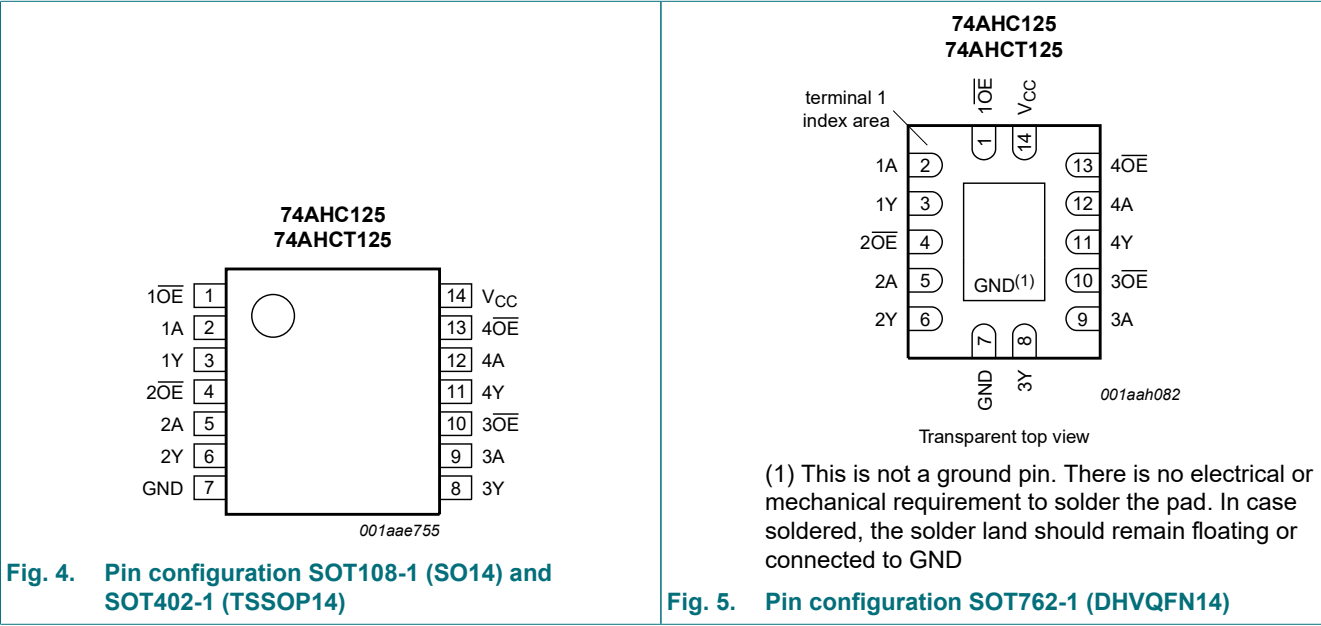
Type number	Package			
	Temperature range	Name	Description	Version
74AHC125D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT125D				
74AHC125PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT125PW				
74AHC125BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT125BQ				

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
L	L	L
	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V [1]	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
 For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
 For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC125			74AHCT125			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC125										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V _{OL}	LOW-level output voltage	I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
		V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
		V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF
74AHCT125										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	µA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; For test circuit see [Fig. 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC125										
t _{pd}	propagation delay	nA to nY; see Fig. 6 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.4	8.0	1.0	9.5	1.0	11.5	ns
		C _L = 50 pF	-	6.2	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t _{en}	enable time	nOE to nY; see Fig. 7 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		C _L = 50 pF	-	6.8	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.3	5.1	1.0	6.0	1.0	6.5	ns
		C _L = 50 pF	-	4.7	7.1	1.0	8.0	1.0	9.0	ns
t _{dis}	disable time	nOE to nY; see Fig. 7 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	6.7	9.7	1.0	11.5	1.0	12.5	ns
		C _L = 50 pF	-	9.6	13.2	1.0	15.0	1.0	16.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.8	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF	-	6.8	8.8	1.0	10.0	1.0	11.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [3]	-	10	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHCT125										
t _{pd}	propagation delay	nA to nY; see Fig. 6 [2]								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nY; see Fig. 7 [2]								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	5.1	1.0	6.0	1.0	6.5	ns
		C _L = 50 pF	-	4.9	7.3	1.0	8.3	1.0	9.5	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nY; see Fig. 7 [2]								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF	-	6.5	8.8	1.0	10.0	1.0	11.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [3]	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5.0\text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

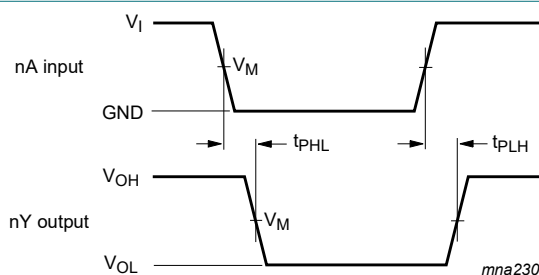
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Propagation delay input (nA) to output (nY)

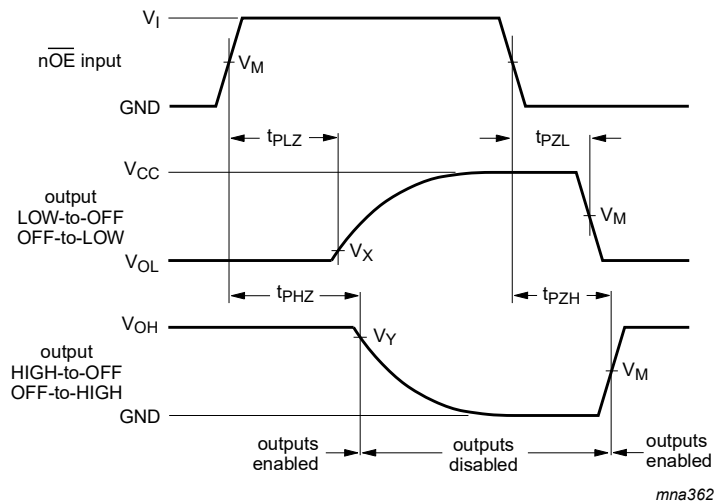
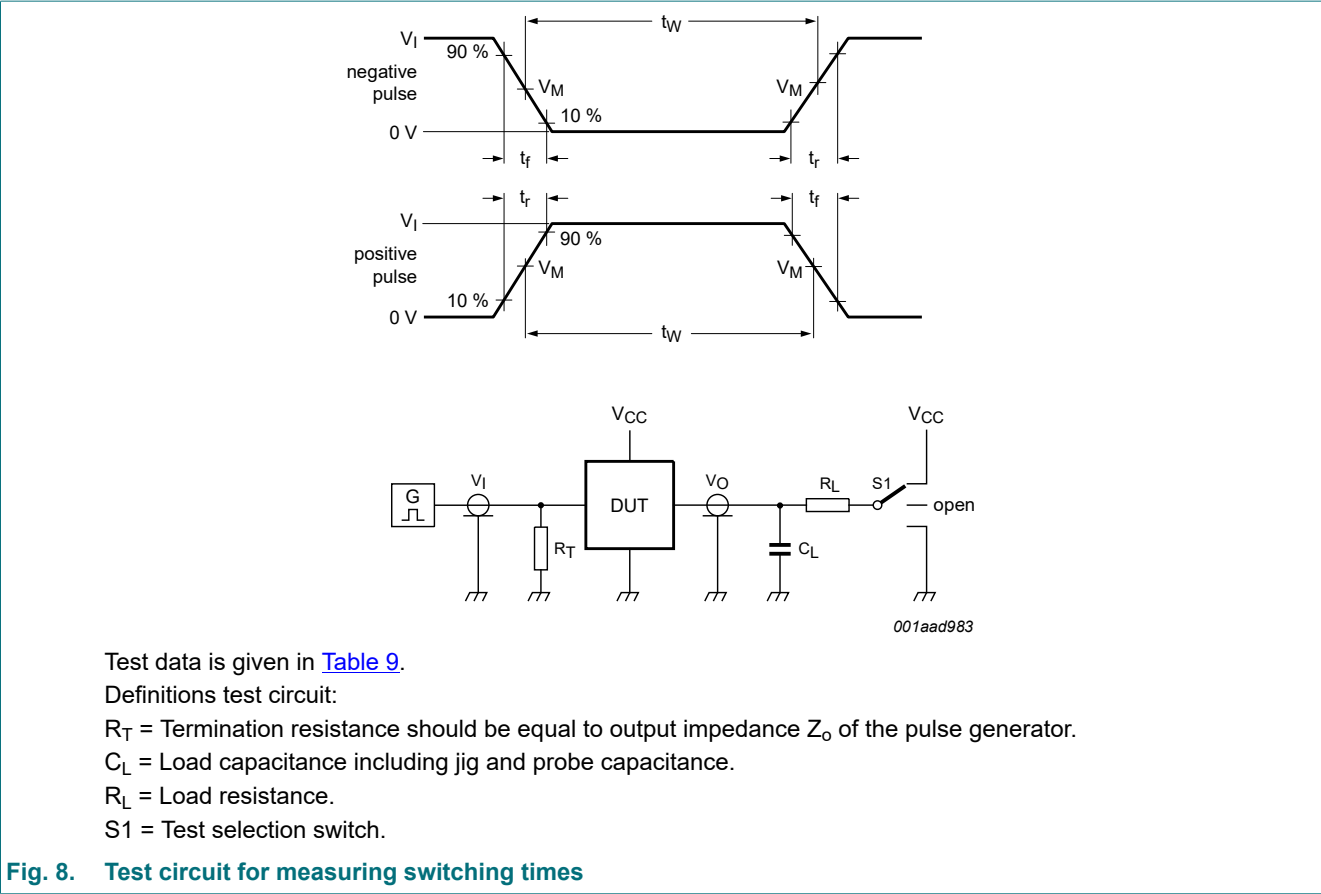


Fig. 7. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC125	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} - 0.3\text{ V}$
74AHCT125	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} - 0.3\text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = Load capacitance including jig and probe capacitance.
 R_L = Load resistance.
 $S1$ = Test selection switch.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC125	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT125	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

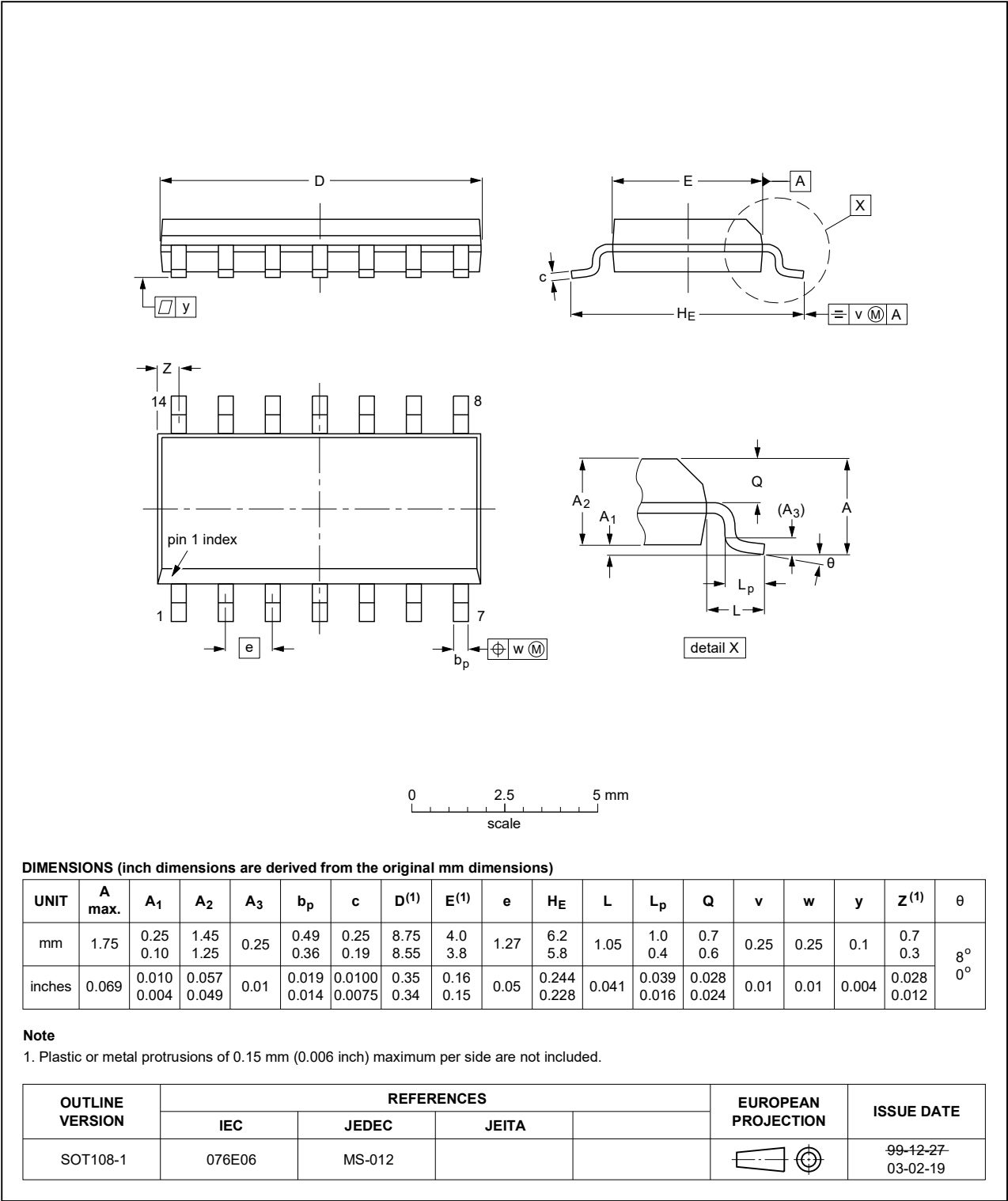


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

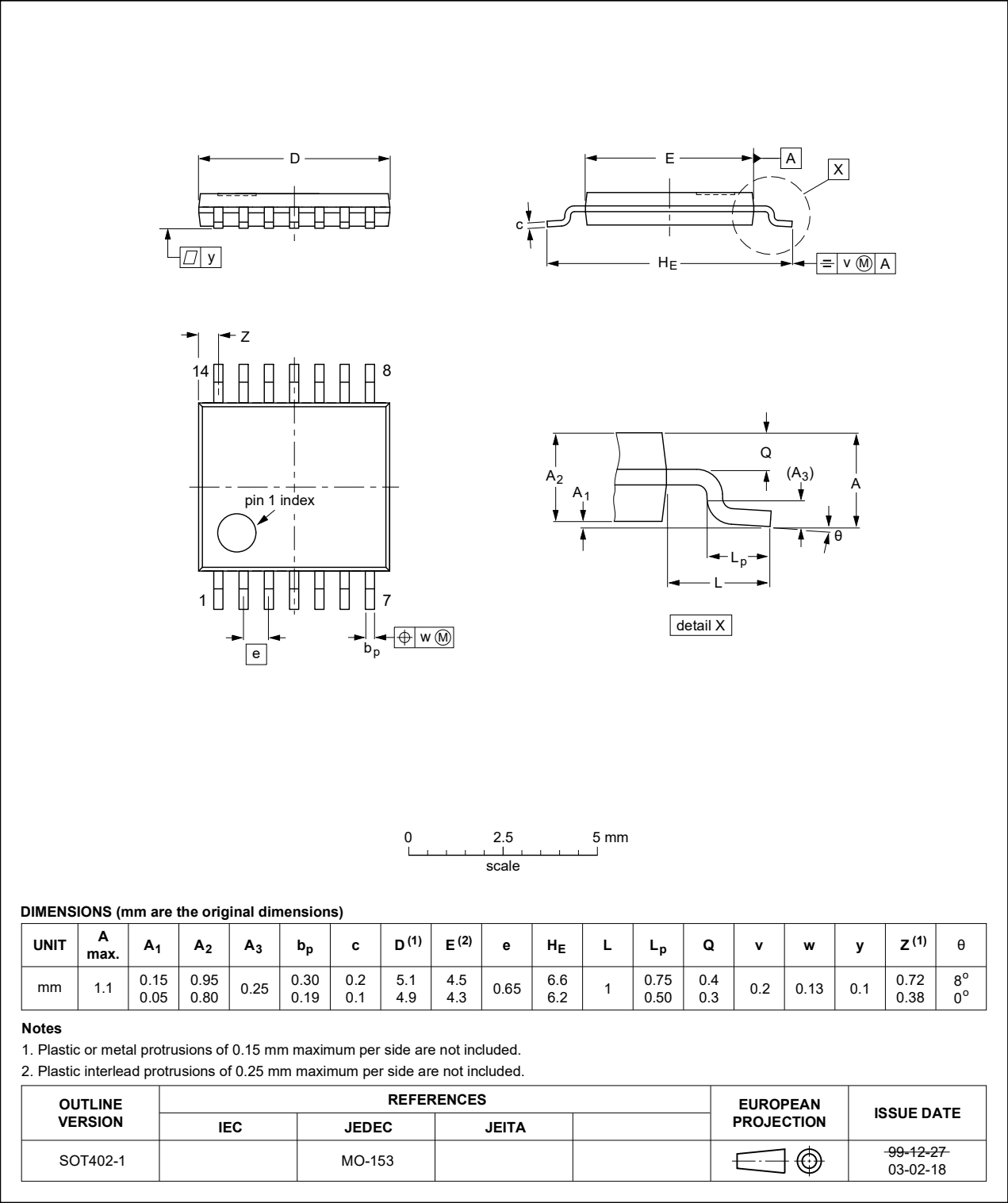
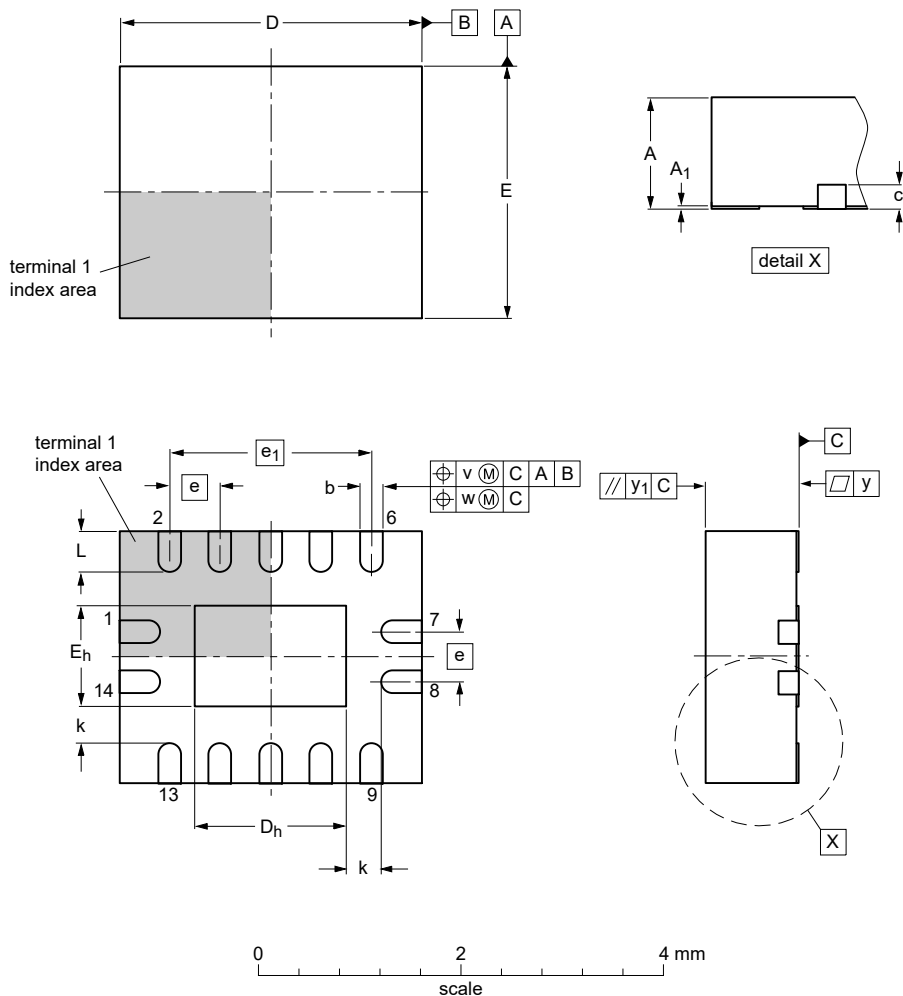


Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit		A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT125 v.5	20200612	Product data sheet	-	74AHC_AHCT125 v.5
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated. Table 6: Conditions for I_{OZ} corrected. - Package outline drawing of SOT762-1 (Fig. 11) updated.			
74AHC_AHCT125 v.4	20080111	Product data sheet	-	74AHC_AHCT125 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN14 package added. Section 7: derating values added for DHVQFN14 package. Section 11: outline drawing added for DHVQFN14 package.			
74AHC_AHCT125 v.3	20060324	Product data sheet	-	74AHC_AHCT125 v.2
74AHC_AHCT125 v.2	19990927	Product specification	-	74AHC_AHCT125 v.1
74AHC_AHCT125 v.1	19990111	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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