XC61G Series

Low Voltage Detectors (V_{DF}= 0.8V～1.5V)
Standard Voltage Detectors (V_{DF} 1.6V～6.0V)

■GENERAL DESCRIPTION

The XC61G series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies.
Detect voltage is extremely accurate with minimal temperature drift.
Both CMOS and N-channel open drain output
configurations are available.

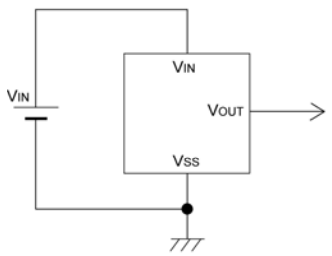
■APPLICATIONS

- ●Microprocessor reset circuitry
- ●Memory battery back-up circuits
- ●Power-on reset circuits
- ●Power failure detection
- ●System battery life and charge voltage monitors

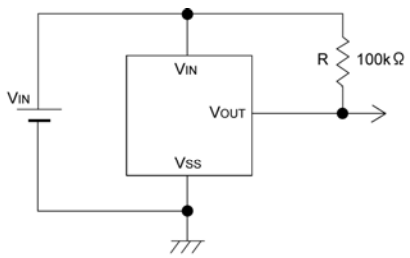
■FEATURES

Highly Accurate : ±2%
Low Power Consumption : 0.7 μA [V_{IN}=1.5V] (TYP.)
Detect Voltage Range : 0.8V ~ 1.5V in 0.1V increments (Low Voltage)
: 1.6V～6.0V in 0.1V increments (Standard Voltage)
Operating Voltage Range : 0.7V ~ 6.0V (Low Voltage)
: 0.7V～10.0V (Standard Voltage)
Detect Voltage Temperature characteristics
: ±100ppm/℃ (TYP.)
Output Configuration : N-channel open drain or CMOS
CMOS
Package : USP-3
Environmentally Friendly: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUITS

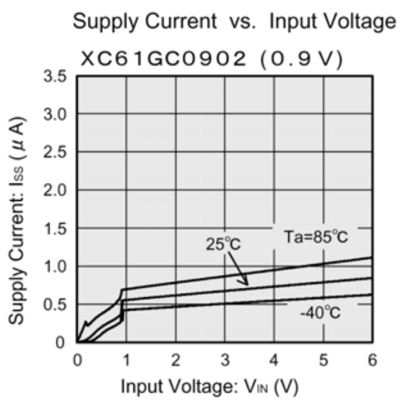


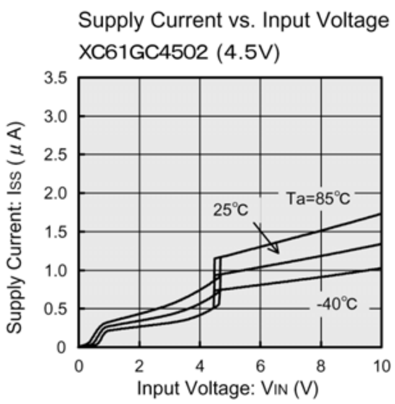
CMOS Output



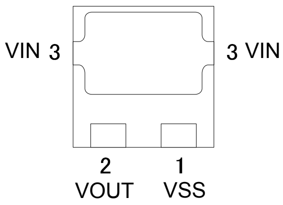
N-ch Open Drain Output

■TYPICAL PERFORMANCE CHARACTERISTICS





■PIN CONFIGURATION



(BOTTOM VIEW)

■PIN ASSIGNMENT

PIN NUMBER USP-3	PIN NAME	FUNCTION
3	VIN	Supply Voltage
1	VSS	Ground
2	VOUT	Output

■PRODUCT CLASSIFICATION

●Ordering Information

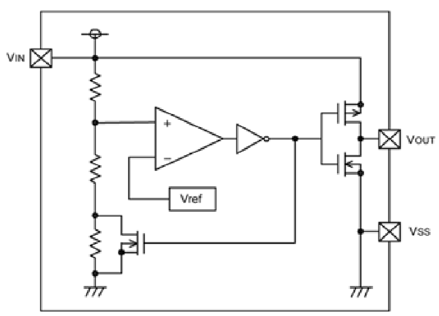
XC61G ①②③④⑤⑥⑦-⑧(*1)

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
② ③	Detect Voltage	08 ~ 60	e.g. 0.8V → ②0, ③8
			e.g. 1.5V → ②1, ③5
④	Output Delay	0	No delay
⑤	Detect Accuracy	2	Within ± 2%
⑥⑦-⑧	Packages Taping Type (*2)	HR	USP-3
		HR-G	USP-3

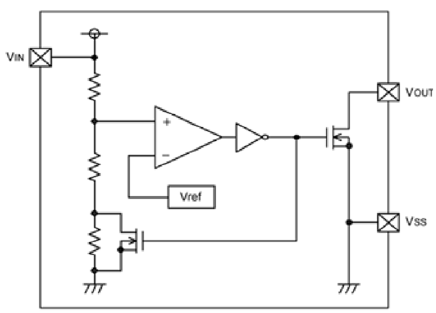
(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.
(*2) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ⑥R-⑧, Reverse orientation: ⑥L-⑧)

■BLOCK DIAGRAMS

(1) CMOS Output



(2) N-ch Open Drain Output



■ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

<table>
<tr><th colspan="3">PARAMETER</th><th>SYMBOL</th><th>RATINGS</th><th>UNITS</th></tr>
<tr><td colspan="2" rowspan="2">Input Voltage</td><td>*1</td><td rowspan="2">V_{IN}</td><td>9.0</td><td rowspan="2">V</td></tr>
<tr><td>*2</td><td>12.0</td></tr>
<tr><td colspan="2" rowspan="2">Output Current</td><td>*1</td><td rowspan="2">I_{OUT}</td><td>50</td><td rowspan="2">mA</td></tr>
<tr><td>*2</td><td>50</td></tr>
<tr><td rowspan="3">Output Voltage</td><td colspan="2">CMOS</td><td rowspan="3">V_{OUT}</td><td>V_{SS} -0.3 ~ V_{IN} +0.3</td><td rowspan="3">V</td></tr>
<tr><td colspan="2">N-ch Open Drain Output *1</td><td>V_{SS} -0.3 ~ 9.0</td></tr>
<tr><td colspan="2">N-ch Open Drain Output *2</td><td>V_{SS} -0.3 ~ 12.0</td></tr>
<tr><td>Power Dissipation</td><td colspan="2">USP-3</td><td>Pd</td><td>120</td><td>mW</td></tr>
<tr><td colspan="3">Operating Temperature Range</td><td>Topr</td><td>-40～+85</td><td>℃</td></tr>
<tr><td colspan="3">Storage Temperature Range</td><td>Tstg</td><td>-40～+125</td><td>℃</td></tr>
</table>

■ELECTRICAL CHARACTERISTICS

$V_{DF\,(T)}$ = 0.9 to 1.5V ± 2%

Ta=25℃

<table>
<tr><th>PARAMETER</th><th>SYMBOL</th><th colspan="2">CONDITIONS</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>UNITS</th><th>CIRCUITS</th></tr>
<tr><td>Detect Voltage</td><td>V_{DF}</td><td colspan="2"></td><td>V_{DF} x 0.98</td><td>V_{DF}</td><td>V_{DF} x 1.02</td><td>V</td><td>1</td></tr>
<tr><td>Hysteresis Range</td><td>V_{HYS}</td><td colspan="2"></td><td>V_{DF} x 0.02</td><td>V_{DF} x 0.05</td><td>V_{DF} x 0.08</td><td>V</td><td>1</td></tr>
<tr><td rowspan="5">Supply Current</td><td rowspan="5">I_{SS}</td><td colspan="2">V_{IN} = 1.5V</td><td>-</td><td>0.7</td><td>2.3</td><td rowspan="5">μA</td><td rowspan="5">2</td></tr>
<tr><td colspan="2">V_{IN} = 2.0V</td><td>-</td><td>0.8</td><td>2.7</td></tr>
<tr><td colspan="2">V_{IN} = 3.0V</td><td>-</td><td>0.9</td><td>3.0</td></tr>
<tr><td colspan="2">V_{IN} = 4.0V</td><td>-</td><td>1.0</td><td>3.2</td></tr>
<tr><td colspan="2">V_{IN} = 5.0V</td><td>-</td><td>1.1</td><td>3.6</td></tr>
<tr><td rowspan="2">Operating Voltage</td><td rowspan="2">V_{IN}</td><td colspan="2">$V_{DF(T)}$ = 0.9V to 1.5V</td><td>0.7</td><td>-</td><td>6.0</td><td rowspan="2">V</td><td rowspan="2">1</td></tr>
<tr><td colspan="2">$V_{DF(T)}$ = 1.6V to 6.0V</td><td>0.7</td><td>-</td><td>10.0</td></tr>
<tr><td rowspan="3">Output Current
(Low Voltage)</td><td rowspan="9">I_{OUT}</td><td rowspan="2">N-ch, V_{DS} = 0.5V</td><td>V_{IN} =0.7V</td><td>0.10</td><td>0.80</td><td>-</td><td rowspan="9">mA</td><td rowspan="2">3</td></tr>
<tr><td>V_{IN} =1.0V</td><td>0.85</td><td>2.70</td><td>-</td></tr>
<tr><td>CMOS, P-ch, V_{DS}=2.1V</td><td>V_{IN} =6.0V</td><td>-</td><td>-7.5</td><td>-1.5</td><td>4</td></tr>
<tr><td rowspan="6">Output Current
(Standard Voltage)</td><td rowspan="5">N-ch, V_{DS} = 0.5V</td><td>V_{IN} =1.0V</td><td>1.0</td><td>2.2</td><td>-</td><td rowspan="5">3</td></tr>
<tr><td>V_{IN} =2.0V</td><td>3.0</td><td>7.7</td><td>-</td></tr>
<tr><td>V_{IN} =3.0V</td><td>5. 0</td><td>10.1</td><td>-</td></tr>
<tr><td>V_{IN} =4.0V</td><td>6.0</td><td>11.5</td><td>-</td></tr>
<tr><td>V_{IN} =5.0V</td><td>7.0</td><td>13.0</td><td>-</td></tr>
<tr><td>CMOS,
P-ch, V_{DS}=2.1V</td><td>V_{IN} =8.0V</td><td>-</td><td>-10.0</td><td>-2.0</td><td>4</td></tr>
<tr><td>Temperature Characteristics</td><td>$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$</td><td colspan="2">-40℃ ≦ Topr ≦ 85℃</td><td>-</td><td>±100</td><td>-</td><td>ppm/℃</td><td>-</td></tr>
<tr><td>Delay Time
(V_{DR} → V_{OUT} inversion)</td><td>tDLY</td><td colspan="2"></td><td>-</td><td>-</td><td>0.2</td><td>ms</td><td>5</td></tr>
</table>

NOTE:
V_{DF} (T): Setting detect voltage
Release Voltage: V_{DR} = V_{DF} + V_{HYS}

■OPERATIONAL EXPLANATION

●CMOS output

① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.

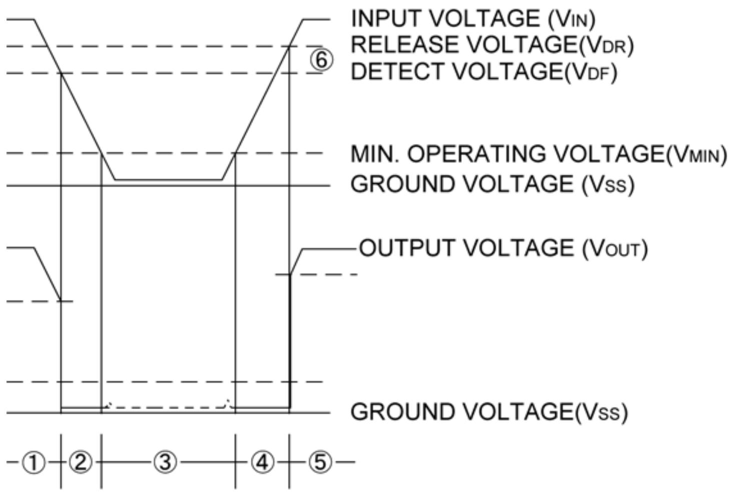
③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)

④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.

⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

●Timing Chart



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
5. In order to stabilize the IC's operations, please ensure that VIN pin's input frequency's rise and fall times are more than several μ s / V.
6. Please use N-ch open drains configuration, when a resistor RIN is connected between the VIN pin and power source.
In such cases, please ensure that RIN is less than 10kΩ and that C is more than 0.1 μ F.

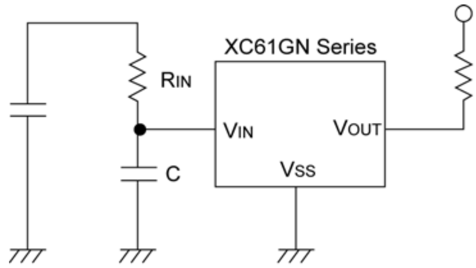


Figure 1: Circuit using an input resistor

●Oscillation Description

(1) Output current oscillation with the CMOS output configuration
When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow at RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.
Oscillation may occur with this "release - detect - release" repetition.
Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current
Since the XC61G series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (RIN) during release voltage operations. (refer to Figure 3)
Since hysteresis exists during detect operations, oscillation is unlikely to occur.

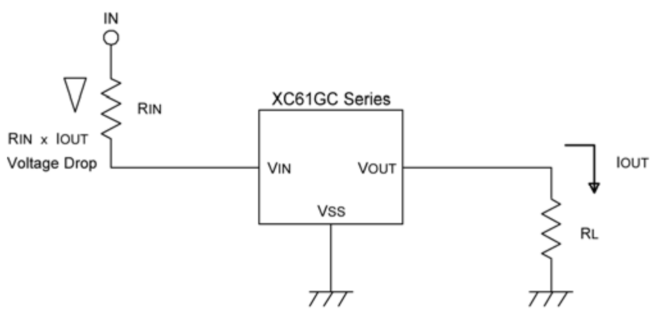


Figure 2: Oscillation in relation to output current

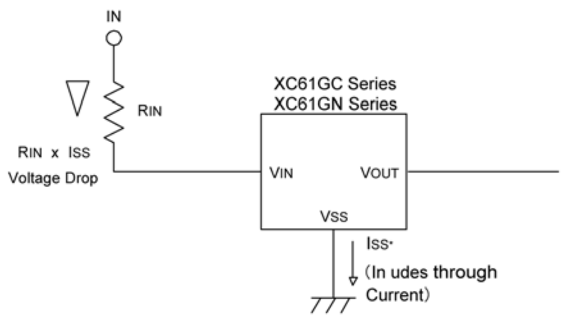
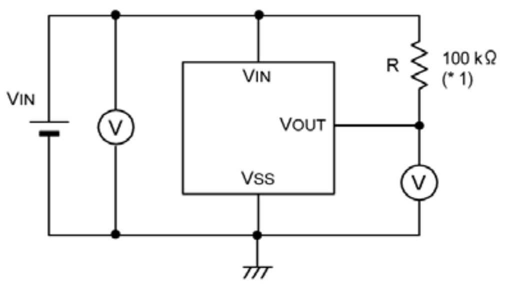


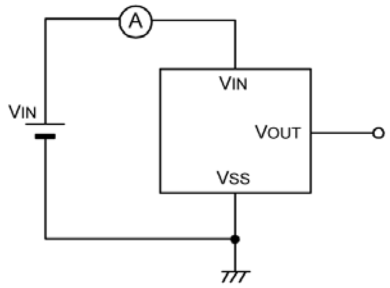
Figure 3: Oscillation in relation to through current

■TEST CIRCUITS

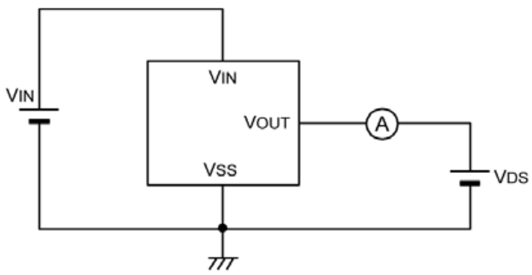
Circuit 1



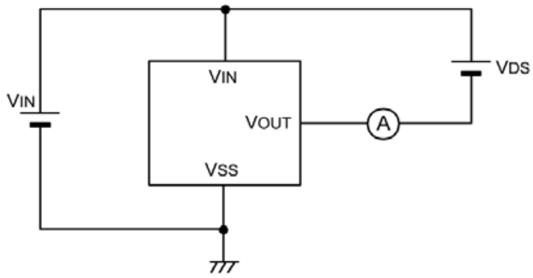
Circuit 2



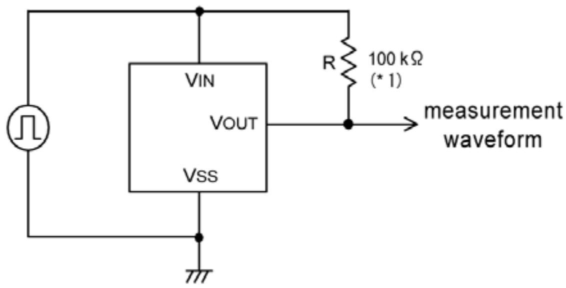
Circuit 3



Circuit 4



Circuit 5

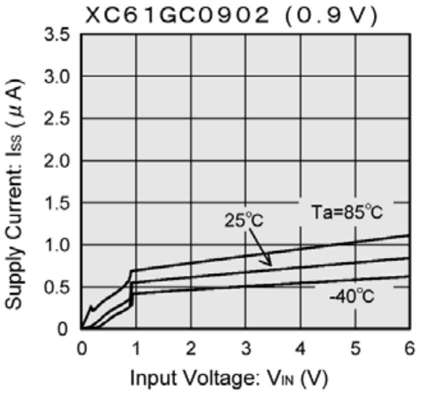


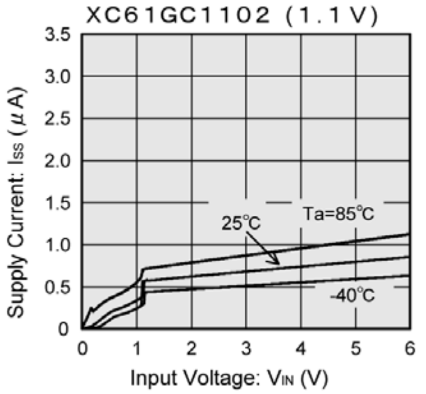
* 1 : The resistor is not necessary with CMOS output products.

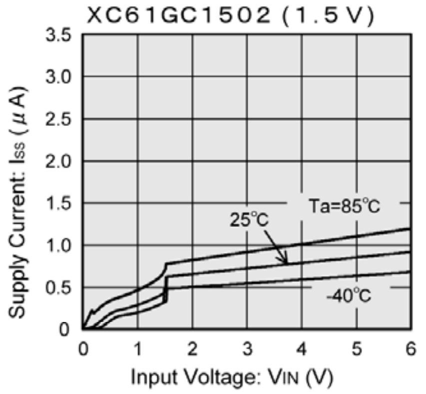
■TYPICAL PERFORMANCE CHARACTERISTICS

●Low Voltage

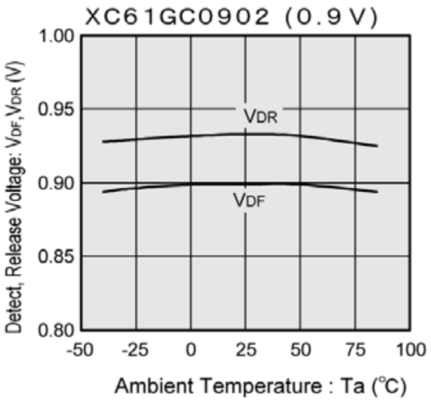
(1) Supply Current vs. Input Voltage

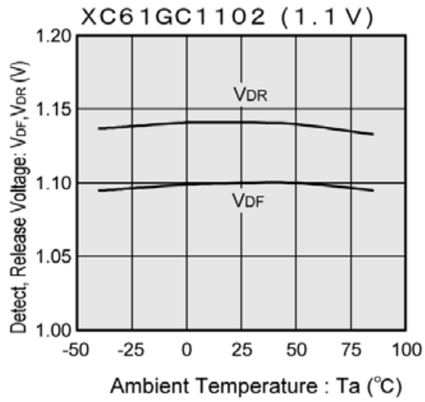


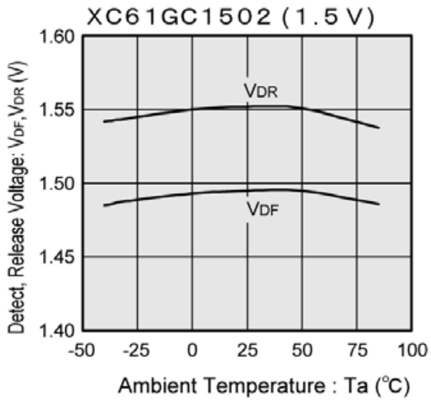




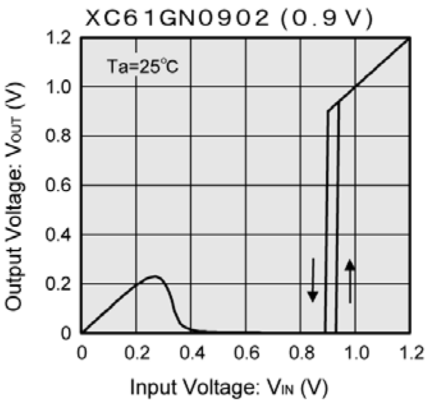
(2) Detect, Release Voltage vs. Ambient Temperature

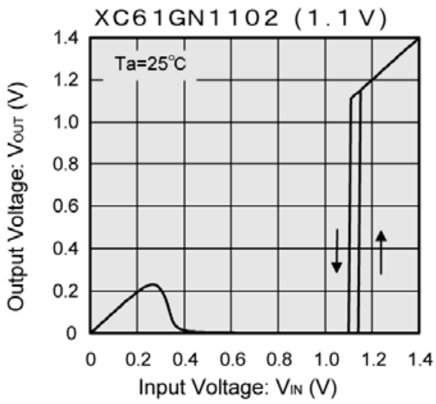


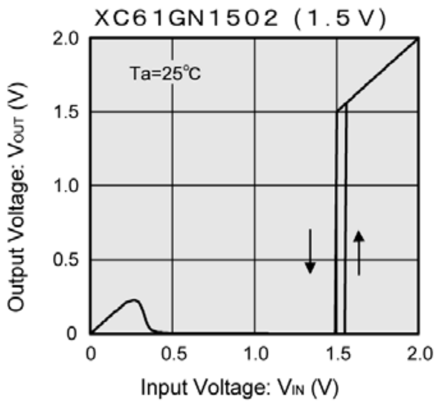




(3) Output Voltage vs. Input Voltage





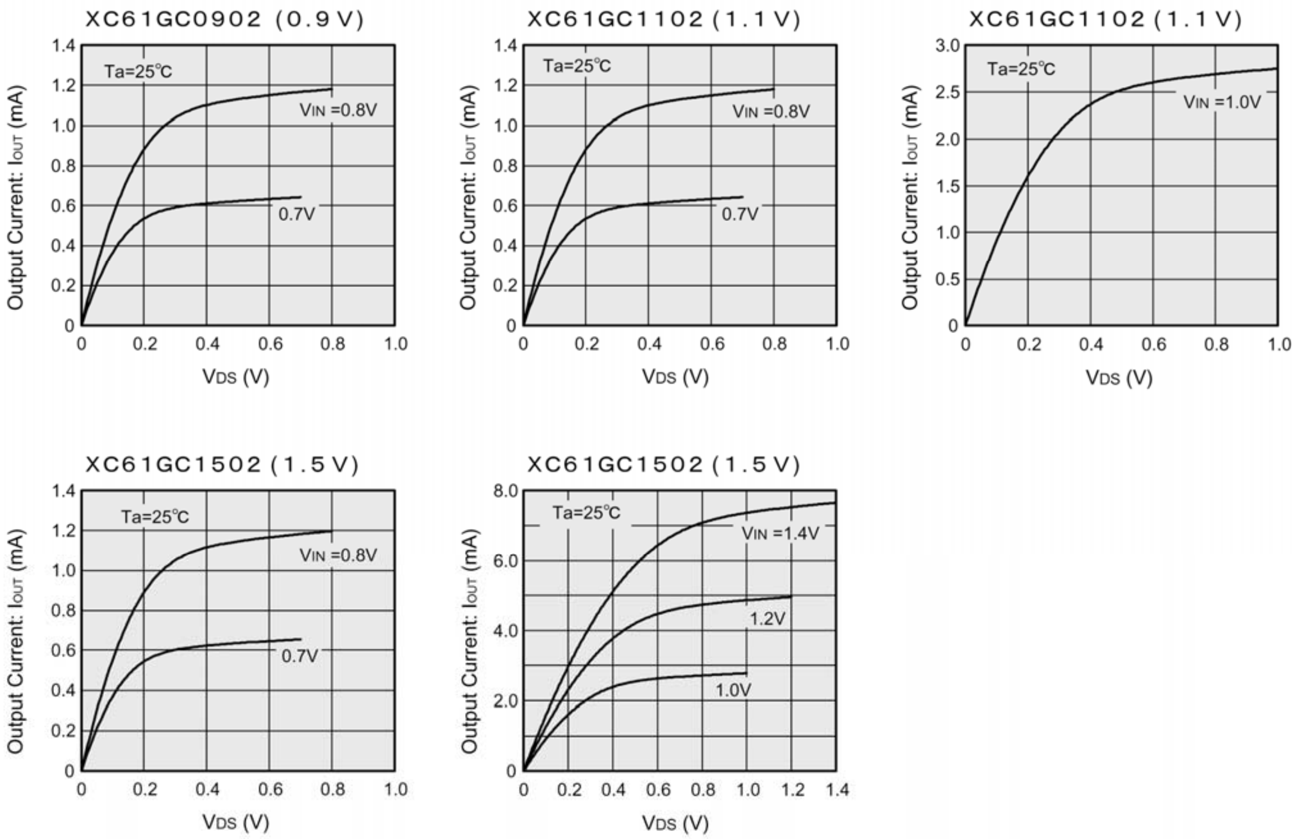


Note : Unless otherwise stated, the N-channel open drain pull-up resistance value is 100kΩ.

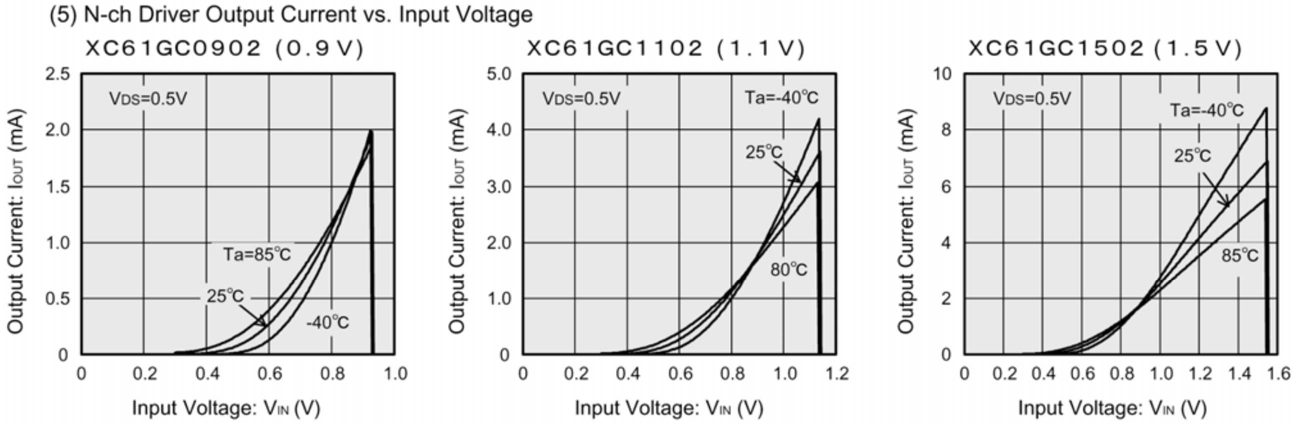
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Low Voltage (Continued)

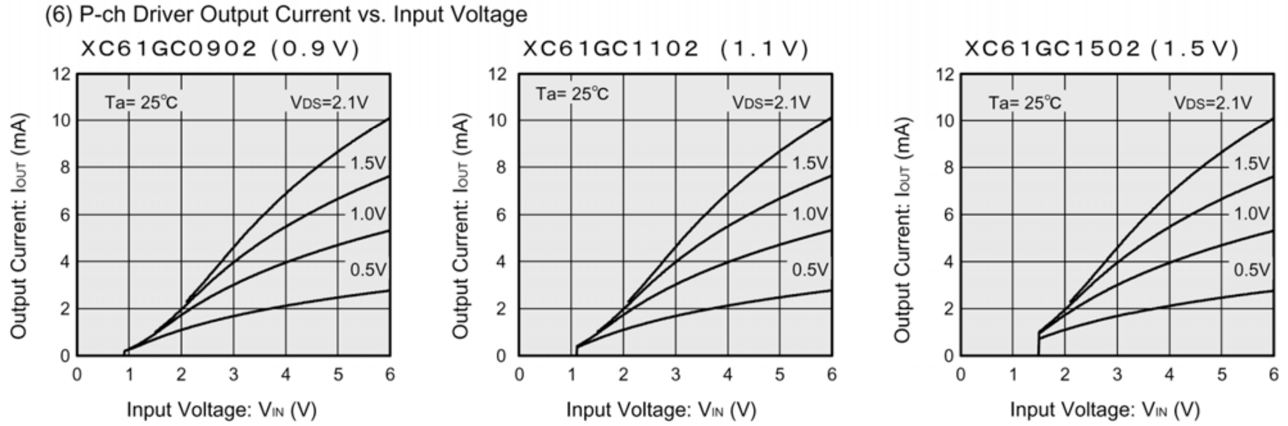
(4) N-ch Driver Output Current vs. VDS



(5) N-ch Driver Output Current vs. Input Voltage



(6) P-ch Driver Output Current vs. Input Voltage

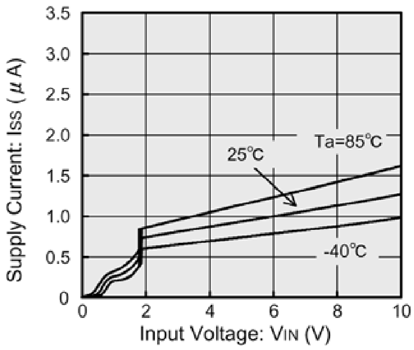


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

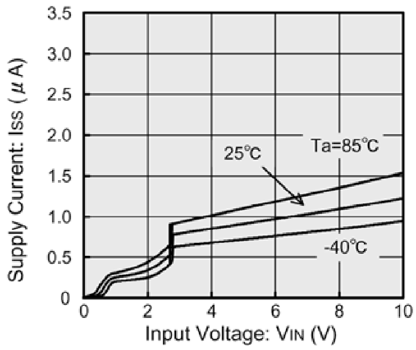
●Standard Voltage

(1) Supply Current vs. Input Voltage

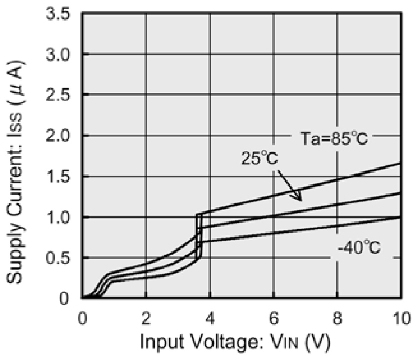
XC61GC1802 (1.8V)



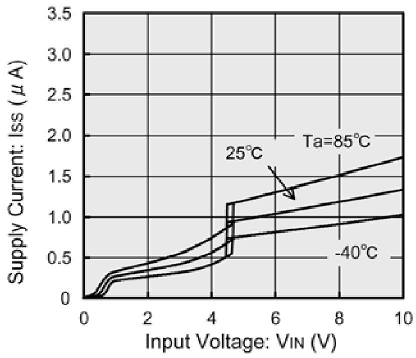
XC61GC2702 (2.7V)



XC61GC3602 (3.6V)

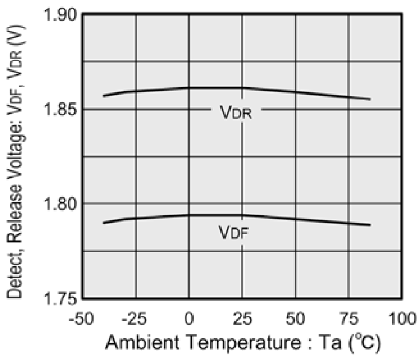


XC61GC4502 (4.5V)

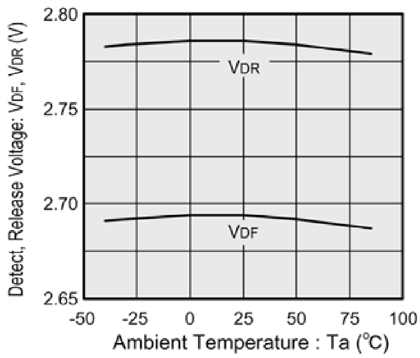


(2) Detect, Release Voltage vs. Ambient Temperature

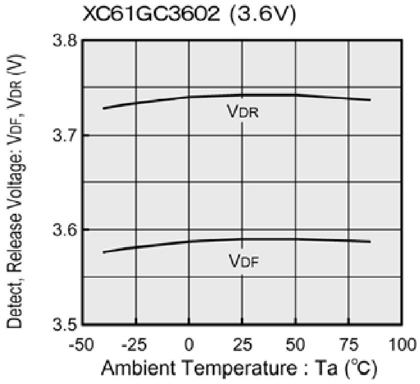
XC61GC1802 (1.8V)



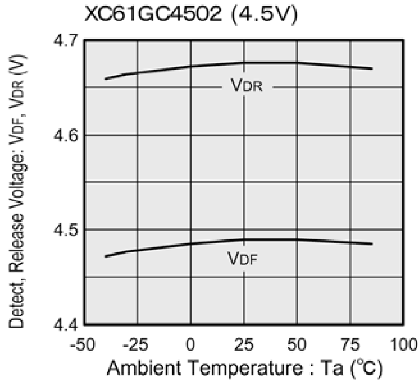
XC61GC2702 (2.7V)



XC61GC3602 (3.6V)



XC61GC4502 (4.5V)

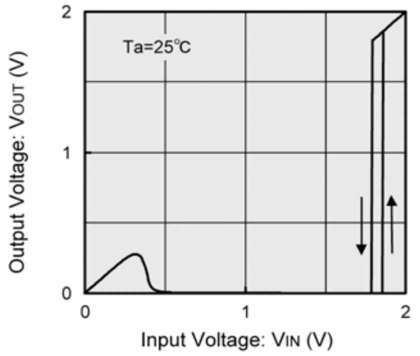


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

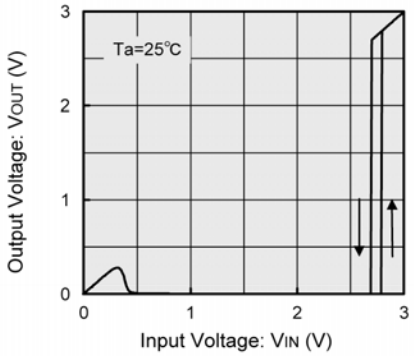
●Standard Voltage (Continued)

(3) Output Voltage vs. Input Voltage

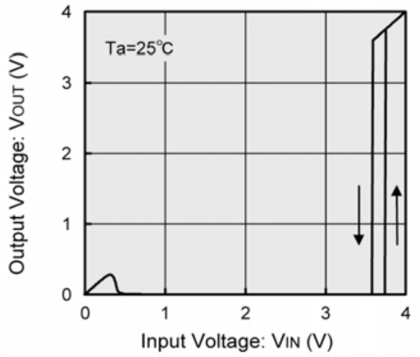
XC61GN1802 (1.8V)



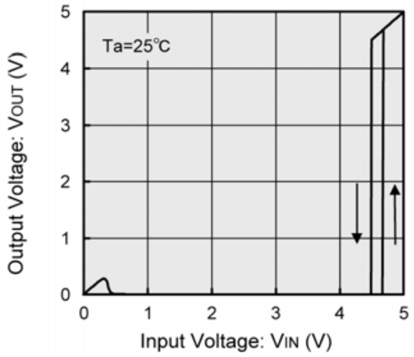
XC61GN2702 (2.7V)



XC61GN3602 (3.6V)



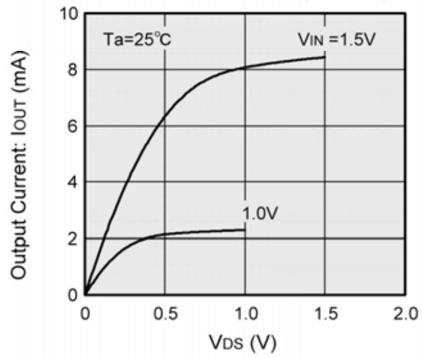
XC61GN4502 (4.5V)



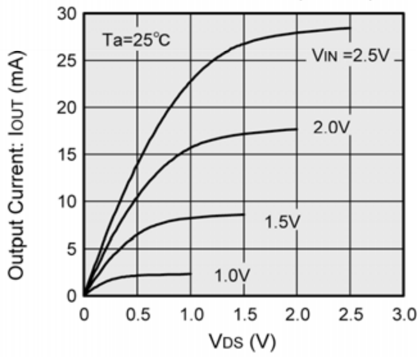
Note : The N-channel open drain pull up resistance value is 100kΩ.

(4) N-ch Driver Output Current vs. VDS

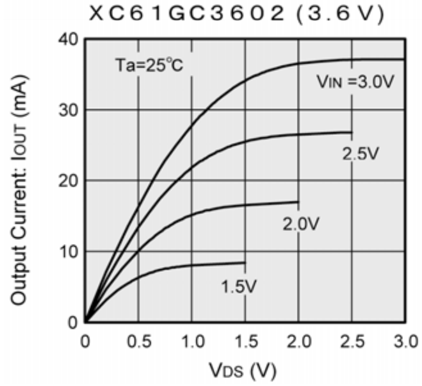
XC61GC1802 (1.8V)



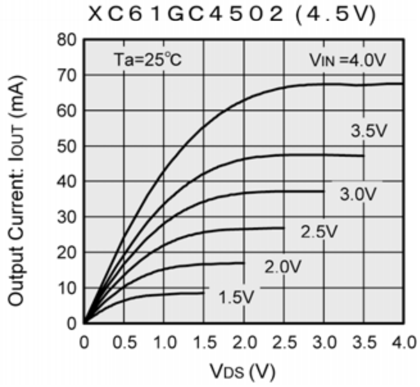
XC61GC2702 (2.7V)



XC61GC3602 (3.6V)



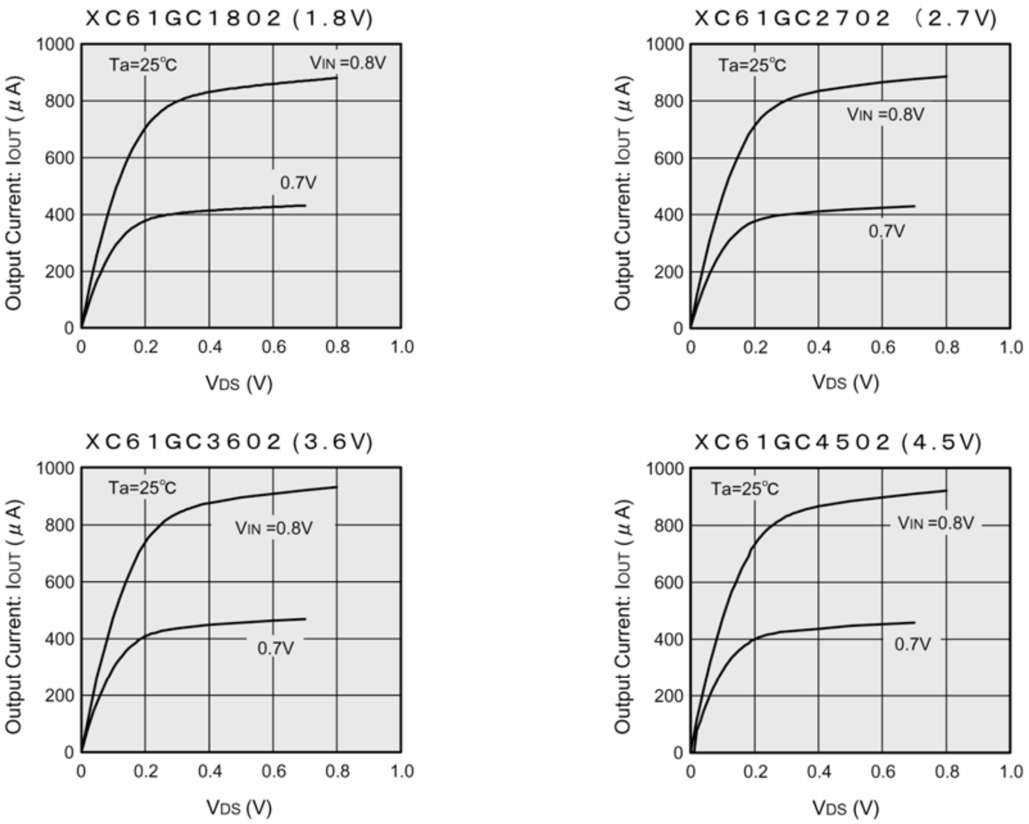
XC61GC4502 (4.5V)



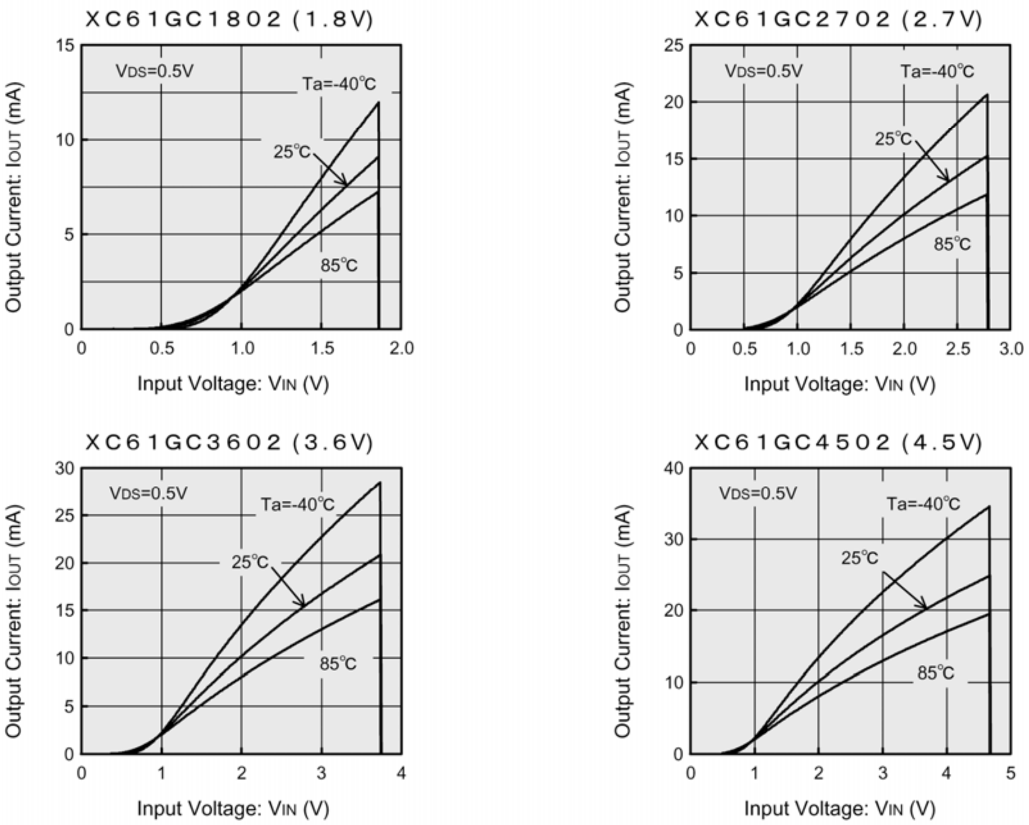
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Standard Voltage (Continued)

(4) N-ch Driver Output Current vs. VDS



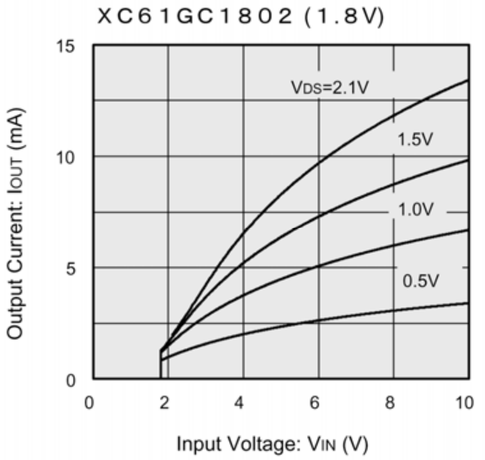
(5) N-ch Driver Output Current vs. Input Voltage

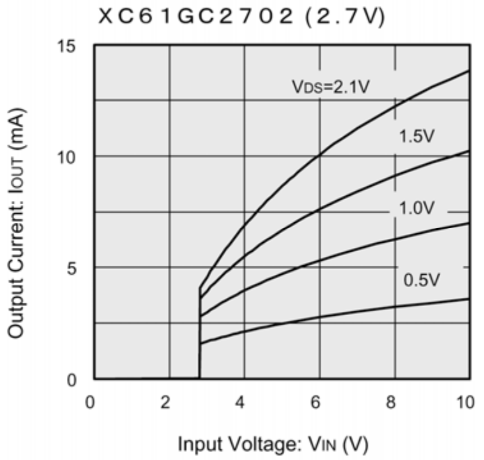


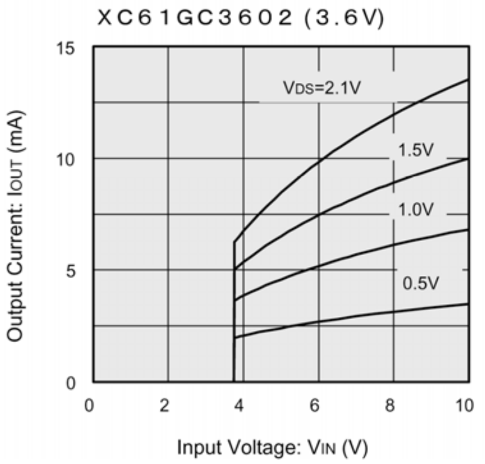
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

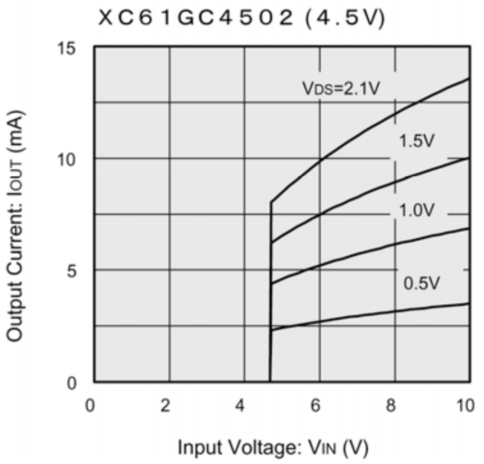
●Standard Voltage (Continued)

(6) P-ch Driver Output Current vs. Input Voltage





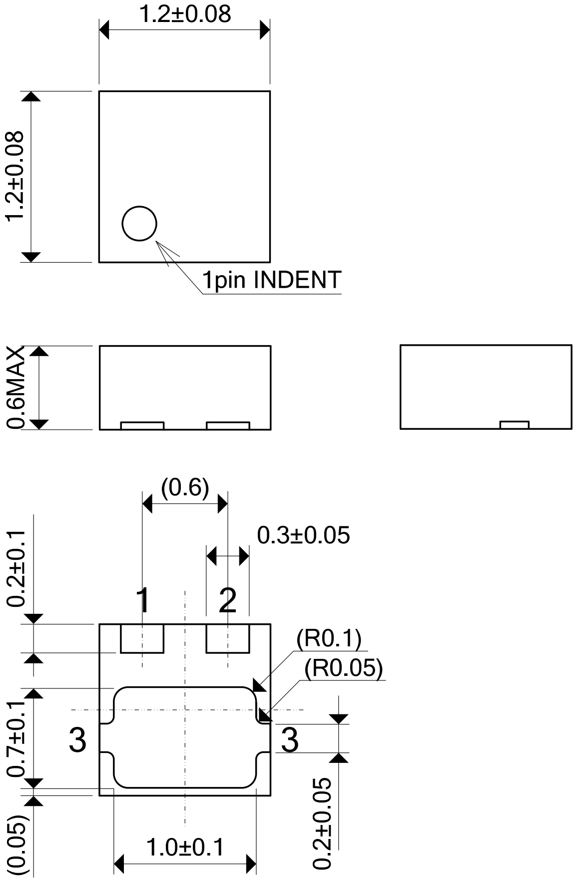




■PACKAGING INFORMATION

●USP-3

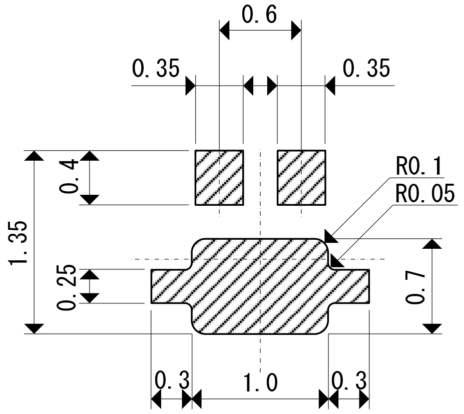
(unit : mm)



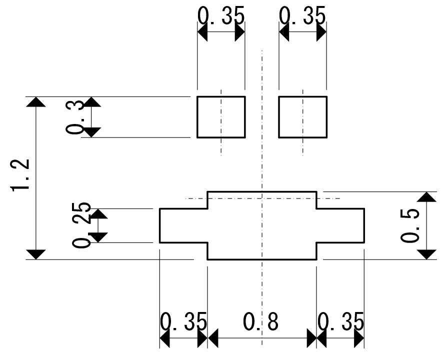
■PACKAGING INFORMATION (Continued)

●USP-3

Reference Pattern Layout Dimension

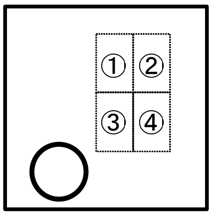


Reference metal mask design



■MARKING RULE

●USP-3



USP-3
（TOP VIEW）

① represents integer of output voltage and detect voltage

CMOS Output (XC61GC series)

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.x
B	CMOS	1.x
C	CMOS	2.x
D	CMOS	3.x
E	CMOS	4.x
F	CMOS	5.x
G	CMOS	6.x

N-channel Open Drain Output (XC61GN series)

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.x
L	N-ch	1.x
M	N-ch	2.x
N	N-ch	3.x
P	N-ch	5.x
R	N-ch	6.x
S	N-ch	7.x

② represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	x.0	5	x.5
1	x.1	6	x.6
2	x.2	7	x.7
3	x.3	8	x.8
4	x.4	9	x.9

③ based on internal standards

MARK
3

④ represents production lot number

0 to 9, A to Z repeated　(G, I, J, O, Q, W excluded)