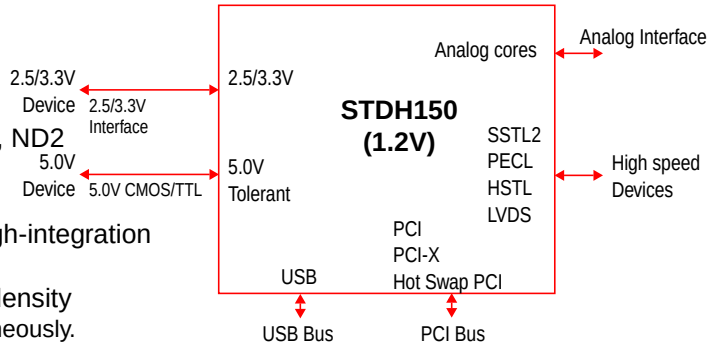
STDH150 Standard Cell
0.13um System-On-Chip ASIC

Jan 2002, V1.0

Features

- L_{drawn} = 0.13um
- Up to 34.3 million gates
- Power dissipation: 13nW/MHz@1.2V, 2SL, ND2
- Gate Delay: 34ps@1.2V, 2SL, ND2
- 2.5/3.3V drive and 5V tolerant I/O
- High-speed compiled SRAM/ROM with high-integration
- 1.2V and 3.3V ADC,DAC and PLLs
- ARM920T/ARM940T, TeakLite/TeakHigh-density

NOTE: 2.5V and 3.3V cannot be used simultaneously.



Description

STDH150 is one of the Samsung ASIC library, which consists of standard cell products implemented in a 0.13um technology. STDH150 utilizes seven layers of interconnect metal having metal 4, 5, 6 and 7 layer options for products. STDH150 is diverse application specific digital and analog IPs for system-on-chip(SOC) application. Samsung provides a full range of products to address the challenges of producing high-speed devices that take advantage of SOC integration.

STDH150 which reduced power dissipation and system cost by merging the logic and IPs as a whole and connecting internally from logic to memory data bus is ideal for high-performance products such as HDD, Network, and Display.

STDH150 supports up to 34.3 million gates counts of logic providing 85% of usable gate. Gate delay is 20%~30% faster than that of STD150, 0.13um library. Logic density is 30% less than that of STD150.

STDH150 also supports fully user-configurable compiled memory elements for high-speed with minimum area loss. In STDH150, the density of compiled memory is 15% less than that of STD150. Each element is provided as a compiler. For high-capacity memory solution in SOC design, the repairable memory containing redundancy scheme is also provided as a compiler.

Variety of IPs are provided in STDH150 family including

- Processor Cores :
  ARM7T/ARM9T/ARM940T/ARM920T/ ARM946E/ARM926EJ/ARM1020E/ETM7/ ETM9 from ARM, TeakLite/TEAK from DSPG
- Memories
  High-speed compiled SRAM/ROM, High-speed repairable SRAM with redundancy
- Analog Cores :
  ADC, DAC, PLL
- IO IPs :
  USB, PCI-X, ATA-6, LVDS, SSTL2, HSTL, PECL

Samsung design methodology offers an comprehensive timing driven design flow including automated time budgeting, tight floorplan synthesis integration, powerful timing analysis and timing driven layout. Its advanced characterization flow provides accurate timing data and robust delay models for a 0.13um very deep-submicron technology. Static verification methods such as static timing analysis and formal equivalence checking provide an effective verification methodology with a variety of simulators. Samsung DFT methodology supports scan design, BIST and JTAG boundary scan. Samsung provides a full set of test-ready IPs with an efficient core test integration methodology.

Samsung ASIC Macros

Analog Cores

- Ultra low voltage analog cores: 1.2V
- High resolution analog cores: 3.3V

Analog Cores	Bit	Supply Voltage		
		3.3V± 5%	2.5V± 5%	1.2V± 5%
ADC	8	- 125MHz	-	30MHz
	10	- 500KHz	- 30MHz	-
DAC	10	- 250MHz	- 300MHz	-
	12	- 250MHz	- 80MHz	-
PLL		-	-	- 50 ~ 300MHz - 100 ~ 500MHz

Digital Cores

Application	Hard macro	Soft macro
ARM cores	- ARM7TDMI - ARM9TDMI - ARM940T - ARM920T - ARM1020E	ARM946E ARM926EJ ETM7, ETM9 AMBA
DSP cores	- Teaklite - Teak	-
Interface cores	-	USB1.1, USB2.0, IrDA UART(16C450,16C550) IEEE1284, P1394a LINK
Communica-tion cores	-	10/100 Ethernet MAC
Peripheral cores for ARM	Memory Controller DAM Controller Timer, WDT, GPIO, SSI, Color LCD con-troller smart CARD I/F	

Memory Compiler

- Fully user-configurable SRAM/ROM
- Single-port(1RW, 1R), dual-port(2RW), multi-port(1R1W, 2R1W, 2R2W)
- Duty-free cycle and zero hold time in synchronous
- Bit-write feature available
- Flexible column mux
- Up to 1M-bit repairable SRAM
- Up to 4M-bit high-capacity SRAM/ROM

Name	Description
SPSRAM_HDH	- Single Port Synchronous static RAM - up to 256Kbits
SPSRAMBW_HDH	- SPSRAM with Bit-Write - up to 256Kbits
SPSRAMR_HDH	- SPSRAM with Redundancy - up to 1Mbits
DPSRAM_HDH	- Dual Port Synchronous static RAM - up to 128Kbits
DPSRAMBW_HDH	- DPSRAM with Bit-Write - up to 128Kbits
VROM_HDH	- Synchronous Via-1 programmable ROM - up to 1Mbits
SRFRAM_HDH	- Multi-port Synchronous Register File - 1R1W, 2R1W and 2R2W available - up to 16Kbits
SRFRAMBW_HDH	- SRFRAM with Bit-Write - 1R1W, 2R1W and 2R2W available - up to 16Kbits
FIFO_HDH*	- Synchronous First-In First-Out Memory - up to 64Kbits
CAM_HDH*	- Synchronous Content Addressable Memory with Binary - up to 32Kbits
HCSPSRAM_HDH*	- Single-Part Synchronous static SRAM with burst Read/Write Feature - up to 4Mbits
HCVROM_HDH*	- Synchronous Via-1 Programmable ROM - up to 4Mbits

* On demand

I/Os and I/O IPs

- 2.5V and 3.3V drive I/Os, and 5V tolerant I/O
  - If you want 3.3V tolerant I/O, please contact SEC technical service engineer
- 3-level (high, medium, no) slew rate control
- Driving capability
  - 1,2,4,8,12mA(for drive I/Os)
  - 1,2,4,6mA(for tolerant I/Os)
- I/O IPs

Name	Description	Frequency(MHz)
PCI	2.2 compliant, 5V tolerant	33, 66
USB	2.0 compliant, High Speed/Full Speed/ Low Speed	480/12/1.5Mbps
SSTL2	Class-I and II, SDRAM Interface	Up to 200
ATA	ATA-6/UDMA100, 3.3/5V tolerant	
PECL	ATM interface	200(single) 500(differential)
HSTL	1.5V, SRAM interface	300
Hot Swap PCI	1V pre-charge, VIO precharge	33, 66
PCI-X	1.0 compliant, 3.3V	133
LVDS	TIA/EIA-644	300

Recommended Operating Conditions

	Parameter	Rating		Unit
V_{DD}	DC supply voltage	1.2V I/O	1.1 to 1.3	V
		2.5V I/O	2.3 to 2.7	
		3.3V I/O	3.0 to 3.6	
		5V tolerant I/O	3.0 to 3.6	
	Analog Core DC supply voltage	3.3V core	3.3V± 5%	
		2.5V core	2.5V± 5%	
		1.2V/1.5V core	1.2V± 5%	
T_A	Commercial temperature range		0 to 70	°C
	Industrial temperature range * If you want this range, please contact field application engineer in Samsung.		– 40 to 85	

ASIC Design Kit and EDA support

Design Flow	Design Kits
Logic Synthesis	Synopsys Design Compiler
Physical Synthesis	Synopsys Physical Compiler
Logic Simulation	Cadence Verilog-XL, Cadence NC-Verilog/VHDL, Mentor ModelSim-Verilog/VHDL, Synopsys VCS
Scan Insertion and ATPG	Synopsys BSDCompiler, Synopsys TetraMax, Mentor Fastscan
Static Timing Analysis	Synopsys PrimeTime
RC Analysis	Avant! Star-RCXT
Power Analysis	Synopsys DesignPower, CubicPower*, Sequence WattWatcher
Formal Verification	Synopsys Formality, Avant ! Design-VERIFYer, Verplex Tuxedo-LEC
Fault Simulation	Cadence Verifault
Delay Calculator	CubicDelay*
Floorplanner	Avant! PlanetPL, Cadence Design-Planner, CubicPlan*
P&R	Avant! Apollo, Cadence Silicon Ensemble
DRC and LVS	Dracula, Hercules, Calibre

* In-house tools

Package Availability

Package Type	# of Pins
QFP	44,48,60,64,80,100,128.144,160,208,240 ,256,304
LQFP	32,48,64,100,128,144,160,176,208,256
TQFP	64,80,100,128,144
BGA	196,208,225,256,272,292,352,388,492
FBGA(PCB)	144,160,176,180,256
FBGA(Tape)	112,144,160,208
Multi Chip Package Availability	32,48,64,68,69,100,256

Samsung ASIC Worldwide

SSI

Samsung Semiconductor Incorporated
85 W. TASMAN DR., San Jose,
CA95134-1713, U.S.A.
TEL (1)-408-544-4545
FAX (1)-408-544-4950

SWTC

South West Technology Center
7700 Irvine Center Drive Suite 600
Irvine, CA 92618 USA
TEL (1)-949-753-7530
FAX (1)-714-236-9664

SSEG

Samsung Semiconductor Europe GMBH
ASIC Design Center, Representation Office Munich
Carl-Zeiss-Ring 9, 85737 Ismaning
TEL (49)-89-9697-7117
FAX (49)-89-9697-7126

SSEL

Samsung Semiconductor Europe Ltd.
Great West House, Great West Road
Brentford, Middlesex TW8 9DQ U. K.
TEL (44)-208-380-7115
FAX (44)-208-380-7095

SEJA

Samsung Electronics Japan Co., Ltd. ASIC Center
Hamacho Center Bldg., 16th Floor 31-1, Nihonbashi-Hamacho, 2-Chome, Chou-ku, Tokyo 103, Japan
TEL (81)-3-5641-9850(8488)
FAX (81)-3-5641-9851

CoAsia

CoAsia Microelectronics Corp.
9F, No. 69, Chou Tze St., Neihu Teipei, Taiwan
TEL (886)-2-2658-2020 Ext. 308
FAX (886)-2-2658-0101

ComSOC

ComSOC Technology Pte Ltd.,
31 International Business Park,
#04-06 Creative Resource
Singapore 609921
TEL (65)-425-2212
FAX (65)-425-2022

C&S

HaeJu bldg. 6th fl., Nonhyun-dong, Gangnam-gu, Seoul, Korea
TEL(02)-515-4468
FAX(02)-515-4469

ECT

JoonSung bldg. 4th fl., 698-30 Yeuksam-dong, Gangnam-gu, Seoul, Korea
TEL(02)-569-1960
FAX(02)-569-2388

Dawin Tech

Osuk bldg. 6th fl., 276-6 Yangje-dong, Seocho-gu, Seoul, Korea
TEL(02)-529-2826
FAX(02)-529-2827

VersaChips

Boram bldg. 6th fl., 288-2 Yangje-dong, Seocho-gu, Seoul, Korea
TEL(02)-572-0756
FAX(02)-571-3857

SAMSUNG ELECTRONICS CO., LTD.

San #24, Nongseo-Ri, Giheng-Eup,
Yongin-City, Gyeonggi-Do, KOREA
TEL : 82-031-209-6500, 6501
FAX : 82-031-209-4920
http://www.samsungelectronics.com/semiconductors/asic/asic.htm

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Introduction 1

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1.1 Library Description

STDH150 is Samsung's next generation Standard Cell library containing standard cells implemented in Samsung's 0.13µm, L13 high-speed(L13HS) process technology. Samsung's L13HS process uses 4 to 7 metal interconnect layers. The STDH150 library contains diverse application specific digital and analog IP for System-on-Chip (SoC) applications. Samsung provides a full range of cells within the STDH150 library to address the challenges of designing and producing high-speed devices that take advantage of SoC integration. STDH150 can help active system performance for high performance applications such as HDD, Networking, and Displays.

STDH150 library supports gate counts of up to 34.3 million gates with 85% usability. Gate delay is 20% faster than that of STD150, 0.13µm library. Logic and compiled memory density are twice denser than those of STD150, respectively.

STDH150 supports also fully user configurable memories suitable for high-speed applications with best density. To get much higher yield for SoC designs, it contains the repairable memory with row redundant elements for high-capacity memory.

STDH150 library also supports a wide range of I/O interface voltages and standards. I/O cells that drive 2.5V, and 3.3V are available as 5V tolerant I/Os. Available I/O standards include LVTTL, LVCMOS, PCI, PCI-X, OSC, AGP, PECL, HSTL, SSTL2, GTLp, LVDS.

To better support SoC design, a robust collection of digital and analog IP cores are available. Digital cores include the ARM7TDMI, ARM9TDMI, ARM920T, ARM940T, ARM946E-S, and ARM926E-JS from ARM Ltd., as well as the Teak and TeakLite DSP cores from the DSP Group. Analog cores include ADCs, DACs, CODECs, and PLLs with various bit configurations and frequency ranges. A thick oxide process option allows for high resolution operation of analog cores with a 3.3V power supply.

In addition, the STDH150 library supports communication and data transmission cores such as, IEEE1284, IEEE1394 link controller, UART, PCI controller, PCMCIA controller and 10/100 ethernet MAC.

Samsung's design methodology offers a comprehensive timing driven design flow including automated time budgeting, tight floor plan synthesis integration, powerful timing analysis, and timing driven layout. Our advanced characterization flow provides accurate timing data and robust delay models for L13HS, our 0.13µm very deep sub-micron process technology. Static verification methods, such as static timing analysis and formal equivalence checking, provide an effective verification methodology with a variety of simulators. Samsung's Design-for-Test (DFT) methodology supports full and partial scan chain design, BIST, JTAG boundary scan, and Built-in-Redundancy-Analysis (BIRA) for reparable SRAM. Samsung provides a full set of test ready IP cores with an efficient core test integration methodology.

1.2 Features

- Robust 1.2V standard cell library including micro processor, DSP, and analog cores.
  - 0.13µm CMOS high-speed process technology with optional 7 metal layers.
  - High gate count design of up to 46 million gates with up to 85% utilization for 7 metal layers.
  - Typical 2 input NAND gate delay of 34ps with a fanout of 2.
  - Characterized to industrial (–40˚C to 85˚C) and commercial (0˚C to 70˚C) temperature ranges.
- Robust Digital Cores
  - Hard macro cells - ARM7TDMI, ARM9TDMI, ARM920T, ARM940T, ARM946E-S, ARM926E-JS, Teak, and TeakLite.
  - ARM embedded trace macro cells - ETM7 and ETM9
  - Soft macro cells - USB1.1, IrDA, 16C450 and 16C550 UART, Fast Ether net MAC, P1394a LINK, IEEE1284, PCI controller, PCMCIA controller.
- Ultra Low Voltage (1.2V) and High Resolution (3.3V) Analog Cores
  - Analog core supply voltages (± 5%) -1.2V, 2.5V, and 3.3V.
  - ADC: 8 bit (250KHz, 1.2V and 125MHz, 3.3V), 10 bit (30MHz, 1.2V), and 12 bit (250KHz-10MHz, 3.3V)
  - DAC: 10 bit (80MHz, 1.2V), 12 bit (2MHz - 300MHz, 3.3V)
  - CODEC: 14 bit Sigma-Delta (8KHz - 11KHz, 2.5V)
  - PLL: 1.2V FSPLL (25MHz - 300MHz and 100MHz - 500MHz), SSCG (1.2V, 200MHz)
- Fully User Configurable SRAMs and ROMs
  - Suitable for high-speed memory configurations with best density
  - Single port (1RW, 1R), dual port (2RW), and multi port (1R1W, 2R1W, 2R2W)
  - Bit-write capability
  - 2 bank architecture available
  - Zero hold time for data in, address and control pins
  - Flexible aspect ratio
  - Up to 256K-bit single port(1RW) SRAM
  - Up to 1M-bit single port(1RW) repairable SRAM
  - Up to 128K-bit dual port(2RW) SRAM
  - Up to 1M-bit single port(1R) via-1 programmable ROM
  - Up to 16K-bit multi port(1R1W, 2R1W, 2R2W) register files
  - Up to 32K-bit CAM with binary (On-demand)
  - Up to 64K-bit FIFO (On-demand)
  - Up to 4M-bit single port(1RW) SRAM with burst operations (On-demand)
  - Up to 4M-bit single port(1R) via-1 programmable ROM (On-demand)
- Full Compliment of I/O Cells
  - 2.5V/3.3V drive and 5.0V tolerant I/Os
  - 3 levels (high, medium, and no) of slew rate control
  - Minimum wire bonded pad pitch
  - 60µm single in line I/Os
  - 30µm staggered I/Os
  - Drive capabilities
    - Up to 12mA for drive I/Os
    - Up to 6mA for 5V tolerant I/Os

- Standard Interface IP
  - PCI 2.1 compliant, 33/66MHz, 5V tolerant
  - USB 1.1 compliant, full speed/low speed, 3.3V
  - SSTL2 Class-I and II SDRAM interface, up to 200MHz
  - ATA4/UDMA66, 3.3V, 5V tolerant
  - AGP 2.0 compliant, 66MHz @ 1X, 133MHz @ 2X, 266MHz @ 4X
  - PECL, 200MHz single ended, 500MHz differential point-to-point ATM interface
  - HSTL, 300MHz, 1.5V SRAM interface with programmable output impedance control
  - Hot Swap PCI - 1V pre-charge, VIO pre-charge
  - PCI-X, 1.0 compliant, 133MHz, 3.3V
- Fully Integrated CAD software and EDA support
  - Logic synthesis: Synopsys Design compiler
  - Physical synthesis: Synopsys Physical compiler
  - Logic simulation: Cadence Verilog XL, Cadence NC-Verilog/VHDL, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VCS.
  - DFT, scan insertion and ATPG: Synopsys TestGen, Synopsys TestCompiler, Synopsys TetraMax, Mentor Fastscan.
  - Static timing analysis: Synopsys PrimeTime
  - RC analysis: Avant! Star-RCXT
  - Power analysis: Synopsys DesignPower, Sequence Watt Watcher, CubicPower (Samsung in-house tool).
  - Formal verification: Synopsys Formality, Avant! Design VERIFYer, Verplex Tuxedo-LEC
  - Fault simulation: Cadence Verifault
  - Delay calculator: CubicDelay (Samsung in-house tool).
  - Floor planner: Avant! PlanerPL, CubicPlan (Samsung in-house tool).
  - Place and Route: Avant! Apollo, Cadence Silicon Ensemble
  - DRC and LVS: Dracula, Hercules, Calibre
- Easy and Accurate Clock Tree Insertion
  - 12 user selectable clock tree cells
  - Accurate pre-layout and post-layout correlation
  - Insertion delay, skew, transition time management
  - Clock tree information file generation
  - Tightly coupled with in-house delay calculator, CubicDelay.

For more information on the CTC flow, refer to "Clock Analysys Flow (with CTC) User Guide for CubicDelay" included in the Samsung Design Kit.

1.3 EDA Support

Samsung provides an effective solution for multi-million gate designs in very deep submicron technology. For large SoC designs, our static timing verification methodology will reduce design cycle time and reduce ever increasing time-to-market pressure. Our design-for-test (DFT) methodology and service enables all phases of test insertion, test pattern generation, and fault grading resulting in the highest test coverage.

The STDH150 design methodology supports a rich collection of industry standard EDA tools from Cadence, Synopsys, Mentor Graphics, and Avant! on Solaris and HP platforms. Customers may choose from among industry leading EDA tools for design capture, synthesis, simulation, DFT and layout. Several powerful proprietary software tools are seamlessly integrated in our design kits to improve design quality.

The STDH150 design methodology uses a proprietary delay calculator, CubicDelay, for high timing simulation accuracy. Cell delay is calculated based on a matrix of delay parameters for each macrocell and signal interconnection delay is calculated based on RC tree analysis.

1.4 Product Family

STDH150 library includes the following design elements:

- Analog core cells
- Digital core cells
- Internal macrocells
- Compiled memory macrocells
- Input/Output cells

1.4.1 ANALOG CORE CELLS

Introduction to Analog Cores (see Appendix A for a glossary of analog terms)

Samsung is a leading supplier of cell based mixed signal design elements. As a leading supplier of mixed signal elements, Samsung has more analog design experience than other ASIC suppliers. Analog cell development has been and will continue to be a part of the strategic focus of Samsung ASIC. Symbolic representations of analog cells are supplied for design entry by Customers or a Samsung design or technology center and are replaced with the cell physicals during place and route. Samsung design methodology uses the same automatic layout and verification tools for analog cells as for digital cells. Mixed signal designs are processed on the same production line as pure digital designs.

Samsung's analog core family consists of ADCs, DACs, PLLs, and CODECs. A brief description of each follows.

Analog-to-Digital Converter

Analog-to-digital converters, ADCs, provides the link between the analog world and digital systems. An ADC produces a digital output, D, as a function of the analog input, A:

$$D = f(A)$$

While the input can assume an infinite number of values, the output takes on only a finite set of digital values determined by the converter's resolution or output word length. Thus, the ADC must approximate each input level with one of these values. This process is also called quantization.

In digital systems, the input signal amplitude, A, is sampled at discrete time intervals and is then quantized into discrete steps and output as a digital value, D. The sampling time interval is also known as the sampling frequency.

Digital-to-Analog Converter

Digital-to-Analog Converters, or DACs, are the digital value to analog signal conversion circuits. The output can be in the form of a current or a voltage wave form. DACs provide the interface between digital systems and the analog world. DACs are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digital controlled attenuators, and process control actuators.

Figure 1-1 shows the functional block diagram of a basic DAC. The input to the DAC is a digital value, D, made up of a stream of bits. The output analog current or voltage quantity, A, is related to the input as:

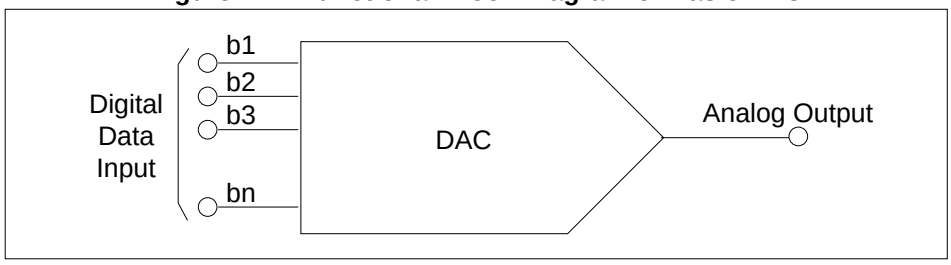
$$A = KV_{REF}\left[\frac{b1}{2^1}+\frac{b2}{2^2}+\ldots+\frac{bn}{2^n}\right]$$

where K is a scale factor, V_{REF} is a reference voltage, n is the resolution expressed as the total number of bits, and b1, b2, …, bn are the bit coefficients. The output exhibits 2^n discrete voltage levels ranging from zero to a maximum value of

$$Vo(max) = V_{REF}\frac{2^n-1}{2^n}$$

with a minimum step change ΔVo given as $\Delta Vo = \frac{V_{REF}}{2^n}$

Figure 1-1. Functional Block Diagram of Basic DAC



Sigma-Delta ADC/DAC

Samsung's L13HS process offers high speed and high density, but reduced accuracy and signal range (dynamic range) for analog components. Hence, an exchange of digital complexity and resolution in time for resolution in signal amplitude is needed. A good solution to this trade-off is an over sampling data converter. An over sampling sigma-delta converter is ideal for slow speed (audio band) applications. It's noise shaping (sigma-delta) feature produces a high resolution output with a signal to noise ratio of 90 to 100dB.

In an ADC, an analog signal is converted to a differential signal and then filtered with an anti-aliasing filter. A sigma delta modulator converts the signal into an over sampled noise-shaping 1-bit pulse density modulated (PDM) signal. A digital decimation filter then rejects the out-of-band noise and outputs a 16-bit high resolution digital signal that is down sampled to the sampling rate, Fs. In a DAC, digital data is over sampled by an interpolation filter and is converted to a noise shaped 1-bit PDM signal through a digital sigma-delta modulator. An analog SoC post filter rejects the out-of-band noise. An anti-image filter then rejects the sampling images and outputs a high resolution analog signal.

Phase Locked Loop

Samsung's PLL cores are implemented as an analog function to provide frequency multiplication enabling SoC designers to synchronize chip level clock networks to a common reference signal.

In the past, designers wishing to incorporate a PLLs into a digital design had only two options:

1) Use a special mixed signal process, typically an expensive process combing bi-polar and CMOS processing on the same silicon, to implement the analog functions.

2) Use and all digital PLL design requiring very large silicon area so that the PLL could be implemented in a standard CMOS digital process. This type of PLL design usually exhibits poor locking time.

Samsung's PLL cores are analog PLLs implemented on our standard digital CMOS process. Advantages of Samsung's PLL cores are:

* Require only a few off-chip passive components to implement the PLL function.
* No need for an expensive mixed signal (bi-polar and CMOS) process.
* Provide a faster locking time than a full digital implementation.
* Have low jitter characteristics.

Customer Service and Technical Support

Samsung provides full support for our customers needing analog cores. Support is provided through Samsung's worldwide Technology and Design Centers. In addition, Samsung analog design engineers are available to design or customize Samsung analog cores to meet specific customer needs. Since mixed signal design is quite different from digital design in terms of design techniques, layout, and test methodology, Samsung provides a mixed signal technical guide describing all development steps. In addition, each core is fully documented and is delivered with a data sheet. The following is a description of analog core data sheets:

Core Preview

Describes the main features and specifications for a core that is under development. Some specifications, such as the exact pin-out, may not be finalized at the time of publication. The purpose of this document is to provide customers with advanced product planning information.

Preliminary Data Sheet

Completely describes a new core. The preliminary data sheet contains a feature list, applications notes, timing diagrams, theory of operation, core pin information, a test guide, a layout guide, and preliminary AC/DC electrical information. The electrical information is based on worst case simulation data and prototype silicon performance. The purpose of this data sheet is to allow customers to confidently begin active development with the core.

Final Data Sheet

Updated version of the preliminary data sheet reflecting fully characterized silicon performance. Updates include more complete and tighter electrical specifications. The purpose of this data sheet is to communicate the confirmed performance of the core after full characterization and passing qualification.

1.4.2 STANDARD LOGIC CELLS

Samsung standard cell library is designed to enable designers to achieve the high-speed with best density in STDH150. In addition, this standard cell library is carefully verified on silicon to ensure much higher manufacturability. Due to this, system-on-chips (SoC) designed using these standard cells will be obtained much higher yield. Rich standard cells, consisting of about 396 cells, with at least four drive strengths have been optimized specifically for synthesis and place and route tools.

The cells were selected to achieve best performance with synthesis tool and to give designers the elements the need to create high-speed designs. Each cell has been carefully hand-crafted to provide the optimal solution for high-speed applications with best density.

Each of cells has been very accurately modeled for both timing and power to guarantee timing closure and to eliminate many meaningless iterative design cycles. All models are carefully qualified and tested using the in-house library automation environment. Some of features in STDH150 standard cell library are summarized as follows:

- Complete optimized library with synthesis and place and route tool
- Hand-crafted layouts for the optimal densities for each process
- Low manufacturing cost
- Reducing design time
- Providing more accurate timing and power
- Complete interfaces with all popular EDA tools

STDH150 standard cell library contains a protection diode cell. The protection diode cell is used to avoid the antenna effect. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the antenna effect rule. The protection diode cell can be used in this case to add a diode on the net close to the input gates which do not meet the rule. Also, the protection diode can be added to the input drivers of soft-macro cores. The protection diode cell is composed of forward and reverse diodes. It is not included in this databook.

In addition, STDH150 standard cell library contains several filler cells. During place and route, the filler cells are used to connect power and ground rails across an area including no cells. The filler cells are also used to make sure that gaps do not occur between well or implant layers which may cause some of design rule violations.

1.4.3 COMPILED MEMORY

Today's System-On-Chip (SoC) designs require various configurations of embedded memories. These configurations must be optimized for each process and also optimized for speed, density, and power consumption. Samsung's memory compiler, called CubicCompiler, is designed under the efficiency of custom memory design to achieve optimal designs. Using CubicCompiler is helpful for designers to perform optimal floorplanning of the design because designers can evaluate architectural tradeoffs between performance, area and power by easily varying the aspect ratios, word depths and word widths of their designs.

Once satisfied with the resulting configuration, CubicCompiler allows designers to easily generate complete EDA models including functional model, timing model, physical layout. In STDH150, high-speed compiled memory with best density is only supported. The high-speed memories are fully optimized for denser area and are targeted for high-speed applications. Memories in STDH150 are fully user-configurable and are provided as a compiler as follows:

High-Speed Compiled Memories
- Single-port synchronous SRAM
- Single-port synchronous SRAM with bit-write
- Single-port synchronous SRAM with redundancy
- Dual-port synchronous SRAM
- Dual-port synchronous SRAM with bit-write
- Dual-port synchronous SRAM with redundancy
- Multi-port synchronous register file
- Multi-port synchronous register file with bit-write
- Single-port Synchronous Binary CAM
- Single-port Synchronous Ternary CAM
- Single-port synchronous via-1 programmable ROM
- Synchronous First-In First-Out Memory (On-demand)
- High-capacity (Up to 4Mbits) single-port synchronous SRAM with burst operations (On-demand)
- High-capacity (Up to 4Mbits) single-port synchronous via-1 programmable ROM (On-demand)

STDH150 compiled memory families adopt most advanced memory design techniques such as self-controlled timing circuits, partial activation architecture, multi-stage low power decoding structure and high-sensitivity sense amplifiers with high stability, to dramatically improve the performance. Such circuits are extensively optimized for the specified voltage, temperature and process and give designers high performance and high stability.

All of compiled memories provide edge-triggered synchronous read and write operations, bit-write or byte write capability, and zero hold time for data-in, addresses and control pins. Fully static design provides low-voltage data retention and zero standby current. In case of multi-port register file, 2-port(1-read/1-writ), 3-port(2-read/1-write) and 4-port(2-read/2-write) are available.

As speciality memory, two types of memories are supported by customer's requirements: Synchronous First-In First-Out Memory (FIFO) and synchronous Content Addressable Memory with Binary state (CAM). FIFO, which is widely used in communication buffering types of applications, has also fully synchronous operation at the rising-edge of clock. CAM, which is useful in many applications such as cache tag tables and translation look-up table buffers, has also fully synchronous operation at the rising-edge of clock. Additional information about the above speciality memory can be obtained from your local Samsung and Design Center or Samsung's worldwide headquarters.

In SoC(System-On-Chip) design, memory becomes much more dominant and larger memory is required. To support it, the high-capacity memory, which covers from 2M-bit to 4M-bit, is provided as the user-configurable compiler: High-Capacity Single-Port Synchronous SRAM with Burst features (HCSPSRAM) and High-Capacity Single-Port Synchronous Via-1Programmable ROM (HCVROM). HCSPSRAM contains both Row-Redundancy and Column-Redundancy schemes to guarantee higher yield and provides 4 burst-read and burst-write operations suitable for cache applications. HCVROM is via-1 programmable and is targeted for high-speed applications with best density. HCVROM can be easily extended to up to 4Mbits. Those memories will be also supported by customer's requirements. Additional information can be obtained from your local Samsung and Design Center or Samsung's worldwide headquarters.

Built-In-Self-Test (BIST) circuitry is available for most of STDH150 compiled memories. BIST circuits are designed to detect a set of fault types that impact the functionality of memory and is generated by a softmacro-based BIST generator. The softmacro-based BIST generator generates either an individual BIST netlist for each memory or a shared BIST netlist for all memories use in a design. However, when several memories of the same or the different type area used in the design, if you generate the individual BIST netlist for each memory, there are some redundant blocks because the individual BIST netlist has same function. In this case, it would better use the shared BIST netlist to eliminate such redundancies. In case of the compiled memory with redundancy, it supports Built-In-Redundancy-Analysis (BIRA) to repair failed bits.

1.4.4 INPUT/OUTPUT CELLS

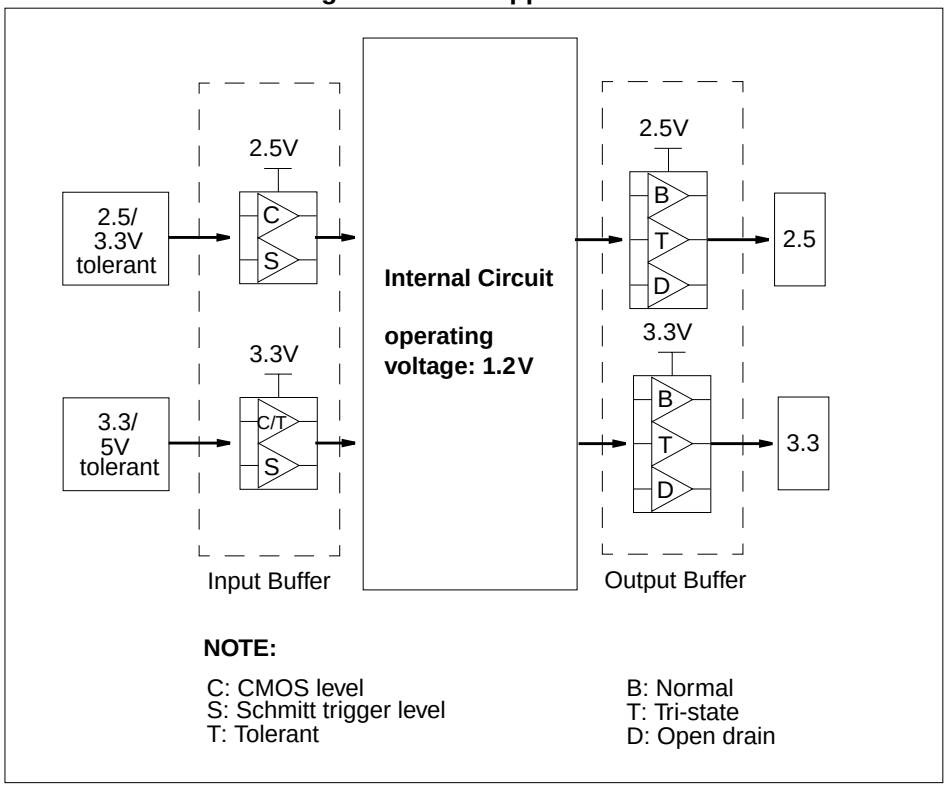
There are about 580 different I/O cells in the STDH150 library for the designer to choose from. Three types of output buffers and bi-directional buffers (non-inverting, tri-state, and open drain) are available in a range of drive capabilities from 1mA to 12mA for 2.5V, and 3.3V drive outputs, and from 1mA to 6mA for 5V tolerant I/O cells. Three levels of slew rate control are provided for each buffer type except 1mA and 2mA drive buffers, to reduce output power and ground noise and signal ringing, especially for simultaneously switching outputs. All I/O buffers have been fully characterized for ESD protection and latch-up resistance.

Test logic is provided to enable efficient parametric testing on input buffers including LVCMOS and TTL level converters, Schmitt trigger input buffers, clock drivers, and oscillator buffers. 100k ohm pull-down and pull-up resistors are optional features.

1.4.4.1 I/O Applications

To support mixed voltage environments, LVCMOS and Schmitt trigger I/O cells are available at 2.5V, 3.3V interface and 5V tolerant interface. The I/O application diagram is as follows.

Figure 1-2. I/O Applications



NOTE: It is not allowed to use together the 2.5V / 3.3V interface IO in a chip.

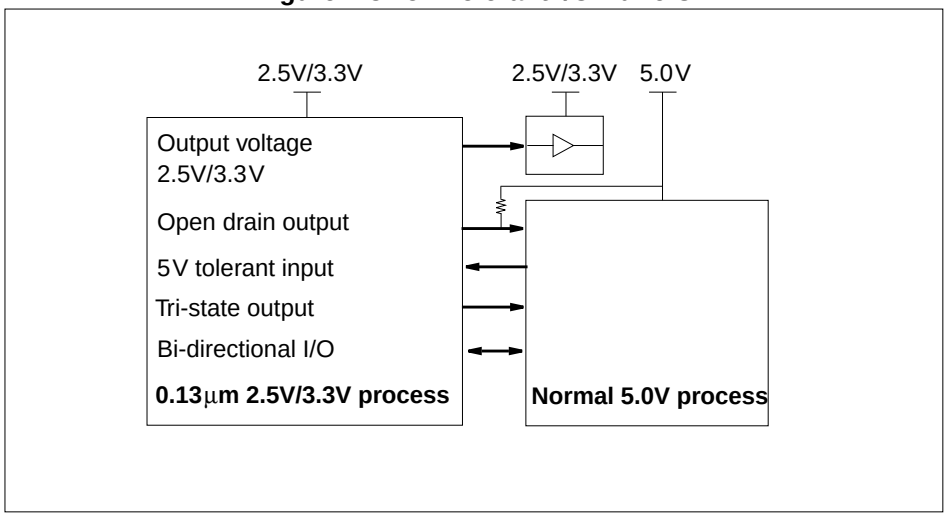
1.4.4.2 I/O Cell Drives Options

To provide flexibility, the designer can choose from various output current drive levels. The choice of current drive level affects propagation delay and noise. Slew rate control helps decrease system noise and output signal overshoot and undershoot caused by the switching of output buffers. The output signal edge slew rates can be slowed down by selecting the high slew rate control cells.

1.4.4.3 5V Tolerant I/O Buffers

Samsung's L13HS process has a thick gate oxide option that is optimized for 2.5V/3.3V circuit operation. The specified maximum voltage across the gate oxide of this process option is 5.25V to avoid gate oxide breakdown. A special circuit is available for a 5V tolerant LVCMOS driver of up to 6mA. This 5V tolerant driver can be used as a normal 2.5V or 3.3V buffer.

Figure 1-3. 5V Tolerant I/O Buffers



1.4.4.4 PCI Buffers

PCI buffers are designed for industry standard PCI high performance 32 or 64 bit local bus applications. The STDH150 library offers input, output, and bi-directional PCI buffers for 33MHz and 66MHz operation compliant with PCI local bus specification 2.2.

1.4.4.5 USB (Universal Serial Bus) Buffers

The STDH150 library offers full speed and low speed USB 1.1 compliant buffers.

1.4.4.6 Other Buffers

The STDH150 library also offers various other I/O buffers including HSTL, SSTL2, GTLp, AGP, PECL, and LVDS. For more information about I/O buffers that are not included in this data book, please contact your local Samsung Technology and Design Centers.

1.5 Timings

1.5.1 WIRE LENGTH LOAD

Table 1-1, Table 1-2, and Appendix B show the equivalent standard load matrix for 4, 5, 6 and 7 metal layer interconnect. The equivalent standard load values are a function of the gate count and fanout. These values are based on capacitive loading and are used with wire length estimates which affect propagation delay.

Table 1-1. Equivalent Standard Loads for 4-layer and 5-layer Metal Interconnect

Gate Count	Fanouts													
	1	2	3	4	5	6	7	8	16	32	64	130	131	132
4LM														
5000	0.569	0.996	1.646	2.364	2.748	3.364	3.766	5.041	7.224	12.585	24.466	27.283	48.047	52.874
10000	0.594	1.443	1.817	2.720	3.079	4.278	4.933	5.957	8.581	14.628	29.120	31.937	54.478	58.819
50000	0.661	1.801	2.528	4.228	5.175	6.356	7.533	7.974	10.281	15.988	31.185	35.624	57.228	60.929
100000	0.982	2.004	3.126	4.518	5.404	6.579	8.691	9.118	11.872	17.179	34.996	43.248	70.549	74.464
150000	3.803	5.152	5.740	7.283	7.874	8.941	9.579	10.276	13.037	19.028	36.644	43.970	77.254	77.852
200000	5.313	6.031	6.783	7.819	8.587	9.561	10.232	10.817	13.707	20.150	38.169	45.913	81.195	81.827
300000	5.846	6.405	7.461	8.705	9.535	10.602	11.331	11.968	15.146	22.238	40.201	47.244	89.551	90.246
400000	6.382	7.348	8.083	9.394	10.313	11.480	12.285	12.951	16.374	23.994	42.291	47.925	96.621	97.354
500000	7.116	8.598	9.081	10.535	11.555	12.852	13.746	14.526	17.427	25.545	45.378	51.010	102.829	103.634
600000	7.620	9.073	9.778	11.327	12.409	13.799	14.750	15.616	17.929	26.283	48.248	52.472	105.777	106.622
800000	8.778	11.100	11.360	13.134	14.374	15.967	17.059	18.106	19.374	28.411	53.894	56.709	114.309	115.246
1000000	9.860	11.602	12.841	14.823	16.205	17.992	19.215	20.435	20.718	30.394	56.413	60.638	122.236	123.260
1500000	12.833	15.508	16.870	19.425	21.213	23.528	25.108	26.785	29.642	36.346	68.258	72.482	146.100	147.376
2000000	15.610	19.274	20.650	23.744	25.902	28.715	30.626	32.736	38.303	41.915	76.518	83.559	168.425	169.933
2500000	18.213	23.191	24.183	27.781	30.293	33.567	35.795	38.305	41.838	47.116	88.273	93.905	189.277	191.004
3000000	20.650	25.447	27.490	31.559	34.394	38.104	40.624	43.514	45.138	51.970	99.332	103.559	208.730	210.659
4000000	23.689	28.614	31.539	36.207	39.457	43.714	46.606	49.919	53.762	59.626	113.175	118.809	239.464	241.681
5000000	26.563	34.346	35.364	40.596	44.246	49.018	52.262	55.974	55.268	66.858	119.138	133.220	268.511	270.996
6000000	29.787	37.789	39.651	45.522	49.614	54.962	58.602	62.766	65.667	74.966	140.927	149.380	301.082	303.868
7000000	32.419	45.929	49.329	54.305	57.604	61.360	65.423	72.876	76.525	93.260	185.830	188.960	374.548	378.017
8000000	36.354	51.498	55.311	60.892	64.590	68.805	73.360	81.716	85.472	104.569	189.592	208.370	419.981	423.867
5LM														
5000	0.518	0.906	1.496	2.150	2.498	3.059	3.423	4.583	6.567	11.441	22.242	24.803	43.679	48.067
10000	0.541	1.311	1.652	2.472	2.799	3.888	4.484	5.415	7.801	13.297	26.472	29.033	49.525	53.472
50000	0.600	1.638	2.297	3.844	4.705	5.778	6.848	7.250	9.346	14.535	28.350	32.386	52.025	55.390
100000	0.894	1.821	2.843	4.106	4.911	5.980	7.902	8.289	10.793	15.618	31.815	39.317	64.136	67.695
150000	3.457	4.683	5.218	6.622	7.157	8.128	8.709	9.341	11.852	17.297	33.313	39.972	70.230	70.775
200000	4.831	5.482	6.167	7.108	7.805	8.691	9.301	9.833	12.461	18.317	34.699	41.740	73.813	74.388
300000	5.315	5.823	6.781	7.913	8.669	9.638	10.301	10.880	13.770	20.216	36.545	42.949	81.409	82.041
400000	5.801	6.681	7.348	8.539	9.376	10.437	11.169	11.774	14.886	21.813	38.447	43.569	87.829	88.504
500000	6.468	7.817	8.256	9.577	10.504	11.683	12.496	13.205	15.842	23.222	41.252	46.372	93.480	94.212
600000	6.927	8.248	8.888	10.297	11.281	12.545	13.409	14.197	16.299	23.894	43.862	47.703	96.161	96.929
800000	7.980	10.091	10.327	11.939	13.067	14.516	15.508	16.461	17.612	25.829	48.994	51.553	103.917	104.769
1000000	8.965	10.547	11.673	13.474	14.732	16.356	17.468	18.577	18.835	27.630	51.285	55.126	111.124	112.055
1500000	11.665	14.098	15.337	17.659	19.283	21.388	22.825	24.350	26.947	33.041	62.053	65.894	132.819	133.978
2000000	14.191	17.522	18.772	21.585	23.547	26.104	27.842	29.760	34.821	38.104	69.561	75.962	153.114	154.484
2500000	16.557	21.083	21.984	25.256	27.539	30.516	32.541	34.823	38.035	42.833	80.248	85.368	172.071	173.639
3000000	18.772	23.134	24.990	28.691	31.268	34.640	36.931	39.557	41.033	47.246	90.303	94.144	189.754	191.507
4000000	21.535	26.014	28.671	32.915	35.870	39.740	42.370	45.382	48.874	54.205	102.886	108.008	217.694	219.710
5000000	24.148	31.224	32.150	36.905	40.224	44.561	47.510	50.886	50.244	60.779	108.307	121.110	244.102	246.360
6000000	27.079	34.354	36.047	41.384	45.104	49.966	53.275	57.059	59.697	68.151	128.116	135.799	273.710	276.244
7000000	29.472	41.754	44.844	49.368	52.368	55.781	59.476	66.250	69.569	84.781	168.937	171.781	340.499	343.651
8000000	33.049	46.817	50.283	55.356	58.718	62.549	66.691	74.287	77.703	95.063	172.356	189.427	381.800	385.334

Table 1-2. Equivalent Standard Loads for 6-layer and 7-layer Metal Interconnect

Gate Count	Fanouts													
	1	2	3	4	5	6	7	8	16	32	64	130	131	132
6LM														
5000	0.467	0.815	1.346	1.935	2.248	2.754	3.081	4.124	5.909	10.297	20.018	22.323	39.311	43.260
10000	0.486	1.179	1.486	2.224	2.520	3.498	1.035	4.874	7.022	11.968	23.825	26.130	44.573	48.126
50000	0.541	1.474	2.067	3.461	4.234	5.201	6.163	6.526	8.411	13.083	25.516	29.148	46.823	49.850
100000	0.805	1.638	2.559	3.695	4.419	5.382	7.112	7.461	9.715	14.057	28.634	35.386	57.722	60.925
150000	3.110	4.215	4.697	5.961	6.441	7.821	7.839	8.405	10.667	15.567	29.982	35.974	63.207	63.699
200000	4.348	4.935	5.551	6.398	7.026	7.821	8.372	8.850	11.215	16.484	31.228	37.567	66.431	66.949
300000	4.783	5.240	6.104	7.122	7.803	8.673	9.272	9.791	12.392	18.195	32.892	38.653	73.268	73.836
400000	5.220	6.014	6.614	7.685	8.439	9.394	10.053	10.596	13.398	19.632	34.602	39.213	79.045	79.653
500000	5.821	7.035	7.431	8.618	9.453	10.516	11.246	11.884	14.258	20.900	37.126	41.734	84.132	84.791
600000	6.234	7.423	8.000	9.268	10.154	11.291	12.069	12.778	14.669	21.504	39.476	42.933	86.545	87.236
800000	7.183	9.081	9.293	10.746	11.760	13.065	13.957	14.815	15.850	23.246	44.094	46.398	93.525	94.293
1000000	8.069	9.492	10.506	12.128	13.260	14.720	15.722	16.718	16.951	24.866	46.157	49.614	100.012	100.850
1500000	10.498	12.689	13.803	15.894	17.354	19.248	20.543	21.915	24.252	29.738	55.848	59.305	119.537	120.580
2000000	12.772	15.770	16.894	19.425	21.193	23.494	25.059	26.783	31.339	34.293	62.604	68.366	137.803	139.035
2500000	14.902	18.974	19.785	22.730	24.785	27.465	29.287	31.340	34.232	38.549	72.222	76.831	154.864	156.275
3000000	16.894	20.821	22.492	25.821	28.142	31.175	33.238	35.600	36.929	42.522	81.273	84.730	170.777	172.356
4000000	19.382	23.411	25.805	29.624	32.283	35.766	38.134	40.844	43.986	48.783	92.596	97.206	195.925	197.740
5000000	21.732	28.102	28.935	33.215	36.203	40.104	42.760	45.797	45.220	54.701	97.476	109.000	219.692	221.724
6000000	24.370	30.919	32.443	37.246	40.594	44.970	47.949	51.352	53.726	61.336	115.305	122.218	246.340	248.620
7000000	26.526	37.579	40.360	44.431	47.132	50.203	53.529	59.626	62.612	76.303	152.043	154.602	306.450	309.285
8000000	29.744	42.136	45.256	49.821	52.846	56.293	60.022	66.858	69.933	85.557	155.120	170.484	343.621	346.800
7LM														
5000	0.419	0.734	1.213	1.742	2.024	2.478	2.774	3.7133	5.319	9.268	18.016	20.091	35.380	38.935
10000	0.439	1.061	1.339	2.002	2.268	3.150	3.632	4.386	6.319	10.772	21.443	23.518	40.116	43.313
50000	0.486	1.327	1.860	3.114	3.811	4.679	5.547	5.872	7.571	11.774	22.965	26.232	42.140	44.866
100000	0.724	1.474	2.303	3.327	3.978	4.844	6.400	6.715	8.742	12.652	25.770	31.846	51.951	54.833
150000	2.799	3.793	4.226	5.364	5.797	6.583	7.053	7.565	9.600	14.010	26.984	32.378	56.886	57.329
200000	3.913	4.441	4.996	5.758	6.323	7.039	7.533	7.965	10.092	14.837	28.106	33.809	59.789	60.254
300000	4.305	4.717	5.492	6.409	7.022	7.807	8.344	8.813	11.154	16.376	29.602	34.789	65.941	66.453
400000	4.699	5.411	5.953	6.917	7.594	8.455	9.047	9.537	12.057	17.669	31.142	35.291	71.142	71.689
500000	5.240	6.333	6.687	7.758	8.508	9.463	10.122	10.695	12.833	18.811	33.413	37.561	75.718	76.313
600000	5.610	6.681	7.199	8.341	9.138	10.161	10.862	11.500	13.203	19.354	35.527	38.640	77.892	78.512
800000	6.465	8.173	8.364	9.671	10.585	11.758	12.561	13.333	14.266	20.921	39.685	41.758	84.173	84.864
1000000	7.262	8.543	9.455	10.913	11.933	13.248	14.150	15.047	15.256	22.380	41.541	44.651	90.010	90.764
1500000	9.449	11.419	12.423	14.305	15.620	17.325	18.488	19.724	21.827	26.764	50.264	53.374	107.582	108.521
2000000	11.494	14.193	15.205	17.484	19.073	21.144	22.553	24.106	28.205	30.864	56.344	61.529	124.021	125.132
2500000	13.411	17.077	17.807	20.457	22.307	24.718	26.358	28.207	30.809	34.695	65.000	69.147	139.378	140.647
3000000	15.205	18.738	20.242	23.240	25.327	28.059	29.913	32.041	33.236	38.270	73.146	76.256	153.700	155.122
4000000	17.443	21.071	23.224	26.661	29.055	32.189	34.319	36.760	39.589	43.905	83.336	87.486	176.332	177.966
5000000	19.559	25.291	26.041	29.894	32.583	36.094	38.482	41.218	40.697	49.232	87.728	98.098	197.722	199.551
6000000	21.933	27.827	29.199	33.522	36.535	40.472	43.153	46.218	48.354	55.203	103.773	109.998	221.872	223.827
7000000	23.872	33.821	36.325	39.988	42.417	45.183	48.175	53.663	56.350	68.673	136.838	139.143	275.805	278.358
8000000	26.770	37.921	40.730	44.838	47.561	50.665	54.020	60.173	62.939	77.002	139.608	153.435	309.259	312.121

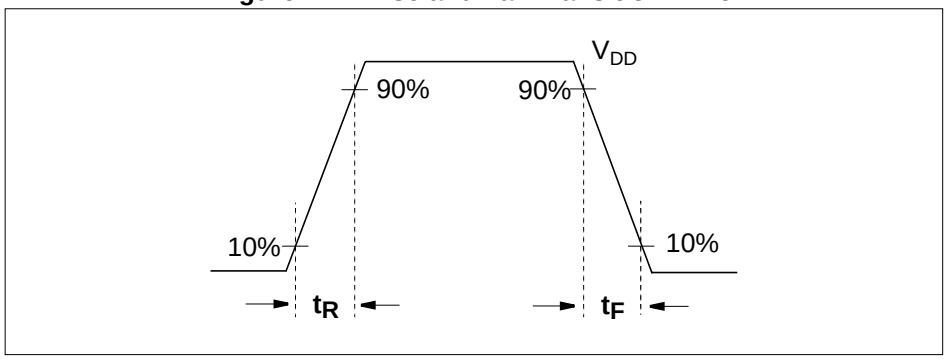
1.5.2 TIMING PARAMETERS

This section defines and discusses AC timing parameters.

1.5.2.1 Rise and Fall Transition Time

Rise time, t_R, and fall time, t_F, are defined as the time that a waveform takes to transition between 10% and 90% of the supply voltage (Figure 1-4).

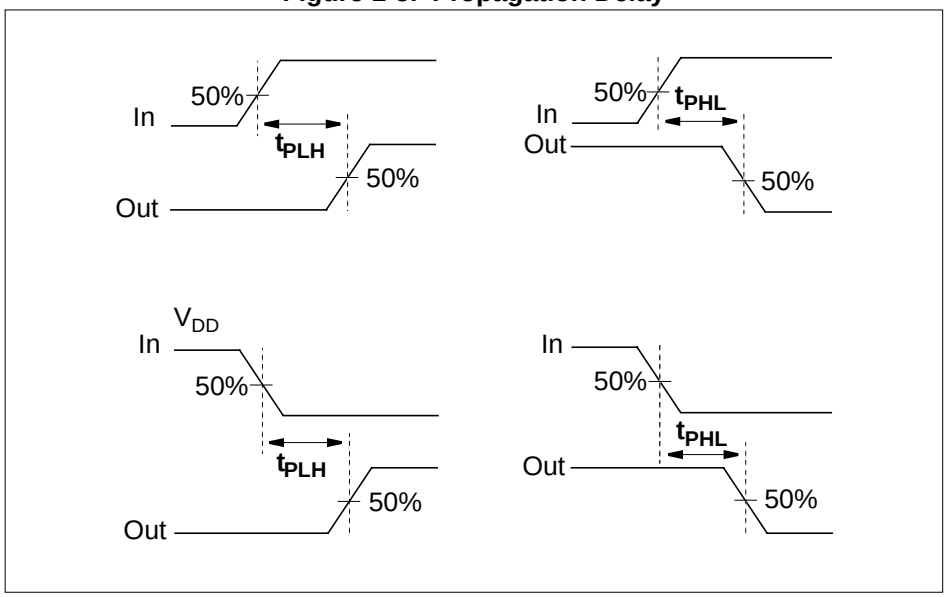
Figure 1-4. Rise and Fall Transition Time



1.5.2.2 Propagation Delay

Propagation delay, t_P, is defined as the time from when the input waveform reaches 50% of the supply voltage to the time that the output waveform reaches 50% of the supply voltage (Figure 1-5).

Figure 1-5. Propagation Delay

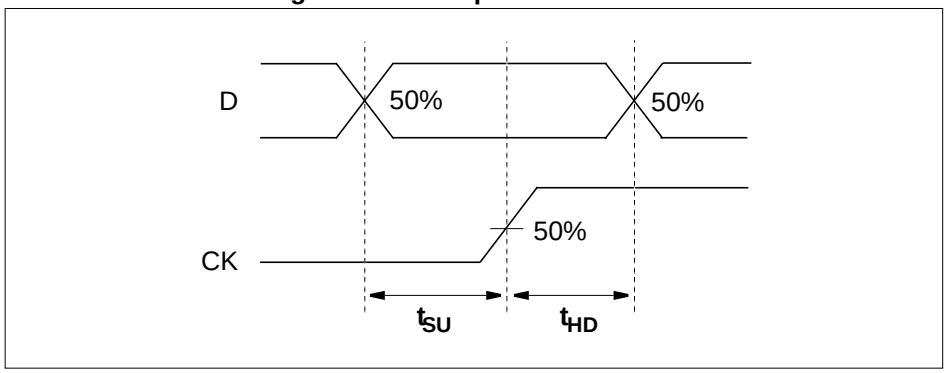


1.5.2.3 Setup and Hold Time

Setup time, t_{SU}, is defined as the minimum time that a data signal must be stable before an active clock transition. Any change to the data signal within this time results in a timing violation, and may result in invalid data being clocked into a circuit (Figure 1-6).

Hold time, t_{HD}, is defined as the minimum time that a data signal must remain valid after an active clock transition. Any change to the data signal within this time results in a timing violation, and may result in invalid data being clocked into a circuit (Figure 1-6).

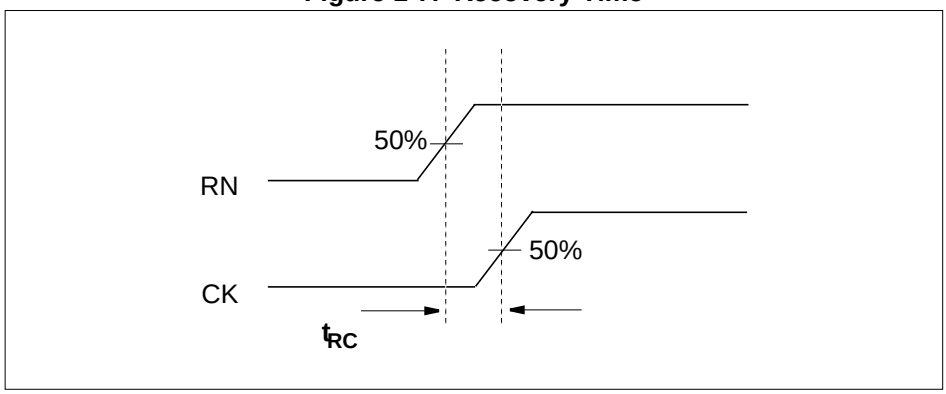
Figure 1-6. Setup and Hold Time



1.5.2.4 Recovery Time

Recovery time, t_{RC}, is defined as the time between the release of an asynchronous control signal from the active state of a circuit to the next active clock edge (Figure 1-7). If an active clock edge occurs too soon after the release of the control signal, a violation occurs that may result in erroneous value being clocked in to the circuit.

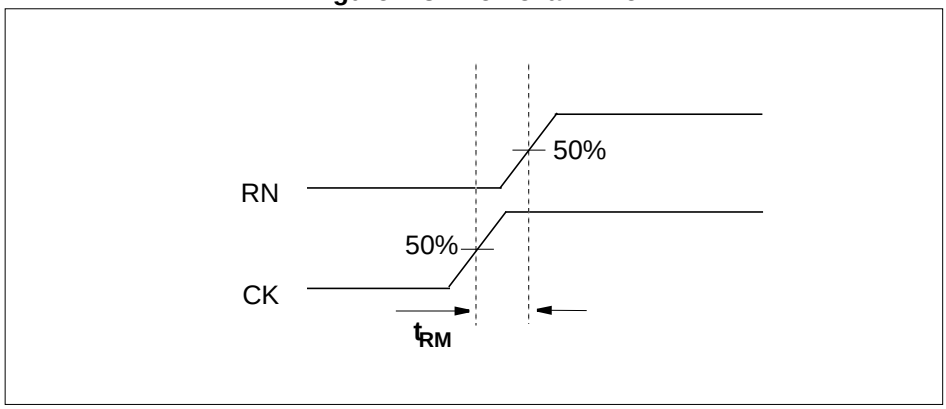
Figure 1-7. Recovery Time



1.5.2.5 Removal Time

Removal time, t_{RM}, is defined as the minimum time between the active clock edge and the release of an asynchronous control signal from the active state (Figure 1-8). If the control signal is released from the active state too soon after an active clock edge, a violation occurs that may result in erroneous value being clocked into the circuit.

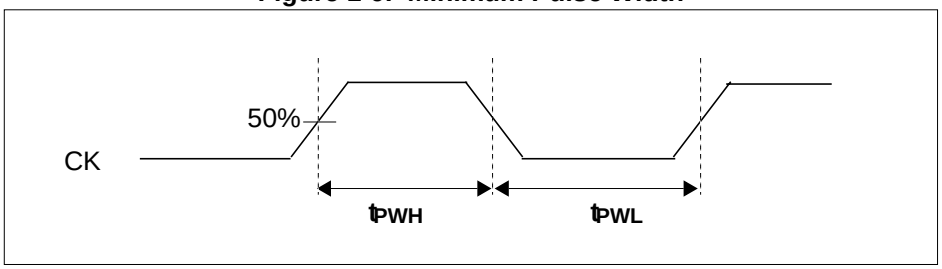
Figure 1-8. Removal Time



1.5.2.6 Minimum Pulse Width

Minimum pulse width, t_{PW}, is defined as the minimum time allowed for the high or low phase of a signal and is measured as the time between the rising and falling edges reaching 50% of the supply voltage (Figure 1-9). A short pulse width results in a timing violation and may result in the signal not being recognized by the circuitry.

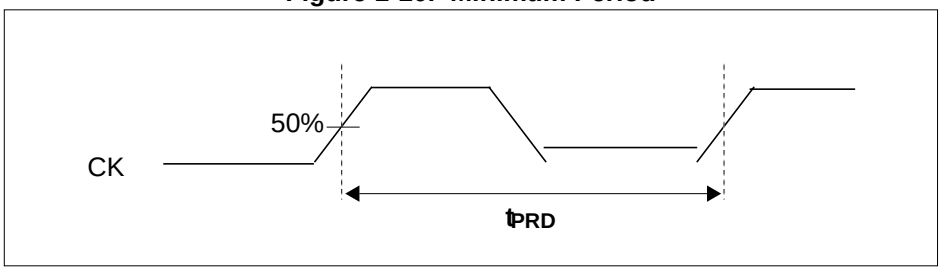
Figure 1-9. Minimum Pulse Width



1.5.2.7 Minimum Period

Minimum period, t_{PRD}, is defined as the minimum allowable time for one complete cycle of a signal (Figure 1-10). A short period results in a timing violation and may result in the signal not being recognized by the circuitry.

Figure 1-10. Minimum Period



1.5.3 BEST AND WORST CASE CONDITIONS

The timing value of best-case (worst-case) can be calculated by using the derating factor derived from the following equations:

$$T_{BC}\ (T_{WC}) = K_P \times K_T \times K_V \times T_{NOM}$$

where,

T_{BC} (T_{WC}) is a best-case (worst-case) timing.

K_P is the local process derating factor which has different value according to each cell,

K_T is the local temperature derating factor which has different value according to each cell,

K_V is the local voltage derating factor which has different value according to each cell,

T_{NOM} is the nominal timing characterized under typical-process, 25°C and 1.2V power supply.

The best-case (worst-case) timing values may be determined by picking the proper derating values from Table 1-3, Table 1-4 and Table 1-5. Derating factors for conditions between those shown in the tables may be determined by a linear interpolation.

1.5.4 DERATING FACTORS OF STDH150

Cell timing is primarily determined by cell drive capability and loading determined by cell input capacitance and wiring. The following critical variables also affect the timing in a system environment of design:

- Process variation (P)
- Supply voltage (V)
- Junction Temperature (T)

Process variation occurs due to the manufacturing environments and the variation may change the physical characteristics. Its variation affects the electrical characteristics of devices, increasing or decreasing performance and power. On the other hand, to design chips which operate in a wide range of voltage and temperature environments, you have to consider typical-case, worst-case and best-case conditions to compensate for all variations. To yield much more timing accuracy, the cell-specific local derating factor is used in STDH150 standard cells.

For an example, the process, temperature and voltage derating factors for IV cell are as follows in Table 1-3, Table 1-4 and Table 1-5 respectively.

Table 1-3. STDH150 Cell Process Derating Factor (K_P)

Process Factor (K_P)	Slow	Typ	Fast
	1.235	1.000	0.858

Table 1-4. STDH150 Cell Temperature Derating Factor (K_T)

Temp. (^oC)	125	85	70	25	0	−40	−55
K_T	1.120	1.073	1.055	1.000	0.977	0.935	0.917

Table 1-5. STDH150 Cell Voltage Derating Factor (K_V)

Voltage (V)	1.05	1.10	1.20	1.30	1.35
K_V	1.190	1.117	1.000	0.930	0.900

Notice that K_P, K_T and K_V shown as Table 1-3, Table 1-4 and Table 1-5 are only available in standard cells.

1.5.5 DELAY MODEL

The STDH150 cell timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout and distributed interconnection wire resistances and capacitances.
- Interconnection wire delay.
- Timing requirement parameters including set up time, hold time, recovery time, skew time, and minimum pulse width.
- Derating factors for junction temperature, power supply voltage, and process variation.

To accomplish accurate timing model, a two dimensional table look-up delay model has been developed. The index variables of this table are input waveform slope and output load capacitance (Figure 1-11). Samsung's SoC design methodology supports an n-dimensional table model, even though a two dimensional model is used.

Figure 1-11. 2-Dimensional Table Delay Model

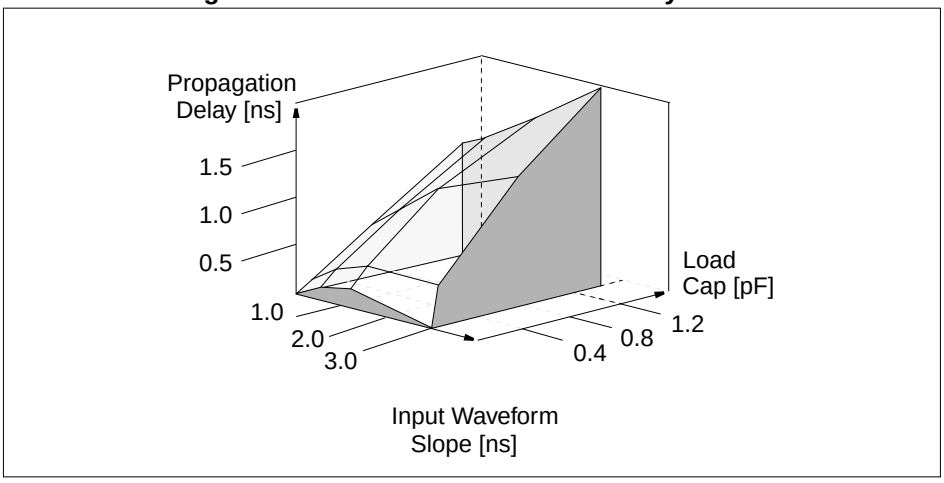


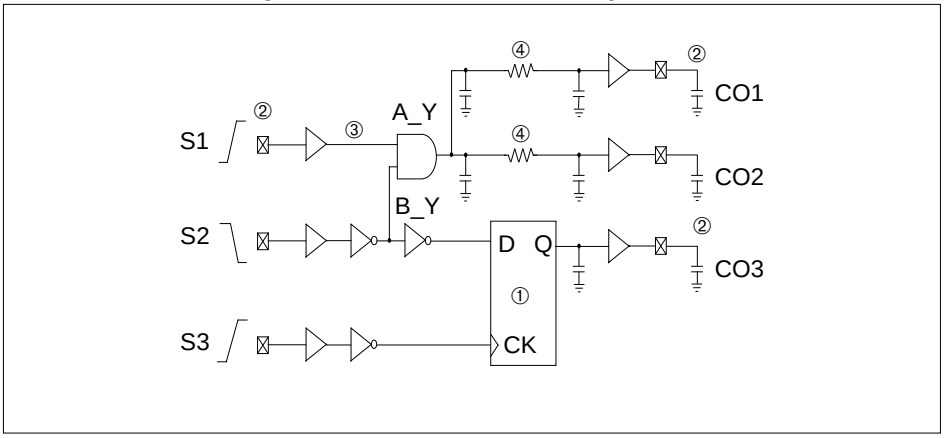
Table 1-6 shows the propagation delay data for a 2-input NAND cell. The data in this table are the high-to-low transition delay times from one of the two input pins to the output pin. The number of points and values of the index variables can differ for each cell.

Table 1-6. Table Delay Model Example

\ CAP SLOPE	0.004	0.018	0.079	0.202	0.386	0.632
0.008	0.01622	0.03194	0.09929	0.23454	0.43690	0.70747
0.083	0.02536	0.04595	0.11343	0.24855	0.45092	0.72148
0.319	0.03125	0.06431	0.15903	0.29564	0.49710	0.76723
0.791	0.02626	0.07294	0.20511	0.38650	0.59322	0.86127
1.500	0.01000	0.06821	0.23614	0.46629	0.72719	1.00780

Notice that a 5-by-6 table is used. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components, such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a way commonly accepted in the industry. Figure 1-12 summarizes the features of the STDH150 library delay model.

Figure 1-12. Features of Delay Model



① Two dimensional table delay model for output loading and input waveform slope is used. The rise and fall times and delay times of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are defined.

④ The effect of distributed interconnection wire resistances and capactitances on cell delay is analysed using lumped capacitances.

1.6 Design for Test (DFT) Methodology

Samsung's libraries are designed with DFT in mind. Samsung's DFT methodology includes the ability to include full or partial scan path testing, boundary-scan JTAG for board level testing, Memory BIST, and analog testing. A brief description of the features of Samsung's scan, BIST, and JTAG as well as a more detailed discussion of boundary scan architecture follows.

1.6.1 SCAN DESIGN

- Multiplexed scan flip-flops that minimize area and delay overhead needed to implement scan design.
- Automated design rule checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

1.6.2 BIST (BUILT-IN SELF-TEST)

- Efficient test solution for compiled memory macrocells
- At speed and parallel testing of multiple memories
- Combination with internal scan design and core testing

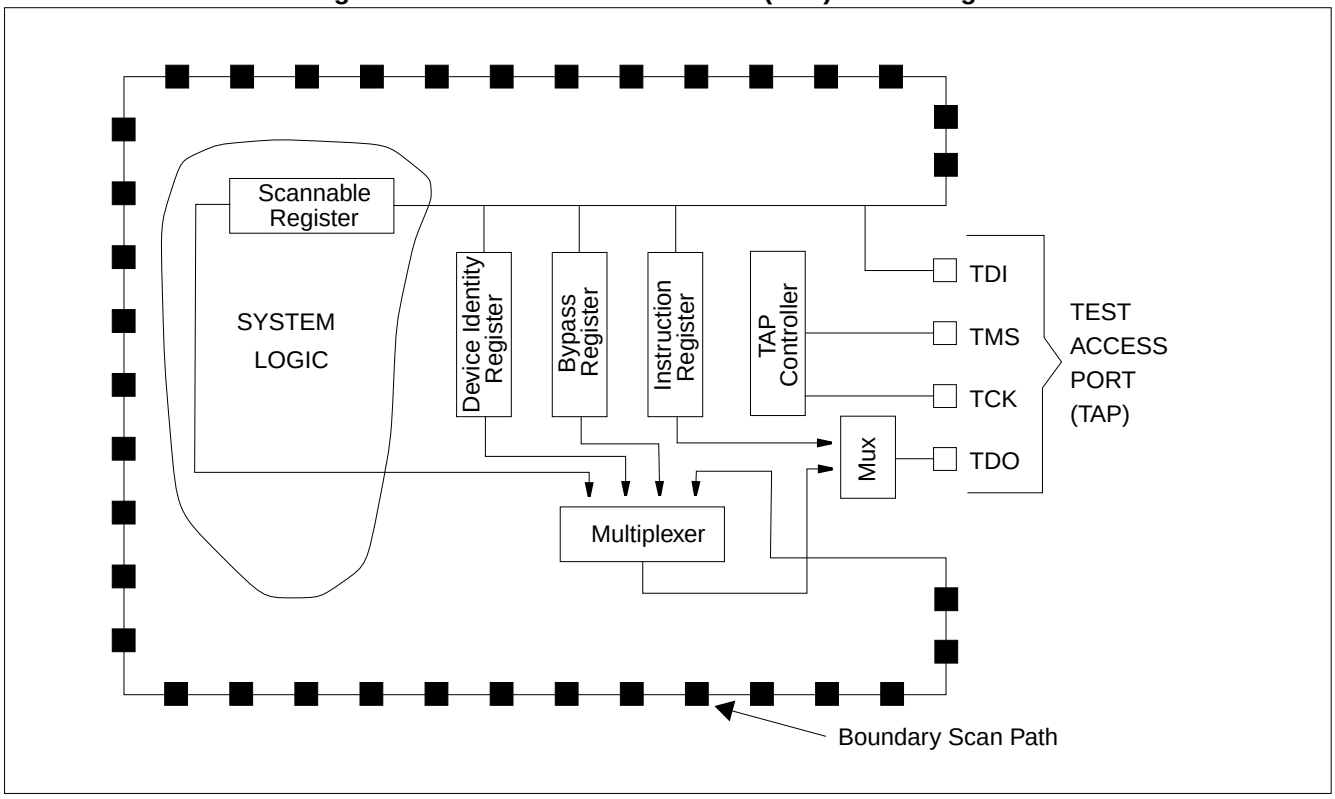
1.6.3 BOUNDARY SCAN

- IEEE Std 1149.1
- JTAG boundary scan registers implemented with primitive cells
- Boundary Scan Description Language (BSDL) for board testing
- May be combed with internal scan design and core testing

JTAG Boundary Scan Architecture

Boundary scan architecture contains a TAP (Test Access Port), a TAP controller, an instruction register, and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output. The common serial data input and output are connected to the TAP, TDI and TDO signals. The TAP controller selects the alternative instruction and test data register paths between TDI and TDO. A schematic view of the top level design of the JTAG test logic architecture is shown in the Figure 1-13

Figure 1-13. JTAG Test Access Port (TAP) Block Diagram



Functional Block Descriptions

TAP (Test Access Port)

The TAP is a general-purpose port that provides access to many test support functions built into a component including the test logic. It includes three inputs (TCK -Test Clock Signal; TMS -Test Mode Signal; and TDI -Test Data Input) and one output (TDO -Test Data Output) required by the test logic. An optional fourth input (TRSTN -Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at the TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO changes on the falling edge of TCK.

TAP Controller

The TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuit as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include tests to be performed or the test data register addresses to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Test data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass and boundary scan registers are mandatory; the rest are optional.

Test Data Registers Description

Bypass register: The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers are selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.

Boundary scan register: The boundary scan register detects typical production defects in board interconnects, such as opens, and shorts. It also allows access to component inputs and outputs when testing their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose.

Design-specific test data register: These optional registers may be provided to allow access to design-specific test support features in the integrated circuit, such as self-test and scan test.

Device identification register: This is an optional test data register that allows the manufacturer part number and revision to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier 1st field	The first four bits beginning from MSB	
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit — tied in High

The ASIC designer is free to fill in the version and part number in any manner as long as all twenty bits are used.

Samsung's JEDEC code: 78 decimal = 1001110

Continuation field (4 bits) = 0000

Contents of device identification register:

XXXX XXXXXXXXXXXXXXX 0000 1001110 1
Users can define these two fields.

1.7 Chip Power Estimation

1.7.1 CHIP POWER

One of the important considerations to deign chip is chip power. High frequencies and multi-million logic devices impose a strict limit on power consumption. Power calculations determine power-supply sizing, current requirements, package types, and criteria for library selection. In the design flow, the early chip power estimation is needed to estimate in the design start step. The purposes of the early chip power estimation are to choose package types, to estimate number of power pad and ground and to select battery requirements. Therefore, quick and reliable chip power estimation is more important. On the other hand, the chip power calculation is needed to calculate before the 1st and 2nd sign-off. The purposes of the chip power calculation are to verify and to confirm the package type, number of power pad and ground pad. In case of chip power calculation, reliable chip power by the power calculation tool, CubicPower (Samsung's internal power calculation tool) is more important.

In general, two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. But, when the devices are operating, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

1.7.2 STATIC POWER CONSUMPTION

The total static power consumption in CMOS circuit consists of the leakage power and DC power of the input and output cells. The leakage power is generally negligible. But the leakage power should be considered since the leakage current is increased by the shorten gate length and increasing the total gate counts.

The following equation is the leakage power in the typical condition of STDH150.

Pdc_leakage (mW) = 0.001 × 16910.4 × Total_Gate_Counts/1,000,000

In case of worst process condition and worst temperature (T_j = 125), the leakage current can be one hundred times than the value of the typical condition.

The DC power is caused by the current flows through I/O buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor in the input buffers is typically on the order of tens of micro amperes, which is also negligible. Therefore, only the DC current that the output buffers source or sink needs to be counted to estimate total static power consumption. The DC power consumption of output and bi-directional buffers is determined by the following equations;

$$P_{DC_OUTPUT}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) / T$$

$$P_{DC_BI}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) \times S_{out} / T$$

where,

n = Number of output and bi-directional buffers

T = Total operation time in output mode

t_H = The sum of logic high state time

t_L = The sum of logic low state time

$t_L + t_H = T$ (assuming that output and bi-directional buffers are not tri-state)

S_{out} is the output mode ratio of bi-directional buffers (typically 0.5)

1.7.3 DYNAMIC POWER CONSUMPTION

When a CMOS logic gate changes state, it draws switching current as a result of charging or discharging a load capacitance, C_L. The power associated with the switching current for a node capacitance, C_L, is

$$C_L \times V_{DD}^2$$

where V_{DD} is the power supply voltage.

In addition to the power consumption by the charging of the load capacitance, COMS circuits consume the power due to current flowing from the power supply to ground through the n- and p-channel transistors during switching.

The dynamic power estimation for an entire chip is difficult since it depends on the switching activity, frequencies, and power management of the circuit such as clock gating. The switching activity is about 10% on the average. That value is recommended to estimate the total dynamic power consumption.

1.7.4 EARLY CHIP POWER ESTIMATION

Early chip power estimation is needed to estimate chip power in the design start step. The purposes of the chip power estimation are to estimate package types, to estimate number of power pad and ground and to select battery requirements. To estimate the quick and reliable chip power value, the following estimation items are required.

- Total gate counts of logic
- Switching activity of the logic and I/O
- Portion of Flip Flop in total gate counts
- Portion of Flip Flop applied simultaneous power management
- Number of input, output and bi-directional cells
- Frequencies of each block

The early chip power estimation is estimated by the four components: internal logic and ip power (Pac_internal), input, output and bi-directional buffer power (Pac_io), leakage power (Pdc_leakage) and DC power (Pdc_dc).

Ptotal = Pac_internal + Pac_io + Pdc_leakage + Pdc_dc (Pdc_output + Pdc_bi)

The leakage power and DC power were mentioned in the previous section. Please refer to the section 1.7.2.

The internal logic and ip power are described by the following equation:

$$Pac_internal(mW) = 0.001 \times \left(\sum_{i=1}^{N_block} (((0.017290 \times S_i) + (0.005471 \times (1 - S_i) \times R_FF_i \times PM_i)) \times G_i \times F_i) + \sum_{j=1}^{N_macro} (P_j \times F_j) \right)$$

Where,

S_i is the switching activity (typically 0.1) for the i-th logic block

G_i is the logic gate count for the i-th logic block

F_i is the frequency for the i-th logic block

R_FF_i is the portion (typically 0.3 ~ 0.4) of flip flop for the i-th logic block

PM_i is the portion of flip flops applied simultaneous power management of flip flop for the i-th logic block. If the power management method like clock gating is not applied in the design, the PM is 1.)

N_block is the number of logic block

P_j is the characterized power for the j-th IP(μW/MHz)

F_j is the frequency for the j-th IP

N_macro is the number of macro cells used.

For information on estimating active power consumption compliable memories, and other IPs, contact a Samsung ASIC representative.

Each term mentioned above is characterized by the following equations:

$$P_{AC_INPUT}\,[mW] = 1.2\times \sum_{i}^{N_1.2V_input}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_input}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)$$
$$+3.3\times \sum_{k}^{N_3.3V_input}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+1.44\times \sum_{l}^{N_total_input}(0.001\times S_l\times F_l\times C_{l_inload})$$

$$P_{AC_OUTPUT}\,[mW] = 1.2\times \sum_{i}^{N_1.2V_output}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_output}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_output}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+1.44\times \sum_{i}^{N_1.2V_output}(0.001\times S_i\times F_i\times C_{i_outload})+$$
$$6.25\times \sum_{j}^{N_2.5V_output}(0.001\times S_j\times F_j\times C_{j_outload})+10.89\times \sum_{k}^{N_3.3V_output}(0.001\times S_k\times F_k\times C_{k_outload})$$

$$P_{AC_BI}\,[mW] = P_{AC_BI_INPUT}\times(1-S_{out})+P_{AC_BI_OUTPUT}\times S_{out}$$

$$P_{AC_BI_INPUT}\,[mW] = 1.2\times \sum_{i}^{N_1.2V_bi}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_bi}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_bi}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+1.44\times \sum_{l}^{N_total_bi}(0.001\times S_l\times F_l\times C_{l_inload})$$

$$P_{AC_BI_OUTPUT}\,[mW] = 1.2\times \sum_{i}^{N_1.2V_bi}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_bi}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_bi}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+1.44\times \sum_{i}^{N_1.2V_bi}(0.001\times S_i\times F_i\times C_{i_outload})+$$
$$6.25\times \sum_{j}^{N_2.5V_bi}(0.001\times S_j\times F_j\times C_{j_outload})+10.89\times \sum_{k}^{N_3.3V_bi}(0.001\times S_k\times F_k\times C_{k_outload})$$

where,

N_1.2V_input is the number of 1.2V interface input buffers used,
N_2.5V_input is the number of 2.5V interface input buffers used,
N_3.3V_input is the number of 3.3V interface input buffers used,
N_total_input = N_1.2V_input + N_2.5V_input + N_3.3V_input,
N_1.2V_output is the number of 1.2V interface output buffers used,
N_2.5V_output is the number of 2.5V interface output buffers used,
N_3.3V_output is the number of 3.3V interface output buffers used,
N_1.2V_bi is the number of 1.2V interface bi-directional buffers used,
N_2.5V_bi is the number of 2.5V interface bi-directional buffers used,
N_3.3V_bi is the number of 3.3V interface bi-directional buffers used,
N_total_bi = N_1.2V_bi + N_2.5V_bi + N_3.3V_bi,
N_macro is the number of macro cells used,
F is the operating frequency of the input, output or bi-directional buffer
S is the estimated switching activity (typically 0.5 for input, output or bi-directional buffer)
leq_p is average current of input/output buffers and bi-direction pre-drives at 100MHz I/O frequency(mA). (In case of bi-directional buffers, leq_p is summation of input and output buffer's leq_p.)

1.7.5 CHIP POWER CALCULATION

If the early chip power wasn't confirmed by the PowerView, the chip power calculation is needed to calculate before the 1st and 2nd sign-off. The purposes of the chip power calculation are to verify and to confirm the package type, number of power pad and ground pad. The CubicPower is Samsung's in-house power calculation tool which uses switching activity information of net from gate level logic simulation. CubicPower uses gate level cell library characterized by spice. Therefore CubicPower can calculate more accurate chip power than early chip power estimator, PowerView. Power calculation results from CubicPower depend on the test vector assigned during gate level logic simulation.

1.8 Crystal Oscillator Consideration

1.8.1 OVERVIEW

The STDH150 library contains a cell commonly referred to as an *on-chip oscillator*. The on-chip oscillator itself is not really an oscillator, but is an amplifier suitable for being used as the feedback amplifier in an oscillator circuit. With proper selection of off-chip components (crystal or ceramic resonator, resistors and capacitors) this oscillator circuit performs better than other types of clock oscillators.

It is very important to select suitable off-chip components for the on-chip oscillator circuitry. It should be noted, however, that Samsung cannot assume responsibility for writing specifications for the off-chip components or for the performance of the finished oscillator design in production since the optimization of the crystal oscillator circuit will be specific to a given application. Samsung does, however, spec and guarantee the performance of the on-chip oscillator cell.

1.8.2 OSCILLATOR DESIGN CONSIDERATIONS

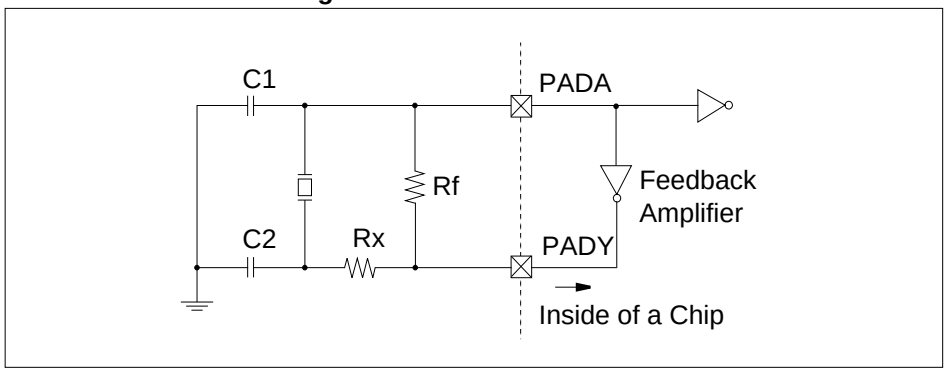
SoC designers have a number of options for clocking the system. A primary decision is whether to use an on-chip oscillator or an external oscillator. If the choice is to use an on-chip oscillator, the designer must then choose the type of oscillator and off-chip component values. These decisions will be based on both economic and technical requirements.The following section discusses some of the factors to be considered.

1.8.2.1 On-Chip Oscillator

In most cases, the on-chip oscillator with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components commonly used for the oscillator circuit are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistors, Rf and Rx, as shown in the Figure below.

Figure 1-14.CMOS Oscillator



1.8.2.2 Crystal Specifications

Specifications for an appropriate crystal are not very critical. Any fundamental mode crystal of medium or better quality can be used. Crystal resistance affects start-up time and steady state amplitude but can be compensated by the choice of C1 and C2, however, the lower the crystal resistance, the better. A discussion of external R and C components follows below.

1.8.2.3 Oscillation Frequency

The oscillation frequency is mainly determined by the crystal. The on-chip oscillator has little effect on the frequency.

The influence of the on-chip oscillator on frequency results from its input and output (pin-to-ground) capacitances which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance which parallels the crystal. The input and pin-to-pin capacitances are about 7pF each.

1.8.2.4 C1 and C2 Selection

Optimal values for C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and on application-specific requirements for start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability because of various reset and initialization requirements.

Accuracy of the oscillator frequency is less commonly critical, as when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 15pF (but they don't have to be either).

Increasing the value of these capacitors above 40pF or 50pF improves frequency stability, but also increases the start-up time. If the capacitors are too large (several hundred pF), the oscillator won't start up at all.

1.8.2.5 Rf and Rx Selection

A large Rf (1MΩ) holds the on-chip oscillator (a CMOS inverter) in it linear region allowing it to oscillate. The inverter has a fairly low output resistance which de-stabilizes the oscillator circuit. Rx of several kΩ is added to the feedback network, as shown in Figure 1-14, to stabilize the oscillator circuit.

At higher oscillator frequencies, a 20pF or 30pF capacitor is sometimes used in place of Rx to compensate for internal propagation delay.

1.8.3 PCB CONSIDERATIONS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins. If possible, use dedicated V_{DD} and V_{SS} pins for the on-chip oscillator.

In addition, surrounding oscillator components with "quiet" traces (V_{DD} and V_{SS}) will alleviate capacitive coupling to signals having fast edges. To minimize inductive coupling, the PCB layout should minimize lead, wire, and trace lengths for oscillator components.

Paths that need to be checked are:
- PADA through the resonator to PADY;
- PADA through C1 to the V_{SS} pin;
- PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 connect to the V_{SS} pin through long traces on the board.

1.8.4 TROUBLESHOOTING OSCILLATOR PROBLEMS

The cause of an oscillator problem may be difficult to find once detected. Below are some suggested first things to investigate if an oscillator problem is detected.

There may be significant differences in stray capacitances between the test fixture and the actual application, particularly if the actual application is on a multi-layer board. This may result in an oscillator problem occurring in the test fixture that will not occur on the board, or a problem occurring on the board that cannot be duplicated on the test fixture.

Noise glitches not present in the test fixture but present on the application board may be another cause for an oscillator problem. Capacitive coupling between the oscillator circuitry and other signal should be investigated. Inductive coupling is also possible if there is a lead, trace, or wire with a large current nearby.

Finally, it should not be overlooked that software problems can mimic the symptoms of a slow-starting oscillator or incorrect frequency. Software should also be invigilated.

Electrical Characteristics

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Contents

DC Electrical Characteristics 2-1

DC ELECTRICAL CHARACTERISTICS

The following tables define the DC electrical characteristics for the standard LVCMOS I/O buffers described in Chapter 4: “Input/Output Cells.” The DC electrical characteristics for oscillator and standard bus interface I/O buffers such as PCI follow the desciptions of those buffer cells in Chapter 4.

V_{DD} = 2.5V± 0.2V, Ta = –40 to 85°C, V_{EXT} = 5V± 0.25 (In Case of 5V Tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		1.7			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.7	
VT	Switching threshold			$0.5V_{DD}$		V
VT^+	Schmitt trigger, positive-going threshold	CMOS			1.7	V
VT –	Schmitt trigger, negative-going threshold	CMOS	0.7			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	25	50	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–50	–25	–10	
V_{OH}	High level output voltage					V
	Type B1 to B12	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	1.9			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
V_{OL}	Low level output voltage					V
	Type B1 to B12	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10		10	µA
I_{DD}	Quiescent supply current				100	µA
C_{IN}	Input capacitance	Any input and Bi-directional buffers			5	pF
C_{OUT}	Output capacitance	Any output buffer			5	pF

V_{DD} = 3.3V± 0.3V, Ta = –40 to 85°C, V_{EXT} = 5V± 0.25 (In Case of 5V Tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold			$0.5V_{DD}$		V
VT^+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT –	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	33	65	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–65	–33	–10	
V_{OH}	High level output voltage					V
	Type B1 to B12	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	2.4			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
V_{OL}	Low level output voltage					V
	Type B1 to B12	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10		10	µA
I_{DD}	Quiescent supply current				100	µA
C_{IN}	Input capacitance	Any input and Bi-directional buffers			5	pF
C_{OUT}	Output capacitance	Any output buffer			5	pF

Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V_{DD}	DC Supply Voltage	1.2V V_{DD}	1.6	V
		2.5V V_{DD}	3.6	
		3.3V V_{DD}	4.8	
V_{IN}	DC Input Voltage	2.5V input buffer	3.6	
		3.3V input buffer	4.8	
		2.5 interface / 3.3V tolerant input buffer	4.8	
		3.3V interface / 5V tolerant input buffer	6.5	
V_{OUT}	DC Output Voltage	2.5V output buffer	3.6	
		3.3V output buffer	4.8	
		2.5V interface / 3.3V tolerant output buffer	4.8	
		3.3V interface / 5V tolerant output buffer	6.5	
I_{Latch}	Latch Up Current	± 200		mA
T_{STG}	Storage Temperature	–65 to 150		°C

Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
			Min	Max	
V_{DD}	DC Supply Voltage for Internal (= V_{DDIN})	1.2V V_{DD}	1.1	1.3	V
	DC Supply Voltage for I/O Block (= V_{DDIO})	2.5V V_{DD}	2.3	2.7	
		3.3V V_{DD}	3.0	3.6	
	DC Supply Voltage for Analog Core (= V_{DDA})	2.5V V_{DD}	2.5 – 5%	2.5 + 5%	
		3.3V V_{DD}	3.3 – 5%	3.3 + 5%	
V_{IN}	DC Input Voltage	2.5V input buffer	–0.3	V_{DDIO}+0.2	
		3.3V input buffer	–0.3	V_{DDIO}+0.3	
		2.5V interface / 3.3V tolerant input buffer	–0.3	3.6	
		3.3V interface / 5V tolerant input buffer	–0.3	5.5	
V_{OUT}	DC Output Voltage	2.5V output buffer	–0.3	V_{DDIO}+0.2	
		3.3V output buffer	–0.3	V_{DDIO}+0.3	
		2.5V interface / 3.3V tolerant output buffer	–0.3	3.6	
		3.3V interface / 5V tolerant output buffer	–0.3	5.5	
T_A	Commercial Temperature Range			0 to 70	°C
	Industrial Temperature Range			–40 to 85	

Internal Macrocells

3

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OVERVIEW

This chapter contains data sheets for standard logic macrocells; combinational logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers. The electrical characteristics of each cell follow each cell's description. A summary table in the following pages list the entire STDH150 standard logic macrocell library by the cell type along with the cell description page number. Moreover, each section begins with a table containing a brief functional description of each cell in that section.

SUMMARY TABLES

Logic Cells

Cell Type	Cell Name	Page
AND Cell	ad2/ad2d2/ad2d4/ad2d8	3-15
	ad2b/ad2bd2/ad2bd4/ad2bd8	3-17
	ad3/ad3d2/ad3d4	3-19
	ad4/ad4d2/ad4d4	3-21
	ad5/ad5d2/ad5d4	3-23
NAND Cell	nd2/nd2d2/nd2d4/nd2d8	3-26
	nd2b/nd2bd2/nd2bd4/nd2bd8	3-28
	nd3/nd3d2/nd3d4/nd3d8	3-30
	nd3b/nd3bd2/nd3bd4/nd3bd8	3-33
	nd4/nd4d2/nd4d4	3-36
	nd5/nd5d2/nd5d4	3-38
	nd6/nd6d2/nd6d4	3-41
	nd8/nd8d2/nd8d4	3-45
NOR Cell	nr2/nr2a/nr2d2/nr2d4/nr2d8	3-49
	nr2b/nr2bd2/nr2bd4/nr2bd8	3-51
	nr3/nr3a/nr3d2/nr3d4	3-53
	nr4/nr4d2/nr4d4	3-56
	nr5/nr5d2/nr5d4	3-58
	nr6/nr6d2/nr6d4	3-62
	nr8/nr8d2/nr8d4	3-66
OR Cell	or2/or2d2/or2d4/or2d8	3-70
	or2b/or2bd2/or2bd4/or2bd8	3-72
	or3/or3d3/or3d4	3-74
	or4/or4d2/or4d4	3-76
	or5/or5d2/or5d4	3-78
Exclusive-NOR Cell	xn2/xn2d2/xn2d4/xn2d8	3-81
	xn3/xn3d2/xn3d4	3-83
Exclusive-OR Cell	xo2/xo2d2/xo2d4/xo2d8	3-85
	xo3/xo3d2/xo3d4	3-87

Cell Type	Cell Name	Page
Combinational Cell of AND and NOR	ao21/ao21d2/ao21d4	3-89
	ao211/ao211d2/ao211d4	3-91
	ao2111/ao2111d2	3-93
	ao22/ao22d2/ao22d4	3-95
	ao22a/ao22d2a	3-97
	ao221/ao221d2/ao221d4	3-99
	ao222/ao222d2/ao222d4	3-102
	ao222a/ao222d2a	3-106
	ao2222/ao2222d2/ao2222d4	3-107
	ao31/ao31d2/ao31d4	3-111
	ao311/ao311d2	3-113
	ao3111/ao3111d2	3-115
	ao32/ao32d2	3-117
	ao321/ao321d2	3-119
	ao322/ao322d2	3-122
	ao33/ao33d2	3-125
	ao331/ao331d2	3-128
	ao332/ao332d2	3-131
Combinational Cell of OR and NAND	oa21/oa21d2/oa21d4	3-134
	oa211/oa211d2/oa211d4	3-136
	oa2111/oa2111d2	3-138
	oa22/oa22d2/oa22d4	3-140
	oa22a/oa22d2a/oa22d4a	3-142
	oa221/oa221d2/oa221d4	3-144
	oa222/oa222d2/oa222d4	3-147
	oa2222/oa2222d2/oa2222d4	3-141
	oa31/oa31d2/oa31d4	3-151
	oa311/oa311d2	3-155
	oa3111/oa3111d2	3-157
	oa32/oa32d2	3-159
	oa321/oa321d2	3-162
	oa322/oa322d2	3-164
	oa33/oa33d2	3-170

Cell Type	Cell Name	Page
Complex Cells	scg1/scg1d2	3-173
	scg2/scg2d2/scg2d4	3-176
	scg3/scg3d2/scg3d4	3-178
	scg4/scg4d2/scg4d4	3-181
	scg5/scg5d2/scg5d4	3-185
	scg6/scg6d2/scg6d4	3-189
	scg7/scg7d2/scg7d4	3-191
	scg8/scg8d2	3-194
	scg9/scg9d2/scg9d4	3-196
	scg10/scg10d2/scg10d4	3-198
	scg11/scg11d2	3-200
	scg12/scg12d2/scg12d4	3-202
	scg13/scg13d2/scg13d4	3-204
	scg14/scg14d2/scg14d4	3-206
	scg15/scg15d2/scg15d4	3-208
	scg16/scg16d2/scg16d4	3-210
	scg17/scg17d2/scg17d4	3-212
	scg18/scg18d2/scg18d4	3-214
	scg19/scg19d2	3-217
	scg20/scg20d2/scg20d4	3-219
	scg21/scg21d2	3-221
	scg22/scg22d2/scg22d4	3-223
Delay Cells	dl1d2	3-225
	dl2d2	3-226
	dl5d2	3-227
	dl10d2	3-228
Inverter	iv/ivd2/ivd3/ivd4/ivd6/ivd8/ivd16/ivd24	3-229
Inverting Tri-State Buffer	ivt/ivtd2/ivtd4/ivtd8/ivtd16	3-232
Non-Inverting Buffer	nid/nid2/nid3/nid4/nid6/nid8/nid16/nid24	3-234
Non-Inverting Tri-State Buffer	nit/nitd2/nitd4/nitd8/nitd16	3-237

Flip-Flops

Cell Type	Cell Name	Page
D Flip-Flop	fd1/fd1d2/fd1d4	3-242
	fd1s/fd1sd2/fd1sd4	3-244
	fd1sq/fd1sqd2/sd1sqd4	3-246
	fd1q/fd1qd2/fd1qd4	3-248
D Flip-Flop with Reset	fd2/fd2d2/fd2d4	3-250
	fd2s/fd2sd2/fd2sd4	3-253
	fd2sq/fd2sqd2/fd2sqd4	3-256
	fd2q/fd2qd2/fd2qd4	3-259
D Flip-Flop with Set	fd3/fd3d2	3-261
	fd3s/fd3sd2	3-263
	fd3sq/fd3sqd2	3-265
	fd3q/fd3qd2	3-267
D Flip-Flop with Reset, Set	fd4/fd4d2	3-269
	fd4s/fd4sd2	3-272
	fd4sq/fd4sqd2	3-276
	fd4q/fd4qd2	3-279
D Flip-Flop with Negative Edge Trigger	fd5/fd5d2	3-281
	fd5s/fd5sd2	3-283
	fd6/fd6d2	3-285
	fd6s/fd6sd2	3-287
	fd7/fd7d2	3-289
	fd7s/fd7sd2	3-291
	fd8/fd8d2	3-293
	fd8s/fd8sd2	3-296
D Flip-Flop with Synchronous Clear	fds2/fds2d2	3-300
	fds2s/fds2sd2	3-302
	fds3/fds3d2	3-304
	fds3s/fds3sd2	3-306
JK Flip-Flop	fj2/fj2d2	3-308
	fj2s/fj2sd2	3-310
	fj4/fj4d2	3-312
	fj4s/fj4sd2	3-315
Toggle Flip-Flop	ft2/ft2d2	3-318

Latches

Cell Type	Cell Name	Page
D Latch with Active High	ld1/ld1d2/ld1d4	3-321
	ld1q/ld1qd2/ld1qd4	3-324
	ld2/ld2d2	3-326
	ld2q/ld2qd2	3-329
	ld3/ld3d2	3-331
	ld4/ld4d2	3-334
D Latch with Active Low	ld5/ld5d2	3-337
	ld5q/ld5qd2	3-339
	ld6/ld6d2	3-341
	ld6q/ld6qd2	3-344

Bus Holder

Cell Type	Cell Name	Page
Bus Holder	busholder	3-346

Adders

Cell Type	Cell Name	Page
Full Adder	fa/fad2/fad4	3-348
Half Adder	ha/had2/had4	3-351

Multiplexers

Cell Type	Cell Name	Page
2 > 1 Non-Inverting Mux	mx2/mx2d2/mx2d4/mx2d8	3-355
2 > 1 Inverting Mux	mx2i/mx2id2/mx2id4	3-358
	mx2ia/mx2id2a/mx2id4a	3-360
4 > 1 Non-Inverting Mux	mx4/mx4d2/mx4d4	3-363

Integrated Clock-Gating Cells

Cell Type	Cell Name	Page
Integrated Clock-Gating Cells	cgln/cglnd2/cglnd4	3-368
	cglp/cglpd2/cglpd4	3-371

Cell Names & Function Descriptions

Cell Name	Function Description
ad2	2-Input AND with 1X Drive
ad2d2	2-Input AND with 2X Drive
ad2d4	2-Input AND with 4X Drive
ad2d8	2-Input AND with 8X Drive
ad2b	2-Input AND with one Inverted Input, 1X Drive
ad2bd2	2-Input AND with one Inverted Input, 2X Drive
ad2bd4	2-Input AND with one Inverted Input, 4X Drive
ad2bd8	2-Input AND with one Inverted Input, 8X Drive
ad3	3-Input AND with 1X Drive
ad3d2	3-Input AND with 2X Drive
ad3d4	3-Input AND with 4X Drive
ad4	4-Input AND with 1X Drive
ad4d2	4-Input AND with 2X Drive
ad4d4	4-Input AND with 4X Drive
ad5	5-Input AND with 1X Drive
ad5d2	5-Input AND with 2X Drive
ad5d4	5-Input AND with 4X Drive
nd2	2-Input NAND with 1X Drive
nd2d2	2-Input NAND with 2X Drive
nd2d4	2-Input NAND with 4X Drive
nd2d8	2-Input NAND with 8X Drive
nd2b	2-Input NAND with one Inverted Input, 1X Drive
nd2bd2	2-Input NAND with one Inverted Input, 2X Drive
nd2bd4	2-Input NAND with one Inverted Input, 4X Drive
nd2bd8	2-Input NAND with one Inverted Input, 8X Drive
nd3	3-Input NAND with 1X Drive
nd3d2	3-Input NAND with 2X Drive
nd3d4	3-Input NAND with 4X Drive
nd3d8	3-Input NAND with 8X Drive
nd3b	3-Input NAND with one Inverted Input, 1X Drive
nd3bd2	3-Input NAND with one Inverted Input, 2X Drive
nd3bd4	3-Input NAND with one Inverted Input, 4X Drive
nd3bd8	3-Input NAND with one Inverted Input, 8X Drive
nd4	4-Input NAND with 1X Drive
nd4d2	4-Input NAND with 2X Drive
nd4d4	4-Input NAND with 4X Drive
nd5	5-Input NAND with 1X Drive
nd5d2	5-Input NAND with 2X Drive
nd5d4	5-Input NAND with 4X Drive
nd6	6-Input NAND with 1X Drive
nd6d2	6-Input NAND with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
nd6d4	6-Input NAND with 4X Drive
nd8	8-Input NAND with 1X Drive
nd8d2	8-Input NAND with 2X Drive
nd8d4	8-Input NAND with 4X Drive
nr2	2-Input NOR with 1X Drive
nr2a	2-Input NR2 with 2X P-Transistor, 1X N-Transistor
nr2d2	2-Input NOR with 2X Drive
nr2d4	2-Input NOR with 4X Drive
nr2d8	2-Input NOR with 8X Drive
nr2b	2-Input NOR with one Inverted Input, 1X Drive
nr2bd2	2-Input NOR with one Inverted Input, 2X Drive
nr2bd4	2-Input NOR with one Inverted Input, 4X Drive
nr2bd8	2-Input NOR with one Inverted Input, 8X Drive
nr3	3-Input NOR with 1X Drive
nr3a	3-Input NOR with 2X P-Transistor, 1X N-Transistor
nr3d2	3-Input NOR with 2X Drive
nr3d4	3-Input NOR with 4X Drive
nr4	4-Input NOR with 1X Drive
nr4d2	4-Input NOR with 2X Drive
nr4d4	4-Input NOR with 4X Drive
nr5	5-Input NOR with 1X Drive
nr5d2	5-Input NOR with 2X Drive
nr5d4	5-Input NOR with 4X Drive
nr6	6-Input NOR with 1X Drive
nr6d2	6-Input NOR with 2X Drive
nr6d4	6-Input NOR with 4X Drive
nr8	8-Input NOR with 1X Drive
nr8d2	8-Input NOR with 2X Drive
nr8d4	8-Input NOR with 4X Drive
or2	2-Input OR with 1X Drive
or2d2	2-Input OR with 2X Drive
or2d4	2-Input OR with 4X Drive
or2d8	2-Input OR with 8X Drive
or2b	2-Input OR with one Inverted Input, 1X Drive
or2bd2	2-Input OR with one Inverted Input, 2X Drive
or2bd4	2-Input OR with one Inverted Input, 4X Drive
or2bd8	2-Input OR with one Inverted Input, 8X Drive
or3	3-Input OR with 1X Drive
or3d2	3-Input OR with 2X Drive
or3d4	3-Input OR with 4X Drive
or4	4-Input OR with 1X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
or4d2	4-Input OR with 2X Drive
or4d4	4-Input OR with 4X Drive
or5	5-Input OR with 1X Drive
or5d2	5-Input OR with 2X Drive
or5d4	5-Input OR with 4X Drive
xn2	2-Input Exclusive-NOR with 1X Drive
xn2d2	2-Input Exclusive-NOR with 2X Drive
xn2d4	2-Input Exclusive-NOR with 4X Drive
xn2d8	2-Input Exclusive-NOR with 8X Drive
xn3	3-Input Exclusive-NOR with 1X Drive
xn3d2	3-Input Exclusive-NOR with 2X Drive
xn3d4	3-Input Exclusive-NOR with 4X Drive
xo2	2-Input Exclusive-OR with 1X Drive
xo2d2	2-Input Exclusive-OR with 2X Drive
xo2d4	2-Input Exclusive-OR with 4X Drive
xo2d8	2-Input Exclusive-OR with 8X Drive
xo3	3-Input Exclusive-OR with 1X Drive
xo3d2	3-Input Exclusive-OR with 2X Drive
xo3d4	3-Input Exclusive-OR with 4X Drive
ao21	2-AND into 2-NOR with 1X Drive
ao21d2	2-AND into 2-NOR with 2X Drive
ao21d4	2-AND into 2-NOR with 4X Drive
ao211	2-AND into 3-NOR with 1X Drive
ao211d2	2-AND into 3-NOR with 2X Drive
ao211d4	2-AND into 3-NOR with 4X Drive
ao2111	2-AND into 4-NOR with 1X Drive
ao2111d2	2-AND into 4-NOR with 2X Drive
ao22	Two 2-ANDs into 2-NOR with 1X Drive
ao22d2	Two 2-ANDs into 2-NOR with 2X Drive
ao22d4	Two 2-ANDs into 2-NOR with 4X Drive
ao22a	2-AND and 2-NOR into 2-NOR with 1X Drive
ao22d2a	2-AND and 2-NOR into 2-NOR with 2X Drive
ao221	Two 2-ANDs into 3-NOR with 1X Drive
ao221d2	Two 2-ANDs into 3-NOR with 2X Drive
ao221d4	Two 2-ANDs into 3-NOR with 4X Drive
ao222	Three 2-ANDs into 3-NOR with 1X Drive
ao222d2	Three 2-ANDs into 3-NOR with 2X Drive
ao222d4	Three 2-ANDs into 3-NOR with 4X Drive
ao222a	Inverting 2-of-3 Majority with 1X Drive
ao222d2a	Inverting 2-of-3 Majority with 2X Drive
ao2222	Four 2-ANDs into 4-NOR with 1X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
ao2222d2	Four 2-ANDs into 4-NOR with 2X Drive
ao2222d4	Four 2-ANDs into 4-NOR with 4X Drive
ao31	3-AND into 2-NOR with 1X Drive
ao31d2	3-AND into 2-NOR with 2X Drive
ao31d4	3-AND into 2-NOR with 4X Drive
ao311	3-AND into 3-NOR with 1X Drive
ao311d2	3-AND into 3-NOR with 2X Drive
ao3111	3-AND into 4-NOR with 1X Drive
ao3111d2	3-AND into 4-NOR with 2X Drive
ao32	3-AND and 2-AND into 2-NOR with 1X Drive
ao32d2	3-AND and 2-AND into 2-NOR with 2X Drive
ao321	3-AND and 2-AND into 3-NOR with 1X Drive
ao321d2	3-AND and 2-AND into 3-NOR with 2X Drive
ao322	3-AND and Two 2-ANDs into 3-NOR with 1X Drive
ao322d2	3-AND and Two 2-ANDs into 3-NOR with 2X Drive
ao33	Two 3-ANDs into 2-NOR with 1X Drive
ao33d2	Two 3-ANDs into 2-NOR with 2X Drive
ao331	Two 3-ANDs into 3-NOR with 1X Drive
ao331d2	Two 3-ANDs into 3-NOR with 2X Drive
ao332	Two 3-ANDs and 2-AND into 3-NOR with 1X Drive
ao332d2	Two 3-ANDs and 2-AND into 3-NOR with 2X Drive
oa21	2-OR into 2-NAND with 1X Drive
oa21d2	2-OR into 2-NAND with 2X Drive
oa21d4	2-OR into 2-NAND with 4X Drive
oa211	2-OR into 3-NAND with 1X Drive
oa211d2	2-OR into 3-NAND with 2X Drive
oa211d4	2-OR into 3-NAND with 4X Drive
oa2111	2-OR into 4-NAND with 1X Drive
oa2111d2	2-OR into 4-NAND with 2X Drive
oa22	Two 2-ORs into 2-NAND with 1X Drive
oa22d2	Two 2-ORs into 2-NAND with 2X Drive
oa22d4	Two 2-ORs into 2-NAND with 4X Drive
oa22a	2-OR and 2-NAND into 2-NAND with 1X Drive
oa22d2a	2-OR and 2-NAND into 2-NAND with 2X Drive
oa22d4a	2-OR and 2-NAND into 2-NAND with 4X Drive
oa221	Two 2-ORs into 3-NAND with 1X Drive
oa221d2	Two 2-ORs into 3-NAND with 2X Drive
oa221d4	Two 2-ORs into 3-NAND with 4X Drive
oa222	Three 2-ORs into 3-NAND with 1X Drive
oa222d2	Three 2-ORs into 3-NAND with 2X Drive
oa222d4	Three 2-ORs into 3-NAND with 4X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
oa2222	Four 2-ORs into 4-NAND with 1X Drive
oa2222d2	Four 2-ORs into 4-NAND with 2X Drive
oa2222d4	Four 2-ORs into 4-NAND with 4X Drive
oa31	3-OR into 2-NAND with 1X Drive
oa31d2	3-OR into 2-NAND with 2X Drive
oa31d4	3-OR into 2-NAND with 4X Drive
oa311	3-OR into 3-NAND with 1X Drive
oa311d2	3-OR into 3-NAND with 2X Drive
oa3111	3-OR into 4-NAND with 1X Drive
oa3111d2	3-OR into 4-NAND with 2X Drive
oa32	3-OR and 2-OR into 2-NAND with 1X Drive
oa32d2	3-OR and 2-OR into 2-NAND with 2X Drive
oa321	3-OR and 2-OR into 3-NAND with 1X Drive
oa321d2	3-OR and 2-OR into 3-NAND with 2X Drive
oa322	3-OR and Two 2-ORs into 3-NAND with 1X Drive
oa322d2	3-OR and Two 2-ORs into 3-NAND wit 2X Drive
oa33	Two 3-ORs into 2-NAND with 1X Drive
oa33d2	Two 3-ORs into 2-NAND with 2X Drive
scg1	2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X Drive
scg1d2	2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 2X Drive
scg2	Two 2-ANDs into 2-OR with 1X Drive
scg2d2	Two 2-ANDs into 2-OR with 2X Drive
scg2d4	Two 2-ANDs into 2-OR with 4X Drive
scg3	Two 2-NANDs into 3-NAND with 1X Drive
scg3d2	Two 2-NANDs into 3-NAND with 2X Drive
scg3d4	Two 2-NANDs into 3-NAND with 4X Drive
scg4	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X Drive
scg4d2	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
scg4d4	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 4X Drive
scg5	Three 2-ANDs into 3-OR with 1X Drive
scg5d2	Three 2-ANDs into 3-OR with 2X Drive
scg5d4	Three 2-ANDs into 3-OR with 4X Drive
scg6	2-AND into 2-OR with 1X Drive
scg6d2	2-AND into 2-OR with 2X Drive
scg6d4	2-AND into 2-OR with 4X Drive
scg7	2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X Drive
scg7d2	2-NAND and (2-AND into 2-NOR) into 2-NAND with 2X Drive
scg7d4	2-NAND and (2-AND into 2-NOR) into 2-NAND with 4X Drive
scg8	2-AND into 3-OR with 1X Drive
scg8d2	2-AND into 3-OR with 2X Drive
scg9	2-OR into 2-AND with 1X Drive
scg9d2	2-OR into 2-AND with 2X Drive
scg9d4	2-OR into 2-AND with 4X Drive
scg10	Two 2-ORs into 2-AND with 1X Drive
scg10d2	Two 2-ORs into 2-AND with 2X Drive
scg10d4	Two 2-ORs into 2-AND with 4X Drive
scg11	Two 2-NORs into 3-NOR with 1X Drive
scg11d2	Two 2-NORs into 3-NOR with 2X Drive
scg12	2-NAND into 2-NOR with 1X Drive
scg12d2	2-NAND into 2-NOR with 2X Drive
scg12d4	2-NAND into 2-NOR with 4X Drive
scg13	2-NOR into 2-NAND with 1X Drive
scg13d2	2-NOR into 2-NAND with 2X Drive
scg13d4	2-NOR into 2-NAND with 4X Drive
scg14	2-NAND into 2-NAND with 1X Drive
scg14d2	2-NAND into 2-NAND with 2X Drive
scg14d4	2-NAND into 2-NAND with 4X Drive
scg15	2-NAND into 3-NAND with 1X Drive
scg15d2	2-NAND into 3-NAND with 2X Drive
scg15d4	2-NAND into 3-NAND with 4X Drive
scg16	2-OR with one inverted input into 2-NAND with 1X Drive
scg16d2	2-OR with one inverted input into 2-NAND with 2X Drive
scg16d4	2-OR with one inverted input into 2-NAND with 4X Drive
scg17	2-AND into 2-NOR into 2-NAND with 1X Drive
scg17d2	2-AND into 2-NOR into 2-NAND with 2X Drive
scg17d4	2-AND into 2-NOR into 2-NAND with 4X Drive

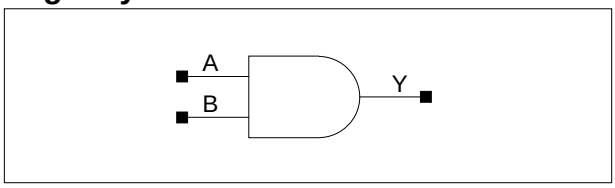
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
scg18	2-AND into 2-NOR into 3-NAND with 1X Drive
scg18d2	2-AND into 2-NOR into 3-NAND with 2X Drive
scg18d4	2-AND into 2-NOR into 3-NAND with 4X Drive
scg19	2-AND into 2-AND into 2-NOR with 1X Drive
scg19d2	2-AND into 2-AND into 2-NOR with 2X Drive
scg20	2-NOR into 2-NOR with 1X Drive
scg20d2	2-NOR into 2-NOR with 2X Drive
scg20d4	2-NOR into 2-NOR with 4X Drive
scg21	2-NOR into 3-NOR with 1X Drive
scg21d2	2-NOR into 3-NOR with 2X Drive
scg22	2-NAND into 2-OR into 2-NAND with 1X Drive
scg22d2	2-NAND into 2-OR into 2-NAND with 2X Drive
scg22d4	2-NAND into 2-OR into 2-NAND with 4X Drive
dl1d2	1ns Delay Cell with 2X Drive
dl2d2	2ns Delay Cell with 2X Drive
dl5d2	5ns Delay Cell with 2X Drive
dl10d2	10ns Delay Cell with 2X Drive
iv	Inverter with 1X Drive
ivd2	Inverter with 2X Drive
ivd3	Inverter with 3X Drive
ivd4	Inverter with 4X Drive
ivd6	Inverter with 6X Drive
ivd8	Inverter with 8X Drive
ivd16	Inverter with 16X Drive
ivd24	Inverter with 24X Drive
ivt	Inverting Tri-State Buffer with Enable High, 1X Drive
ivtd2	Inverting Tri-State Buffer with Enable High, 2X Drive
ivtd4	Inverting Tri-State Buffer with Enable High, 4X Drive
ivtd8	Inverting Tri-State Buffer with Enable High, 8X Drive
ivtd16	Inverting Tri-State Buffer with Enable High, 16X Drive
nid	Non-Inverting Buffer with 1X Drive
nid2	Non-Inverting Buffer with 2X Drive
nid3	Non-Inverting Buffer with 3X Drive
nid4	Non-Inverting Buffer with 4X Drive
nid6	Non-Inverting Buffer with 6X Drive
nid8	Non-Inverting Buffer with 8X Drive
nid16	Non-Inverting Buffer with 16X Drive
nid24	Non-Inverting Buffer with 24X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
nit	Non-Inverting Tri-State Buffer with Enable High, 1X Drive
nitd2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
nitd4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
nitd8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
nitd16	Non-Inverting Tri-State Buffer with Enable High, 16X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)								Gate Count			
ad2		*ad2d2*		*ad2d4*		*ad2d8*		*ad2*	*ad2d2*	*ad2d4*	*ad2d8*
A	B	A	B	A	B	A	B				
1.1	1.2	1.1	1.2	1.1	1.2	2.1	2.4	1.67	2.00	3.00	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.023 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.034	0.020 + 0.007*SL	0.017 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.051	0.041 + 0.005*SL	0.043 + 0.005*SL	0.044 + 0.004*SL
	t_{PHL}	0.055	0.045 + 0.005*SL	0.048 + 0.004*SL	0.049 + 0.004*SL
B to Y	t_R	0.040	0.020 + 0.010*SL	0.020 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.035	0.020 + 0.008*SL	0.021 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.052	0.042 + 0.005*SL	0.044 + 0.005*SL	0.045 + 0.004*SL
	t_{PHL}	0.059	0.049 + 0.005*SL	0.052 + 0.004*SL	0.054 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ad2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.021 + 0.007*SL	0.031 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.020 + 0.005*SL	0.024 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.053	0.047 + 0.003*SL	0.050 + 0.002*SL	0.052 + 0.002*SL
	t_{PHL}	0.057	0.051 + 0.003*SL	0.054 + 0.002*SL	0.058 + 0.002*SL
B to Y	t_R	0.033	0.024 + 0.004*SL	0.022 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.030	0.024 + 0.003*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.053	0.047 + 0.003*SL	0.050 + 0.002*SL	0.053 + 0.002*SL
	t_{PHL}	0.060	0.054 + 0.003*SL	0.058 + 0.002*SL	0.062 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.031 + 0.003*SL	0.033 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.033	0.028 + 0.002*SL	0.030 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.064	0.060 + 0.002*SL	0.062 + 0.001*SL	0.069 + 0.001*SL
	t_{PHL}	0.067	0.063 + 0.002*SL	0.065 + 0.001*SL	0.075 + 0.001*SL
B to Y	t_R	0.038	0.030 + 0.004*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.033	0.030 + 0.001*SL	0.028 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.064	0.060 + 0.002*SL	0.062 + 0.001*SL	0.069 + 0.001*SL
	t_{PHL}	0.070	0.066 + 0.002*SL	0.069 + 0.001*SL	0.079 + 0.001*SL

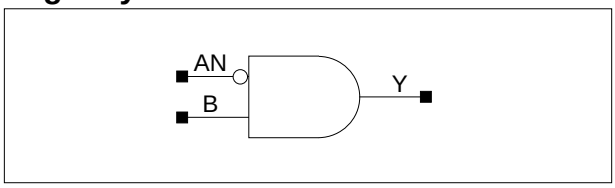
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ad2d8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.033 + 0.001*SL	0.031 + 0.001*SL	0.021 + 0.001*SL
	t_F	0.031	0.029 + 0.001*SL	0.029 + 0.001*SL	0.025 + 0.001*SL
	t_{PLH}	0.061	0.060 + 0.001*SL	0.061 + 0.001*SL	0.069 + 0.001*SL
	t_{PHL}	0.065	0.063 + 0.001*SL	0.064 + 0.001*SL	0.075 + 0.001*SL
B to Y	t_R	0.035	0.031 + 0.002*SL	0.035 + 0.001*SL	0.021 + 0.001*SL
	t_F	0.032	0.029 + 0.001*SL	0.030 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.061	0.060 + 0.001*SL	0.061 + 0.001*SL	0.069 + 0.001*SL
	t_{PHL}	0.068	0.066 + 0.001*SL	0.067 + 0.001*SL	0.078 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

AN	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

Cell Data

Input Load (SL)								Gate Count			
ad2b		*ad2bd2*		*ad2bd4*		*ad2bd8*		*ad2b*	*ad2bd2*	*ad2bd4*	*ad2bd8*
AN	B	AN	B	AN	B	AN	B				
0.6	1.2	0.6	1.2	0.6	1.1	0.9	2.4	2.33	2.33	3.33	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad2b

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.041	0.022 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.032	0.015 + 0.009*SL	0.019 + 0.008*SL	0.012 + 0.008*SL
	t_{PLH}	0.089	0.079 + 0.005*SL	0.081 + 0.005*SL	0.082 + 0.004*SL
	t_{PHL}	0.074	0.065 + 0.005*SL	0.067 + 0.004*SL	0.069 + 0.004*SL
B to Y	t_R	0.041	0.023 + 0.009*SL	0.019 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.038	0.018 + 0.010*SL	0.029 + 0.007*SL	0.014 + 0.008*SL
	t_{PLH}	0.053	0.043 + 0.005*SL	0.046 + 0.005*SL	0.047 + 0.004*SL
	t_{PHL}	0.060	0.049 + 0.005*SL	0.053 + 0.004*SL	0.054 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad2bd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.032	0.023 + 0.005*SL	0.022 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.090	0.084 + 0.003*SL	0.087 + 0.002*SL	0.090 + 0.002*SL
	t_{PHL}	0.075	0.069 + 0.003*SL	0.073 + 0.002*SL	0.077 + 0.002*SL
B to Y	t_R	0.033	0.022 + 0.005*SL	0.024 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.053	0.047 + 0.003*SL	0.050 + 0.002*SL	0.053 + 0.002*SL
	t_{PHL}	0.059	0.053 + 0.003*SL	0.056 + 0.002*SL	0.061 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ad2bd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.036	0.031 + 0.002*SL	0.031 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.026 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.108 + 0.001*SL
	t_{PHL}	0.085	0.082 + 0.002*SL	0.084 + 0.001*SL	0.094 + 0.001*SL
B to Y	t_R	0.036	0.033 + 0.002*SL	0.030 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.032	0.029 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.064	0.060 + 0.002*SL	0.063 + 0.001*SL	0.070 + 0.001*SL
	t_{PHL}	0.069	0.065 + 0.002*SL	0.068 + 0.001*SL	0.078 + 0.001*SL

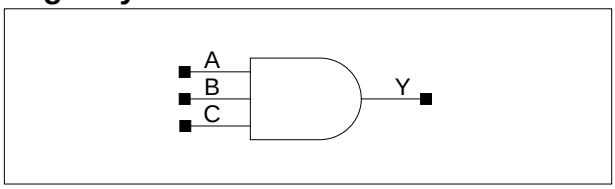
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ad2bd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.034	0.031 + 0.002*SL	0.032 + 0.001*SL	0.023 + 0.001*SL
	t_F	0.029	0.026 + 0.001*SL	0.027 + 0.001*SL	0.020 + 0.001*SL
	t_{PLH}	0.096	0.094 + 0.001*SL	0.096 + 0.001*SL	0.104 + 0.001*SL
	t_{PHL}	0.085	0.083 + 0.001*SL	0.084 + 0.001*SL	0.095 + 0.001*SL
B to Y	t_R	0.035	0.033 + 0.001*SL	0.033 + 0.001*SL	0.022 + 0.001*SL
	t_F	0.031	0.028 + 0.001*SL	0.030 + 0.001*SL	0.023 + 0.001*SL
	t_{PLH}	0.063	0.061 + 0.001*SL	0.062 + 0.001*SL	0.070 + 0.001*SL
	t_{PHL}	0.067	0.065 + 0.001*SL	0.066 + 0.001*SL	0.078 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
ad3			*ad3d2*			*ad3d4*			*ad3*	*ad3d2*	*ad3d4*
A	B	C	A	B	C	A	B	C			
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	2.00	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.025 + 0.010*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.038	0.025 + 0.007*SL	0.020 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.062	0.051 + 0.006*SL	0.055 + 0.005*SL	0.056 + 0.004*SL
	t_{PHL}	0.064	0.054 + 0.005*SL	0.058 + 0.004*SL	0.060 + 0.004*SL
B to Y	t_R	0.047	0.032 + 0.008*SL	0.023 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.037	0.022 + 0.008*SL	0.022 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.064	0.053 + 0.006*SL	0.057 + 0.005*SL	0.059 + 0.004*SL
	t_{PHL}	0.069	0.058 + 0.005*SL	0.062 + 0.004*SL	0.065 + 0.004*SL
C to Y	t_R	0.045	0.028 + 0.009*SL	0.023 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.039	0.025 + 0.007*SL	0.022 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.065	0.053 + 0.006*SL	0.057 + 0.005*SL	0.059 + 0.004*SL
	t_{PHL}	0.072	0.061 + 0.006*SL	0.066 + 0.004*SL	0.070 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

3-Input AND with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.030 + 0.005*SL	0.030 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.033	0.027 + 0.003*SL	0.025 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.064	0.058 + 0.003*SL	0.062 + 0.002*SL	0.068 + 0.002*SL
	t_{PHL}	0.066	0.060 + 0.003*SL	0.064 + 0.002*SL	0.071 + 0.002*SL
B to Y	t_R	0.043	0.031 + 0.006*SL	0.037 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.033	0.026 + 0.004*SL	0.026 + 0.004*SL	0.021 + 0.004*SL
	t_{PLH}	0.066	0.060 + 0.003*SL	0.064 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.070	0.063 + 0.003*SL	0.068 + 0.002*SL	0.075 + 0.002*SL
C to Y	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.034	0.025 + 0.005*SL	0.029 + 0.004*SL	0.021 + 0.004*SL
	t_{PLH}	0.067	0.060 + 0.003*SL	0.064 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.074	0.067 + 0.003*SL	0.072 + 0.002*SL	0.080 + 0.002*SL

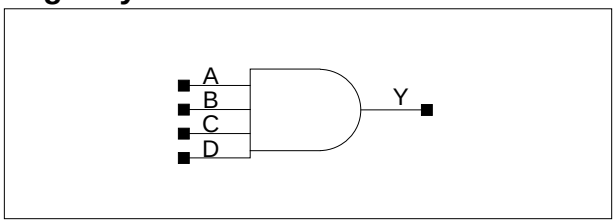
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ad3d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.038 + 0.002*SL	0.038 + 0.002*SL	0.032 + 0.003*SL
	t_F	0.037	0.033 + 0.002*SL	0.034 + 0.002*SL	0.029 + 0.002*SL
	t_{PLH}	0.078	0.074 + 0.002*SL	0.077 + 0.001*SL	0.089 + 0.001*SL
	t_{PHL}	0.079	0.075 + 0.002*SL	0.078 + 0.001*SL	0.091 + 0.001*SL
B to Y	t_R	0.045	0.040 + 0.002*SL	0.040 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.039	0.034 + 0.002*SL	0.036 + 0.002*SL	0.030 + 0.002*SL
	t_{PLH}	0.080	0.076 + 0.002*SL	0.079 + 0.001*SL	0.092 + 0.001*SL
	t_{PHL}	0.082	0.078 + 0.002*SL	0.082 + 0.001*SL	0.095 + 0.001*SL
C to Y	t_R	0.045	0.040 + 0.003*SL	0.041 + 0.002*SL	0.032 + 0.003*SL
	t_F	0.040	0.036 + 0.002*SL	0.037 + 0.002*SL	0.031 + 0.002*SL
	t_{PLH}	0.080	0.076 + 0.002*SL	0.079 + 0.001*SL	0.091 + 0.001*SL
	t_{PHL}	0.086	0.082 + 0.002*SL	0.085 + 0.001*SL	0.100 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)											
ad4				*ad4d2*				*ad4d4*			
A	B	C	D	A	B	C	D	A	B	C	D
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.9

Gate Count		
ad4	*ad4d2*	*ad4d4*
2.33	2.67	3.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.050	0.032 + 0.009*SL	0.028 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.025 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.068	0.056 + 0.006*SL	0.062 + 0.005*SL	0.065 + 0.004*SL
	t_{PHL}	0.074	0.063 + 0.006*SL	0.069 + 0.004*SL	0.073 + 0.004*SL
B to Y	t_R	0.052	0.036 + 0.008*SL	0.030 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.042	0.026 + 0.008*SL	0.028 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.073	0.061 + 0.006*SL	0.066 + 0.005*SL	0.070 + 0.004*SL
	t_{PHL}	0.080	0.069 + 0.006*SL	0.075 + 0.004*SL	0.080 + 0.004*SL
C to Y	t_R	0.050	0.031 + 0.009*SL	0.029 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.044	0.028 + 0.008*SL	0.031 + 0.007*SL	0.022 + 0.008*SL
	t_{PLH}	0.075	0.063 + 0.006*SL	0.069 + 0.005*SL	0.073 + 0.004*SL
	t_{PHL}	0.086	0.074 + 0.006*SL	0.080 + 0.004*SL	0.085 + 0.004*SL
D to Y	t_R	0.048	0.030 + 0.009*SL	0.028 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.045	0.029 + 0.008*SL	0.031 + 0.008*SL	0.024 + 0.008*SL
	t_{PLH}	0.077	0.064 + 0.006*SL	0.070 + 0.005*SL	0.074 + 0.004*SL
	t_{PHL}	0.090	0.078 + 0.006*SL	0.084 + 0.004*SL	0.090 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.044	0.034 + 0.005*SL	0.035 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.038	0.028 + 0.005*SL	0.032 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.071	0.064 + 0.004*SL	0.069 + 0.003*SL	0.078 + 0.002*SL
	t_{PHL}	0.078	0.071 + 0.004*SL	0.076 + 0.002*SL	0.085 + 0.002*SL
B to Y	t_R	0.043	0.033 + 0.005*SL	0.033 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.039	0.029 + 0.005*SL	0.033 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.076	0.068 + 0.004*SL	0.073 + 0.003*SL	0.082 + 0.002*SL
	t_{PHL}	0.083	0.076 + 0.004*SL	0.081 + 0.002*SL	0.092 + 0.002*SL
C to Y	t_R	0.047	0.038 + 0.004*SL	0.037 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.041	0.032 + 0.004*SL	0.034 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.077	0.070 + 0.004*SL	0.075 + 0.003*SL	0.084 + 0.002*SL
	t_{PHL}	0.088	0.081 + 0.004*SL	0.086 + 0.002*SL	0.097 + 0.002*SL
D to Y	t_R	0.044	0.034 + 0.005*SL	0.034 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.041	0.032 + 0.005*SL	0.035 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.079	0.072 + 0.004*SL	0.077 + 0.003*SL	0.086 + 0.002*SL
	t_{PHL}	0.093	0.085 + 0.004*SL	0.091 + 0.002*SL	0.103 + 0.002*SL

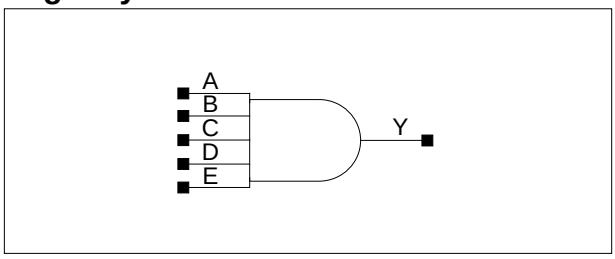
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ad4d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.053	0.048 + 0.002*SL	0.048 + 0.002*SL	0.043 + 0.002*SL
	t_F	0.047	0.042 + 0.002*SL	0.043 + 0.002*SL	0.041 + 0.002*SL
	t_{PLH}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.106 + 0.001*SL
	t_{PHL}	0.097	0.092 + 0.002*SL	0.096 + 0.001*SL	0.114 + 0.001*SL
B to Y	t_R	0.053	0.049 + 0.002*SL	0.048 + 0.002*SL	0.041 + 0.002*SL
	t_F	0.049	0.044 + 0.002*SL	0.046 + 0.002*SL	0.041 + 0.002*SL
	t_{PLH}	0.095	0.091 + 0.002*SL	0.094 + 0.001*SL	0.111 + 0.001*SL
	t_{PHL}	0.102	0.098 + 0.002*SL	0.101 + 0.001*SL	0.120 + 0.001*SL
C to Y	t_R	0.053	0.048 + 0.002*SL	0.048 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.053	0.048 + 0.002*SL	0.050 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.098	0.093 + 0.002*SL	0.096 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.107	0.103 + 0.002*SL	0.106 + 0.001*SL	0.126 + 0.001*SL
D to Y	t_R	0.053	0.047 + 0.003*SL	0.049 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.055	0.051 + 0.002*SL	0.052 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.099	0.095 + 0.002*SL	0.098 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.112	0.107 + 0.002*SL	0.111 + 0.001*SL	0.131 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)														
ad5					*ad5d2*					*ad5d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.1	1.2	1.0	1.0	1.0	1.1	1.2	1.0	1.0	1.1	1.2	1.2
Gate Count														
ad5					*ad5d2*					*ad5d4*				
3.33					3.67					5.33				

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.076	0.038 + 0.019*SL	0.034 + 0.020*SL	0.029 + 0.020*SL
	t_F	0.037	0.024 + 0.006*SL	0.021 + 0.007*SL	0.017 + 0.008*SL
	t_{PLH}	0.077	0.057 + 0.010*SL	0.060 + 0.009*SL	0.060 + 0.009*SL
	t_{PHL}	0.066	0.056 + 0.005*SL	0.060 + 0.004*SL	0.063 + 0.004*SL
B to Y	t_R	0.077	0.039 + 0.019*SL	0.034 + 0.020*SL	0.030 + 0.020*SL
	t_F	0.037	0.022 + 0.008*SL	0.024 + 0.007*SL	0.017 + 0.008*SL
	t_{PLH}	0.079	0.060 + 0.010*SL	0.062 + 0.009*SL	0.063 + 0.009*SL
	t_{PHL}	0.071	0.060 + 0.005*SL	0.065 + 0.004*SL	0.068 + 0.004*SL
C to Y	t_R	0.076	0.038 + 0.019*SL	0.034 + 0.020*SL	0.030 + 0.020*SL
	t_F	0.040	0.025 + 0.008*SL	0.026 + 0.007*SL	0.020 + 0.007*SL
	t_{PLH}	0.079	0.060 + 0.010*SL	0.062 + 0.009*SL	0.063 + 0.009*SL
	t_{PHL}	0.074	0.063 + 0.005*SL	0.068 + 0.004*SL	0.072 + 0.004*SL
D to Y	t_R	0.074	0.035 + 0.019*SL	0.031 + 0.020*SL	0.029 + 0.020*SL
	t_F	0.039	0.025 + 0.007*SL	0.023 + 0.007*SL	0.019 + 0.008*SL
	t_{PLH}	0.074	0.055 + 0.010*SL	0.057 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.058	0.049 + 0.005*SL	0.052 + 0.004*SL	0.053 + 0.004*SL
E to Y	t_R	0.072	0.033 + 0.020*SL	0.030 + 0.020*SL	0.029 + 0.020*SL
	t_F	0.039	0.023 + 0.008*SL	0.025 + 0.007*SL	0.019 + 0.008*SL
	t_{PLH}	0.075	0.056 + 0.010*SL	0.058 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.062	0.053 + 0.005*SL	0.056 + 0.004*SL	0.057 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.032 + 0.010*SL
	t_F	0.033	0.025 + 0.004*SL	0.026 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.077	0.066 + 0.005*SL	0.069 + 0.005*SL	0.071 + 0.005*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.065 + 0.002*SL	0.072 + 0.002*SL
B to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.031 + 0.010*SL
	t_F	0.035	0.028 + 0.004*SL	0.028 + 0.004*SL	0.021 + 0.004*SL
	t_{PLH}	0.079	0.068 + 0.005*SL	0.071 + 0.005*SL	0.074 + 0.005*SL
	t_{PHL}	0.072	0.065 + 0.003*SL	0.070 + 0.002*SL	0.077 + 0.002*SL
C to Y	t_R	0.060	0.040 + 0.010*SL	0.040 + 0.010*SL	0.031 + 0.010*SL
	t_F	0.037	0.029 + 0.004*SL	0.030 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.079	0.068 + 0.005*SL	0.071 + 0.005*SL	0.074 + 0.005*SL
	t_{PHL}	0.075	0.068 + 0.003*SL	0.073 + 0.002*SL	0.081 + 0.002*SL
D to Y	t_R	0.056	0.036 + 0.010*SL	0.035 + 0.010*SL	0.030 + 0.010*SL
	t_F	0.036	0.029 + 0.004*SL	0.029 + 0.004*SL	0.023 + 0.004*SL
	t_{PLH}	0.075	0.065 + 0.005*SL	0.067 + 0.005*SL	0.070 + 0.005*SL
	t_{PHL}	0.063	0.057 + 0.003*SL	0.060 + 0.002*SL	0.065 + 0.002*SL
E to Y	t_R	0.055	0.035 + 0.010*SL	0.034 + 0.010*SL	0.030 + 0.010*SL
	t_F	0.035	0.028 + 0.004*SL	0.028 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.076	0.065 + 0.005*SL	0.068 + 0.005*SL	0.070 + 0.005*SL
	t_{PHL}	0.067	0.061 + 0.003*SL	0.064 + 0.002*SL	0.069 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ad5d4

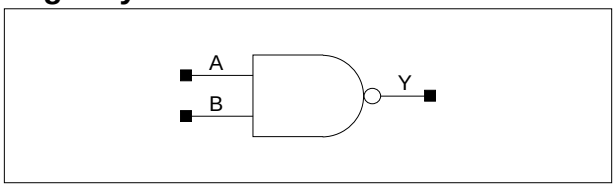
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.003*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.023 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.129	0.126 + 0.002*SL	0.128 + 0.001*SL	0.133 + 0.001*SL
	t_{PHL}	0.109	0.106 + 0.002*SL	0.109 + 0.001*SL	0.117 + 0.001*SL
B to Y	t_R	0.033	0.028 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.024 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.132	0.128 + 0.002*SL	0.131 + 0.001*SL	0.135 + 0.001*SL
	t_{PHL}	0.114	0.110 + 0.002*SL	0.113 + 0.001*SL	0.121 + 0.001*SL
C to Y	t_R	0.033	0.028 + 0.003*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.018 + 0.002*SL
	t_{PLH}	0.132	0.128 + 0.002*SL	0.131 + 0.001*SL	0.136 + 0.001*SL
	t_{PHL}	0.116	0.112 + 0.002*SL	0.115 + 0.001*SL	0.122 + 0.001*SL
D to Y	t_R	0.034	0.029 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.024 + 0.002*SL	0.018 + 0.002*SL
	t_{PLH}	0.123	0.119 + 0.002*SL	0.122 + 0.001*SL	0.127 + 0.001*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.108 + 0.001*SL
E to Y	t_R	0.034	0.029 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.027	0.023 + 0.002*SL	0.024 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.123	0.120 + 0.002*SL	0.122 + 0.001*SL	0.127 + 0.001*SL
	t_{PHL}	0.105	0.101 + 0.002*SL	0.104 + 0.001*SL	0.112 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd2/nd2d2/nd2d4/nd2d8

2-Input NAND with 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)								Gate Count			
nd2		*nd2d2*		*nd2d4*		*nd2d8*		*nd2*	*nd2d2*	*nd2d4*	*nd2d8*
A	B	A	B	A	B	A	B				
1.1	1.2	2.2	2.4	4.5	4.9	1.1	1.2	1.00	2.00	3.67	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.040 + 0.009*SL	0.035 + 0.010*SL	0.020 + 0.011*SL
	t_F	0.053	0.037 + 0.008*SL	0.033 + 0.009*SL	0.020 + 0.010*SL
	t_{PLH}	0.036	0.024 + 0.006*SL	0.030 + 0.005*SL	0.030 + 0.005*SL
	t_{PHL}	0.032	0.019 + 0.006*SL	0.026 + 0.005*SL	0.027 + 0.005*SL
B to Y	t_R	0.061	0.042 + 0.009*SL	0.038 + 0.010*SL	0.025 + 0.011*SL
	t_F	0.047	0.031 + 0.008*SL	0.026 + 0.009*SL	0.019 + 0.010*SL
	t_{PLH}	0.040	0.028 + 0.006*SL	0.033 + 0.005*SL	0.032 + 0.005*SL
	t_{PHL}	0.033	0.021 + 0.006*SL	0.026 + 0.005*SL	0.027 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nd2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.049	0.039 + 0.005*SL	0.040 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.045	0.035 + 0.005*SL	0.037 + 0.004*SL	0.021 + 0.005*SL
	t_{PLH}	0.030	0.023 + 0.004*SL	0.027 + 0.002*SL	0.030 + 0.002*SL
	t_{PHL}	0.026	0.018 + 0.004*SL	0.023 + 0.003*SL	0.026 + 0.002*SL
B to Y	t_R	0.051	0.044 + 0.004*SL	0.039 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.039	0.031 + 0.004*SL	0.028 + 0.005*SL	0.020 + 0.005*SL
	t_{PLH}	0.034	0.027 + 0.003*SL	0.031 + 0.002*SL	0.032 + 0.002*SL
	t_{PHL}	0.027	0.020 + 0.003*SL	0.024 + 0.003*SL	0.027 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.044	0.040 + 0.002*SL	0.039 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.040	0.035 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.026	0.022 + 0.002*SL	0.025 + 0.001*SL	0.030 + 0.001*SL
	t_{PHL}	0.022	0.018 + 0.002*SL	0.021 + 0.001*SL	0.026 + 0.001*SL
B to Y	t_R	0.047	0.043 + 0.002*SL	0.041 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.034	0.029 + 0.002*SL	0.030 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.030	0.027 + 0.002*SL	0.029 + 0.001*SL	0.032 + 0.001*SL
	t_{PHL}	0.023	0.020 + 0.002*SL	0.022 + 0.001*SL	0.027 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd2d8

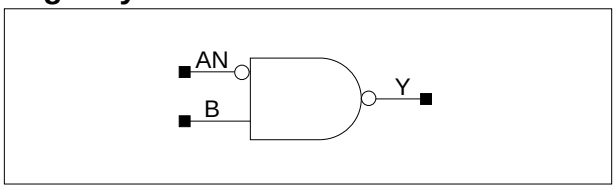
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.030	0.028 + 0.001*SL	0.028 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.029	0.027 + 0.001*SL	0.027 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.088	0.086 + 0.001*SL	0.088 + 0.001*SL	0.093 + 0.001*SL
	t_{PHL}	0.086	0.084 + 0.001*SL	0.086 + 0.001*SL	0.095 + 0.001*SL
B to Y	t_R	0.030	0.027 + 0.001*SL	0.028 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.027 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.092	0.090 + 0.001*SL	0.092 + 0.001*SL	0.097 + 0.001*SL
	t_{PHL}	0.087	0.085 + 0.001*SL	0.086 + 0.001*SL	0.095 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

nd2b/nd2bd2/nd2bd4/nd2bd8

2-Input NAND with one Inverted Input, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

AN	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

Cell Data

Input Load (SL)								Gate Count			
nd2b		*nd2bd2*		*nd2bd4*		*nd2bd8*		*nd2b*	*nd2bd2*	*nd2bd4*	*nd2bd8*
AN	B	AN	B	AN	B	AN	B				
0.8	1.2	1.0	2.5	1.0	4.9	0.9	1.2	1.67	2.67	4.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd2b

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.047	0.027 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.011*SL
	t_F	0.044	0.026 + 0.009*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_{PLH}	0.059	0.049 + 0.005*SL	0.051 + 0.005*SL	0.051 + 0.005*SL
	t_{PHL}	0.057	0.046 + 0.005*SL	0.048 + 0.005*SL	0.049 + 0.005*SL
B to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.026 + 0.011*SL
	t_F	0.049	0.032 + 0.009*SL	0.030 + 0.009*SL	0.021 + 0.010*SL
	t_{PLH}	0.040	0.028 + 0.006*SL	0.032 + 0.005*SL	0.032 + 0.005*SL
	t_{PHL}	0.034	0.021 + 0.006*SL	0.026 + 0.005*SL	0.028 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd2bd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.038	0.029 + 0.005*SL	0.027 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.027 + 0.005*SL	0.019 + 0.005*SL
	t_{PLH}	0.058	0.052 + 0.003*SL	0.054 + 0.002*SL	0.055 + 0.002*SL
	t_{PHL}	0.056	0.050 + 0.003*SL	0.052 + 0.002*SL	0.054 + 0.002*SL
B to Y	t_R	0.052	0.044 + 0.004*SL	0.040 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.039	0.031 + 0.004*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_{PLH}	0.033	0.026 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
	t_{PHL}	0.027	0.020 + 0.004*SL	0.024 + 0.003*SL	0.029 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nd2bd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.040	0.036 + 0.002*SL	0.034 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.039	0.037 + 0.001*SL	0.032 + 0.002*SL	0.027 + 0.002*SL
	t_{PLH}	0.066	0.063 + 0.002*SL	0.065 + 0.001*SL	0.068 + 0.001*SL
	t_{PHL}	0.068	0.065 + 0.002*SL	0.067 + 0.001*SL	0.072 + 0.001*SL
B to Y	t_R	0.048	0.044 + 0.002*SL	0.042 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.035	0.030 + 0.003*SL	0.031 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.029	0.026 + 0.002*SL	0.028 + 0.001*SL	0.032 + 0.001*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.022 + 0.001*SL	0.030 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd2bd8

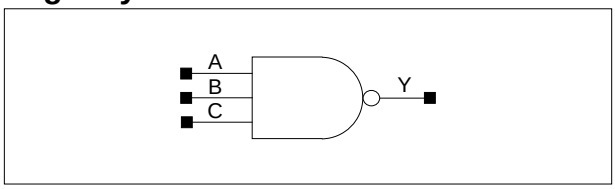
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.029	0.027 + 0.001*SL	0.027 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.026 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.110	0.108 + 0.001*SL	0.109 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.109	0.107 + 0.001*SL	0.108 + 0.001*SL	0.118 + 0.001*SL
B to Y	t_R	0.030	0.027 + 0.001*SL	0.028 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.027 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.092	0.090 + 0.001*SL	0.091 + 0.001*SL	0.096 + 0.001*SL
	t_{PHL}	0.087	0.085 + 0.001*SL	0.086 + 0.001*SL	0.096 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

nd3/nd3d2/nd3d4/nd3d8

3-Input NAND with 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)											
nd3			*nd3d2*			*nd3d4*			*nd3d8*		
A	B	C	A	B	C	A	B	C	A	B	C
0.9	1.0	1.0	1.8	2.1	2.2	0.9	1.0	1.0	0.9	1.0	1.0
Gate Count											
nd3			*nd3d2*			*nd3d4*			*nd3d8*		
1.67			3.00			3.67			5.67		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.076	0.050 + 0.013*SL	0.039 + 0.015*SL	0.027 + 0.016*SL
	t_F	0.070	0.047 + 0.012*SL	0.040 + 0.013*SL	0.027 + 0.014*SL
	t_{PLH}	0.049	0.034 + 0.008*SL	0.036 + 0.007*SL	0.036 + 0.007*SL
	t_{PHL}	0.041	0.026 + 0.008*SL	0.029 + 0.007*SL	0.029 + 0.007*SL
B to Y	t_R	0.079	0.051 + 0.014*SL	0.044 + 0.016*SL	0.033 + 0.016*SL
	t_F	0.065	0.041 + 0.012*SL	0.035 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.053	0.039 + 0.007*SL	0.040 + 0.007*SL	0.039 + 0.007*SL
	t_{PHL}	0.044	0.028 + 0.008*SL	0.032 + 0.007*SL	0.032 + 0.007*SL
C to Y	t_R	0.085	0.056 + 0.014*SL	0.051 + 0.016*SL	0.040 + 0.016*SL
	t_F	0.062	0.037 + 0.013*SL	0.033 + 0.014*SL	0.026 + 0.014*SL
	t_{PLH}	0.057	0.042 + 0.007*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.044	0.029 + 0.007*SL	0.032 + 0.007*SL	0.032 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nd3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.057	0.043 + 0.007*SL	0.040 + 0.008*SL	0.023 + 0.008*SL
	t_F	0.053	0.042 + 0.006*SL	0.039 + 0.007*SL	0.025 + 0.007*SL
	t_{PLH}	0.038	0.029 + 0.005*SL	0.034 + 0.004*SL	0.034 + 0.004*SL
	t_{PHL}	0.030	0.021 + 0.005*SL	0.026 + 0.003*SL	0.027 + 0.003*SL
B to Y	t_R	0.063	0.050 + 0.007*SL	0.046 + 0.008*SL	0.030 + 0.008*SL
	t_F	0.049	0.037 + 0.006*SL	0.034 + 0.007*SL	0.024 + 0.007*SL
	t_{PLH}	0.044	0.035 + 0.004*SL	0.038 + 0.003*SL	0.038 + 0.004*SL
	t_{PHL}	0.034	0.025 + 0.004*SL	0.029 + 0.003*SL	0.030 + 0.003*SL
C to Y	t_R	0.067	0.053 + 0.007*SL	0.050 + 0.008*SL	0.036 + 0.008*SL
	t_F	0.045	0.031 + 0.007*SL	0.031 + 0.007*SL	0.023 + 0.007*SL
	t_{PLH}	0.048	0.040 + 0.004*SL	0.041 + 0.003*SL	0.041 + 0.004*SL
	t_{PHL}	0.034	0.026 + 0.004*SL	0.029 + 0.003*SL	0.030 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd3d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.027 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.097	0.093 + 0.002*SL	0.095 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.091	0.087 + 0.002*SL	0.090 + 0.001*SL	0.098 + 0.001*SL
B to Y	t_R	0.032	0.028 + 0.002*SL	0.027 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.102	0.098 + 0.002*SL	0.100 + 0.001*SL	0.105 + 0.001*SL
	t_{PHL}	0.093	0.090 + 0.002*SL	0.092 + 0.001*SL	0.101 + 0.001*SL
C to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.094	0.090 + 0.002*SL	0.093 + 0.001*SL	0.101 + 0.001*SL

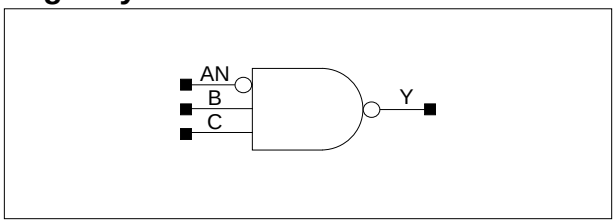
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd3d8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.031	0.030 + 0.001*SL	0.028 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.028 + 0.001*SL	0.029 + 0.001*SL	0.023 + 0.001*SL
	t_{PLH}	0.105	0.103 + 0.001*SL	0.104 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.099	0.097 + 0.001*SL	0.098 + 0.001*SL	0.108 + 0.001*SL
B to Y	t_R	0.033	0.030 + 0.001*SL	0.031 + 0.001*SL	0.019 + 0.001*SL
	t_F	0.029	0.027 + 0.001*SL	0.028 + 0.001*SL	0.020 + 0.001*SL
	t_{PLH}	0.110	0.108 + 0.001*SL	0.109 + 0.001*SL	0.116 + 0.001*SL
	t_{PHL}	0.101	0.099 + 0.001*SL	0.100 + 0.001*SL	0.110 + 0.001*SL
C to Y	t_R	0.033	0.029 + 0.002*SL	0.031 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.028 + 0.001*SL	0.028 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.115	0.113 + 0.001*SL	0.114 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.101	0.099 + 0.001*SL	0.101 + 0.001*SL	0.111 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

AN	B	C	Y
0	1	1	0
Other Stares			1

Cell Data

Input Load (SL)											
nd3b			*nd3bd2*			*nd3bd4*			*nd3bd8*		
AN	B	C	AN	B	C	AN	B	C	AN	B	C
0.8	1.0	1.0	1.0	2.0	1.9	0.8	1.0	1.0	0.8	1.0	1.0

Gate Count			
nd3b	*nd3bd2*	*nd3bd4*	*nd3bd8*
2.00	3.33	4.33	6.33

nd3b/nd3bd2/nd3bd4/nd3bd8

3-Input NAND with one Inverted Input, 1X/2X/4X/8X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd3b

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.065	0.035 + 0.015*SL	0.030 + 0.016*SL	0.027 + 0.016*SL
	t_F	0.059	0.031 + 0.014*SL	0.031 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.067	0.052 + 0.007*SL	0.054 + 0.007*SL	0.054 + 0.007*SL
	t_{PHL}	0.064	0.049 + 0.007*SL	0.051 + 0.007*SL	0.051 + 0.007*SL
B to Y	t_R	0.078	0.050 + 0.014*SL	0.044 + 0.016*SL	0.033 + 0.016*SL
	t_F	0.066	0.041 + 0.012*SL	0.036 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.053	0.038 + 0.007*SL	0.039 + 0.007*SL	0.039 + 0.007*SL
	t_{PHL}	0.044	0.028 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL
C to Y	t_R	0.085	0.056 + 0.014*SL	0.051 + 0.016*SL	0.040 + 0.016*SL
	t_F	0.062	0.035 + 0.013*SL	0.034 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.056	0.042 + 0.007*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.044	0.029 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nd3bd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.050	0.034 + 0.008*SL	0.034 + 0.008*SL	0.027 + 0.008*SL
	t_F	0.049	0.036 + 0.006*SL	0.033 + 0.007*SL	0.027 + 0.007*SL
	t_{PLH}	0.066	0.058 + 0.004*SL	0.059 + 0.004*SL	0.060 + 0.004*SL
	t_{PHL}	0.062	0.054 + 0.004*SL	0.056 + 0.003*SL	0.057 + 0.003*SL
B to Y	t_R	0.065	0.052 + 0.007*SL	0.048 + 0.008*SL	0.033 + 0.008*SL
	t_F	0.052	0.039 + 0.007*SL	0.038 + 0.007*SL	0.028 + 0.007*SL
	t_{PLH}	0.045	0.037 + 0.004*SL	0.039 + 0.003*SL	0.039 + 0.004*SL
	t_{PHL}	0.036	0.027 + 0.004*SL	0.031 + 0.003*SL	0.033 + 0.003*SL
C to Y	t_R	0.069	0.054 + 0.008*SL	0.054 + 0.008*SL	0.039 + 0.008*SL
	t_F	0.048	0.034 + 0.007*SL	0.035 + 0.007*SL	0.028 + 0.007*SL
	t_{PLH}	0.049	0.041 + 0.004*SL	0.042 + 0.004*SL	0.042 + 0.004*SL
	t_{PHL}	0.037	0.028 + 0.004*SL	0.031 + 0.003*SL	0.033 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd3bd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.033	0.028 + 0.003*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.116	0.112 + 0.002*SL	0.115 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.114	0.111 + 0.002*SL	0.113 + 0.001*SL	0.122 + 0.001*SL
B to Y	t_R	0.033	0.029 + 0.002*SL	0.027 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.102	0.099 + 0.002*SL	0.101 + 0.001*SL	0.105 + 0.001*SL
	t_{PHL}	0.094	0.091 + 0.002*SL	0.093 + 0.001*SL	0.102 + 0.001*SL
C to Y	t_R	0.033	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.094	0.091 + 0.002*SL	0.094 + 0.001*SL	0.102 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd3bd8

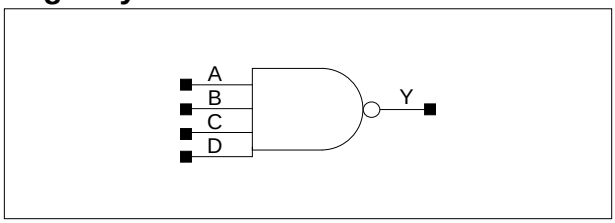
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.031	0.030 + 0.001*SL	0.027 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.028 + 0.001*SL	0.028 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.124	0.122 + 0.001*SL	0.124 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.122	0.120 + 0.001*SL	0.122 + 0.001*SL	0.131 + 0.001*SL
B to Y	t_R	0.033	0.030 + 0.001*SL	0.031 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.028 + 0.001*SL	0.028 + 0.001*SL	0.022 + 0.001*SL
	t_{PLH}	0.110	0.108 + 0.001*SL	0.109 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.102	0.100 + 0.001*SL	0.101 + 0.001*SL	0.111 + 0.001*SL
C to Y	t_R	0.033	0.030 + 0.001*SL	0.030 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.027 + 0.001*SL	0.028 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.115	0.113 + 0.001*SL	0.114 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.102	0.100 + 0.001*SL	0.102 + 0.001*SL	0.111 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

nd4/nd4d2/nd4d4

4-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)											
nd4				*nd4d2*				*nd4d4*			
A	B	C	D	A	B	C	D	A	B	C	D
0.8	0.9	0.9	0.9	1.6	1.9	1.8	1.7	0.9	0.9	0.9	0.9
Gate Count											
nd4				*nd4d2*				*nd4d4*			
2.00				3.67				4.00			

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.052 + 0.018*SL	0.042 + 0.021*SL	0.034 + 0.021*SL
	t_F	0.084	0.051 + 0.016*SL	0.046 + 0.018*SL	0.034 + 0.018*SL
	t_{PLH}	0.058	0.039 + 0.009*SL	0.040 + 0.009*SL	0.040 + 0.009*SL
	t_{PHL}	0.047	0.028 + 0.009*SL	0.030 + 0.009*SL	0.030 + 0.009*SL
B to Y	t_R	0.096	0.058 + 0.019*SL	0.050 + 0.021*SL	0.042 + 0.021*SL
	t_F	0.081	0.048 + 0.016*SL	0.042 + 0.018*SL	0.035 + 0.018*SL
	t_{PLH}	0.064	0.045 + 0.009*SL	0.045 + 0.009*SL	0.045 + 0.009*SL
	t_{PHL}	0.052	0.033 + 0.009*SL	0.035 + 0.009*SL	0.036 + 0.009*SL
C to Y	t_R	0.103	0.065 + 0.019*SL	0.057 + 0.021*SL	0.050 + 0.021*SL
	t_F	0.078	0.044 + 0.017*SL	0.040 + 0.018*SL	0.035 + 0.018*SL
	t_{PLH}	0.068	0.049 + 0.009*SL	0.050 + 0.009*SL	0.050 + 0.009*SL
	t_{PHL}	0.054	0.035 + 0.009*SL	0.037 + 0.009*SL	0.037 + 0.009*SL
D to Y	t_R	0.110	0.070 + 0.020*SL	0.065 + 0.021*SL	0.058 + 0.021*SL
	t_F	0.075	0.040 + 0.017*SL	0.038 + 0.018*SL	0.035 + 0.018*SL
	t_{PLH}	0.071	0.053 + 0.009*SL	0.053 + 0.009*SL	0.054 + 0.009*SL
	t_{PHL}	0.054	0.036 + 0.009*SL	0.038 + 0.009*SL	0.038 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.070	0.054 + 0.008*SL	0.045 + 0.010*SL	0.032 + 0.011*SL
	t_F	0.068	0.053 + 0.007*SL	0.047 + 0.009*SL	0.034 + 0.009*SL
	t_{PLH}	0.048	0.037 + 0.005*SL	0.040 + 0.005*SL	0.039 + 0.005*SL
	t_{PHL}	0.036	0.026 + 0.005*SL	0.029 + 0.004*SL	0.029 + 0.004*SL
B to Y	t_R	0.076	0.059 + 0.008*SL	0.051 + 0.010*SL	0.041 + 0.011*SL
	t_F	0.063	0.048 + 0.008*SL	0.044 + 0.009*SL	0.034 + 0.009*SL
	t_{PLH}	0.054	0.044 + 0.005*SL	0.045 + 0.005*SL	0.045 + 0.005*SL
	t_{PHL}	0.042	0.031 + 0.005*SL	0.034 + 0.004*SL	0.035 + 0.004*SL
C to Y	t_R	0.084	0.066 + 0.009*SL	0.060 + 0.010*SL	0.052 + 0.011*SL
	t_F	0.059	0.044 + 0.008*SL	0.039 + 0.009*SL	0.034 + 0.009*SL
	t_{PLH}	0.060	0.050 + 0.005*SL	0.051 + 0.005*SL	0.052 + 0.005*SL
	t_{PHL}	0.046	0.037 + 0.005*SL	0.038 + 0.004*SL	0.039 + 0.004*SL
D to Y	t_R	0.092	0.074 + 0.009*SL	0.069 + 0.010*SL	0.060 + 0.011*SL
	t_F	0.057	0.040 + 0.009*SL	0.039 + 0.009*SL	0.034 + 0.009*SL
	t_{PLH}	0.063	0.053 + 0.005*SL	0.054 + 0.005*SL	0.056 + 0.005*SL
	t_{PHL}	0.047	0.038 + 0.005*SL	0.039 + 0.004*SL	0.039 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nd4d4

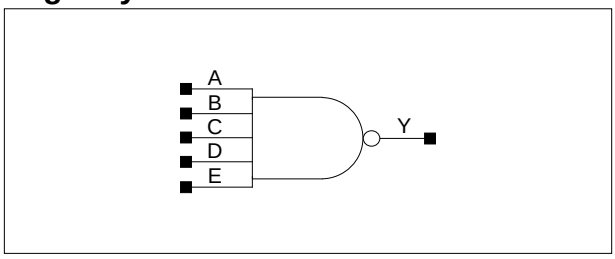
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.108	0.104 + 0.002*SL	0.107 + 0.001*SL	0.112 + 0.001*SL
	t_{PHL}	0.099	0.096 + 0.002*SL	0.099 + 0.001*SL	0.107 + 0.001*SL
B to Y	t_R	0.034	0.029 + 0.003*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.029 + 0.001*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.115	0.111 + 0.002*SL	0.113 + 0.001*SL	0.118 + 0.001*SL
	t_{PHL}	0.104	0.100 + 0.002*SL	0.103 + 0.001*SL	0.111 + 0.001*SL
C to Y	t_R	0.035	0.030 + 0.002*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.031	0.028 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.121	0.117 + 0.002*SL	0.119 + 0.001*SL	0.125 + 0.001*SL
	t_{PHL}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.114 + 0.001*SL
D to Y	t_R	0.035	0.030 + 0.003*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.126	0.122 + 0.002*SL	0.125 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.107	0.104 + 0.002*SL	0.107 + 0.001*SL	0.115 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nd5/nd5d2/nd5d4

5-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)														
nd5					*nd5d2*					*nd5d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.2	1.2	0.9	1.0	1.0	1.2	1.2	0.9	1.0	1.0	1.2	1.2
Gate Count														
nd5					*nd5d2*					*nd5d4*				
4.00					4.33					5.33				

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.022 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.040	0.023 + 0.009*SL	0.027 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.091	0.081 + 0.005*SL	0.083 + 0.004*SL	0.083 + 0.004*SL
	t_{PHL}	0.096	0.084 + 0.006*SL	0.090 + 0.004*SL	0.094 + 0.004*SL
B to Y	t_R	0.039	0.021 + 0.009*SL	0.017 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.040	0.023 + 0.008*SL	0.027 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.096	0.086 + 0.005*SL	0.088 + 0.005*SL	0.089 + 0.004*SL
	t_{PHL}	0.098	0.087 + 0.006*SL	0.092 + 0.004*SL	0.096 + 0.004*SL
C to Y	t_R	0.039	0.020 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.040	0.024 + 0.008*SL	0.026 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.100	0.090 + 0.005*SL	0.092 + 0.004*SL	0.092 + 0.004*SL
	t_{PHL}	0.098	0.087 + 0.006*SL	0.092 + 0.004*SL	0.097 + 0.004*SL
D to Y	t_R	0.040	0.022 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.040	0.024 + 0.008*SL	0.026 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.081	0.071 + 0.005*SL	0.073 + 0.005*SL	0.074 + 0.004*SL
	t_{PHL}	0.093	0.082 + 0.006*SL	0.087 + 0.004*SL	0.092 + 0.004*SL
E to Y	t_R	0.039	0.020 + 0.009*SL	0.017 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.040	0.023 + 0.008*SL	0.026 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.085	0.075 + 0.005*SL	0.077 + 0.005*SL	0.078 + 0.004*SL
	t_{PHL}	0.094	0.083 + 0.006*SL	0.088 + 0.004*SL	0.092 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.023 + 0.005*SL	0.022 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.026 + 0.005*SL	0.030 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.092	0.086 + 0.003*SL	0.089 + 0.002*SL	0.091 + 0.002*SL
	t_{PHL}	0.100	0.093 + 0.004*SL	0.098 + 0.002*SL	0.108 + 0.002*SL
B to Y	t_R	0.032	0.022 + 0.005*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.097	0.091 + 0.003*SL	0.094 + 0.002*SL	0.096 + 0.002*SL
	t_{PHL}	0.102	0.095 + 0.004*SL	0.100 + 0.002*SL	0.110 + 0.002*SL
C to Y	t_R	0.033	0.023 + 0.005*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.028 + 0.004*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.101	0.095 + 0.003*SL	0.098 + 0.002*SL	0.100 + 0.002*SL
	t_{PHL}	0.103	0.096 + 0.004*SL	0.101 + 0.002*SL	0.111 + 0.002*SL
D to Y	t_R	0.039	0.027 + 0.006*SL	0.031 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.036	0.027 + 0.004*SL	0.029 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.081	0.075 + 0.003*SL	0.077 + 0.002*SL	0.080 + 0.002*SL
	t_{PHL}	0.098	0.091 + 0.004*SL	0.096 + 0.002*SL	0.106 + 0.002*SL
E to Y	t_R	0.033	0.023 + 0.005*SL	0.023 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.028 + 0.004*SL	0.029 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.086	0.080 + 0.003*SL	0.083 + 0.002*SL	0.085 + 0.002*SL
	t_{PHL}	0.099	0.092 + 0.004*SL	0.097 + 0.002*SL	0.107 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

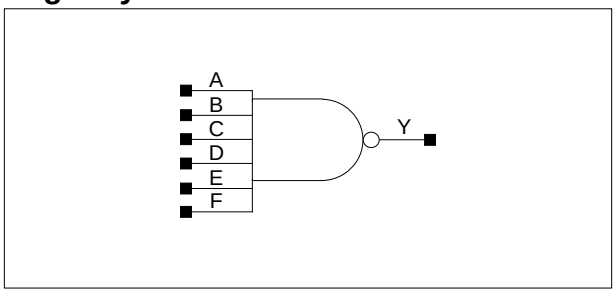
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd5d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.024 + 0.002*SL	0.024 + 0.002*SL	0.015 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.102 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.110 + 0.001*SL
B to Y	t_R	0.031	0.026 + 0.003*SL	0.026 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.029 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.105	0.102 + 0.002*SL	0.104 + 0.001*SL	0.108 + 0.001*SL
	t_{PHL}	0.102	0.099 + 0.002*SL	0.101 + 0.001*SL	0.113 + 0.001*SL
C to Y	t_R	0.031	0.026 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.031	0.028 + 0.002*SL	0.027 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.108 + 0.001*SL	0.112 + 0.001*SL
	t_{PHL}	0.102	0.099 + 0.002*SL	0.102 + 0.001*SL	0.113 + 0.001*SL
D to Y	t_R	0.031	0.026 + 0.002*SL	0.026 + 0.002*SL	0.015 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.027 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.089	0.086 + 0.002*SL	0.088 + 0.001*SL	0.092 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.110 + 0.001*SL
E to Y	t_R	0.029	0.025 + 0.002*SL	0.024 + 0.002*SL	0.015 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.093	0.089 + 0.002*SL	0.091 + 0.001*SL	0.096 + 0.001*SL
	t_{PHL}	0.099	0.096 + 0.002*SL	0.099 + 0.001*SL	0.110 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	1	1	1	0
Other States						1

Cell Data

Input Load (SL)																	
nd6						*nd6d2*						*nd6d4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.9	1.0	1.0	0.9	1.0	1.0	1.0	1.0	1.0

Gate Count		
nd6	*nd6d2*	*nd6d4*
4.33	4.67	6.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.042	0.026 + 0.008*SL	0.018 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.039	0.022 + 0.009*SL	0.026 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.088	0.078 + 0.005*SL	0.080 + 0.004*SL	0.080 + 0.004*SL
	t_{PHL}	0.093	0.082 + 0.006*SL	0.087 + 0.004*SL	0.091 + 0.004*SL
B to Y	t_R	0.044	0.029 + 0.008*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.039	0.021 + 0.009*SL	0.026 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.092	0.082 + 0.005*SL	0.084 + 0.004*SL	0.084 + 0.004*SL
	t_{PHL}	0.096	0.085 + 0.006*SL	0.090 + 0.004*SL	0.094 + 0.004*SL
C to Y	t_R	0.039	0.021 + 0.009*SL	0.016 + 0.010*SL	0.012 + 0.010*SL
	t_F	0.039	0.022 + 0.008*SL	0.025 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.098	0.088 + 0.005*SL	0.090 + 0.005*SL	0.091 + 0.004*SL
	t_{PHL}	0.096	0.085 + 0.006*SL	0.090 + 0.004*SL	0.094 + 0.004*SL
D to Y	t_R	0.040	0.022 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.026 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.096	0.086 + 0.005*SL	0.088 + 0.005*SL	0.089 + 0.004*SL
	t_{PHL}	0.102	0.091 + 0.006*SL	0.096 + 0.004*SL	0.101 + 0.004*SL
E to Y	t_R	0.040	0.022 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.039	0.022 + 0.008*SL	0.025 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.101	0.091 + 0.005*SL	0.094 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.105	0.093 + 0.006*SL	0.099 + 0.004*SL	0.103 + 0.004*SL
F to Y	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.024 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.105	0.095 + 0.005*SL	0.097 + 0.005*SL	0.098 + 0.004*SL
	t_{PHL}	0.105	0.093 + 0.006*SL	0.099 + 0.004*SL	0.103 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd6d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.022 + 0.005*SL	0.022 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.026 + 0.005*SL	0.030 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.091	0.085 + 0.003*SL	0.088 + 0.002*SL	0.090 + 0.002*SL
	t_{PHL}	0.098	0.091 + 0.004*SL	0.096 + 0.002*SL	0.106 + 0.002*SL
B to Y	t_R	0.032	0.023 + 0.005*SL	0.022 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.027 + 0.004*SL	0.030 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.101	0.094 + 0.004*SL	0.099 + 0.002*SL	0.109 + 0.002*SL
C to Y	t_R	0.032	0.022 + 0.005*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.036	0.027 + 0.004*SL	0.030 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.100	0.094 + 0.003*SL	0.097 + 0.002*SL	0.099 + 0.002*SL
	t_{PHL}	0.102	0.095 + 0.004*SL	0.099 + 0.002*SL	0.109 + 0.002*SL
D to Y	t_R	0.034	0.024 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.030 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.106	0.099 + 0.004*SL	0.104 + 0.002*SL	0.114 + 0.002*SL
E to Y	t_R	0.034	0.024 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.031 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.101	0.095 + 0.003*SL	0.098 + 0.002*SL	0.100 + 0.002*SL
	t_{PHL}	0.108	0.101 + 0.004*SL	0.106 + 0.002*SL	0.116 + 0.002*SL
F to Y	t_R	0.034	0.024 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.037	0.028 + 0.004*SL	0.030 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.105	0.099 + 0.003*SL	0.102 + 0.002*SL	0.104 + 0.002*SL
	t_{PHL}	0.109	0.102 + 0.004*SL	0.107 + 0.002*SL	0.117 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Switching Characteristics

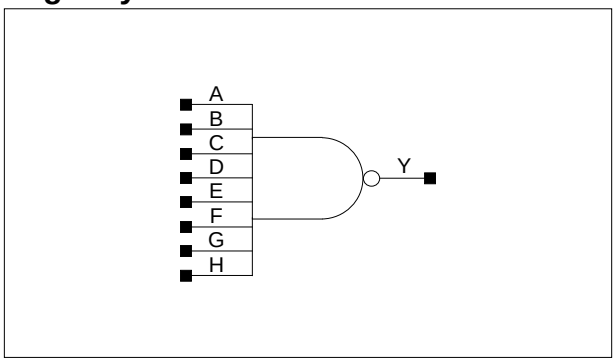
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd6d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.023 + 0.003*SL	0.024 + 0.002*SL	0.014 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.100	0.097 + 0.002*SL	0.099 + 0.001*SL	0.103 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.111 + 0.001*SL
B to Y	t_R	0.030	0.025 + 0.003*SL	0.026 + 0.002*SL	0.015 + 0.003*SL
	t_F	0.031	0.026 + 0.003*SL	0.028 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.105	0.102 + 0.002*SL	0.104 + 0.001*SL	0.108 + 0.001*SL
	t_{PHL}	0.103	0.099 + 0.002*SL	0.102 + 0.001*SL	0.113 + 0.001*SL
C to Y	t_R	0.031	0.026 + 0.002*SL	0.026 + 0.002*SL	0.014 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.027 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.113 + 0.001*SL
	t_{PHL}	0.103	0.099 + 0.002*SL	0.102 + 0.001*SL	0.113 + 0.001*SL
D to Y	t_R	0.031	0.026 + 0.003*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.109	0.106 + 0.002*SL	0.109 + 0.001*SL	0.120 + 0.001*SL
E to Y	t_R	0.033	0.027 + 0.003*SL	0.028 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.112	0.108 + 0.002*SL	0.111 + 0.001*SL	0.122 + 0.001*SL
F to Y	t_R	0.032	0.027 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.028 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.116	0.112 + 0.002*SL	0.115 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.112	0.108 + 0.002*SL	0.111 + 0.001*SL	0.123 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	1	1	1	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
nd8								*nd8*
A	B	C	D	E	F	G	H	
0.8	0.9	0.9	0.9	0.9	0.9	0.9	0.9	5.00
nd8d2								*nd8d2*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	5.33
nd8d4								*nd8d4*
A	B	C	D	E	F	G	H	
0.8	0.9	0.9	0.9	0.8	0.9	0.9	0.9	6.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.022 + 0.015*SL	0.017 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.022 + 0.011*SL	0.023 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.104	0.090 + 0.007*SL	0.091 + 0.007*SL	0.091 + 0.007*SL
	t_{PHL}	0.100	0.087 + 0.007*SL	0.092 + 0.006*SL	0.095 + 0.005*SL
B to Y	t_R	0.052	0.022 + 0.015*SL	0.018 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.044	0.024 + 0.010*SL	0.023 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.111	0.096 + 0.007*SL	0.097 + 0.007*SL	0.097 + 0.007*SL
	t_{PHL}	0.104	0.090 + 0.007*SL	0.096 + 0.006*SL	0.099 + 0.005*SL
C to Y	t_R	0.052	0.022 + 0.015*SL	0.018 + 0.016*SL	0.013 + 0.016*SL
	t_F	0.044	0.023 + 0.011*SL	0.023 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.117	0.102 + 0.007*SL	0.103 + 0.007*SL	0.103 + 0.007*SL
	t_{PHL}	0.107	0.094 + 0.007*SL	0.099 + 0.006*SL	0.102 + 0.005*SL
D to Y	t_R	0.053	0.023 + 0.015*SL	0.019 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.022 + 0.010*SL	0.022 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.121	0.107 + 0.007*SL	0.108 + 0.007*SL	0.108 + 0.007*SL
	t_{PHL}	0.108	0.095 + 0.007*SL	0.100 + 0.006*SL	0.102 + 0.005*SL
E to Y	t_R	0.052	0.023 + 0.015*SL	0.018 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.022 + 0.010*SL	0.022 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.108	0.093 + 0.007*SL	0.095 + 0.007*SL	0.095 + 0.007*SL
	t_{PHL}	0.106	0.092 + 0.007*SL	0.097 + 0.006*SL	0.100 + 0.005*SL
F to Y	t_R	0.053	0.023 + 0.015*SL	0.019 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.023 + 0.010*SL	0.022 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.115	0.100 + 0.007*SL	0.101 + 0.007*SL	0.102 + 0.007*SL
	t_{PHL}	0.110	0.096 + 0.007*SL	0.102 + 0.006*SL	0.104 + 0.005*SL
G to Y	t_R	0.052	0.023 + 0.015*SL	0.018 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.023 + 0.010*SL	0.022 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.120	0.105 + 0.007*SL	0.107 + 0.007*SL	0.107 + 0.007*SL
	t_{PHL}	0.113	0.099 + 0.007*SL	0.104 + 0.006*SL	0.107 + 0.005*SL
H to Y	t_R	0.053	0.023 + 0.015*SL	0.019 + 0.016*SL	0.014 + 0.016*SL
	t_F	0.043	0.022 + 0.010*SL	0.022 + 0.010*SL	0.016 + 0.011*SL
	t_{PLH}	0.126	0.111 + 0.007*SL	0.113 + 0.007*SL	0.113 + 0.007*SL
	t_{PHL}	0.115	0.101 + 0.007*SL	0.106 + 0.006*SL	0.109 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd8d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.024 + 0.005*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.038	0.030 + 0.004*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.104	0.098 + 0.003*SL	0.101 + 0.002*SL	0.103 + 0.002*SL
	t_{PHL}	0.108	0.101 + 0.004*SL	0.106 + 0.002*SL	0.116 + 0.002*SL
B to Y	t_R	0.033	0.024 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.110	0.104 + 0.003*SL	0.107 + 0.002*SL	0.109 + 0.002*SL
	t_{PHL}	0.112	0.105 + 0.004*SL	0.110 + 0.002*SL	0.120 + 0.002*SL
C to Y	t_R	0.034	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.027 + 0.004*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.116	0.110 + 0.003*SL	0.113 + 0.002*SL	0.115 + 0.002*SL
	t_{PHL}	0.115	0.108 + 0.004*SL	0.113 + 0.002*SL	0.123 + 0.002*SL
D to Y	t_R	0.034	0.025 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.037	0.028 + 0.005*SL	0.031 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.121	0.115 + 0.003*SL	0.118 + 0.002*SL	0.121 + 0.002*SL
	t_{PHL}	0.116	0.109 + 0.004*SL	0.114 + 0.002*SL	0.124 + 0.002*SL
E to Y	t_R	0.033	0.024 + 0.005*SL	0.022 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.029 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.107	0.100 + 0.003*SL	0.104 + 0.002*SL	0.106 + 0.002*SL
	t_{PHL}	0.113	0.105 + 0.004*SL	0.110 + 0.002*SL	0.121 + 0.002*SL
F to Y	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.037	0.028 + 0.005*SL	0.032 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.114	0.107 + 0.003*SL	0.111 + 0.002*SL	0.113 + 0.002*SL
	t_{PHL}	0.118	0.111 + 0.004*SL	0.116 + 0.002*SL	0.126 + 0.002*SL
G to Y	t_R	0.035	0.026 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.036	0.027 + 0.004*SL	0.030 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.119	0.113 + 0.003*SL	0.116 + 0.002*SL	0.119 + 0.002*SL
	t_{PHL}	0.120	0.113 + 0.004*SL	0.118 + 0.002*SL	0.128 + 0.002*SL
H to Y	t_R	0.035	0.026 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.037	0.028 + 0.005*SL	0.032 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.125	0.118 + 0.003*SL	0.122 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.121	0.114 + 0.004*SL	0.119 + 0.002*SL	0.129 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

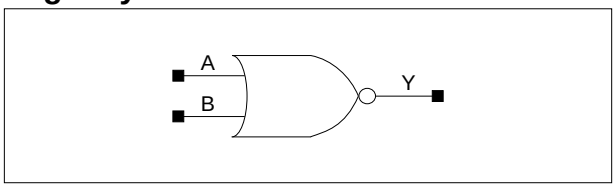
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nd8d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.034	0.031 + 0.002*SL	0.030 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.114	0.111 + 0.002*SL	0.113 + 0.001*SL	0.117 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.120 + 0.001*SL
B to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.029 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.121	0.118 + 0.002*SL	0.120 + 0.001*SL	0.124 + 0.001*SL
	t_{PHL}	0.115	0.111 + 0.002*SL	0.114 + 0.001*SL	0.125 + 0.001*SL
C to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.035	0.030 + 0.002*SL	0.032 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.127	0.123 + 0.002*SL	0.126 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.117	0.113 + 0.002*SL	0.116 + 0.001*SL	0.127 + 0.001*SL
D to Y	t_R	0.033	0.029 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.030 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.132	0.128 + 0.002*SL	0.131 + 0.001*SL	0.135 + 0.001*SL
	t_{PHL}	0.118	0.115 + 0.002*SL	0.117 + 0.001*SL	0.129 + 0.001*SL
E to Y	t_R	0.034	0.028 + 0.003*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.120	0.117 + 0.002*SL	0.119 + 0.001*SL	0.123 + 0.001*SL
	t_{PHL}	0.119	0.115 + 0.002*SL	0.118 + 0.001*SL	0.130 + 0.001*SL
F to Y	t_R	0.035	0.030 + 0.003*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.126	0.123 + 0.002*SL	0.125 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.123	0.119 + 0.002*SL	0.122 + 0.001*SL	0.133 + 0.001*SL
G to Y	t_R	0.035	0.030 + 0.002*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.132	0.129 + 0.002*SL	0.131 + 0.001*SL	0.136 + 0.001*SL
	t_{PHL}	0.125	0.121 + 0.002*SL	0.124 + 0.001*SL	0.136 + 0.001*SL
H to Y	t_R	0.034	0.030 + 0.002*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.035	0.032 + 0.001*SL	0.029 + 0.002*SL	0.030 + 0.002*SL
	t_{PLH}	0.137	0.133 + 0.002*SL	0.136 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.124	0.120 + 0.002*SL	0.123 + 0.001*SL	0.132 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)									
nr2		*nr2a*		*nr2d2*		*nr2d4*		*nr2d8*	
A	B	A	B	A	B	A	B	A	B
1.0	1.1	1.6	1.9	2.0	2.3	4.2	4.5	1.1	1.2

Gate Count				
nr2	*nr2a*	*nr2d2*	*nr2d4*	*nr2d8*
1.33	1.67	2.00	3.67	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.084	0.048 + 0.018*SL	0.040 + 0.020*SL	0.028 + 0.020*SL
	t_F	0.043	0.029 + 0.007*SL	0.029 + 0.007*SL	0.016 + 0.008*SL
	t_{PLH}	0.050	0.031 + 0.009*SL	0.033 + 0.009*SL	0.032 + 0.009*SL
	t_{PHL}	0.030	0.018 + 0.006*SL	0.026 + 0.004*SL	0.028 + 0.004*SL
B to Y	t_R	0.078	0.041 + 0.018*SL	0.034 + 0.020*SL	0.028 + 0.020*SL
	t_F	0.050	0.039 + 0.005*SL	0.033 + 0.007*SL	0.022 + 0.007*SL
	t_{PLH}	0.053	0.034 + 0.009*SL	0.036 + 0.009*SL	0.036 + 0.009*SL
	t_{PHL}	0.034	0.023 + 0.005*SL	0.029 + 0.004*SL	0.030 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nr2a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.061	0.045 + 0.008*SL	0.040 + 0.009*SL	0.028 + 0.010*SL
	t_F	0.047	0.032 + 0.007*SL	0.031 + 0.007*SL	0.018 + 0.008*SL
	t_{PLH}	0.033	0.021 + 0.006*SL	0.027 + 0.005*SL	0.028 + 0.004*SL
	t_{PHL}	0.036	0.025 + 0.006*SL	0.031 + 0.004*SL	0.032 + 0.004*SL
B to Y	t_R	0.054	0.037 + 0.009*SL	0.032 + 0.010*SL	0.025 + 0.010*SL
	t_F	0.056	0.040 + 0.008*SL	0.041 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.039	0.028 + 0.005*SL	0.032 + 0.005*SL	0.033 + 0.005*SL
	t_{PHL}	0.045	0.035 + 0.005*SL	0.038 + 0.004*SL	0.039 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.050 + 0.008*SL	0.042 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.036	0.030 + 0.003*SL	0.029 + 0.003*SL	0.017 + 0.004*SL
	t_{PLH}	0.038	0.027 + 0.006*SL	0.032 + 0.004*SL	0.031 + 0.005*SL
	t_{PHL}	0.023	0.015 + 0.004*SL	0.022 + 0.002*SL	0.027 + 0.002*SL
B to Y	t_R	0.057	0.040 + 0.008*SL	0.034 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.042	0.037 + 0.003*SL	0.034 + 0.003*SL	0.023 + 0.004*SL
	t_{PLH}	0.043	0.032 + 0.005*SL	0.035 + 0.005*SL	0.036 + 0.005*SL
	t_{PHL}	0.028	0.021 + 0.003*SL	0.026 + 0.002*SL	0.030 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nr2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.051 + 0.003*SL	0.045 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.033	0.030 + 0.001*SL	0.029 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.033	0.027 + 0.003*SL	0.030 + 0.002*SL	0.031 + 0.002*SL
	t_{PHL}	0.019	0.015 + 0.002*SL	0.019 + 0.001*SL	0.027 + 0.001*SL
B to Y	t_R	0.050	0.041 + 0.004*SL	0.038 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.040	0.036 + 0.002*SL	0.037 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.038	0.032 + 0.003*SL	0.034 + 0.002*SL	0.036 + 0.002*SL
	t_{PHL}	0.024	0.021 + 0.002*SL	0.024 + 0.001*SL	0.030 + 0.001*SL

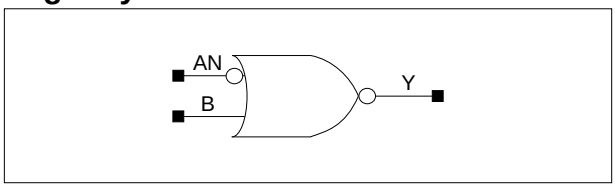
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr2d8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.031 + 0.001*SL	0.029 + 0.001*SL	0.019 + 0.001*SL
	t_F	0.027	0.025 + 0.001*SL	0.025 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.109	0.107 + 0.001*SL	0.108 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.076	0.074 + 0.001*SL	0.075 + 0.001*SL	0.084 + 0.001*SL
B to Y	t_R	0.034	0.031 + 0.001*SL	0.032 + 0.001*SL	0.019 + 0.001*SL
	t_F	0.027	0.025 + 0.001*SL	0.025 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.113	0.111 + 0.001*SL	0.112 + 0.001*SL	0.118 + 0.001*SL
	t_{PHL}	0.080	0.078 + 0.001*SL	0.080 + 0.001*SL	0.089 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

AN	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

Cell Data

Input Load (SL)							
nr2b		*nr2bd2*		*nr2bd4*		*nr2bd8*	
AN	B	AN	B	AN	B	AN	B
0.7	1.1	0.7	2.2	0.7	4.6	0.7	1.2

Gate Count			
nr2b	*nr2bd2*	*nr2bd4*	*nr2bd8*
1.67	2.67	4.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr2b

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.073	0.034 + 0.020*SL	0.031 + 0.020*SL	0.029 + 0.020*SL
	t_F	0.038	0.023 + 0.007*SL	0.024 + 0.007*SL	0.019 + 0.008*SL
	t_{PLH}	0.063	0.045 + 0.009*SL	0.046 + 0.009*SL	0.046 + 0.009*SL
	t_{PHL}	0.067	0.057 + 0.005*SL	0.061 + 0.004*SL	0.064 + 0.004*SL
B to Y	t_R	0.079	0.042 + 0.019*SL	0.036 + 0.020*SL	0.029 + 0.020*SL
	t_F	0.050	0.039 + 0.005*SL	0.033 + 0.007*SL	0.022 + 0.007*SL
	t_{PLH}	0.053	0.034 + 0.010*SL	0.036 + 0.009*SL	0.037 + 0.009*SL
	t_{PHL}	0.033	0.022 + 0.005*SL	0.028 + 0.004*SL	0.030 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nr2bd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.055	0.036 + 0.009*SL	0.034 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.040	0.033 + 0.004*SL	0.033 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.062	0.053 + 0.005*SL	0.054 + 0.005*SL	0.054 + 0.005*SL
	t_{PHL}	0.075	0.069 + 0.003*SL	0.073 + 0.002*SL	0.081 + 0.002*SL
B to Y	t_R	0.059	0.041 + 0.009*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.043	0.037 + 0.003*SL	0.035 + 0.003*SL	0.023 + 0.004*SL
	t_{PLH}	0.044	0.033 + 0.005*SL	0.036 + 0.005*SL	0.037 + 0.005*SL
	t_{PHL}	0.027	0.020 + 0.003*SL	0.025 + 0.002*SL	0.030 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr2bd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.052	0.045 + 0.004*SL	0.039 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.053	0.049 + 0.002*SL	0.050 + 0.002*SL	0.046 + 0.002*SL
	t_{PLH}	0.075	0.069 + 0.003*SL	0.071 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.102	0.098 + 0.002*SL	0.101 + 0.001*SL	0.118 + 0.001*SL
B to Y	t_R	0.053	0.045 + 0.004*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.040	0.037 + 0.002*SL	0.038 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.039	0.033 + 0.003*SL	0.036 + 0.002*SL	0.039 + 0.002*SL
	t_{PHL}	0.023	0.020 + 0.002*SL	0.023 + 0.001*SL	0.030 + 0.001*SL

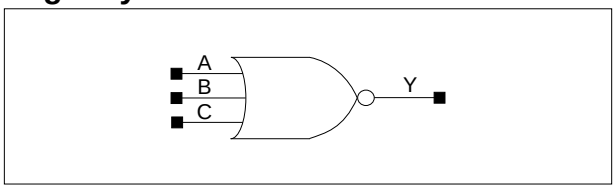
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr2bd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.033	0.030 + 0.001*SL	0.032 + 0.001*SL	0.019 + 0.001*SL
	t_F	0.026	0.024 + 0.001*SL	0.025 + 0.001*SL	0.019 + 0.001*SL
	t_{PLH}	0.123	0.121 + 0.001*SL	0.122 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.114	0.112 + 0.001*SL	0.114 + 0.001*SL	0.123 + 0.001*SL
B to Y	t_R	0.034	0.031 + 0.001*SL	0.032 + 0.001*SL	0.019 + 0.001*SL
	t_F	0.026	0.024 + 0.001*SL	0.024 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.114	0.112 + 0.001*SL	0.114 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.080	0.079 + 0.001*SL	0.080 + 0.001*SL	0.089 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
Other States			0

Cell Data

Input Load (SL)											
nr3			*nr3a*			*nr3d2*			*nr3d4*		
A	B	C	A	B	C	A	B	C	A	B	C
0.9	1.0	1.0	1.6	1.8	1.9	1.8	2.0	2.2	1.0	1.0	1.0

Gate Count			
nr3	*nr3a*	*nr3d2*	*nr3d4*
1.67	2.33	3.00	3.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.060 + 0.028*SL	0.051 + 0.030*SL	0.045 + 0.031*SL
	t_F	0.054	0.032 + 0.011*SL	0.027 + 0.012*SL	0.014 + 0.013*SL
	t_{PLH}	0.060	0.033 + 0.014*SL	0.033 + 0.014*SL	0.033 + 0.014*SL
	t_{PHL}	0.042	0.027 + 0.008*SL	0.032 + 0.007*SL	0.032 + 0.007*SL
B to Y	t_R	0.113	0.056 + 0.029*SL	0.049 + 0.030*SL	0.045 + 0.031*SL
	t_F	0.063	0.040 + 0.011*SL	0.036 + 0.012*SL	0.023 + 0.013*SL
	t_{PLH}	0.072	0.044 + 0.014*SL	0.045 + 0.014*SL	0.046 + 0.014*SL
	t_{PHL}	0.049	0.034 + 0.007*SL	0.037 + 0.007*SL	0.037 + 0.007*SL
C to Y	t_R	0.109	0.050 + 0.029*SL	0.046 + 0.030*SL	0.045 + 0.031*SL
	t_F	0.069	0.045 + 0.012*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_{PLH}	0.076	0.049 + 0.014*SL	0.049 + 0.014*SL	0.049 + 0.014*SL
	t_{PHL}	0.051	0.037 + 0.007*SL	0.039 + 0.007*SL	0.041 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nr3a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.086	0.061 + 0.013*SL	0.053 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.054	0.038 + 0.008*SL	0.031 + 0.010*SL	0.020 + 0.011*SL
	t_{PLH}	0.042	0.027 + 0.007*SL	0.030 + 0.007*SL	0.030 + 0.007*SL
	t_{PHL}	0.044	0.031 + 0.006*SL	0.035 + 0.005*SL	0.036 + 0.005*SL
B to Y	t_R	0.079	0.052 + 0.014*SL	0.047 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.066	0.047 + 0.009*SL	0.044 + 0.010*SL	0.034 + 0.011*SL
	t_{PLH}	0.055	0.040 + 0.007*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.054	0.043 + 0.006*SL	0.044 + 0.005*SL	0.045 + 0.005*SL
C to Y	t_R	0.076	0.047 + 0.015*SL	0.046 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.079	0.062 + 0.008*SL	0.055 + 0.010*SL	0.047 + 0.011*SL
	t_{PLH}	0.060	0.046 + 0.007*SL	0.047 + 0.007*SL	0.048 + 0.007*SL
	t_{PHL}	0.060	0.048 + 0.006*SL	0.050 + 0.006*SL	0.053 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.061 + 0.013*SL	0.052 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.042	0.031 + 0.005*SL	0.028 + 0.006*SL	0.014 + 0.006*SL
	t_{PLH}	0.044	0.030 + 0.007*SL	0.032 + 0.007*SL	0.031 + 0.007*SL
	t_{PHL}	0.033	0.023 + 0.005*SL	0.029 + 0.003*SL	0.031 + 0.003*SL
B to Y	t_R	0.082	0.055 + 0.014*SL	0.049 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.050	0.038 + 0.006*SL	0.038 + 0.006*SL	0.023 + 0.006*SL
	t_{PLH}	0.056	0.042 + 0.007*SL	0.043 + 0.007*SL	0.044 + 0.007*SL
	t_{PHL}	0.040	0.032 + 0.004*SL	0.035 + 0.003*SL	0.037 + 0.003*SL
C to Y	t_R	0.077	0.048 + 0.015*SL	0.046 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.057	0.043 + 0.007*SL	0.047 + 0.006*SL	0.031 + 0.006*SL
	t_{PLH}	0.062	0.047 + 0.007*SL	0.049 + 0.007*SL	0.050 + 0.007*SL
	t_{PHL}	0.044	0.035 + 0.004*SL	0.039 + 0.003*SL	0.041 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nr3d4

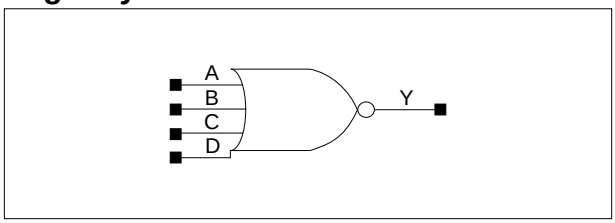
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.003*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.023 + 0.002*SL	0.025 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.088	0.084 + 0.002*SL	0.087 + 0.001*SL	0.095 + 0.001*SL
B to Y	t_R	0.033	0.029 + 0.002*SL	0.027 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.122	0.119 + 0.002*SL	0.121 + 0.001*SL	0.126 + 0.001*SL
	t_{PHL}	0.094	0.090 + 0.002*SL	0.093 + 0.001*SL	0.101 + 0.001*SL
C to Y	t_R	0.034	0.029 + 0.002*SL	0.028 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.127	0.123 + 0.002*SL	0.126 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.106 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr4/nr4d2/nr4d4

4-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
Other States				0

Cell Data

Input Load (SL)											
nr4				*nr4d2*				*nr4d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.2	1.2	1.2	1.1	1.2	1.1	1.2	1.1	1.2	1.1	1.2

Gate Count		
nr4	*nr4d2*	*nr4d4*
3.33	3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.024 + 0.009*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.022 + 0.008*SL	0.022 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.097	0.086 + 0.005*SL	0.089 + 0.005*SL	0.091 + 0.004*SL
	t_{PHL}	0.076	0.065 + 0.005*SL	0.070 + 0.004*SL	0.072 + 0.004*SL
B to Y	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.038	0.021 + 0.008*SL	0.023 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.100	0.089 + 0.005*SL	0.092 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.080	0.070 + 0.005*SL	0.074 + 0.004*SL	0.077 + 0.004*SL
C to Y	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.023 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.096	0.085 + 0.005*SL	0.088 + 0.005*SL	0.090 + 0.004*SL
	t_{PHL}	0.078	0.067 + 0.005*SL	0.072 + 0.004*SL	0.075 + 0.004*SL
D to Y	t_R	0.043	0.024 + 0.009*SL	0.021 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.038	0.021 + 0.008*SL	0.025 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.100	0.089 + 0.005*SL	0.092 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.083	0.072 + 0.005*SL	0.077 + 0.004*SL	0.080 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.024 + 0.005*SL	0.024 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.026	0.018 + 0.004*SL	0.019 + 0.004*SL	0.012 + 0.004*SL
	t_{PLH}	0.095	0.088 + 0.003*SL	0.092 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.066	0.060 + 0.003*SL	0.063 + 0.002*SL	0.067 + 0.002*SL
B to Y	t_R	0.033	0.024 + 0.005*SL	0.024 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.026	0.017 + 0.004*SL	0.018 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.098	0.092 + 0.003*SL	0.095 + 0.002*SL	0.098 + 0.002*SL
	t_{PHL}	0.071	0.065 + 0.003*SL	0.068 + 0.002*SL	0.072 + 0.002*SL
C to Y	t_R	0.032	0.022 + 0.005*SL	0.022 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.095	0.089 + 0.003*SL	0.092 + 0.002*SL	0.096 + 0.002*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.066 + 0.002*SL	0.070 + 0.002*SL
D to Y	t_R	0.033	0.023 + 0.005*SL	0.024 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.018 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.100	0.093 + 0.003*SL	0.097 + 0.002*SL	0.100 + 0.002*SL
	t_{PHL}	0.073	0.067 + 0.003*SL	0.071 + 0.002*SL	0.075 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nr4d4

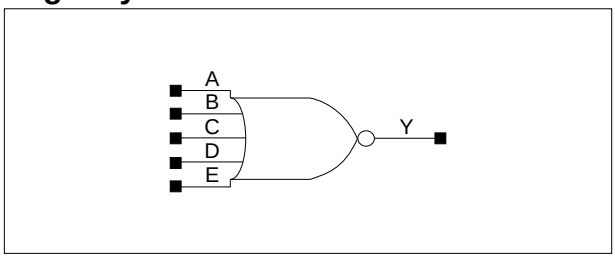
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.031 + 0.003*SL	0.032 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.105	0.101 + 0.002*SL	0.104 + 0.001*SL	0.112 + 0.001*SL
	t_{PHL}	0.075	0.071 + 0.002*SL	0.074 + 0.001*SL	0.083 + 0.001*SL
B to Y	t_R	0.037	0.031 + 0.003*SL	0.033 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.029	0.026 + 0.002*SL	0.025 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.108	0.105 + 0.002*SL	0.107 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.080	0.076 + 0.002*SL	0.079 + 0.001*SL	0.088 + 0.001*SL
C to Y	t_R	0.037	0.031 + 0.003*SL	0.033 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.108	0.105 + 0.002*SL	0.107 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.079	0.075 + 0.002*SL	0.078 + 0.001*SL	0.088 + 0.001*SL
D to Y	t_R	0.037	0.032 + 0.003*SL	0.034 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.112	0.108 + 0.002*SL	0.111 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.083	0.080 + 0.002*SL	0.083 + 0.001*SL	0.092 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr5/nr5d2/nr5d4

5-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
Other States					0

Cell Data

Input Load (SL)														
nr5					*nr5d2*					*nr5d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.1	1.2	1.0	1.0	1.0	1.1	1.2	0.9	1.0	1.0	1.1	1.2
Gate Count														
nr5					*nr5d2*					*nr5d4*				
4.00					4.33					5.00				

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.028 + 0.009*SL	0.025 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.022 + 0.008*SL	0.021 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.108	0.097 + 0.005*SL	0.101 + 0.005*SL	0.103 + 0.004*SL
	t_{PHL}	0.088	0.077 + 0.005*SL	0.082 + 0.004*SL	0.084 + 0.004*SL
B to Y	t_R	0.046	0.028 + 0.009*SL	0.024 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.021 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.119	0.108 + 0.005*SL	0.112 + 0.005*SL	0.113 + 0.004*SL
	t_{PHL}	0.094	0.084 + 0.005*SL	0.088 + 0.004*SL	0.091 + 0.004*SL
C to Y	t_R	0.046	0.028 + 0.009*SL	0.024 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.123	0.112 + 0.005*SL	0.116 + 0.005*SL	0.117 + 0.004*SL
	t_{PHL}	0.098	0.087 + 0.005*SL	0.092 + 0.004*SL	0.095 + 0.004*SL
D to Y	t_R	0.042	0.023 + 0.010*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.022 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.096	0.085 + 0.005*SL	0.089 + 0.005*SL	0.090 + 0.004*SL
	t_{PHL}	0.077	0.066 + 0.005*SL	0.071 + 0.004*SL	0.074 + 0.004*SL
E to Y	t_R	0.043	0.025 + 0.009*SL	0.021 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.024 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.100	0.089 + 0.005*SL	0.092 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.082	0.071 + 0.005*SL	0.076 + 0.004*SL	0.079 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.027 + 0.005*SL	0.027 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.026	0.018 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.111	0.105 + 0.003*SL	0.108 + 0.002*SL	0.112 + 0.002*SL
	t_{PHL}	0.081	0.075 + 0.003*SL	0.078 + 0.002*SL	0.082 + 0.002*SL
B to Y	t_R	0.034	0.025 + 0.004*SL	0.023 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.025	0.017 + 0.004*SL	0.018 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.122	0.116 + 0.003*SL	0.119 + 0.002*SL	0.123 + 0.002*SL
	t_{PHL}	0.087	0.081 + 0.003*SL	0.084 + 0.002*SL	0.088 + 0.002*SL
C to Y	t_R	0.035	0.024 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.026	0.017 + 0.004*SL	0.019 + 0.004*SL	0.013 + 0.004*SL
	t_{PLH}	0.127	0.120 + 0.003*SL	0.124 + 0.002*SL	0.128 + 0.002*SL
	t_{PHL}	0.091	0.085 + 0.003*SL	0.088 + 0.002*SL	0.092 + 0.002*SL
D to Y	t_R	0.033	0.023 + 0.005*SL	0.023 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.026	0.017 + 0.005*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.095	0.088 + 0.003*SL	0.092 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.065 + 0.002*SL	0.070 + 0.002*SL
E to Y	t_R	0.033	0.024 + 0.005*SL	0.023 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.099	0.092 + 0.003*SL	0.096 + 0.002*SL	0.099 + 0.002*SL
	t_{PHL}	0.072	0.066 + 0.003*SL	0.070 + 0.002*SL	0.074 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr5d4

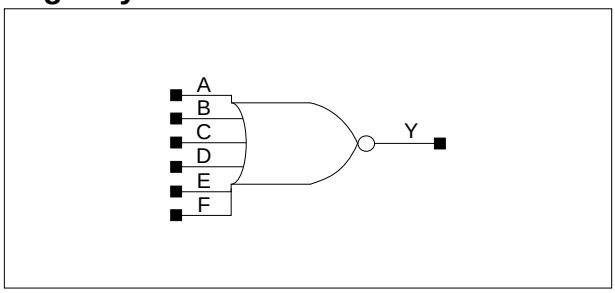
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.037 + 0.002*SL	0.036 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.123	0.119 + 0.002*SL	0.122 + 0.001*SL	0.131 + 0.001*SL
	t_{PHL}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.098 + 0.001*SL
B to Y	t_R	0.038	0.034 + 0.002*SL	0.034 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.135	0.131 + 0.002*SL	0.134 + 0.001*SL	0.143 + 0.001*SL
	t_{PHL}	0.096	0.093 + 0.002*SL	0.095 + 0.001*SL	0.105 + 0.001*SL
C to Y	t_R	0.038	0.033 + 0.002*SL	0.034 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.139	0.135 + 0.002*SL	0.138 + 0.001*SL	0.147 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.109 + 0.001*SL
D to Y	t_R	0.036	0.030 + 0.003*SL	0.032 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.026 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.107	0.103 + 0.002*SL	0.105 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.077	0.074 + 0.002*SL	0.077 + 0.001*SL	0.086 + 0.001*SL
E to Y	t_R	0.037	0.031 + 0.003*SL	0.033 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.111	0.107 + 0.002*SL	0.110 + 0.001*SL	0.118 + 0.001*SL
	t_{PHL}	0.082	0.078 + 0.002*SL	0.081 + 0.001*SL	0.091 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr6/nr6d2/nr6d4

6-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
nr6						*nr6d2*						*nr6d4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.9	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Gate Count		
nr6	*nr6d2*	*nr6d4*
4.33	4.67	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.027 + 0.009*SL	0.023 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.105	0.094 + 0.005*SL	0.098 + 0.005*SL	0.099 + 0.004*SL
	t_{PHL}	0.085	0.074 + 0.005*SL	0.078 + 0.004*SL	0.081 + 0.004*SL
B to Y	t_R	0.045	0.026 + 0.009*SL	0.024 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.116	0.105 + 0.005*SL	0.108 + 0.005*SL	0.110 + 0.004*SL
	t_{PHL}	0.091	0.081 + 0.005*SL	0.085 + 0.004*SL	0.087 + 0.004*SL
C to Y	t_R	0.044	0.027 + 0.009*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.040	0.019 + 0.011*SL	0.033 + 0.007*SL	0.019 + 0.008*SL
	t_{PLH}	0.120	0.109 + 0.005*SL	0.112 + 0.005*SL	0.114 + 0.004*SL
	t_{PHL}	0.094	0.085 + 0.005*SL	0.086 + 0.004*SL	0.090 + 0.004*SL
D to Y	t_R	0.043	0.025 + 0.009*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.023 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.109	0.099 + 0.005*SL	0.102 + 0.005*SL	0.104 + 0.004*SL
	t_{PHL}	0.090	0.080 + 0.005*SL	0.084 + 0.004*SL	0.087 + 0.004*SL
E to Y	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.020 + 0.008*SL	0.023 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.120	0.110 + 0.005*SL	0.113 + 0.005*SL	0.115 + 0.004*SL
	t_{PHL}	0.097	0.086 + 0.005*SL	0.091 + 0.004*SL	0.093 + 0.004*SL
F to Y	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.038	0.021 + 0.008*SL	0.024 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.124	0.113 + 0.005*SL	0.117 + 0.005*SL	0.121 + 0.004*SL
	t_{PHL}	0.101	0.090 + 0.005*SL	0.094 + 0.004*SL	0.097 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr6d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.027 + 0.005*SL	0.028 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.112	0.106 + 0.003*SL	0.110 + 0.002*SL	0.114 + 0.002*SL
	t_{PHL}	0.082	0.076 + 0.003*SL	0.079 + 0.002*SL	0.084 + 0.002*SL
B to Y	t_R	0.036	0.027 + 0.004*SL	0.025 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.026	0.017 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.123	0.116 + 0.003*SL	0.120 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.088	0.082 + 0.003*SL	0.085 + 0.002*SL	0.089 + 0.002*SL
C to Y	t_R	0.036	0.026 + 0.005*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.026	0.018 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.128 + 0.002*SL
	t_{PHL}	0.091	0.085 + 0.003*SL	0.089 + 0.002*SL	0.093 + 0.002*SL
D to Y	t_R	0.036	0.025 + 0.005*SL	0.026 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.026	0.018 + 0.004*SL	0.019 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.109	0.102 + 0.003*SL	0.106 + 0.002*SL	0.110 + 0.002*SL
	t_{PHL}	0.081	0.075 + 0.003*SL	0.079 + 0.002*SL	0.083 + 0.002*SL
E to Y	t_R	0.036	0.026 + 0.005*SL	0.026 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.027	0.020 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.120	0.113 + 0.003*SL	0.117 + 0.002*SL	0.121 + 0.002*SL
	t_{PHL}	0.088	0.081 + 0.003*SL	0.085 + 0.002*SL	0.090 + 0.002*SL
F to Y	t_R	0.035	0.025 + 0.005*SL	0.026 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.124	0.117 + 0.003*SL	0.121 + 0.002*SL	0.125 + 0.002*SL
	t_{PHL}	0.092	0.085 + 0.003*SL	0.089 + 0.002*SL	0.094 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr6d4

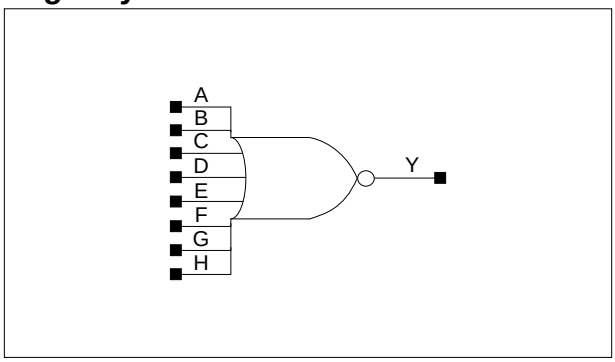
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.037 + 0.002*SL	0.037 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.026 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.098 + 0.001*SL
B to Y	t_R	0.042	0.037 + 0.002*SL	0.038 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.133	0.129 + 0.002*SL	0.131 + 0.001*SL	0.140 + 0.001*SL
	t_{PHL}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.104 + 0.001*SL
C to Y	t_R	0.042	0.037 + 0.003*SL	0.038 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.030	0.027 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.137	0.133 + 0.002*SL	0.136 + 0.001*SL	0.144 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.108 + 0.001*SL
D to Y	t_R	0.041	0.035 + 0.003*SL	0.037 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.092	0.088 + 0.002*SL	0.091 + 0.001*SL	0.101 + 0.001*SL
E to Y	t_R	0.040	0.035 + 0.002*SL	0.035 + 0.002*SL	0.024 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.133	0.129 + 0.002*SL	0.132 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.107 + 0.001*SL
F to Y	t_R	0.039	0.035 + 0.002*SL	0.035 + 0.002*SL	0.024 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.146 + 0.001*SL
	t_{PHL}	0.102	0.098 + 0.002*SL	0.101 + 0.001*SL	0.111 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

nr8/nr8d2/nr8d4

8-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
nr8								*nr8*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	0.9	1.0	1.0	1.1	1.2	5.33
nr8d2								*nr8d2*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	0.9	1.0	1.0	1.1	1.2	5.67
nr8d4								*nr8d4*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	0.9	1.0	1.0	1.1	1.2	6.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.033 + 0.009*SL	0.030 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.039	0.022 + 0.008*SL	0.025 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.122	0.110 + 0.006*SL	0.115 + 0.005*SL	0.118 + 0.004*SL
	t_{PHL}	0.091	0.080 + 0.005*SL	0.084 + 0.004*SL	0.087 + 0.004*SL
B to Y	t_R	0.050	0.032 + 0.009*SL	0.030 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.024 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.132	0.121 + 0.006*SL	0.126 + 0.005*SL	0.129 + 0.004*SL
	t_{PHL}	0.097	0.086 + 0.005*SL	0.091 + 0.004*SL	0.094 + 0.004*SL
C to Y	t_R	0.053	0.035 + 0.009*SL	0.031 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.039	0.022 + 0.008*SL	0.025 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.137	0.125 + 0.006*SL	0.130 + 0.005*SL	0.134 + 0.004*SL
	t_{PHL}	0.101	0.090 + 0.005*SL	0.095 + 0.004*SL	0.098 + 0.004*SL
D to Y	t_R	0.051	0.034 + 0.009*SL	0.029 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.039	0.022 + 0.009*SL	0.026 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.123	0.111 + 0.006*SL	0.116 + 0.005*SL	0.120 + 0.004*SL
	t_{PHL}	0.093	0.082 + 0.006*SL	0.087 + 0.004*SL	0.090 + 0.004*SL
E to Y	t_R	0.052	0.034 + 0.009*SL	0.031 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.040	0.024 + 0.008*SL	0.026 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.134	0.122 + 0.006*SL	0.127 + 0.005*SL	0.131 + 0.004*SL
	t_{PHL}	0.099	0.088 + 0.005*SL	0.093 + 0.004*SL	0.097 + 0.004*SL
F to Y	t_R	0.052	0.034 + 0.009*SL	0.030 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.040	0.024 + 0.008*SL	0.026 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.137	0.126 + 0.006*SL	0.131 + 0.005*SL	0.135 + 0.004*SL
	t_{PHL}	0.103	0.092 + 0.006*SL	0.097 + 0.004*SL	0.101 + 0.004*SL
G to Y	t_R	0.050	0.031 + 0.010*SL	0.030 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.041	0.026 + 0.008*SL	0.026 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.107 + 0.004*SL
	t_{PHL}	0.083	0.071 + 0.006*SL	0.077 + 0.004*SL	0.081 + 0.004*SL
H to Y	t_R	0.049	0.031 + 0.009*SL	0.028 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.041	0.024 + 0.008*SL	0.027 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.115	0.103 + 0.006*SL	0.108 + 0.005*SL	0.111 + 0.004*SL
	t_{PHL}	0.088	0.077 + 0.006*SL	0.082 + 0.004*SL	0.086 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr8d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.019 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.123	0.116 + 0.004*SL	0.120 + 0.002*SL	0.128 + 0.002*SL
	t_{PHL}	0.083	0.076 + 0.003*SL	0.080 + 0.002*SL	0.084 + 0.002*SL
B to Y	t_R	0.042	0.033 + 0.005*SL	0.033 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.134	0.127 + 0.004*SL	0.131 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.089	0.082 + 0.003*SL	0.086 + 0.002*SL	0.091 + 0.002*SL
C to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.138	0.131 + 0.004*SL	0.135 + 0.002*SL	0.143 + 0.002*SL
	t_{PHL}	0.092	0.086 + 0.003*SL	0.090 + 0.002*SL	0.095 + 0.002*SL
D to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.029	0.020 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.131	0.124 + 0.004*SL	0.129 + 0.002*SL	0.137 + 0.002*SL
	t_{PHL}	0.088	0.082 + 0.003*SL	0.086 + 0.002*SL	0.091 + 0.002*SL
E to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.142	0.135 + 0.004*SL	0.140 + 0.002*SL	0.148 + 0.002*SL
	t_{PHL}	0.094	0.088 + 0.003*SL	0.092 + 0.002*SL	0.098 + 0.002*SL
F to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.146	0.139 + 0.004*SL	0.144 + 0.002*SL	0.152 + 0.002*SL
	t_{PHL}	0.098	0.091 + 0.003*SL	0.095 + 0.002*SL	0.101 + 0.002*SL
G to Y	t_R	0.042	0.031 + 0.005*SL	0.033 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.029	0.020 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.116	0.109 + 0.004*SL	0.114 + 0.002*SL	0.121 + 0.002*SL
	t_{PHL}	0.076	0.069 + 0.003*SL	0.073 + 0.002*SL	0.079 + 0.002*SL
H to Y	t_R	0.041	0.031 + 0.005*SL	0.033 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.120	0.112 + 0.004*SL	0.117 + 0.002*SL	0.125 + 0.002*SL
	t_{PHL}	0.080	0.073 + 0.003*SL	0.078 + 0.002*SL	0.084 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nr8d4

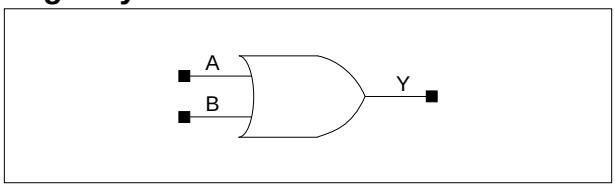
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.048 + 0.002*SL	0.045 + 0.002*SL	0.037 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.142	0.137 + 0.002*SL	0.141 + 0.001*SL	0.155 + 0.001*SL
	t_{PHL}	0.094	0.090 + 0.002*SL	0.093 + 0.001*SL	0.104 + 0.001*SL
B to Y	t_R	0.050	0.045 + 0.003*SL	0.046 + 0.002*SL	0.037 + 0.002*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.153	0.149 + 0.002*SL	0.152 + 0.001*SL	0.166 + 0.001*SL
	t_{PHL}	0.100	0.096 + 0.002*SL	0.099 + 0.001*SL	0.110 + 0.001*SL
C to Y	t_R	0.050	0.046 + 0.002*SL	0.044 + 0.002*SL	0.037 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.157	0.152 + 0.002*SL	0.156 + 0.001*SL	0.170 + 0.001*SL
	t_{PHL}	0.103	0.099 + 0.002*SL	0.102 + 0.001*SL	0.114 + 0.001*SL
D to Y	t_R	0.052	0.048 + 0.002*SL	0.046 + 0.002*SL	0.037 + 0.003*SL
	t_F	0.034	0.029 + 0.003*SL	0.032 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.149	0.144 + 0.002*SL	0.148 + 0.001*SL	0.162 + 0.001*SL
	t_{PHL}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.109 + 0.001*SL
E to Y	t_R	0.050	0.045 + 0.003*SL	0.046 + 0.002*SL	0.037 + 0.002*SL
	t_F	0.034	0.031 + 0.002*SL	0.030 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.160	0.155 + 0.002*SL	0.159 + 0.001*SL	0.174 + 0.001*SL
	t_{PHL}	0.104	0.100 + 0.002*SL	0.103 + 0.001*SL	0.115 + 0.001*SL
F to Y	t_R	0.051	0.046 + 0.002*SL	0.046 + 0.002*SL	0.037 + 0.002*SL
	t_F	0.035	0.030 + 0.002*SL	0.031 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.164	0.160 + 0.002*SL	0.163 + 0.001*SL	0.178 + 0.001*SL
	t_{PHL}	0.108	0.104 + 0.002*SL	0.107 + 0.001*SL	0.119 + 0.001*SL
G to Y	t_R	0.048	0.043 + 0.003*SL	0.045 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.030 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.131	0.127 + 0.002*SL	0.130 + 0.001*SL	0.145 + 0.001*SL
	t_{PHL}	0.085	0.081 + 0.002*SL	0.084 + 0.001*SL	0.096 + 0.001*SL
H to Y	t_R	0.050	0.045 + 0.003*SL	0.046 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.034	0.029 + 0.002*SL	0.031 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.136	0.131 + 0.002*SL	0.134 + 0.001*SL	0.149 + 0.001*SL
	t_{PHL}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.101 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

or2/or2d2/or2d4/or2d8

2-Input OR with 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)								Gate Count			
or2		*or2d2*		*or2d4*		*or2d8*		*or2*	*or2d2*	*or2d4*	*or2d8*
A	B	A	B	A	B	A	B				
1.0	1.1	1.0	1.0	1.9	2.2	1.8	2.3	1.67	2.00	3.67	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.021 + 0.009*SL	0.016 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.040	0.024 + 0.008*SL	0.025 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.051	0.042 + 0.005*SL	0.043 + 0.004*SL	0.044 + 0.004*SL
	t_{PHL}	0.066	0.055 + 0.006*SL	0.060 + 0.004*SL	0.064 + 0.004*SL
B to Y	t_R	0.040	0.020 + 0.010*SL	0.019 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.039	0.023 + 0.008*SL	0.025 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.057	0.048 + 0.005*SL	0.050 + 0.004*SL	0.050 + 0.004*SL
	t_{PHL}	0.071	0.059 + 0.006*SL	0.064 + 0.004*SL	0.068 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

or2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.022 + 0.005*SL	0.024 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.035	0.026 + 0.004*SL	0.028 + 0.004*SL	0.025 + 0.004*SL
	t_{PLH}	0.054	0.048 + 0.003*SL	0.050 + 0.002*SL	0.052 + 0.002*SL
	t_{PHL}	0.072	0.065 + 0.003*SL	0.069 + 0.002*SL	0.079 + 0.002*SL
B to Y	t_R	0.033	0.025 + 0.004*SL	0.022 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.037	0.027 + 0.005*SL	0.031 + 0.004*SL	0.024 + 0.004*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.056 + 0.002*SL	0.058 + 0.002*SL
	t_{PHL}	0.076	0.069 + 0.004*SL	0.074 + 0.002*SL	0.083 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.027	0.023 + 0.002*SL	0.022 + 0.002*SL	0.013 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.051	0.048 + 0.002*SL	0.049 + 0.001*SL	0.052 + 0.001*SL
	t_{PHL}	0.068	0.064 + 0.002*SL	0.067 + 0.001*SL	0.079 + 0.001*SL
B to Y	t_R	0.029	0.022 + 0.004*SL	0.028 + 0.002*SL	0.014 + 0.003*SL
	t_F	0.033	0.030 + 0.002*SL	0.030 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.056	0.053 + 0.002*SL	0.055 + 0.001*SL	0.058 + 0.001*SL
	t_{PHL}	0.072	0.068 + 0.002*SL	0.071 + 0.001*SL	0.083 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

or2d8

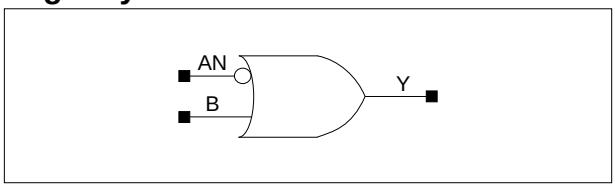
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.032 + 0.001*SL	0.030 + 0.001*SL	0.021 + 0.001*SL
	t_F	0.046	0.044 + 0.001*SL	0.044 + 0.001*SL	0.040 + 0.001*SL
	t_{PLH}	0.066	0.064 + 0.001*SL	0.066 + 0.001*SL	0.073 + 0.001*SL
	t_{PHL}	0.088	0.085 + 0.001*SL	0.087 + 0.001*SL	0.105 + 0.001*SL
B to Y	t_R	0.038	0.037 + 0.001*SL	0.035 + 0.001*SL	0.023 + 0.001*SL
	t_F	0.045	0.044 + 0.001*SL	0.043 + 0.001*SL	0.041 + 0.001*SL
	t_{PLH}	0.072	0.069 + 0.001*SL	0.071 + 0.001*SL	0.079 + 0.001*SL
	t_{PHL}	0.093	0.090 + 0.001*SL	0.092 + 0.001*SL	0.110 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

or2b/or2bd2/or2bd4/or2bd8

2-Input OR with one Inverted Input, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

AN	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

Cell Data

Input Load (SL)								Gate Count			
or2b		*or2bd2*		*or2bd4*		*or2bd8*		*or2b*	*or2bd2*	*or2bd4*	*or2bd8*
AN	B	AN	B	AN	B	AN	B				
0.7	1.1	0.7	1.2	0.9	2.2	0.9	2.1	2.33	2.67	4.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or2b

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.040	0.021 + 0.009*SL	0.018 + 0.010*SL	0.012 + 0.010*SL
	t_F	0.038	0.023 + 0.008*SL	0.022 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.089	0.079 + 0.005*SL	0.081 + 0.005*SL	0.081 + 0.004*SL
	t_{PHL}	0.081	0.069 + 0.006*SL	0.074 + 0.004*SL	0.079 + 0.004*SL
B to Y	t_R	0.041	0.023 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.019 + 0.008*SL
	t_{PLH}	0.058	0.048 + 0.005*SL	0.050 + 0.004*SL	0.050 + 0.004*SL
	t_{PHL}	0.072	0.061 + 0.006*SL	0.066 + 0.004*SL	0.071 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

or2bd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.029	0.019 + 0.005*SL	0.020 + 0.005*SL	0.011 + 0.005*SL
	t_F	0.036	0.027 + 0.005*SL	0.030 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.085	0.079 + 0.003*SL	0.082 + 0.002*SL	0.083 + 0.002*SL
	t_{PHL}	0.090	0.083 + 0.004*SL	0.088 + 0.002*SL	0.098 + 0.002*SL
B to Y	t_R	0.030	0.021 + 0.005*SL	0.020 + 0.005*SL	0.012 + 0.005*SL
	t_F	0.039	0.030 + 0.004*SL	0.032 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.049	0.044 + 0.003*SL	0.046 + 0.002*SL	0.047 + 0.002*SL
	t_{PHL}	0.080	0.072 + 0.004*SL	0.077 + 0.002*SL	0.088 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or2bd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.027	0.022 + 0.003*SL	0.023 + 0.002*SL	0.013 + 0.003*SL
	t_F	0.031	0.028 + 0.002*SL	0.027 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.084	0.081 + 0.002*SL	0.083 + 0.001*SL	0.086 + 0.001*SL
	t_{PHL}	0.085	0.082 + 0.002*SL	0.084 + 0.001*SL	0.096 + 0.001*SL
B to Y	t_R	0.028	0.022 + 0.003*SL	0.025 + 0.002*SL	0.014 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.026 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.054	0.051 + 0.002*SL	0.053 + 0.001*SL	0.056 + 0.001*SL
	t_{PHL}	0.071	0.067 + 0.002*SL	0.070 + 0.001*SL	0.081 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

or2bd8

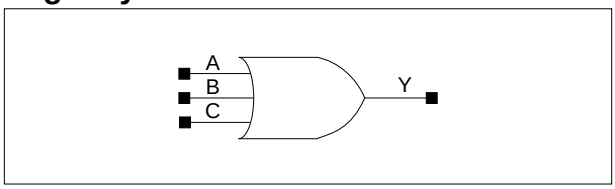
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.034	0.032 + 0.001*SL	0.031 + 0.001*SL	0.021 + 0.001*SL
	t_F	0.044	0.042 + 0.001*SL	0.043 + 0.001*SL	0.040 + 0.001*SL
	t_{PLH}	0.100	0.098 + 0.001*SL	0.100 + 0.001*SL	0.108 + 0.001*SL
	t_{PHL}	0.106	0.104 + 0.001*SL	0.106 + 0.001*SL	0.124 + 0.001*SL
B to Y	t_R	0.039	0.036 + 0.002*SL	0.038 + 0.001*SL	0.022 + 0.001*SL
	t_F	0.046	0.044 + 0.001*SL	0.045 + 0.001*SL	0.039 + 0.001*SL
	t_{PLH}	0.071	0.069 + 0.001*SL	0.070 + 0.001*SL	0.078 + 0.001*SL
	t_{PHL}	0.093	0.091 + 0.001*SL	0.092 + 0.001*SL	0.111 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

or3/or3d2/or3d4

3-Input OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)									Gate Count		
or3			*or3d2*			*or3d4*			*or3*	*or3d2*	*or3d4*
A	B	C	A	B	C	A	B	C			
1.0	1.0	1.0	0.9	1.0	1.0	1.8	2.1	2.2	2.00	2.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.047	0.029 + 0.009*SL	0.034 + 0.008*SL	0.030 + 0.008*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.049 + 0.004*SL
	t_{PHL}	0.083	0.070 + 0.006*SL	0.077 + 0.005*SL	0.087 + 0.004*SL
B to Y	t_R	0.042	0.025 + 0.008*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.048	0.031 + 0.009*SL	0.035 + 0.008*SL	0.029 + 0.008*SL
	t_{PLH}	0.063	0.053 + 0.005*SL	0.055 + 0.005*SL	0.056 + 0.004*SL
	t_{PHL}	0.094	0.081 + 0.007*SL	0.089 + 0.005*SL	0.098 + 0.004*SL
C to Y	t_R	0.043	0.025 + 0.009*SL	0.020 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.048	0.029 + 0.009*SL	0.037 + 0.008*SL	0.030 + 0.008*SL
	t_{PLH}	0.067	0.056 + 0.005*SL	0.059 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.099	0.086 + 0.007*SL	0.093 + 0.005*SL	0.103 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.023 + 0.005*SL	0.022 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.042 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.056 + 0.002*SL	0.058 + 0.002*SL
	t_{PHL}	0.092	0.083 + 0.004*SL	0.089 + 0.003*SL	0.106 + 0.002*SL
B to Y	t_R	0.037	0.028 + 0.004*SL	0.025 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.049	0.040 + 0.004*SL	0.042 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.065	0.058 + 0.003*SL	0.062 + 0.002*SL	0.064 + 0.002*SL
	t_{PHL}	0.103	0.095 + 0.004*SL	0.101 + 0.003*SL	0.118 + 0.002*SL
C to Y	t_R	0.040	0.034 + 0.003*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.049	0.039 + 0.005*SL	0.044 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.068	0.061 + 0.003*SL	0.066 + 0.002*SL	0.069 + 0.002*SL
	t_{PHL}	0.108	0.100 + 0.004*SL	0.106 + 0.003*SL	0.123 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

or3d4

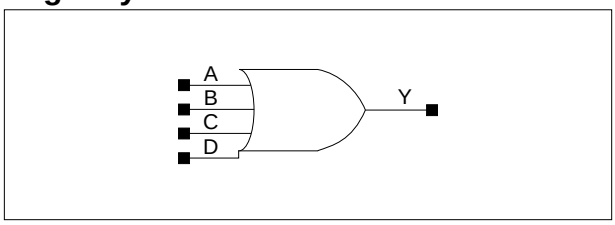
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.024 + 0.003*SL	0.024 + 0.002*SL	0.013 + 0.003*SL
	t_F	0.042	0.037 + 0.003*SL	0.040 + 0.002*SL	0.038 + 0.002*SL
	t_{PLH}	0.054	0.051 + 0.002*SL	0.053 + 0.001*SL	0.056 + 0.001*SL
	t_{PHL}	0.084	0.079 + 0.002*SL	0.083 + 0.001*SL	0.101 + 0.001*SL
B to Y	t_R	0.031	0.024 + 0.004*SL	0.029 + 0.002*SL	0.014 + 0.003*SL
	t_F	0.043	0.037 + 0.003*SL	0.040 + 0.002*SL	0.038 + 0.002*SL
	t_{PLH}	0.060	0.057 + 0.002*SL	0.058 + 0.001*SL	0.063 + 0.001*SL
	t_{PHL}	0.096	0.091 + 0.002*SL	0.095 + 0.001*SL	0.114 + 0.001*SL
C to Y	t_R	0.033	0.030 + 0.001*SL	0.026 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.042	0.037 + 0.002*SL	0.039 + 0.002*SL	0.038 + 0.002*SL
	t_{PLH}	0.063	0.060 + 0.002*SL	0.062 + 0.001*SL	0.067 + 0.001*SL
	t_{PHL}	0.101	0.096 + 0.002*SL	0.100 + 0.001*SL	0.119 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

or4/or4d2/or4d4

4-Input OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)											
or4				*or4d2*				*or4d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.2	1.1	1.2	1.1	1.2	1.1	1.2	2.1	2.5	2.1	2.5

Gate Count		
or4	*or4d2*	*or4d4*
3.00	3.33	6.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.025 + 0.010*SL	0.025 + 0.011*SL	0.020 + 0.011*SL
	t_F	0.052	0.033 + 0.009*SL	0.033 + 0.010*SL	0.027 + 0.010*SL
	t_{PLH}	0.051	0.041 + 0.005*SL	0.042 + 0.005*SL	0.042 + 0.005*SL
	t_{PHL}	0.077	0.065 + 0.006*SL	0.069 + 0.005*SL	0.072 + 0.005*SL
B to Y	t_R	0.048	0.028 + 0.010*SL	0.025 + 0.011*SL	0.020 + 0.011*SL
	t_F	0.052	0.032 + 0.010*SL	0.034 + 0.009*SL	0.027 + 0.010*SL
	t_{PLH}	0.055	0.045 + 0.005*SL	0.046 + 0.005*SL	0.046 + 0.005*SL
	t_{PHL}	0.080	0.068 + 0.006*SL	0.072 + 0.005*SL	0.075 + 0.005*SL
C to Y	t_R	0.051	0.030 + 0.011*SL	0.030 + 0.011*SL	0.025 + 0.011*SL
	t_F	0.049	0.030 + 0.010*SL	0.029 + 0.010*SL	0.026 + 0.010*SL
	t_{PLH}	0.053	0.043 + 0.005*SL	0.044 + 0.005*SL	0.044 + 0.005*SL
	t_{PHL}	0.079	0.067 + 0.006*SL	0.070 + 0.005*SL	0.074 + 0.005*SL
D to Y	t_R	0.052	0.032 + 0.010*SL	0.030 + 0.011*SL	0.025 + 0.011*SL
	t_F	0.049	0.030 + 0.010*SL	0.030 + 0.010*SL	0.025 + 0.010*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.048 + 0.005*SL	0.049 + 0.005*SL
	t_{PHL}	0.082	0.070 + 0.006*SL	0.074 + 0.005*SL	0.076 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.026 + 0.005*SL	0.024 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.045	0.035 + 0.005*SL	0.037 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.050	0.045 + 0.003*SL	0.046 + 0.002*SL	0.047 + 0.002*SL
	t_{PHL}	0.080	0.073 + 0.004*SL	0.076 + 0.003*SL	0.083 + 0.002*SL
B to Y	t_R	0.036	0.025 + 0.005*SL	0.026 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.046	0.034 + 0.006*SL	0.039 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.054	0.049 + 0.003*SL	0.050 + 0.002*SL	0.051 + 0.002*SL
	t_{PHL}	0.083	0.076 + 0.004*SL	0.079 + 0.003*SL	0.087 + 0.002*SL
C to Y	t_R	0.039	0.029 + 0.005*SL	0.028 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.042	0.030 + 0.006*SL	0.035 + 0.005*SL	0.030 + 0.005*SL
	t_{PLH}	0.054	0.048 + 0.003*SL	0.049 + 0.002*SL	0.051 + 0.002*SL
	t_{PHL}	0.084	0.077 + 0.004*SL	0.081 + 0.003*SL	0.089 + 0.002*SL
D to Y	t_R	0.040	0.029 + 0.005*SL	0.030 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.041	0.030 + 0.006*SL	0.033 + 0.005*SL	0.030 + 0.005*SL
	t_{PLH}	0.058	0.053 + 0.003*SL	0.054 + 0.002*SL	0.054 + 0.002*SL
	t_{PHL}	0.088	0.081 + 0.004*SL	0.085 + 0.003*SL	0.093 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

or4d4

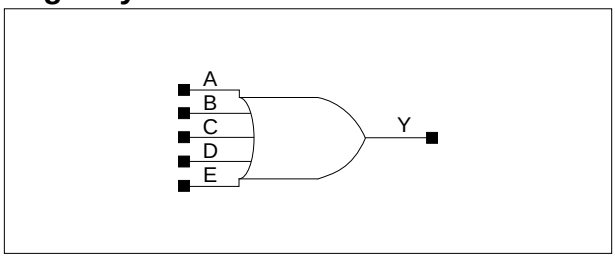
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.024 + 0.003*SL	0.024 + 0.003*SL	0.016 + 0.003*SL
	t_F	0.038	0.033 + 0.002*SL	0.034 + 0.002*SL	0.029 + 0.002*SL
	t_{PLH}	0.046	0.043 + 0.001*SL	0.044 + 0.001*SL	0.046 + 0.001*SL
	t_{PHL}	0.074	0.070 + 0.002*SL	0.073 + 0.001*SL	0.081 + 0.001*SL
B to Y	t_R	0.030	0.025 + 0.002*SL	0.024 + 0.003*SL	0.018 + 0.003*SL
	t_F	0.040	0.035 + 0.003*SL	0.036 + 0.002*SL	0.030 + 0.002*SL
	t_{PLH}	0.050	0.047 + 0.001*SL	0.048 + 0.001*SL	0.050 + 0.001*SL
	t_{PHL}	0.078	0.074 + 0.002*SL	0.076 + 0.001*SL	0.085 + 0.001*SL
C to Y	t_R	0.034	0.030 + 0.002*SL	0.028 + 0.003*SL	0.021 + 0.003*SL
	t_F	0.035	0.030 + 0.002*SL	0.030 + 0.002*SL	0.030 + 0.002*SL
	t_{PLH}	0.050	0.047 + 0.001*SL	0.048 + 0.001*SL	0.049 + 0.001*SL
	t_{PHL}	0.079	0.075 + 0.002*SL	0.077 + 0.001*SL	0.087 + 0.001*SL
D to Y	t_R	0.035	0.030 + 0.002*SL	0.029 + 0.003*SL	0.022 + 0.003*SL
	t_F	0.036	0.030 + 0.003*SL	0.032 + 0.002*SL	0.029 + 0.002*SL
	t_{PLH}	0.054	0.051 + 0.001*SL	0.052 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.083	0.079 + 0.002*SL	0.082 + 0.001*SL	0.091 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

or5/or5d2/or5d4

5-Input OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)															Gate Count		
or5					*or5d2*					*or5d4*					*or5*	*or5d2*	*or5d4*
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
1.0	1.0	1.0	1.1	1.2	0.9	1.0	1.0	1.1	1.2	1.8	2.0	2.3	2.1	2.4	3.33	3.67	7.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.027 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.011*SL
	t_F	0.056	0.036 + 0.010*SL	0.038 + 0.009*SL	0.033 + 0.010*SL
	t_{PLH}	0.062	0.051 + 0.005*SL	0.053 + 0.005*SL	0.054 + 0.005*SL
	t_{PHL}	0.087	0.074 + 0.007*SL	0.080 + 0.005*SL	0.087 + 0.005*SL
B to Y	t_R	0.046	0.027 + 0.010*SL	0.023 + 0.011*SL	0.019 + 0.011*SL
	t_F	0.057	0.037 + 0.010*SL	0.040 + 0.009*SL	0.033 + 0.010*SL
	t_{PLH}	0.068	0.057 + 0.005*SL	0.059 + 0.005*SL	0.060 + 0.005*SL
	t_{PHL}	0.099	0.085 + 0.007*SL	0.091 + 0.005*SL	0.099 + 0.005*SL
C to Y	t_R	0.049	0.030 + 0.010*SL	0.027 + 0.010*SL	0.021 + 0.011*SL
	t_F	0.057	0.036 + 0.010*SL	0.040 + 0.009*SL	0.033 + 0.010*SL
	t_{PLH}	0.071	0.061 + 0.005*SL	0.063 + 0.005*SL	0.064 + 0.005*SL
	t_{PHL}	0.103	0.090 + 0.007*SL	0.096 + 0.005*SL	0.103 + 0.005*SL
D to Y	t_R	0.048	0.027 + 0.010*SL	0.026 + 0.011*SL	0.021 + 0.011*SL
	t_F	0.047	0.026 + 0.010*SL	0.029 + 0.010*SL	0.025 + 0.010*SL
	t_{PLH}	0.051	0.041 + 0.005*SL	0.042 + 0.005*SL	0.042 + 0.005*SL
	t_{PHL}	0.076	0.064 + 0.006*SL	0.068 + 0.005*SL	0.072 + 0.005*SL
E to Y	t_R	0.049	0.030 + 0.010*SL	0.027 + 0.011*SL	0.021 + 0.011*SL
	t_F	0.047	0.026 + 0.010*SL	0.029 + 0.010*SL	0.025 + 0.010*SL
	t_{PLH}	0.055	0.045 + 0.005*SL	0.047 + 0.005*SL	0.047 + 0.005*SL
	t_{PHL}	0.080	0.068 + 0.006*SL	0.072 + 0.005*SL	0.076 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.044	0.038 + 0.003*SL	0.029 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.057	0.047 + 0.005*SL	0.048 + 0.005*SL	0.044 + 0.005*SL
	t_{PLH}	0.065	0.059 + 0.003*SL	0.062 + 0.002*SL	0.063 + 0.002*SL
	t_{PHL}	0.097	0.089 + 0.004*SL	0.094 + 0.003*SL	0.107 + 0.002*SL
B to Y	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.057	0.047 + 0.005*SL	0.048 + 0.005*SL	0.044 + 0.005*SL
	t_{PLH}	0.071	0.065 + 0.003*SL	0.067 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.109	0.101 + 0.004*SL	0.106 + 0.003*SL	0.119 + 0.002*SL
C to Y	t_R	0.047	0.040 + 0.003*SL	0.032 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.057	0.046 + 0.005*SL	0.050 + 0.005*SL	0.042 + 0.005*SL
	t_{PLH}	0.074	0.067 + 0.003*SL	0.070 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.113	0.105 + 0.004*SL	0.110 + 0.003*SL	0.123 + 0.002*SL
D to Y	t_R	0.039	0.029 + 0.005*SL	0.028 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.041	0.031 + 0.005*SL	0.033 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.054	0.048 + 0.003*SL	0.049 + 0.002*SL	0.050 + 0.002*SL
	t_{PHL}	0.084	0.077 + 0.004*SL	0.081 + 0.003*SL	0.090 + 0.002*SL
E to Y	t_R	0.040	0.029 + 0.005*SL	0.030 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.041	0.030 + 0.005*SL	0.032 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.058	0.052 + 0.003*SL	0.053 + 0.002*SL	0.054 + 0.002*SL
	t_{PHL}	0.088	0.081 + 0.004*SL	0.084 + 0.003*SL	0.093 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

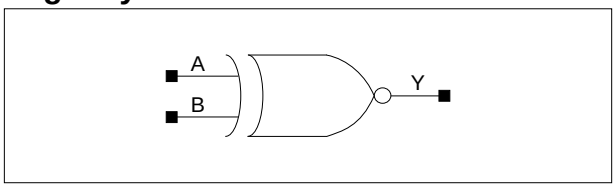
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

or5d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.002*SL	0.028 + 0.003*SL	0.019 + 0.003*SL
	t_F	0.051	0.045 + 0.003*SL	0.047 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.060	0.057 + 0.002*SL	0.059 + 0.001*SL	0.061 + 0.001*SL
	t_{PHL}	0.090	0.086 + 0.002*SL	0.088 + 0.001*SL	0.103 + 0.001*SL
B to Y	t_R	0.038	0.035 + 0.002*SL	0.031 + 0.003*SL	0.021 + 0.003*SL
	t_F	0.051	0.046 + 0.002*SL	0.047 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.066	0.063 + 0.002*SL	0.065 + 0.001*SL	0.068 + 0.001*SL
	t_{PHL}	0.103	0.098 + 0.002*SL	0.101 + 0.001*SL	0.116 + 0.001*SL
C to Y	t_R	0.040	0.030 + 0.005*SL	0.040 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.050	0.044 + 0.003*SL	0.046 + 0.002*SL	0.042 + 0.002*SL
	t_{PLH}	0.069	0.066 + 0.001*SL	0.067 + 0.001*SL	0.073 + 0.001*SL
	t_{PHL}	0.107	0.103 + 0.002*SL	0.106 + 0.001*SL	0.121 + 0.001*SL
D to Y	t_R	0.034	0.028 + 0.003*SL	0.028 + 0.003*SL	0.022 + 0.003*SL
	t_F	0.035	0.030 + 0.003*SL	0.031 + 0.002*SL	0.032 + 0.002*SL
	t_{PLH}	0.049	0.047 + 0.001*SL	0.047 + 0.001*SL	0.049 + 0.001*SL
	t_{PHL}	0.078	0.074 + 0.002*SL	0.077 + 0.001*SL	0.087 + 0.001*SL
E to Y	t_R	0.034	0.029 + 0.002*SL	0.028 + 0.003*SL	0.022 + 0.003*SL
	t_F	0.036	0.030 + 0.003*SL	0.031 + 0.002*SL	0.032 + 0.002*SL
	t_{PLH}	0.053	0.051 + 0.001*SL	0.052 + 0.001*SL	0.053 + 0.001*SL
	t_{PHL}	0.082	0.078 + 0.002*SL	0.081 + 0.001*SL	0.091 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)							
xn2		*xn2d2*		*xn2d4*		*xn2d8*	
A	B	A	B	A	B	A	B
1.1	1.6	1.1	1.6	1.1	1.6	2.0	2.2

Gate Count			
xn2	*xn2d2*	*xn2d4*	*xn2d8*
2.67	3.33	4.00	7.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xn2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.052	0.037 + 0.008*SL	0.028 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.052	0.036 + 0.008*SL	0.038 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.092	0.081 + 0.005*SL	0.084 + 0.005*SL	0.086 + 0.004*SL
	t_{PHL}	0.095	0.084 + 0.006*SL	0.090 + 0.004*SL	0.094 + 0.004*SL
B to Y	t_R	0.047	0.030 + 0.009*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.050	0.033 + 0.008*SL	0.036 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.093	0.082 + 0.005*SL	0.086 + 0.005*SL	0.088 + 0.004*SL
	t_{PHL}	0.086	0.072 + 0.007*SL	0.080 + 0.005*SL	0.090 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xn2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.047	0.037 + 0.005*SL	0.037 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.054	0.045 + 0.005*SL	0.049 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.094	0.088 + 0.003*SL	0.091 + 0.002*SL	0.097 + 0.002*SL
	t_{PHL}	0.100	0.093 + 0.004*SL	0.097 + 0.002*SL	0.109 + 0.002*SL
B to Y	t_R	0.045	0.035 + 0.005*SL	0.035 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.052	0.043 + 0.004*SL	0.045 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.095	0.089 + 0.003*SL	0.093 + 0.002*SL	0.098 + 0.002*SL
	t_{PHL}	0.091	0.082 + 0.004*SL	0.089 + 0.003*SL	0.107 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

xn2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.054 + 0.002*SL	0.052 + 0.002*SL	0.043 + 0.002*SL
	t_F	0.075	0.069 + 0.003*SL	0.072 + 0.002*SL	0.075 + 0.002*SL
	t_{PLH}	0.109	0.105 + 0.002*SL	0.108 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.120	0.116 + 0.002*SL	0.118 + 0.002*SL	0.144 + 0.001*SL
B to Y	t_R	0.056	0.053 + 0.002*SL	0.050 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.075	0.072 + 0.002*SL	0.070 + 0.002*SL	0.076 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.114	0.109 + 0.003*SL	0.113 + 0.002*SL	0.142 + 0.001*SL

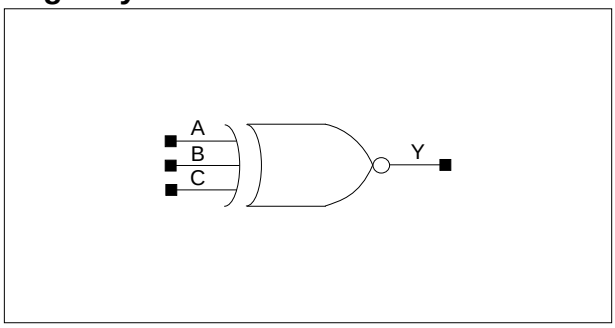
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

xn2d8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.063	0.061 + 0.001*SL	0.061 + 0.001*SL	0.052 + 0.001*SL
	t_F	0.083	0.081 + 0.001*SL	0.082 + 0.001*SL	0.089 + 0.001*SL
	t_{PLH}	0.115	0.112 + 0.001*SL	0.114 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.125	0.123 + 0.001*SL	0.125 + 0.001*SL	0.158 + 0.001*SL
B to Y	t_R	0.063	0.060 + 0.002*SL	0.062 + 0.001*SL	0.053 + 0.001*SL
	t_F	0.085	0.083 + 0.001*SL	0.082 + 0.001*SL	0.088 + 0.001*SL
	t_{PLH}	0.126	0.124 + 0.001*SL	0.125 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.127	0.124 + 0.001*SL	0.126 + 0.001*SL	0.160 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)									Gate Count		
xn3			*xn3d2*			*xn3d4*			*xn3*	*xn3d2*	*xn3d4*
A	B	C	A	B	C	A	B	C			
1.4	1.1	1.5	1.4	1.1	1.5	1.4	1.1	1.5	4.67	5.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xn3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.060	0.039 + 0.010*SL	0.042 + 0.010*SL	0.034 + 0.010*SL
	t_F	0.065	0.045 + 0.010*SL	0.052 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.096	0.083 + 0.007*SL	0.090 + 0.005*SL	0.099 + 0.005*SL
	t_{PHL}	0.093	0.076 + 0.008*SL	0.087 + 0.006*SL	0.107 + 0.004*SL
B to Y	t_R	0.063	0.045 + 0.009*SL	0.042 + 0.010*SL	0.035 + 0.010*SL
	t_F	0.071	0.055 + 0.008*SL	0.057 + 0.008*SL	0.054 + 0.008*SL
	t_{PLH}	0.145	0.134 + 0.006*SL	0.138 + 0.005*SL	0.140 + 0.004*SL
	t_{PHL}	0.152	0.136 + 0.008*SL	0.146 + 0.005*SL	0.164 + 0.004*SL
C to Y	t_R	0.063	0.043 + 0.010*SL	0.045 + 0.009*SL	0.036 + 0.010*SL
	t_F	0.071	0.054 + 0.008*SL	0.057 + 0.008*SL	0.054 + 0.008*SL
	t_{PLH}	0.141	0.128 + 0.007*SL	0.135 + 0.005*SL	0.143 + 0.005*SL
	t_{PHL}	0.150	0.139 + 0.006*SL	0.145 + 0.004*SL	0.150 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

3-Input Exclusive-NOR with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xn3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.049 + 0.004*SL	0.047 + 0.005*SL	0.045 + 0.005*SL
	t_F	0.077	0.068 + 0.005*SL	0.069 + 0.004*SL	0.083 + 0.004*SL
	t_{PLH}	0.103	0.095 + 0.004*SL	0.100 + 0.003*SL	0.117 + 0.002*SL
	t_{PHL}	0.105	0.095 + 0.005*SL	0.103 + 0.003*SL	0.134 + 0.002*SL
B to Y	t_R	0.061	0.052 + 0.005*SL	0.052 + 0.005*SL	0.046 + 0.005*SL
	t_F	0.074	0.064 + 0.005*SL	0.068 + 0.004*SL	0.069 + 0.004*SL
	t_{PLH}	0.147	0.139 + 0.004*SL	0.145 + 0.003*SL	0.160 + 0.002*SL
	t_{PHL}	0.162	0.152 + 0.005*SL	0.160 + 0.003*SL	0.186 + 0.002*SL
C to Y	t_R	0.063	0.053 + 0.005*SL	0.053 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.091	0.081 + 0.005*SL	0.084 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.148	0.140 + 0.004*SL	0.146 + 0.003*SL	0.161 + 0.002*SL
	t_{PHL}	0.152	0.141 + 0.005*SL	0.149 + 0.003*SL	0.182 + 0.002*SL

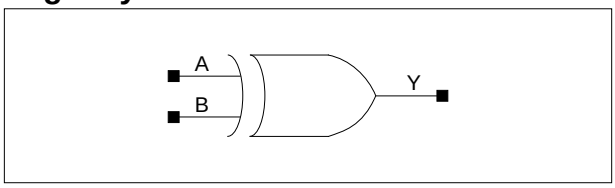
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

xn3d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.080	0.077 + 0.002*SL	0.074 + 0.002*SL	0.073 + 0.002*SL
	t_F	0.126	0.123 + 0.002*SL	0.121 + 0.002*SL	0.132 + 0.002*SL
	t_{PLH}	0.133	0.128 + 0.002*SL	0.131 + 0.002*SL	0.156 + 0.001*SL
	t_{PHL}	0.154	0.148 + 0.003*SL	0.152 + 0.002*SL	0.193 + 0.001*SL
B to Y	t_R	0.076	0.073 + 0.002*SL	0.070 + 0.002*SL	0.066 + 0.002*SL
	t_F	0.103	0.100 + 0.001*SL	0.098 + 0.002*SL	0.106 + 0.002*SL
	t_{PLH}	0.175	0.171 + 0.002*SL	0.174 + 0.002*SL	0.197 + 0.001*SL
	t_{PHL}	0.199	0.193 + 0.003*SL	0.197 + 0.002*SL	0.233 + 0.001*SL
C to Y	t_R	0.082	0.079 + 0.001*SL	0.075 + 0.002*SL	0.074 + 0.002*SL
	t_F	0.132	0.129 + 0.002*SL	0.128 + 0.002*SL	0.136 + 0.002*SL
	t_{PLH}	0.176	0.172 + 0.002*SL	0.175 + 0.002*SL	0.198 + 0.001*SL
	t_{PHL}	0.197	0.191 + 0.003*SL	0.195 + 0.002*SL	0.235 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)							
xo2		*xo2d2*		*xo2d4*		*xo2d8*	
A	B	A	B	A	B	A	B
1.1	1.2	1.1	1.2	1.1	1.2	2.1	1.5

Gate Count			
xo2	*xo2d2*	*xo2d4*	*xo2d8*
3.00	3.67	4.33	7.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xo2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.050	0.031 + 0.009*SL	0.030 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.053	0.036 + 0.009*SL	0.041 + 0.007*SL	0.034 + 0.008*SL
	t_{PLH}	0.094	0.083 + 0.006*SL	0.087 + 0.005*SL	0.088 + 0.004*SL
	t_{PHL}	0.099	0.088 + 0.006*SL	0.094 + 0.004*SL	0.099 + 0.004*SL
B to Y	t_R	0.051	0.033 + 0.009*SL	0.030 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.048	0.030 + 0.009*SL	0.036 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.096	0.085 + 0.006*SL	0.090 + 0.005*SL	0.093 + 0.004*SL
	t_{PHL}	0.084	0.071 + 0.007*SL	0.079 + 0.005*SL	0.089 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

2-Input Exclusive-OR with 1X/2X/4X/8X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xo2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.036 + 0.005*SL	0.038 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.052	0.042 + 0.005*SL	0.047 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.096	0.089 + 0.003*SL	0.093 + 0.002*SL	0.099 + 0.002*SL
	t_{PHL}	0.103	0.096 + 0.004*SL	0.101 + 0.002*SL	0.111 + 0.002*SL
B to Y	t_R	0.046	0.036 + 0.005*SL	0.037 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.050	0.041 + 0.004*SL	0.043 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.099	0.092 + 0.004*SL	0.097 + 0.002*SL	0.105 + 0.002*SL
	t_{PHL}	0.091	0.083 + 0.004*SL	0.089 + 0.003*SL	0.108 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

xo2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.053 + 0.002*SL	0.053 + 0.002*SL	0.045 + 0.002*SL
	t_F	0.075	0.070 + 0.002*SL	0.071 + 0.002*SL	0.075 + 0.002*SL
	t_{PLH}	0.111	0.107 + 0.002*SL	0.110 + 0.001*SL	0.122 + 0.001*SL
	t_{PHL}	0.124	0.119 + 0.002*SL	0.122 + 0.001*SL	0.145 + 0.001*SL
B to Y	t_R	0.060	0.056 + 0.002*SL	0.055 + 0.002*SL	0.044 + 0.002*SL
	t_F	0.073	0.069 + 0.002*SL	0.069 + 0.002*SL	0.075 + 0.002*SL
	t_{PLH}	0.117	0.113 + 0.002*SL	0.116 + 0.001*SL	0.133 + 0.001*SL
	t_{PHL}	0.117	0.112 + 0.003*SL	0.116 + 0.002*SL	0.145 + 0.001*SL

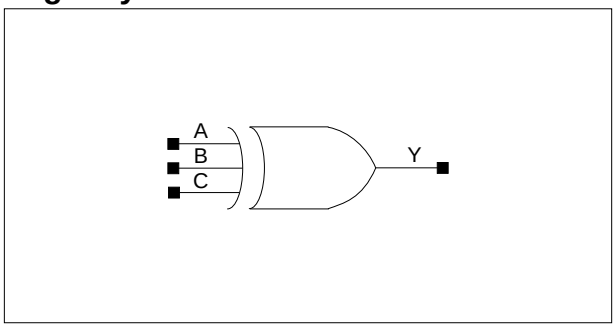
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

xo2d8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.063 + 0.001*SL	0.063 + 0.001*SL	0.054 + 0.001*SL
	t_F	0.081	0.078 + 0.002*SL	0.080 + 0.001*SL	0.087 + 0.001*SL
	t_{PLH}	0.116	0.113 + 0.001*SL	0.115 + 0.001*SL	0.132 + 0.001*SL
	t_{PHL}	0.127	0.124 + 0.001*SL	0.126 + 0.001*SL	0.153 + 0.001*SL
B to Y	t_R	0.066	0.063 + 0.002*SL	0.065 + 0.001*SL	0.055 + 0.001*SL
	t_F	0.083	0.081 + 0.001*SL	0.081 + 0.001*SL	0.088 + 0.001*SL
	t_{PLH}	0.136	0.133 + 0.001*SL	0.135 + 0.001*SL	0.156 + 0.001*SL
	t_{PHL}	0.132	0.130 + 0.001*SL	0.132 + 0.001*SL	0.165 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
xo3			*xo3d2*			*xo3d4*			*xo3*	*xo3d2*	*xo3d4*
A	B	C	A	B	C	A	B	C			
1.6	1.0	1.5	1.6	1.1	1.5	1.6	1.0	1.5	4.67	5.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xo3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.057	0.038 + 0.010*SL	0.037 + 0.010*SL	0.032 + 0.010*SL
	t_F	0.071	0.052 + 0.010*SL	0.059 + 0.008*SL	0.064 + 0.008*SL
	t_{PLH}	0.090	0.079 + 0.006*SL	0.082 + 0.005*SL	0.084 + 0.004*SL
	t_{PHL}	0.103	0.086 + 0.009*SL	0.097 + 0.006*SL	0.120 + 0.004*SL
B to Y	t_R	0.063	0.045 + 0.009*SL	0.042 + 0.010*SL	0.035 + 0.010*SL
	t_F	0.071	0.053 + 0.009*SL	0.058 + 0.007*SL	0.054 + 0.008*SL
	t_{PLH}	0.148	0.137 + 0.006*SL	0.141 + 0.005*SL	0.143 + 0.004*SL
	t_{PHL}	0.155	0.139 + 0.008*SL	0.150 + 0.005*SL	0.168 + 0.004*SL
C to Y	t_R	0.063	0.045 + 0.009*SL	0.043 + 0.010*SL	0.035 + 0.010*SL
	t_F	0.083	0.066 + 0.009*SL	0.069 + 0.008*SL	0.071 + 0.008*SL
	t_{PLH}	0.133	0.120 + 0.006*SL	0.127 + 0.005*SL	0.133 + 0.004*SL
	t_{PHL}	0.142	0.125 + 0.009*SL	0.137 + 0.006*SL	0.161 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

3-Input Exclusive-OR with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

xo3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.049	0.039 + 0.005*SL	0.040 + 0.005*SL	0.035 + 0.005*SL
	t_F	0.084	0.074 + 0.005*SL	0.078 + 0.004*SL	0.087 + 0.004*SL
	t_{PLH}	0.092	0.085 + 0.003*SL	0.089 + 0.002*SL	0.094 + 0.002*SL
	t_{PHL}	0.116	0.105 + 0.005*SL	0.114 + 0.003*SL	0.147 + 0.002*SL
B to Y	t_R	0.062	0.053 + 0.005*SL	0.052 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.075	0.065 + 0.005*SL	0.070 + 0.004*SL	0.071 + 0.004*SL
	t_{PLH}	0.152	0.145 + 0.003*SL	0.149 + 0.002*SL	0.155 + 0.002*SL
	t_{PHL}	0.167	0.157 + 0.005*SL	0.165 + 0.003*SL	0.191 + 0.002*SL
C to Y	t_R	0.063	0.053 + 0.005*SL	0.055 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.092	0.084 + 0.004*SL	0.085 + 0.004*SL	0.094 + 0.004*SL
	t_{PLH}	0.140	0.132 + 0.004*SL	0.137 + 0.003*SL	0.150 + 0.002*SL
	t_{PHL}	0.156	0.145 + 0.005*SL	0.153 + 0.003*SL	0.186 + 0.002*SL

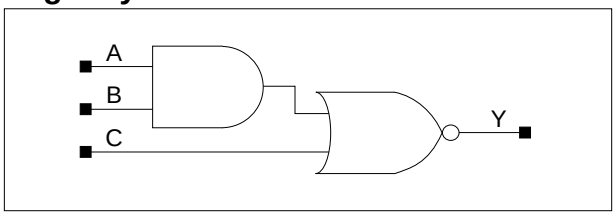
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

xo3d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.081	0.077 + 0.002*SL	0.075 + 0.002*SL	0.073 + 0.002*SL
	t_F	0.129	0.126 + 0.001*SL	0.123 + 0.002*SL	0.133 + 0.002*SL
	t_{PLH}	0.115	0.110 + 0.002*SL	0.113 + 0.002*SL	0.139 + 0.001*SL
	t_{PHL}	0.161	0.155 + 0.003*SL	0.159 + 0.002*SL	0.200 + 0.001*SL
B to Y	t_R	0.051	0.047 + 0.002*SL	0.045 + 0.002*SL	0.034 + 0.003*SL
	t_F	0.103	0.098 + 0.002*SL	0.099 + 0.002*SL	0.107 + 0.002*SL
	t_{PLH}	0.167	0.163 + 0.002*SL	0.166 + 0.001*SL	0.178 + 0.001*SL
	t_{PHL}	0.202	0.196 + 0.003*SL	0.200 + 0.002*SL	0.235 + 0.001*SL
C to Y	t_R	0.068	0.064 + 0.002*SL	0.063 + 0.002*SL	0.058 + 0.002*SL
	t_F	0.132	0.128 + 0.002*SL	0.128 + 0.002*SL	0.136 + 0.002*SL
	t_{PLH}	0.163	0.158 + 0.002*SL	0.162 + 0.002*SL	0.183 + 0.001*SL
	t_{PHL}	0.199	0.193 + 0.003*SL	0.197 + 0.002*SL	0.237 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	0	1
x	0	0	1
Other States			0

Cell Data

Input Load (SL)								
ao21			*ao21d2*			*ao21d4*		
A	B	C	A	B	C	A	B	C
1.0	1.0	1.0	1.9	2.0	1.9	1.0	1.0	1.0
Gate Count								
ao21			*ao21d2*			*ao21d4*		
1.67			3.00			3.67		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.053 + 0.018*SL	0.045 + 0.020*SL	0.035 + 0.020*SL
	t_F	0.068	0.042 + 0.013*SL	0.034 + 0.015*SL	0.024 + 0.016*SL
	t_{PLH}	0.051	0.033 + 0.009*SL	0.034 + 0.009*SL	0.033 + 0.009*SL
	t_{PHL}	0.048	0.031 + 0.008*SL	0.034 + 0.008*SL	0.034 + 0.008*SL
B to Y	t_R	0.094	0.056 + 0.019*SL	0.052 + 0.020*SL	0.041 + 0.020*SL
	t_F	0.066	0.039 + 0.014*SL	0.032 + 0.015*SL	0.024 + 0.016*SL
	t_{PLH}	0.055	0.036 + 0.009*SL	0.037 + 0.009*SL	0.036 + 0.009*SL
	t_{PHL}	0.048	0.031 + 0.009*SL	0.034 + 0.008*SL	0.035 + 0.008*SL
C to Y	t_R	0.089	0.051 + 0.019*SL	0.046 + 0.020*SL	0.041 + 0.020*SL
	t_F	0.064	0.046 + 0.009*SL	0.044 + 0.010*SL	0.032 + 0.010*SL
	t_{PLH}	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.047 + 0.009*SL
	t_{PHL}	0.048	0.036 + 0.006*SL	0.039 + 0.005*SL	0.039 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao21d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.072	0.056 + 0.008*SL	0.049 + 0.010*SL	0.035 + 0.010*SL
	t_F	0.055	0.042 + 0.007*SL	0.039 + 0.007*SL	0.024 + 0.008*SL
	t_{PLH}	0.041	0.030 + 0.005*SL	0.033 + 0.004*SL	0.033 + 0.005*SL
	t_{PHL}	0.039	0.029 + 0.005*SL	0.033 + 0.004*SL	0.033 + 0.004*SL
B to Y	t_R	0.077	0.060 + 0.008*SL	0.055 + 0.010*SL	0.041 + 0.010*SL
	t_F	0.050	0.035 + 0.007*SL	0.035 + 0.008*SL	0.023 + 0.008*SL
	t_{PLH}	0.045	0.035 + 0.005*SL	0.037 + 0.004*SL	0.036 + 0.005*SL
	t_{PHL}	0.039	0.030 + 0.005*SL	0.033 + 0.004*SL	0.035 + 0.004*SL
C to Y	t_R	0.069	0.051 + 0.009*SL	0.046 + 0.010*SL	0.041 + 0.010*SL
	t_F	0.053	0.044 + 0.004*SL	0.042 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.055	0.045 + 0.005*SL	0.046 + 0.005*SL	0.047 + 0.005*SL
	t_{PHL}	0.042	0.036 + 0.003*SL	0.038 + 0.003*SL	0.039 + 0.003*SL

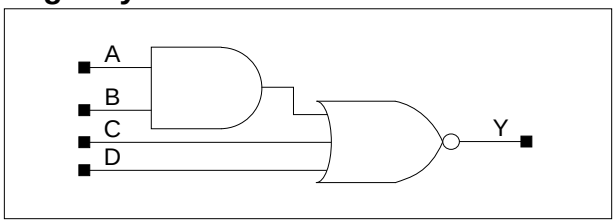
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao21d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.028 + 0.003*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.102	0.098 + 0.002*SL	0.100 + 0.001*SL	0.105 + 0.001*SL
	t_{PHL}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.105 + 0.001*SL
B to Y	t_R	0.034	0.029 + 0.003*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.105	0.102 + 0.002*SL	0.104 + 0.001*SL	0.109 + 0.001*SL
	t_{PHL}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.104 + 0.001*SL
C to Y	t_R	0.034	0.029 + 0.002*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.115	0.112 + 0.002*SL	0.114 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.097	0.094 + 0.002*SL	0.097 + 0.001*SL	0.105 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	0	1
x	0	0	0	1
Other States				0

Cell Data

Input Load (SL)											
ao211				*ao211d2*				*ao211d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.0	1.0	1.8	2.0	1.9	1.9	1.0	1.0	1.0	1.0

Gate Count		
ao211	*ao211d2*	*ao211d4*
2.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.135	0.078 + 0.029*SL	0.071 + 0.030*SL	0.068 + 0.031*SL
	t_F	0.071	0.044 + 0.013*SL	0.036 + 0.015*SL	0.027 + 0.016*SL
	t_{PLH}	0.067	0.040 + 0.013*SL	0.039 + 0.014*SL	0.039 + 0.014*SL
	t_{PHL}	0.050	0.034 + 0.008*SL	0.036 + 0.008*SL	0.036 + 0.008*SL
B to Y	t_R	0.143	0.086 + 0.028*SL	0.078 + 0.030*SL	0.076 + 0.031*SL
	t_F	0.067	0.039 + 0.014*SL	0.033 + 0.015*SL	0.027 + 0.016*SL
	t_{PLH}	0.071	0.045 + 0.013*SL	0.044 + 0.014*SL	0.043 + 0.014*SL
	t_{PHL}	0.050	0.033 + 0.008*SL	0.036 + 0.008*SL	0.037 + 0.008*SL
C to Y	t_R	0.142	0.083 + 0.029*SL	0.078 + 0.030*SL	0.076 + 0.031*SL
	t_F	0.071	0.051 + 0.010*SL	0.045 + 0.011*SL	0.036 + 0.012*SL
	t_{PLH}	0.093	0.065 + 0.014*SL	0.066 + 0.014*SL	0.066 + 0.014*SL
	t_{PHL}	0.055	0.042 + 0.006*SL	0.044 + 0.006*SL	0.044 + 0.006*SL
D to Y	t_R	0.141	0.082 + 0.029*SL	0.078 + 0.030*SL	0.076 + 0.031*SL
	t_F	0.078	0.059 + 0.010*SL	0.052 + 0.011*SL	0.043 + 0.012*SL
	t_{PLH}	0.097	0.070 + 0.014*SL	0.070 + 0.014*SL	0.070 + 0.014*SL
	t_{PHL}	0.058	0.045 + 0.006*SL	0.047 + 0.006*SL	0.048 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao211d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.076 + 0.014*SL	0.073 + 0.015*SL	0.066 + 0.015*SL
	t_F	0.057	0.044 + 0.006*SL	0.040 + 0.007*SL	0.026 + 0.008*SL
	t_{PLH}	0.052	0.039 + 0.007*SL	0.038 + 0.007*SL	0.038 + 0.007*SL
	t_{PHL}	0.041	0.031 + 0.005*SL	0.035 + 0.004*SL	0.035 + 0.004*SL
B to Y	t_R	0.113	0.085 + 0.014*SL	0.081 + 0.015*SL	0.074 + 0.015*SL
	t_F	0.051	0.037 + 0.007*SL	0.036 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.057	0.044 + 0.006*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.042	0.032 + 0.005*SL	0.035 + 0.004*SL	0.037 + 0.004*SL
C to Y	t_R	0.111	0.083 + 0.014*SL	0.079 + 0.015*SL	0.075 + 0.015*SL
	t_F	0.059	0.047 + 0.006*SL	0.048 + 0.006*SL	0.036 + 0.006*SL
	t_{PLH}	0.080	0.066 + 0.007*SL	0.066 + 0.007*SL	0.067 + 0.007*SL
	t_{PHL}	0.049	0.042 + 0.003*SL	0.044 + 0.003*SL	0.045 + 0.003*SL
D to Y	t_R	0.110	0.082 + 0.014*SL	0.078 + 0.015*SL	0.075 + 0.015*SL
	t_F	0.066	0.053 + 0.006*SL	0.056 + 0.006*SL	0.044 + 0.006*SL
	t_{PLH}	0.083	0.069 + 0.007*SL	0.069 + 0.007*SL	0.070 + 0.007*SL
	t_{PHL}	0.051	0.045 + 0.003*SL	0.046 + 0.003*SL	0.048 + 0.003*SL

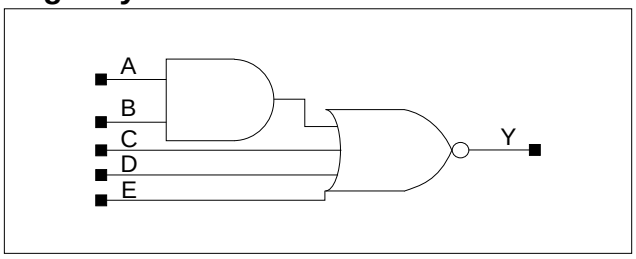
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao211d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.033 + 0.002*SL	0.031 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.124	0.121 + 0.002*SL	0.123 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.102	0.099 + 0.002*SL	0.102 + 0.001*SL	0.110 + 0.001*SL
B to Y	t_R	0.039	0.035 + 0.002*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.026 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.130	0.126 + 0.002*SL	0.129 + 0.001*SL	0.135 + 0.001*SL
	t_{PHL}	0.102	0.099 + 0.002*SL	0.101 + 0.001*SL	0.110 + 0.001*SL
C to Y	t_R	0.039	0.034 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.030	0.027 + 0.001*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.152	0.148 + 0.002*SL	0.151 + 0.001*SL	0.156 + 0.001*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.108 + 0.001*SL
D to Y	t_R	0.039	0.034 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.156	0.152 + 0.002*SL	0.155 + 0.001*SL	0.161 + 0.001*SL
	t_{PHL}	0.105	0.101 + 0.002*SL	0.104 + 0.001*SL	0.113 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other states					1

Cell Data

Input Load (SL)										Gate Count	
ao2111					*ao2111d2*					*ao2111*	*ao2111d2*
A	B	C	D	E	A	B	C	D	E		
0.9	0.9	0.9	1.0	1.0	0.9	0.9	0.9	1.0	1.0	2.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao2111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.178	0.100 + 0.039*SL	0.093 + 0.041*SL	0.097 + 0.041*SL
	t_F	0.078	0.044 + 0.017*SL	0.037 + 0.019*SL	0.030 + 0.019*SL
	t_{PLH}	0.075	0.040 + 0.018*SL	0.037 + 0.018*SL	0.038 + 0.018*SL
	t_{PHL}	0.056	0.037 + 0.010*SL	0.039 + 0.009*SL	0.039 + 0.009*SL
B to Y	t_R	0.187	0.109 + 0.039*SL	0.102 + 0.041*SL	0.105 + 0.041*SL
	t_F	0.077	0.043 + 0.017*SL	0.037 + 0.019*SL	0.030 + 0.019*SL
	t_{PLH}	0.080	0.045 + 0.018*SL	0.043 + 0.018*SL	0.043 + 0.018*SL
	t_{PHL}	0.056	0.037 + 0.010*SL	0.039 + 0.009*SL	0.039 + 0.009*SL
C to Y	t_R	0.192	0.112 + 0.040*SL	0.108 + 0.041*SL	0.106 + 0.041*SL
	t_F	0.081	0.054 + 0.014*SL	0.049 + 0.015*SL	0.042 + 0.015*SL
	t_{PLH}	0.113	0.077 + 0.018*SL	0.077 + 0.018*SL	0.078 + 0.018*SL
	t_{PHL}	0.065	0.049 + 0.008*SL	0.050 + 0.008*SL	0.051 + 0.008*SL
D to Y	t_R	0.191	0.111 + 0.040*SL	0.108 + 0.041*SL	0.107 + 0.041*SL
	t_F	0.091	0.064 + 0.014*SL	0.059 + 0.015*SL	0.052 + 0.015*SL
	t_{PLH}	0.125	0.088 + 0.019*SL	0.089 + 0.018*SL	0.090 + 0.018*SL
	t_{PHL}	0.070	0.053 + 0.008*SL	0.055 + 0.008*SL	0.057 + 0.008*SL
E to Y	t_R	0.191	0.111 + 0.040*SL	0.108 + 0.041*SL	0.107 + 0.041*SL
	t_F	0.099	0.071 + 0.014*SL	0.067 + 0.015*SL	0.062 + 0.015*SL
	t_{PLH}	0.129	0.092 + 0.018*SL	0.092 + 0.018*SL	0.093 + 0.018*SL
	t_{PHL}	0.072	0.055 + 0.008*SL	0.057 + 0.008*SL	0.061 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

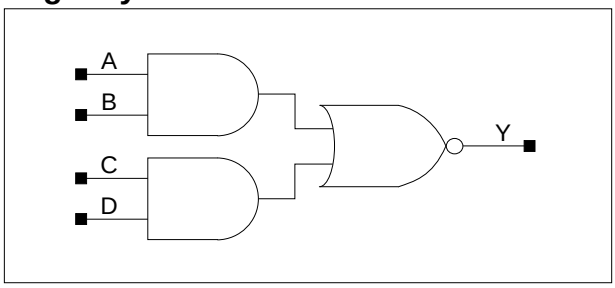
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao2111d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.118 + 0.002*SL
	t_{PHL}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.097 + 0.002*SL
B to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.124	0.118 + 0.003*SL	0.121 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.097 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.159	0.153 + 0.003*SL	0.156 + 0.002*SL	0.159 + 0.002*SL
	t_{PHL}	0.102	0.097 + 0.003*SL	0.100 + 0.002*SL	0.103 + 0.002*SL
D to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.170	0.164 + 0.003*SL	0.167 + 0.002*SL	0.170 + 0.002*SL
	t_{PHL}	0.108	0.102 + 0.003*SL	0.105 + 0.002*SL	0.109 + 0.002*SL
E to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.175	0.168 + 0.003*SL	0.172 + 0.002*SL	0.175 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.109 + 0.002*SL	0.113 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)											
ao22				*ao22d2*				*ao22d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.1	1.1	1.1	2.0	2.3	2.0	2.3	1.1	1.1	1.1	1.1

Gate Count		
ao22	*ao22d2*	*ao22d4*
2.00	3.67	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.098	0.061 + 0.019*SL	0.056 + 0.020*SL	0.046 + 0.020*SL
	t_F	0.066	0.044 + 0.011*SL	0.040 + 0.012*SL	0.029 + 0.012*SL
	t_{PLH}	0.057	0.039 + 0.009*SL	0.039 + 0.009*SL	0.038 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.032 + 0.006*SL	0.033 + 0.006*SL
B to Y	t_R	0.104	0.066 + 0.019*SL	0.061 + 0.020*SL	0.053 + 0.020*SL
	t_F	0.061	0.038 + 0.012*SL	0.037 + 0.012*SL	0.028 + 0.012*SL
	t_{PLH}	0.061	0.043 + 0.009*SL	0.043 + 0.009*SL	0.042 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.033 + 0.006*SL	0.034 + 0.006*SL
C to Y	t_R	0.093	0.053 + 0.020*SL	0.052 + 0.020*SL	0.046 + 0.020*SL
	t_F	0.077	0.055 + 0.011*SL	0.052 + 0.012*SL	0.043 + 0.012*SL
	t_{PLH}	0.071	0.053 + 0.009*SL	0.054 + 0.009*SL	0.054 + 0.009*SL
	t_{PHL}	0.055	0.042 + 0.007*SL	0.044 + 0.006*SL	0.045 + 0.006*SL
D to Y	t_R	0.099	0.060 + 0.020*SL	0.058 + 0.020*SL	0.054 + 0.020*SL
	t_F	0.075	0.053 + 0.011*SL	0.049 + 0.012*SL	0.042 + 0.012*SL
	t_{PLH}	0.076	0.057 + 0.009*SL	0.058 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.056	0.042 + 0.007*SL	0.044 + 0.006*SL	0.046 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao22d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.059 + 0.009*SL	0.057 + 0.010*SL	0.046 + 0.010*SL
	t_F	0.056	0.045 + 0.006*SL	0.044 + 0.006*SL	0.030 + 0.006*SL
	t_{PLH}	0.047	0.038 + 0.005*SL	0.039 + 0.004*SL	0.038 + 0.005*SL
	t_{PHL}	0.035	0.027 + 0.004*SL	0.031 + 0.003*SL	0.033 + 0.003*SL
B to Y	t_R	0.086	0.067 + 0.009*SL	0.065 + 0.010*SL	0.053 + 0.010*SL
	t_F	0.052	0.040 + 0.006*SL	0.039 + 0.006*SL	0.029 + 0.006*SL
	t_{PLH}	0.052	0.043 + 0.005*SL	0.043 + 0.004*SL	0.043 + 0.005*SL
	t_{PHL}	0.036	0.028 + 0.004*SL	0.031 + 0.003*SL	0.034 + 0.003*SL
C to Y	t_R	0.073	0.054 + 0.010*SL	0.053 + 0.010*SL	0.046 + 0.010*SL
	t_F	0.066	0.055 + 0.006*SL	0.054 + 0.006*SL	0.042 + 0.006*SL
	t_{PLH}	0.061	0.052 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.005*SL
	t_{PHL}	0.048	0.041 + 0.003*SL	0.042 + 0.003*SL	0.044 + 0.003*SL
D to Y	t_R	0.079	0.060 + 0.010*SL	0.059 + 0.010*SL	0.053 + 0.010*SL
	t_F	0.061	0.050 + 0.006*SL	0.049 + 0.006*SL	0.041 + 0.006*SL
	t_{PLH}	0.066	0.057 + 0.005*SL	0.057 + 0.005*SL	0.058 + 0.005*SL
	t_{PHL}	0.049	0.041 + 0.004*SL	0.043 + 0.003*SL	0.045 + 0.003*SL

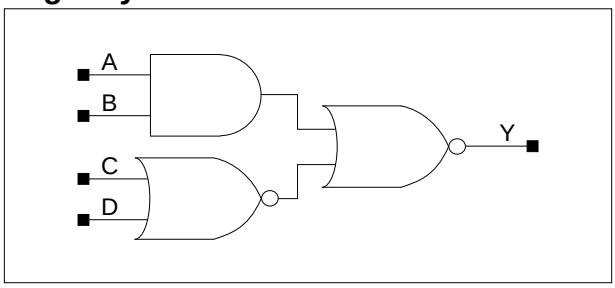
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao22d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.031 + 0.002*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.111	0.107 + 0.002*SL	0.110 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.096	0.093 + 0.002*SL	0.095 + 0.001*SL	0.104 + 0.001*SL
B to Y	t_R	0.036	0.031 + 0.003*SL	0.033 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.116	0.112 + 0.002*SL	0.115 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.096	0.093 + 0.002*SL	0.095 + 0.001*SL	0.104 + 0.001*SL
C to Y	t_R	0.035	0.031 + 0.002*SL	0.030 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.126	0.123 + 0.002*SL	0.125 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.111	0.107 + 0.002*SL	0.110 + 0.001*SL	0.118 + 0.001*SL
D to Y	t_R	0.037	0.032 + 0.003*SL	0.033 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.131	0.127 + 0.002*SL	0.130 + 0.001*SL	0.135 + 0.001*SL
	t_{PHL}	0.110	0.107 + 0.002*SL	0.109 + 0.001*SL	0.118 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
ao22a				*ao22d2a*				*ao22a*	*ao22d2a*
A	B	C	D	A	B	C	D		
1.0	1.1	0.7	0.7	2.1	2.1	1.2	1.2	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao22a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.064 + 0.019*SL	0.058 + 0.020*SL	0.049 + 0.020*SL
	t_F	0.068	0.048 + 0.010*SL	0.040 + 0.012*SL	0.031 + 0.012*SL
	t_{PLH}	0.058	0.040 + 0.009*SL	0.040 + 0.009*SL	0.040 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.033 + 0.006*SL	0.034 + 0.006*SL
B to Y	t_R	0.106	0.069 + 0.019*SL	0.064 + 0.020*SL	0.056 + 0.020*SL
	t_F	0.064	0.039 + 0.013*SL	0.043 + 0.012*SL	0.030 + 0.012*SL
	t_{PLH}	0.062	0.044 + 0.009*SL	0.044 + 0.009*SL	0.044 + 0.009*SL
	t_{PHL}	0.044	0.029 + 0.007*SL	0.033 + 0.006*SL	0.035 + 0.006*SL
C to Y	t_R	0.092	0.051 + 0.020*SL	0.050 + 0.020*SL	0.049 + 0.020*SL
	t_F	0.064	0.046 + 0.009*SL	0.043 + 0.010*SL	0.040 + 0.010*SL
	t_{PLH}	0.090	0.072 + 0.009*SL	0.073 + 0.009*SL	0.074 + 0.009*SL
	t_{PHL}	0.080	0.069 + 0.006*SL	0.071 + 0.005*SL	0.073 + 0.005*SL
D to Y	t_R	0.100	0.061 + 0.020*SL	0.058 + 0.020*SL	0.057 + 0.020*SL
	t_F	0.061	0.041 + 0.010*SL	0.041 + 0.010*SL	0.038 + 0.010*SL
	t_{PLH}	0.094	0.076 + 0.009*SL	0.077 + 0.009*SL	0.077 + 0.009*SL
	t_{PHL}	0.082	0.071 + 0.006*SL	0.073 + 0.005*SL	0.075 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

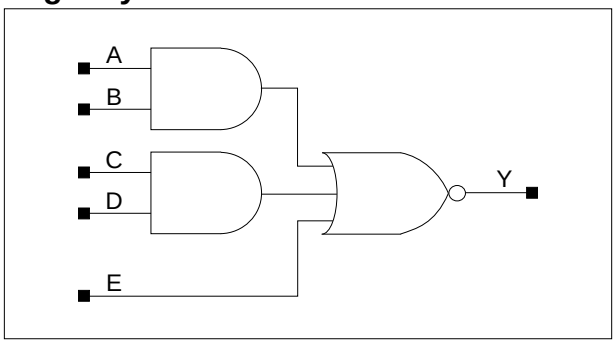
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao22d2a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.064 + 0.009*SL	0.062 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.058	0.049 + 0.005*SL	0.044 + 0.006*SL	0.032 + 0.006*SL
	t_{PLH}	0.049	0.039 + 0.005*SL	0.040 + 0.005*SL	0.040 + 0.005*SL
	t_{PHL}	0.036	0.028 + 0.004*SL	0.032 + 0.003*SL	0.033 + 0.003*SL
B to Y	t_R	0.089	0.071 + 0.009*SL	0.068 + 0.010*SL	0.057 + 0.010*SL
	t_F	0.053	0.043 + 0.005*SL	0.040 + 0.006*SL	0.031 + 0.006*SL
	t_{PLH}	0.053	0.044 + 0.005*SL	0.045 + 0.004*SL	0.044 + 0.005*SL
	t_{PHL}	0.036	0.028 + 0.004*SL	0.032 + 0.003*SL	0.035 + 0.003*SL
C to Y	t_R	0.072	0.053 + 0.010*SL	0.051 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.053	0.045 + 0.004*SL	0.042 + 0.005*SL	0.040 + 0.005*SL
	t_{PLH}	0.080	0.071 + 0.005*SL	0.071 + 0.005*SL	0.073 + 0.005*SL
	t_{PHL}	0.074	0.068 + 0.003*SL	0.069 + 0.003*SL	0.072 + 0.002*SL
D to Y	t_R	0.081	0.061 + 0.010*SL	0.060 + 0.010*SL	0.057 + 0.010*SL
	t_F	0.052	0.043 + 0.005*SL	0.041 + 0.005*SL	0.039 + 0.005*SL
	t_{PLH}	0.085	0.075 + 0.005*SL	0.076 + 0.005*SL	0.077 + 0.005*SL
	t_{PHL}	0.077	0.071 + 0.003*SL	0.072 + 0.003*SL	0.076 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)														
ao221					*ao221d2*					*ao221d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Gate Count		
ao221	*ao221d2*	*ao221d4*
2.67	4.00	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao221

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.147	0.089 + 0.029*SL	0.083 + 0.031*SL	0.082 + 0.031*SL
	t_F	0.077	0.049 + 0.014*SL	0.043 + 0.015*SL	0.033 + 0.016*SL
	t_{PLH}	0.069	0.043 + 0.013*SL	0.041 + 0.014*SL	0.041 + 0.014*SL
	t_{PHL}	0.051	0.035 + 0.008*SL	0.037 + 0.008*SL	0.038 + 0.008*SL
B to Y	t_R	0.155	0.097 + 0.029*SL	0.090 + 0.031*SL	0.090 + 0.031*SL
	t_F	0.073	0.044 + 0.014*SL	0.040 + 0.015*SL	0.033 + 0.016*SL
	t_{PLH}	0.073	0.047 + 0.013*SL	0.045 + 0.014*SL	0.045 + 0.014*SL
	t_{PHL}	0.051	0.034 + 0.008*SL	0.037 + 0.008*SL	0.038 + 0.008*SL
C to Y	t_R	0.148	0.089 + 0.030*SL	0.086 + 0.030*SL	0.083 + 0.031*SL
	t_F	0.093	0.064 + 0.015*SL	0.060 + 0.015*SL	0.053 + 0.016*SL
	t_{PLH}	0.099	0.071 + 0.014*SL	0.072 + 0.014*SL	0.073 + 0.014*SL
	t_{PHL}	0.067	0.051 + 0.008*SL	0.052 + 0.008*SL	0.054 + 0.008*SL
D to Y	t_R	0.156	0.097 + 0.030*SL	0.094 + 0.030*SL	0.091 + 0.031*SL
	t_F	0.091	0.062 + 0.015*SL	0.058 + 0.016*SL	0.053 + 0.016*SL
	t_{PLH}	0.104	0.077 + 0.014*SL	0.077 + 0.014*SL	0.077 + 0.014*SL
	t_{PHL}	0.068	0.051 + 0.008*SL	0.053 + 0.008*SL	0.055 + 0.008*SL
E to Y	t_R	0.156	0.096 + 0.030*SL	0.093 + 0.030*SL	0.091 + 0.031*SL
	t_F	0.089	0.068 + 0.011*SL	0.063 + 0.012*SL	0.056 + 0.012*SL
	t_{PLH}	0.114	0.087 + 0.014*SL	0.087 + 0.014*SL	0.088 + 0.014*SL
	t_{PHL}	0.066	0.052 + 0.007*SL	0.054 + 0.006*SL	0.058 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao221d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.027 + 0.004*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.119	0.113 + 0.003*SL	0.116 + 0.002*SL	0.118 + 0.002*SL
	t_{PHL}	0.097	0.091 + 0.003*SL	0.095 + 0.002*SL	0.099 + 0.002*SL
B to Y	t_R	0.037	0.027 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.124	0.118 + 0.003*SL	0.121 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.097	0.091 + 0.003*SL	0.094 + 0.002*SL	0.098 + 0.002*SL
C to Y	t_R	0.036	0.028 + 0.004*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.145	0.139 + 0.003*SL	0.142 + 0.002*SL	0.144 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.110 + 0.002*SL	0.114 + 0.002*SL
D to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.151	0.145 + 0.003*SL	0.148 + 0.002*SL	0.150 + 0.002*SL
	t_{PHL}	0.113	0.107 + 0.003*SL	0.110 + 0.002*SL	0.114 + 0.002*SL
E to Y	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.013 + 0.004*SL
	t_{PLH}	0.161	0.155 + 0.003*SL	0.158 + 0.002*SL	0.161 + 0.002*SL
	t_{PHL}	0.102	0.096 + 0.003*SL	0.099 + 0.002*SL	0.103 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao221d4

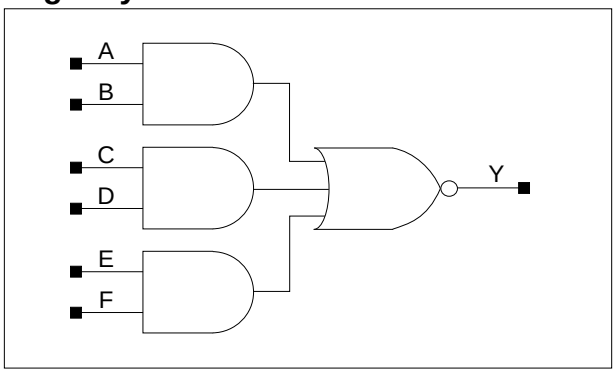
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.036 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.031	0.028 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.134	0.130 + 0.002*SL	0.133 + 0.001*SL	0.139 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.117 + 0.001*SL
B to Y	t_R	0.041	0.038 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.140	0.136 + 0.002*SL	0.138 + 0.001*SL	0.144 + 0.001*SL
	t_{PHL}	0.109	0.106 + 0.002*SL	0.108 + 0.001*SL	0.117 + 0.001*SL
C to Y	t_R	0.040	0.036 + 0.002*SL	0.034 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.160	0.156 + 0.002*SL	0.158 + 0.001*SL	0.165 + 0.001*SL
	t_{PHL}	0.125	0.121 + 0.002*SL	0.124 + 0.001*SL	0.133 + 0.001*SL
D to Y	t_R	0.041	0.036 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.166	0.162 + 0.002*SL	0.165 + 0.001*SL	0.171 + 0.001*SL
	t_{PHL}	0.125	0.121 + 0.002*SL	0.124 + 0.001*SL	0.133 + 0.001*SL
E to Y	t_R	0.039	0.035 + 0.002*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.175	0.172 + 0.002*SL	0.174 + 0.001*SL	0.180 + 0.001*SL
	t_{PHL}	0.113	0.109 + 0.002*SL	0.112 + 0.001*SL	0.120 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ao222/ao222d2/ao222d4

Three 2-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)						Gate Count
ao222						*ao222*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.0	3.33
ao222d2						*ao222d2*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.4	1.0	4.33
ao222d4						*ao222d4*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.0	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.165	0.106 + 0.029*SL	0.101 + 0.031*SL	0.101 + 0.031*SL
	t_F	0.088	0.060 + 0.014*SL	0.054 + 0.015*SL	0.046 + 0.016*SL
	t_{PLH}	0.080	0.053 + 0.014*SL	0.053 + 0.014*SL	0.053 + 0.014*SL
	t_{PHL}	0.057	0.041 + 0.008*SL	0.042 + 0.008*SL	0.043 + 0.008*SL
B to Y	t_R	0.173	0.114 + 0.029*SL	0.109 + 0.031*SL	0.109 + 0.031*SL
	t_F	0.085	0.056 + 0.015*SL	0.053 + 0.015*SL	0.046 + 0.016*SL
	t_{PLH}	0.084	0.057 + 0.014*SL	0.057 + 0.014*SL	0.057 + 0.014*SL
	t_{PHL}	0.057	0.040 + 0.008*SL	0.042 + 0.008*SL	0.044 + 0.008*SL
C to Y	t_R	0.166	0.106 + 0.030*SL	0.103 + 0.031*SL	0.102 + 0.031*SL
	t_F	0.102	0.071 + 0.015*SL	0.070 + 0.015*SL	0.063 + 0.016*SL
	t_{PLH}	0.107	0.079 + 0.014*SL	0.080 + 0.014*SL	0.081 + 0.014*SL
	t_{PHL}	0.071	0.054 + 0.008*SL	0.055 + 0.008*SL	0.057 + 0.008*SL
D to Y	t_R	0.174	0.114 + 0.030*SL	0.112 + 0.031*SL	0.111 + 0.031*SL
	t_F	0.101	0.071 + 0.015*SL	0.069 + 0.016*SL	0.063 + 0.016*SL
	t_{PLH}	0.112	0.084 + 0.014*SL	0.084 + 0.014*SL	0.085 + 0.014*SL
	t_{PHL}	0.071	0.055 + 0.008*SL	0.056 + 0.008*SL	0.058 + 0.008*SL
E to Y	t_R	0.166	0.107 + 0.030*SL	0.104 + 0.030*SL	0.102 + 0.031*SL
	t_F	0.118	0.087 + 0.015*SL	0.086 + 0.016*SL	0.081 + 0.016*SL
	t_{PLH}	0.121	0.094 + 0.014*SL	0.094 + 0.014*SL	0.095 + 0.014*SL
	t_{PHL}	0.081	0.063 + 0.009*SL	0.066 + 0.008*SL	0.070 + 0.008*SL
F to Y	t_R	0.174	0.114 + 0.030*SL	0.112 + 0.031*SL	0.110 + 0.031*SL
	t_F	0.117	0.086 + 0.016*SL	0.086 + 0.016*SL	0.082 + 0.016*SL
	t_{PLH}	0.127	0.099 + 0.014*SL	0.100 + 0.014*SL	0.100 + 0.014*SL
	t_{PHL}	0.082	0.064 + 0.009*SL	0.067 + 0.008*SL	0.071 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao222d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.027 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.123	0.117 + 0.003*SL	0.120 + 0.002*SL	0.123 + 0.002*SL
	t_{PHL}	0.100	0.094 + 0.003*SL	0.097 + 0.002*SL	0.101 + 0.002*SL
B to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.129	0.123 + 0.003*SL	0.126 + 0.002*SL	0.129 + 0.002*SL
	t_{PHL}	0.099	0.093 + 0.003*SL	0.097 + 0.002*SL	0.101 + 0.002*SL
C to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.020 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.154	0.148 + 0.003*SL	0.151 + 0.002*SL	0.154 + 0.002*SL
	t_{PHL}	0.117	0.111 + 0.003*SL	0.115 + 0.002*SL	0.119 + 0.002*SL
D to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.160	0.153 + 0.003*SL	0.157 + 0.002*SL	0.159 + 0.002*SL
	t_{PHL}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.119 + 0.002*SL
E to Y	t_R	0.037	0.027 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.165	0.159 + 0.003*SL	0.162 + 0.002*SL	0.164 + 0.002*SL
	t_{PHL}	0.127	0.121 + 0.003*SL	0.125 + 0.002*SL	0.129 + 0.002*SL
F to Y	t_R	0.037	0.028 + 0.004*SL	0.027 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.171	0.165 + 0.003*SL	0.169 + 0.002*SL	0.171 + 0.002*SL
	t_{PHL}	0.128	0.122 + 0.003*SL	0.126 + 0.002*SL	0.130 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao222d4

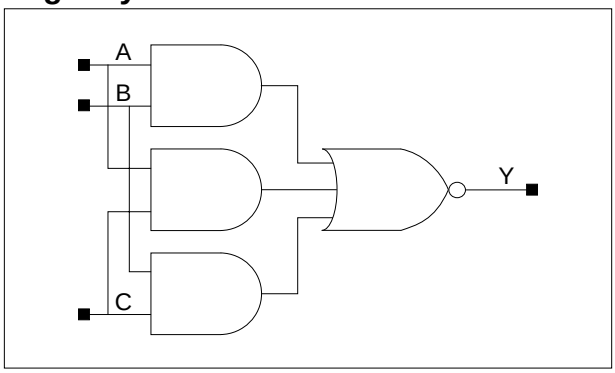
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.036 + 0.003*SL	0.037 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.135	0.131 + 0.002*SL	0.134 + 0.001*SL	0.140 + 0.001*SL
	t_{PHL}	0.110	0.107 + 0.002*SL	0.109 + 0.001*SL	0.118 + 0.001*SL
B to Y	t_R	0.042	0.038 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.141	0.137 + 0.002*SL	0.140 + 0.001*SL	0.145 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.118 + 0.001*SL
C to Y	t_R	0.041	0.036 + 0.003*SL	0.037 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.032	0.029 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.167	0.163 + 0.002*SL	0.166 + 0.001*SL	0.172 + 0.001*SL
	t_{PHL}	0.129	0.125 + 0.002*SL	0.128 + 0.001*SL	0.137 + 0.001*SL
D to Y	t_R	0.042	0.039 + 0.002*SL	0.036 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.172	0.169 + 0.002*SL	0.171 + 0.001*SL	0.177 + 0.001*SL
	t_{PHL}	0.129	0.125 + 0.002*SL	0.128 + 0.001*SL	0.137 + 0.001*SL
E to Y	t_R	0.039	0.035 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.033	0.028 + 0.002*SL	0.030 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.180	0.176 + 0.002*SL	0.179 + 0.001*SL	0.185 + 0.001*SL
	t_{PHL}	0.141	0.138 + 0.002*SL	0.140 + 0.001*SL	0.149 + 0.001*SL
F to Y	t_R	0.041	0.036 + 0.002*SL	0.036 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.035	0.032 + 0.002*SL	0.030 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.186	0.182 + 0.002*SL	0.185 + 0.001*SL	0.191 + 0.001*SL
	t_{PHL}	0.142	0.138 + 0.002*SL	0.141 + 0.001*SL	0.150 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ao222a/ao222d2a

Inverting 2-of-3 Majority with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
ao222a			*ao222d2a*			*ao222a*	*ao222d2a*
A	B	C	A	B	C		
1.7	1.8	2.1	3.5	3.8	4.1	2.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao222a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.139	0.101 + 0.019*SL	0.097 + 0.020*SL	0.089 + 0.020*SL
	t_F	0.092	0.063 + 0.015*SL	0.059 + 0.016*SL	0.054 + 0.016*SL
	t_{PLH}	0.068	0.049 + 0.009*SL	0.049 + 0.009*SL	0.051 + 0.009*SL
	t_{PHL}	0.069	0.053 + 0.008*SL	0.054 + 0.008*SL	0.056 + 0.008*SL
B to Y	t_R	0.136	0.098 + 0.019*SL	0.094 + 0.020*SL	0.090 + 0.020*SL
	t_F	0.098	0.070 + 0.014*SL	0.063 + 0.016*SL	0.059 + 0.016*SL
	t_{PLH}	0.070	0.052 + 0.009*SL	0.052 + 0.009*SL	0.054 + 0.009*SL
	t_{PHL}	0.075	0.059 + 0.008*SL	0.060 + 0.008*SL	0.062 + 0.008*SL
C to Y	t_R	0.127	0.089 + 0.019*SL	0.084 + 0.020*SL	0.079 + 0.020*SL
	t_F	0.098	0.068 + 0.015*SL	0.065 + 0.016*SL	0.060 + 0.016*SL
	t_{PLH}	0.072	0.054 + 0.009*SL	0.054 + 0.009*SL	0.055 + 0.009*SL
	t_{PHL}	0.071	0.055 + 0.008*SL	0.056 + 0.008*SL	0.057 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao222d2a

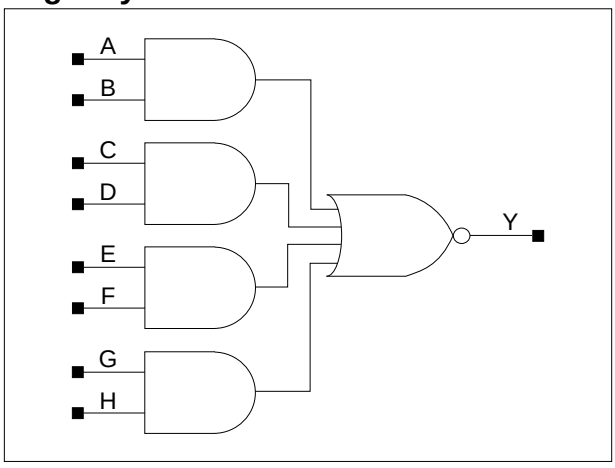
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.120	0.102 + 0.009*SL	0.098 + 0.010*SL	0.088 + 0.010*SL
	t_F	0.076	0.062 + 0.007*SL	0.059 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.058	0.048 + 0.005*SL	0.050 + 0.005*SL	0.051 + 0.005*SL
	t_{PHL}	0.060	0.052 + 0.004*SL	0.052 + 0.004*SL	0.054 + 0.004*SL
B to Y	t_R	0.116	0.097 + 0.010*SL	0.095 + 0.010*SL	0.088 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.066 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.060	0.051 + 0.005*SL	0.051 + 0.005*SL	0.053 + 0.005*SL
	t_{PHL}	0.066	0.058 + 0.004*SL	0.059 + 0.004*SL	0.061 + 0.004*SL
C to Y	t_R	0.106	0.088 + 0.009*SL	0.083 + 0.010*SL	0.077 + 0.010*SL
	t_F	0.081	0.066 + 0.008*SL	0.065 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.062	0.053 + 0.005*SL	0.053 + 0.005*SL	0.053 + 0.005*SL
	t_{PHL}	0.061	0.053 + 0.004*SL	0.054 + 0.004*SL	0.055 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao2222/ao2222d2/ao2222d4

Four 2-ANDs into 4-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	0
x	x	1	1	x	x	x	x	0
x	x	x	x	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
ao2222								*ao2222*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	1.0	0.9	1.0	1.0	1.0	4.00
ao2222d2								*ao2222d2*
A	B	C	D	E	F	G	H	
0.9	0.9	1.0	1.0	1.2	1.0	1.0	1.0	5.33
ao2222d4								*ao2222d4*
A	B	C	D	E	F	G	H	
0.9	1.0	1.1	1.0	1.1	1.0	1.0	1.0	6.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.222	0.141 + 0.040*SL	0.136 + 0.041*SL	0.146 + 0.041*SL
	t_F	0.104	0.069 + 0.017*SL	0.063 + 0.019*SL	0.056 + 0.019*SL
	t_{PLH}	0.086	0.051 + 0.018*SL	0.048 + 0.018*SL	0.049 + 0.018*SL
	t_{PHL}	0.065	0.046 + 0.010*SL	0.046 + 0.009*SL	0.049 + 0.009*SL
B to Y	t_R	0.231	0.150 + 0.040*SL	0.145 + 0.041*SL	0.155 + 0.041*SL
	t_F	0.103	0.068 + 0.017*SL	0.062 + 0.019*SL	0.056 + 0.019*SL
	t_{PLH}	0.091	0.055 + 0.018*SL	0.053 + 0.018*SL	0.054 + 0.018*SL
	t_{PHL}	0.065	0.045 + 0.010*SL	0.047 + 0.009*SL	0.050 + 0.009*SL
C to Y	t_R	0.235	0.154 + 0.040*SL	0.153 + 0.041*SL	0.151 + 0.041*SL
	t_F	0.127	0.091 + 0.018*SL	0.087 + 0.019*SL	0.082 + 0.019*SL
	t_{PLH}	0.134	0.096 + 0.019*SL	0.098 + 0.018*SL	0.099 + 0.018*SL
	t_{PHL}	0.085	0.066 + 0.010*SL	0.067 + 0.009*SL	0.069 + 0.009*SL
D to Y	t_R	0.244	0.163 + 0.040*SL	0.162 + 0.041*SL	0.160 + 0.041*SL
	t_F	0.125	0.089 + 0.018*SL	0.086 + 0.019*SL	0.082 + 0.019*SL
	t_{PLH}	0.139	0.102 + 0.019*SL	0.103 + 0.018*SL	0.104 + 0.018*SL
	t_{PHL}	0.086	0.066 + 0.010*SL	0.068 + 0.009*SL	0.070 + 0.009*SL
E to Y	t_R	0.245	0.165 + 0.040*SL	0.163 + 0.041*SL	0.161 + 0.041*SL
	t_F	0.149	0.112 + 0.019*SL	0.111 + 0.019*SL	0.107 + 0.019*SL
	t_{PLH}	0.167	0.130 + 0.019*SL	0.131 + 0.018*SL	0.133 + 0.018*SL
	t_{PHL}	0.098	0.077 + 0.010*SL	0.080 + 0.010*SL	0.084 + 0.009*SL
F to Y	t_R	0.254	0.174 + 0.040*SL	0.172 + 0.041*SL	0.170 + 0.041*SL
	t_F	0.148	0.110 + 0.019*SL	0.109 + 0.019*SL	0.107 + 0.019*SL
	t_{PLH}	0.173	0.136 + 0.019*SL	0.137 + 0.018*SL	0.138 + 0.018*SL
	t_{PHL}	0.099	0.078 + 0.010*SL	0.081 + 0.010*SL	0.085 + 0.009*SL
G to Y	t_R	0.245	0.166 + 0.040*SL	0.163 + 0.041*SL	0.161 + 0.041*SL
	t_F	0.171	0.133 + 0.019*SL	0.133 + 0.019*SL	0.133 + 0.019*SL
	t_{PLH}	0.181	0.143 + 0.019*SL	0.145 + 0.018*SL	0.147 + 0.018*SL
	t_{PHL}	0.106	0.084 + 0.011*SL	0.088 + 0.010*SL	0.096 + 0.009*SL
H to Y	t_R	0.255	0.175 + 0.040*SL	0.172 + 0.041*SL	0.170 + 0.041*SL
	t_F	0.170	0.132 + 0.019*SL	0.132 + 0.019*SL	0.133 + 0.019*SL
	t_{PLH}	0.187	0.150 + 0.019*SL	0.150 + 0.018*SL	0.152 + 0.018*SL
	t_{PHL}	0.107	0.085 + 0.011*SL	0.089 + 0.010*SL	0.097 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao2222d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.032 + 0.004*SL	0.031 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.142	0.135 + 0.003*SL	0.139 + 0.002*SL	0.142 + 0.002*SL
	t_{PHL}	0.116	0.110 + 0.003*SL	0.113 + 0.002*SL	0.118 + 0.002*SL
B to Y	t_R	0.042	0.033 + 0.004*SL	0.032 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.149	0.142 + 0.003*SL	0.146 + 0.002*SL	0.149 + 0.002*SL
	t_{PHL}	0.116	0.110 + 0.003*SL	0.114 + 0.002*SL	0.118 + 0.002*SL
C to Y	t_R	0.041	0.032 + 0.005*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.184	0.178 + 0.003*SL	0.182 + 0.002*SL	0.185 + 0.002*SL
	t_{PHL}	0.136	0.130 + 0.003*SL	0.134 + 0.002*SL	0.138 + 0.002*SL
D to Y	t_R	0.042	0.034 + 0.004*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.031	0.024 + 0.003*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.189	0.182 + 0.003*SL	0.186 + 0.002*SL	0.189 + 0.002*SL
	t_{PHL}	0.136	0.130 + 0.003*SL	0.133 + 0.002*SL	0.138 + 0.002*SL
E to Y	t_R	0.040	0.031 + 0.005*SL	0.030 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.032	0.025 + 0.003*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.223	0.217 + 0.003*SL	0.221 + 0.002*SL	0.224 + 0.002*SL
	t_{PHL}	0.153	0.147 + 0.003*SL	0.151 + 0.002*SL	0.156 + 0.002*SL
F to Y	t_R	0.043	0.034 + 0.004*SL	0.033 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.032	0.026 + 0.003*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.228	0.222 + 0.003*SL	0.226 + 0.002*SL	0.229 + 0.002*SL
	t_{PHL}	0.153	0.147 + 0.003*SL	0.151 + 0.002*SL	0.156 + 0.002*SL
G to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.034	0.027 + 0.003*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.235	0.228 + 0.003*SL	0.232 + 0.002*SL	0.235 + 0.002*SL
	t_{PHL}	0.162	0.156 + 0.003*SL	0.160 + 0.002*SL	0.165 + 0.002*SL
H to Y	t_R	0.043	0.034 + 0.004*SL	0.033 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.034	0.026 + 0.004*SL	0.027 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.240	0.234 + 0.003*SL	0.238 + 0.002*SL	0.241 + 0.002*SL
	t_{PHL}	0.162	0.156 + 0.003*SL	0.160 + 0.002*SL	0.165 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao2222d4

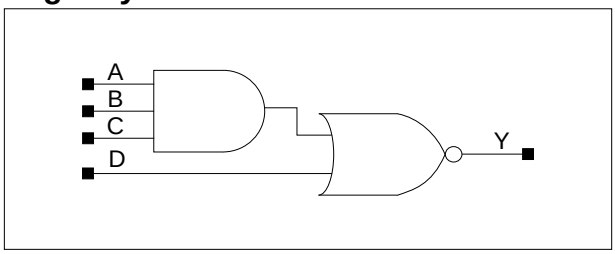
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.041 + 0.002*SL	0.039 + 0.002*SL	0.024 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.147	0.143 + 0.002*SL	0.146 + 0.001*SL	0.153 + 0.001*SL
	t_{PHL}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.130 + 0.001*SL
B to Y	t_R	0.046	0.042 + 0.002*SL	0.041 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.033	0.030 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.154	0.150 + 0.002*SL	0.153 + 0.001*SL	0.160 + 0.001*SL
	t_{PHL}	0.120	0.117 + 0.002*SL	0.119 + 0.001*SL	0.128 + 0.001*SL
C to Y	t_R	0.044	0.040 + 0.002*SL	0.039 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.034	0.030 + 0.002*SL	0.031 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.190	0.186 + 0.002*SL	0.189 + 0.001*SL	0.196 + 0.001*SL
	t_{PHL}	0.143	0.139 + 0.002*SL	0.142 + 0.001*SL	0.151 + 0.001*SL
D to Y	t_R	0.046	0.041 + 0.002*SL	0.041 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.034	0.029 + 0.002*SL	0.031 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.195	0.192 + 0.002*SL	0.194 + 0.001*SL	0.202 + 0.001*SL
	t_{PHL}	0.143	0.139 + 0.002*SL	0.142 + 0.001*SL	0.151 + 0.001*SL
E to Y	t_R	0.044	0.040 + 0.002*SL	0.040 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.037	0.033 + 0.002*SL	0.034 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.231	0.227 + 0.002*SL	0.230 + 0.001*SL	0.238 + 0.001*SL
	t_{PHL}	0.162	0.158 + 0.002*SL	0.161 + 0.001*SL	0.171 + 0.001*SL
F to Y	t_R	0.047	0.042 + 0.002*SL	0.043 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.037	0.032 + 0.002*SL	0.034 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.237	0.233 + 0.002*SL	0.236 + 0.001*SL	0.244 + 0.001*SL
	t_{PHL}	0.163	0.159 + 0.002*SL	0.162 + 0.001*SL	0.171 + 0.001*SL
G to Y	t_R	0.044	0.039 + 0.002*SL	0.040 + 0.002*SL	0.023 + 0.003*SL
	t_F	0.039	0.036 + 0.002*SL	0.035 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.242	0.238 + 0.002*SL	0.241 + 0.001*SL	0.248 + 0.001*SL
	t_{PHL}	0.170	0.167 + 0.002*SL	0.169 + 0.001*SL	0.179 + 0.001*SL
H to Y	t_R	0.047	0.042 + 0.002*SL	0.043 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.039	0.036 + 0.002*SL	0.035 + 0.002*SL	0.025 + 0.002*SL
	t_{PLH}	0.249	0.245 + 0.002*SL	0.248 + 0.001*SL	0.255 + 0.001*SL
	t_{PHL}	0.171	0.168 + 0.002*SL	0.171 + 0.001*SL	0.180 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ao31/ao31d2/ao31d4

3-AND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)												Gate Count		
ao31				*ao31d2*				*ao31d4*				*ao31*	*ao31d2*	*ao31d4*
A	B	C	D	A	B	C	D	A	B	C	D			
1.0	1.0	1.1	1.0	2.0	2.3	2.3	1.9	1.0	1.1	1.1	1.0	2.00	3.67	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.066 + 0.018*SL	0.059 + 0.020*SL	0.050 + 0.020*SL
	t_F	0.087	0.056 + 0.015*SL	0.049 + 0.017*SL	0.040 + 0.018*SL
	t_{PLH}	0.058	0.040 + 0.009*SL	0.040 + 0.009*SL	0.039 + 0.009*SL
	t_{PHL}	0.057	0.039 + 0.009*SL	0.040 + 0.009*SL	0.040 + 0.009*SL
B to Y	t_R	0.108	0.070 + 0.019*SL	0.065 + 0.020*SL	0.057 + 0.020*SL
	t_F	0.083	0.049 + 0.017*SL	0.048 + 0.017*SL	0.041 + 0.018*SL
	t_{PLH}	0.062	0.044 + 0.009*SL	0.044 + 0.009*SL	0.043 + 0.009*SL
	t_{PHL}	0.059	0.041 + 0.009*SL	0.043 + 0.009*SL	0.043 + 0.009*SL
C to Y	t_R	0.114	0.077 + 0.019*SL	0.072 + 0.020*SL	0.063 + 0.020*SL
	t_F	0.081	0.047 + 0.017*SL	0.046 + 0.017*SL	0.041 + 0.018*SL
	t_{PLH}	0.065	0.047 + 0.009*SL	0.047 + 0.009*SL	0.047 + 0.009*SL
	t_{PHL}	0.059	0.041 + 0.009*SL	0.043 + 0.009*SL	0.043 + 0.009*SL
D to Y	t_R	0.109	0.069 + 0.020*SL	0.067 + 0.020*SL	0.064 + 0.020*SL
	t_F	0.075	0.057 + 0.009*SL	0.052 + 0.010*SL	0.043 + 0.011*SL
	t_{PLH}	0.077	0.059 + 0.009*SL	0.059 + 0.009*SL	0.060 + 0.009*SL
	t_{PHL}	0.057	0.046 + 0.006*SL	0.047 + 0.006*SL	0.047 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao31d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.080	0.063 + 0.009*SL	0.058 + 0.010*SL	0.047 + 0.010*SL
	t_F	0.068	0.054 + 0.007*SL	0.048 + 0.009*SL	0.038 + 0.009*SL
	t_{PLH}	0.046	0.037 + 0.005*SL	0.038 + 0.004*SL	0.037 + 0.005*SL
	t_{PHL}	0.046	0.036 + 0.005*SL	0.038 + 0.004*SL	0.038 + 0.004*SL
B to Y	t_R	0.087	0.068 + 0.009*SL	0.066 + 0.010*SL	0.054 + 0.010*SL
	t_F	0.065	0.052 + 0.007*SL	0.045 + 0.009*SL	0.037 + 0.009*SL
	t_{PLH}	0.051	0.042 + 0.005*SL	0.042 + 0.004*SL	0.041 + 0.005*SL
	t_{PHL}	0.048	0.039 + 0.005*SL	0.041 + 0.004*SL	0.042 + 0.004*SL
C to Y	t_R	0.092	0.074 + 0.009*SL	0.070 + 0.010*SL	0.060 + 0.010*SL
	t_F	0.063	0.048 + 0.008*SL	0.044 + 0.009*SL	0.037 + 0.009*SL
	t_{PLH}	0.054	0.045 + 0.005*SL	0.045 + 0.004*SL	0.045 + 0.005*SL
	t_{PHL}	0.048	0.038 + 0.005*SL	0.040 + 0.004*SL	0.041 + 0.004*SL
D to Y	t_R	0.085	0.065 + 0.010*SL	0.065 + 0.010*SL	0.060 + 0.010*SL
	t_F	0.063	0.052 + 0.005*SL	0.053 + 0.005*SL	0.042 + 0.005*SL
	t_{PLH}	0.068	0.058 + 0.005*SL	0.059 + 0.005*SL	0.060 + 0.005*SL
	t_{PHL}	0.051	0.045 + 0.003*SL	0.046 + 0.003*SL	0.047 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao31d4

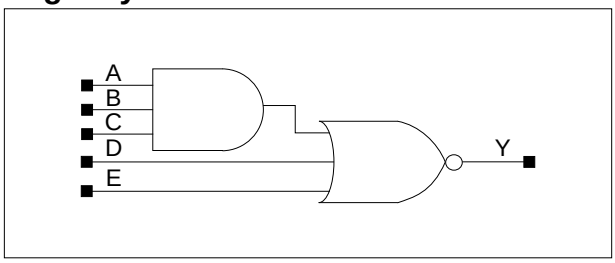
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.028 + 0.003*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.111	0.107 + 0.002*SL	0.110 + 0.001*SL	0.119 + 0.001*SL
B to Y	t_R	0.035	0.030 + 0.003*SL	0.031 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.117	0.113 + 0.002*SL	0.116 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.114	0.110 + 0.002*SL	0.113 + 0.001*SL	0.121 + 0.001*SL
C to Y	t_R	0.035	0.030 + 0.002*SL	0.031 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.121	0.118 + 0.002*SL	0.120 + 0.001*SL	0.125 + 0.001*SL
	t_{PHL}	0.114	0.110 + 0.002*SL	0.113 + 0.001*SL	0.121 + 0.001*SL
D to Y	t_R	0.035	0.031 + 0.002*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.133	0.130 + 0.002*SL	0.132 + 0.001*SL	0.138 + 0.001*SL
	t_{PHL}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.119 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ao311/ao311d2

3-AND into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)									
ao311					*ao311d2*				
A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.1	0.9	1.0	1.0	1.0	1.1	0.9	1.0

Gate Count	
ao311	*ao311d2*
2.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao311

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.154	0.096 + 0.029*SL	0.089 + 0.031*SL	0.088 + 0.031*SL
	t_F	0.087	0.055 + 0.016*SL	0.049 + 0.017*SL	0.043 + 0.018*SL
	t_{PLH}	0.074	0.047 + 0.013*SL	0.046 + 0.014*SL	0.046 + 0.014*SL
	t_{PHL}	0.059	0.041 + 0.009*SL	0.042 + 0.009*SL	0.042 + 0.009*SL
B to Y	t_R	0.163	0.105 + 0.029*SL	0.099 + 0.031*SL	0.098 + 0.031*SL
	t_F	0.086	0.053 + 0.016*SL	0.049 + 0.017*SL	0.042 + 0.018*SL
	t_{PLH}	0.079	0.052 + 0.013*SL	0.052 + 0.014*SL	0.052 + 0.014*SL
	t_{PHL}	0.061	0.043 + 0.009*SL	0.044 + 0.009*SL	0.045 + 0.009*SL
C to Y	t_R	0.173	0.115 + 0.029*SL	0.109 + 0.031*SL	0.108 + 0.031*SL
	t_F	0.084	0.050 + 0.017*SL	0.047 + 0.017*SL	0.042 + 0.018*SL
	t_{PLH}	0.084	0.057 + 0.014*SL	0.057 + 0.014*SL	0.057 + 0.014*SL
	t_{PHL}	0.061	0.043 + 0.009*SL	0.044 + 0.009*SL	0.045 + 0.009*SL
D to Y	t_R	0.173	0.113 + 0.030*SL	0.110 + 0.030*SL	0.109 + 0.031*SL
	t_F	0.086	0.062 + 0.012*SL	0.058 + 0.013*SL	0.051 + 0.013*SL
	t_{PLH}	0.112	0.084 + 0.014*SL	0.085 + 0.014*SL	0.086 + 0.014*SL
	t_{PHL}	0.068	0.055 + 0.007*SL	0.055 + 0.007*SL	0.056 + 0.007*SL
E to Y	t_R	0.172	0.112 + 0.030*SL	0.110 + 0.030*SL	0.109 + 0.031*SL
	t_F	0.094	0.071 + 0.012*SL	0.066 + 0.013*SL	0.060 + 0.013*SL
	t_{PLH}	0.115	0.087 + 0.014*SL	0.088 + 0.014*SL	0.089 + 0.014*SL
	t_{PHL}	0.072	0.057 + 0.007*SL	0.059 + 0.007*SL	0.060 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao311d2

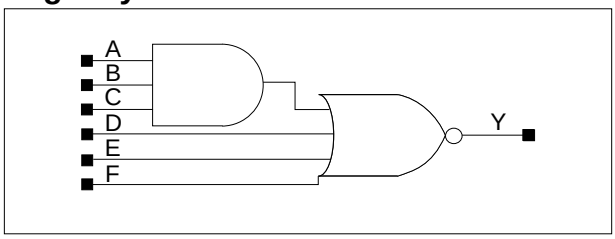
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.119	0.113 + 0.003*SL	0.116 + 0.002*SL	0.118 + 0.002*SL
	t_{PHL}	0.102	0.096 + 0.003*SL	0.099 + 0.002*SL	0.103 + 0.002*SL
B to Y	t_R	0.037	0.027 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.126	0.120 + 0.003*SL	0.123 + 0.002*SL	0.125 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.101 + 0.002*SL	0.105 + 0.002*SL
C to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.028	0.019 + 0.004*SL	0.021 + 0.004*SL	0.013 + 0.004*SL
	t_{PLH}	0.133	0.126 + 0.003*SL	0.130 + 0.002*SL	0.132 + 0.002*SL
	t_{PHL}	0.104	0.098 + 0.003*SL	0.101 + 0.002*SL	0.105 + 0.002*SL
D to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.160	0.153 + 0.003*SL	0.157 + 0.002*SL	0.159 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.104 + 0.002*SL
E to Y	t_R	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.163	0.156 + 0.003*SL	0.160 + 0.002*SL	0.162 + 0.002*SL
	t_{PHL}	0.106	0.100 + 0.003*SL	0.103 + 0.002*SL	0.107 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

ao3111/ao3111d2

3-AND into 4-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)											
ao3111						*ao3111d2*					
A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.0	1.0	0.9	1.0	1.0	1.0	1.0	1.0	0.9	1.0	1.0

Gate Count	
ao3111	*ao3111d2*
3.00	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao3111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.209	0.129 + 0.040*SL	0.124 + 0.041*SL	0.130 + 0.041*SL
	t_F	0.098	0.058 + 0.020*SL	0.056 + 0.021*SL	0.049 + 0.021*SL
	t_{PLH}	0.086	0.050 + 0.018*SL	0.048 + 0.018*SL	0.049 + 0.018*SL
	t_{PHL}	0.066	0.046 + 0.010*SL	0.046 + 0.010*SL	0.046 + 0.010*SL
B to Y	t_R	0.220	0.140 + 0.040*SL	0.136 + 0.041*SL	0.142 + 0.041*SL
	t_F	0.098	0.059 + 0.019*SL	0.054 + 0.021*SL	0.050 + 0.021*SL
	t_{PLH}	0.091	0.055 + 0.018*SL	0.054 + 0.018*SL	0.055 + 0.018*SL
	t_{PHL}	0.069	0.048 + 0.010*SL	0.049 + 0.010*SL	0.050 + 0.010*SL
C to Y	t_R	0.231	0.151 + 0.040*SL	0.147 + 0.041*SL	0.153 + 0.041*SL
	t_F	0.096	0.056 + 0.020*SL	0.053 + 0.021*SL	0.050 + 0.021*SL
	t_{PLH}	0.098	0.061 + 0.018*SL	0.061 + 0.018*SL	0.062 + 0.018*SL
	t_{PHL}	0.069	0.048 + 0.010*SL	0.049 + 0.010*SL	0.050 + 0.010*SL
D to Y	t_R	0.238	0.157 + 0.040*SL	0.156 + 0.041*SL	0.154 + 0.041*SL
	t_F	0.095	0.067 + 0.014*SL	0.064 + 0.015*SL	0.058 + 0.015*SL
	t_{PLH}	0.140	0.102 + 0.019*SL	0.103 + 0.018*SL	0.105 + 0.018*SL
	t_{PHL}	0.075	0.060 + 0.008*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
E to Y	t_R	0.238	0.158 + 0.040*SL	0.156 + 0.041*SL	0.154 + 0.041*SL
	t_F	0.104	0.075 + 0.015*SL	0.074 + 0.015*SL	0.069 + 0.015*SL
	t_{PLH}	0.151	0.114 + 0.019*SL	0.115 + 0.018*SL	0.116 + 0.018*SL
	t_{PHL}	0.080	0.064 + 0.008*SL	0.065 + 0.008*SL	0.067 + 0.008*SL
F to Y	t_R	0.238	0.158 + 0.040*SL	0.155 + 0.041*SL	0.154 + 0.041*SL
	t_F	0.112	0.082 + 0.015*SL	0.083 + 0.015*SL	0.078 + 0.015*SL
	t_{PLH}	0.156	0.119 + 0.019*SL	0.119 + 0.018*SL	0.120 + 0.018*SL
	t_{PHL}	0.084	0.067 + 0.008*SL	0.069 + 0.008*SL	0.072 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao3111d2

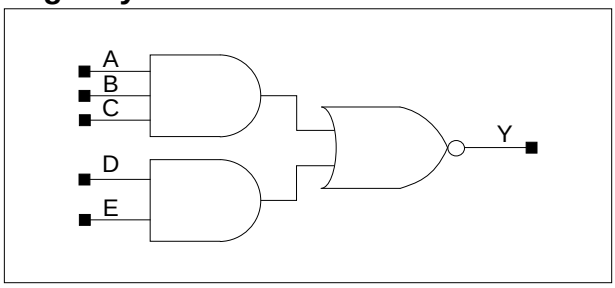
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.031 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.132	0.125 + 0.003*SL	0.129 + 0.002*SL	0.132 + 0.002*SL
	t_{PHL}	0.110	0.103 + 0.003*SL	0.107 + 0.002*SL	0.111 + 0.002*SL
B to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.139	0.133 + 0.003*SL	0.137 + 0.002*SL	0.140 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.109 + 0.002*SL	0.114 + 0.002*SL
C to Y	t_R	0.042	0.033 + 0.004*SL	0.031 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.147	0.141 + 0.003*SL	0.145 + 0.002*SL	0.148 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.109 + 0.002*SL	0.114 + 0.002*SL
D to Y	t_R	0.042	0.033 + 0.004*SL	0.031 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.189	0.183 + 0.003*SL	0.187 + 0.002*SL	0.190 + 0.002*SL
	t_{PHL}	0.115	0.109 + 0.003*SL	0.113 + 0.002*SL	0.117 + 0.002*SL
E to Y	t_R	0.042	0.033 + 0.004*SL	0.031 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.201	0.194 + 0.003*SL	0.198 + 0.002*SL	0.201 + 0.002*SL
	t_{PHL}	0.121	0.115 + 0.003*SL	0.118 + 0.002*SL	0.123 + 0.002*SL
F to Y	t_R	0.041	0.032 + 0.005*SL	0.031 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.029	0.022 + 0.003*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.205	0.199 + 0.003*SL	0.203 + 0.002*SL	0.206 + 0.002*SL
	t_{PHL}	0.125	0.119 + 0.003*SL	0.122 + 0.002*SL	0.126 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao32/ao32d2

3-AND and 2-AND into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
ao32					*ao32d2*					*ao32*	*ao32d2*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	1.1	1.0	1.1	1.1	1.1	1.2	1.1	1.1	2.67	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao32

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.114	0.076 + 0.019*SL	0.071 + 0.020*SL	0.064 + 0.020*SL
	t_F	0.084	0.060 + 0.012*SL	0.053 + 0.014*SL	0.044 + 0.014*SL
	t_{PLH}	0.064	0.046 + 0.009*SL	0.046 + 0.009*SL	0.046 + 0.009*SL
	t_{PHL}	0.051	0.036 + 0.007*SL	0.038 + 0.007*SL	0.039 + 0.007*SL
B to Y	t_R	0.121	0.084 + 0.019*SL	0.078 + 0.020*SL	0.072 + 0.020*SL
	t_F	0.080	0.055 + 0.013*SL	0.050 + 0.014*SL	0.044 + 0.014*SL
	t_{PLH}	0.069	0.051 + 0.009*SL	0.051 + 0.009*SL	0.051 + 0.009*SL
	t_{PHL}	0.053	0.038 + 0.007*SL	0.040 + 0.007*SL	0.042 + 0.007*SL
C to Y	t_R	0.129	0.091 + 0.019*SL	0.086 + 0.020*SL	0.080 + 0.020*SL
	t_F	0.078	0.052 + 0.013*SL	0.048 + 0.014*SL	0.044 + 0.014*SL
	t_{PLH}	0.074	0.056 + 0.009*SL	0.055 + 0.009*SL	0.056 + 0.009*SL
	t_{PHL}	0.053	0.038 + 0.007*SL	0.040 + 0.007*SL	0.041 + 0.007*SL
D to Y	t_R	0.119	0.080 + 0.020*SL	0.077 + 0.020*SL	0.074 + 0.020*SL
	t_F	0.097	0.074 + 0.012*SL	0.071 + 0.012*SL	0.063 + 0.013*SL
	t_{PLH}	0.087	0.069 + 0.009*SL	0.069 + 0.009*SL	0.070 + 0.009*SL
	t_{PHL}	0.066	0.052 + 0.007*SL	0.053 + 0.006*SL	0.055 + 0.006*SL
E to Y	t_R	0.126	0.087 + 0.020*SL	0.084 + 0.020*SL	0.081 + 0.020*SL
	t_F	0.095	0.071 + 0.012*SL	0.070 + 0.012*SL	0.063 + 0.013*SL
	t_{PLH}	0.091	0.073 + 0.009*SL	0.074 + 0.009*SL	0.074 + 0.009*SL
	t_{PHL}	0.066	0.053 + 0.007*SL	0.054 + 0.006*SL	0.056 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao32d2

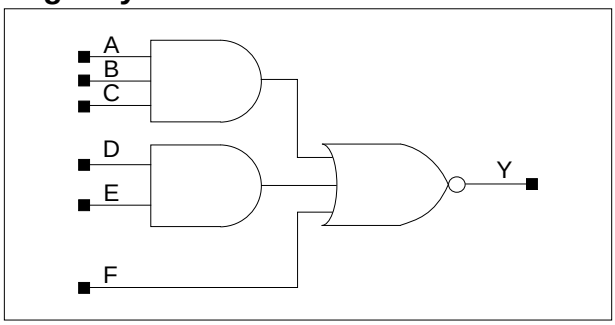
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.024 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.106	0.100 + 0.003*SL	0.103 + 0.002*SL	0.104 + 0.002*SL
	t_{PHL}	0.094	0.088 + 0.003*SL	0.091 + 0.002*SL	0.095 + 0.002*SL
B to Y	t_R	0.034	0.024 + 0.005*SL	0.024 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.112	0.106 + 0.003*SL	0.109 + 0.002*SL	0.111 + 0.002*SL
	t_{PHL}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.097 + 0.002*SL
C to Y	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.028	0.019 + 0.004*SL	0.021 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.117 + 0.002*SL
	t_{PHL}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.097 + 0.002*SL
D to Y	t_R	0.034	0.025 + 0.005*SL	0.024 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.131	0.125 + 0.003*SL	0.128 + 0.002*SL	0.130 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.109 + 0.002*SL	0.113 + 0.002*SL
E to Y	t_R	0.035	0.026 + 0.004*SL	0.024 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.021 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.136	0.130 + 0.003*SL	0.133 + 0.002*SL	0.135 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.108 + 0.002*SL	0.113 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao321/ao321d2

3-AND and 2-AND into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)											
ao321						*ao321d2*					
A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.1	1.1	1.0	1.0	1.0

Gate Count	
ao321	*ao321d2*
3.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao321

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.169	0.110 + 0.029*SL	0.105 + 0.031*SL	0.106 + 0.031*SL
	t_F	0.097	0.066 + 0.016*SL	0.060 + 0.017*SL	0.052 + 0.018*SL
	t_{PLH}	0.078	0.052 + 0.013*SL	0.050 + 0.014*SL	0.051 + 0.014*SL
	t_{PHL}	0.061	0.044 + 0.009*SL	0.044 + 0.009*SL	0.045 + 0.009*SL
B to Y	t_R	0.179	0.120 + 0.029*SL	0.114 + 0.031*SL	0.116 + 0.031*SL
	t_F	0.095	0.062 + 0.016*SL	0.058 + 0.017*SL	0.052 + 0.018*SL
	t_{PLH}	0.083	0.056 + 0.014*SL	0.056 + 0.014*SL	0.056 + 0.014*SL
	t_{PHL}	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.048 + 0.009*SL
C to Y	t_R	0.188	0.129 + 0.030*SL	0.124 + 0.031*SL	0.126 + 0.031*SL
	t_F	0.093	0.059 + 0.017*SL	0.057 + 0.017*SL	0.052 + 0.018*SL
	t_{PLH}	0.089	0.062 + 0.014*SL	0.061 + 0.014*SL	0.062 + 0.014*SL
	t_{PHL}	0.063	0.045 + 0.009*SL	0.047 + 0.009*SL	0.048 + 0.009*SL
D to Y	t_R	0.183	0.122 + 0.030*SL	0.122 + 0.030*SL	0.119 + 0.031*SL
	t_F	0.108	0.078 + 0.015*SL	0.076 + 0.016*SL	0.071 + 0.016*SL
	t_{PLH}	0.120	0.092 + 0.014*SL	0.093 + 0.014*SL	0.094 + 0.014*SL
	t_{PHL}	0.078	0.062 + 0.008*SL	0.063 + 0.008*SL	0.064 + 0.008*SL
E to Y	t_R	0.191	0.131 + 0.030*SL	0.129 + 0.030*SL	0.128 + 0.031*SL
	t_F	0.107	0.077 + 0.015*SL	0.074 + 0.016*SL	0.070 + 0.016*SL
	t_{PLH}	0.124	0.096 + 0.014*SL	0.097 + 0.014*SL	0.098 + 0.014*SL
	t_{PHL}	0.078	0.062 + 0.008*SL	0.063 + 0.008*SL	0.065 + 0.008*SL
F to Y	t_R	0.191	0.131 + 0.030*SL	0.129 + 0.030*SL	0.128 + 0.031*SL
	t_F	0.113	0.089 + 0.012*SL	0.085 + 0.013*SL	0.081 + 0.013*SL
	t_{PLH}	0.133	0.106 + 0.014*SL	0.106 + 0.014*SL	0.107 + 0.014*SL
	t_{PHL}	0.079	0.064 + 0.007*SL	0.066 + 0.007*SL	0.070 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

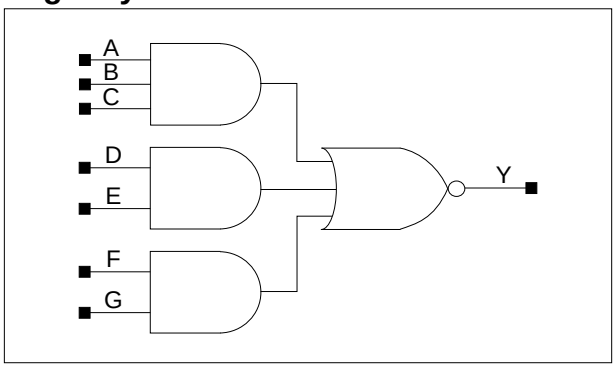
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao321d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.124	0.118 + 0.003*SL	0.121 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.106	0.100 + 0.003*SL	0.103 + 0.002*SL	0.108 + 0.002*SL
B to Y	t_R	0.038	0.028 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.131	0.125 + 0.003*SL	0.128 + 0.002*SL	0.131 + 0.002*SL
	t_{PHL}	0.108	0.103 + 0.003*SL	0.106 + 0.002*SL	0.110 + 0.002*SL
C to Y	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.138	0.132 + 0.003*SL	0.135 + 0.002*SL	0.138 + 0.002*SL
	t_{PHL}	0.108	0.102 + 0.003*SL	0.105 + 0.002*SL	0.110 + 0.002*SL
D to Y	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.168	0.162 + 0.003*SL	0.165 + 0.002*SL	0.168 + 0.002*SL
	t_{PHL}	0.126	0.120 + 0.003*SL	0.124 + 0.002*SL	0.128 + 0.002*SL
E to Y	t_R	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.174	0.167 + 0.003*SL	0.171 + 0.002*SL	0.173 + 0.002*SL
	t_{PHL}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.128 + 0.002*SL
F to Y	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.184	0.178 + 0.003*SL	0.181 + 0.002*SL	0.183 + 0.002*SL
	t_{PHL}	0.115	0.109 + 0.003*SL	0.113 + 0.002*SL	0.117 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	x	x	0
x	x	x	x	x	1	1	0
Other States							1

Cell Data

Input Load (SL)						
ao322						
A	B	C	D	E	F	G
1.0	1.1	1.1	1.0	1.0	1.0	1.1
ao322d2						
A	B	C	D	E	F	G
1.0	1.1	1.1	1.0	1.0	1.0	1.1

Gate Count	
ao322	*ao322d2*
3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.179	0.120 + 0.030*SL	0.115 + 0.031*SL	0.117 + 0.031*SL
	t_F	0.104	0.071 + 0.016*SL	0.067 + 0.017*SL	0.060 + 0.018*SL
	t_{PLH}	0.083	0.056 + 0.013*SL	0.055 + 0.014*SL	0.056 + 0.014*SL
	t_{PHL}	0.063	0.046 + 0.009*SL	0.046 + 0.009*SL	0.048 + 0.009*SL
B to Y	t_R	0.189	0.130 + 0.030*SL	0.126 + 0.031*SL	0.128 + 0.031*SL
	t_F	0.102	0.070 + 0.016*SL	0.065 + 0.017*SL	0.060 + 0.018*SL
	t_{PLH}	0.089	0.062 + 0.014*SL	0.061 + 0.014*SL	0.061 + 0.014*SL
	t_{PHL}	0.066	0.048 + 0.009*SL	0.049 + 0.009*SL	0.051 + 0.009*SL
C to Y	t_R	0.199	0.139 + 0.030*SL	0.135 + 0.031*SL	0.137 + 0.031*SL
	t_F	0.101	0.069 + 0.016*SL	0.063 + 0.018*SL	0.060 + 0.018*SL
	t_{PLH}	0.095	0.067 + 0.014*SL	0.067 + 0.014*SL	0.068 + 0.014*SL
	t_{PHL}	0.066	0.048 + 0.009*SL	0.049 + 0.009*SL	0.051 + 0.009*SL
D to Y	t_R	0.195	0.135 + 0.030*SL	0.133 + 0.031*SL	0.131 + 0.031*SL
	t_F	0.121	0.091 + 0.015*SL	0.089 + 0.015*SL	0.083 + 0.016*SL
	t_{PLH}	0.126	0.098 + 0.014*SL	0.099 + 0.014*SL	0.100 + 0.014*SL
	t_{PHL}	0.080	0.064 + 0.008*SL	0.065 + 0.008*SL	0.068 + 0.008*SL
E to Y	t_R	0.203	0.142 + 0.030*SL	0.141 + 0.031*SL	0.140 + 0.031*SL
	t_F	0.119	0.089 + 0.015*SL	0.088 + 0.016*SL	0.083 + 0.016*SL
	t_{PLH}	0.130	0.103 + 0.014*SL	0.103 + 0.014*SL	0.104 + 0.014*SL
	t_{PHL}	0.080	0.064 + 0.008*SL	0.065 + 0.008*SL	0.068 + 0.008*SL
F to Y	t_R	0.195	0.135 + 0.030*SL	0.132 + 0.031*SL	0.131 + 0.031*SL
	t_F	0.142	0.111 + 0.015*SL	0.110 + 0.016*SL	0.105 + 0.016*SL
	t_{PLH}	0.141	0.113 + 0.014*SL	0.114 + 0.014*SL	0.115 + 0.014*SL
	t_{PHL}	0.091	0.073 + 0.009*SL	0.076 + 0.008*SL	0.080 + 0.008*SL
G to Y	t_R	0.203	0.142 + 0.030*SL	0.141 + 0.031*SL	0.140 + 0.031*SL
	t_F	0.140	0.109 + 0.015*SL	0.109 + 0.016*SL	0.105 + 0.016*SL
	t_{PLH}	0.145	0.118 + 0.014*SL	0.118 + 0.014*SL	0.119 + 0.014*SL
	t_{PHL}	0.091	0.074 + 0.009*SL	0.076 + 0.008*SL	0.081 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao322d2

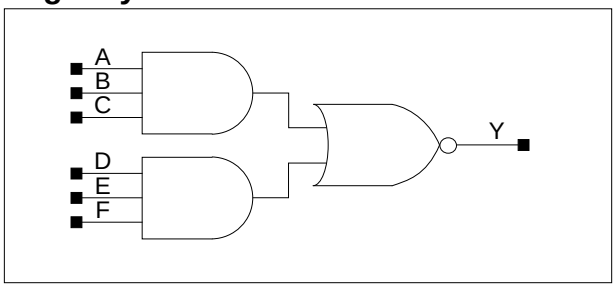
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.132	0.125 + 0.003*SL	0.129 + 0.002*SL	0.131 + 0.002*SL
	t_{PHL}	0.110	0.104 + 0.003*SL	0.108 + 0.002*SL	0.112 + 0.002*SL
B to Y	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.138	0.132 + 0.003*SL	0.136 + 0.002*SL	0.138 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.110 + 0.002*SL	0.114 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.145	0.139 + 0.003*SL	0.142 + 0.002*SL	0.145 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.110 + 0.002*SL	0.114 + 0.002*SL
D to Y	t_R	0.038	0.029 + 0.005*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.175	0.169 + 0.003*SL	0.172 + 0.002*SL	0.175 + 0.002*SL
	t_{PHL}	0.130	0.124 + 0.003*SL	0.127 + 0.002*SL	0.132 + 0.002*SL
E to Y	t_R	0.040	0.031 + 0.005*SL	0.030 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.181	0.175 + 0.003*SL	0.178 + 0.002*SL	0.181 + 0.002*SL
	t_{PHL}	0.131	0.124 + 0.003*SL	0.128 + 0.002*SL	0.133 + 0.002*SL
F to Y	t_R	0.038	0.029 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.187	0.181 + 0.003*SL	0.184 + 0.002*SL	0.187 + 0.002*SL
	t_{PHL}	0.141	0.135 + 0.003*SL	0.138 + 0.002*SL	0.143 + 0.002*SL
G to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.194	0.188 + 0.003*SL	0.191 + 0.002*SL	0.194 + 0.002*SL
	t_{PHL}	0.143	0.136 + 0.003*SL	0.140 + 0.002*SL	0.145 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao33/ao33d2

Two 3-ANDs into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)					
ao33					
A	B	C	D	E	F
1.1	1.1	1.1	1.1	1.1	1.2
ao33d2					
A	B	C	D	E	F
1.1	1.1	1.1	1.1	1.2	1.2

Gate Count	
ao33	*ao33d2*
3.00	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.122	0.085 + 0.019*SL	0.078 + 0.020*SL	0.073 + 0.020*SL
	t_F	0.094	0.068 + 0.013*SL	0.065 + 0.013*SL	0.054 + 0.014*SL
	t_{PLH}	0.069	0.051 + 0.009*SL	0.051 + 0.009*SL	0.051 + 0.009*SL
	t_{PHL}	0.051	0.036 + 0.007*SL	0.037 + 0.007*SL	0.039 + 0.007*SL
B to Y	t_R	0.129	0.091 + 0.019*SL	0.087 + 0.020*SL	0.082 + 0.020*SL
	t_F	0.090	0.064 + 0.013*SL	0.060 + 0.014*SL	0.054 + 0.014*SL
	t_{PLH}	0.074	0.056 + 0.009*SL	0.056 + 0.009*SL	0.057 + 0.009*SL
	t_{PHL}	0.053	0.039 + 0.007*SL	0.040 + 0.007*SL	0.042 + 0.007*SL
C to Y	t_R	0.137	0.099 + 0.019*SL	0.094 + 0.020*SL	0.090 + 0.020*SL
	t_F	0.088	0.062 + 0.013*SL	0.059 + 0.014*SL	0.054 + 0.014*SL
	t_{PLH}	0.079	0.061 + 0.009*SL	0.061 + 0.009*SL	0.062 + 0.009*SL
	t_{PHL}	0.053	0.038 + 0.007*SL	0.040 + 0.007*SL	0.042 + 0.007*SL
D to Y	t_R	0.120	0.081 + 0.019*SL	0.077 + 0.020*SL	0.074 + 0.020*SL
	t_F	0.111	0.086 + 0.012*SL	0.080 + 0.014*SL	0.074 + 0.014*SL
	t_{PLH}	0.089	0.071 + 0.009*SL	0.072 + 0.009*SL	0.073 + 0.009*SL
	t_{PHL}	0.069	0.055 + 0.007*SL	0.056 + 0.007*SL	0.058 + 0.007*SL
E to Y	t_R	0.128	0.089 + 0.019*SL	0.085 + 0.020*SL	0.083 + 0.020*SL
	t_F	0.109	0.083 + 0.013*SL	0.080 + 0.014*SL	0.074 + 0.014*SL
	t_{PLH}	0.095	0.077 + 0.009*SL	0.077 + 0.009*SL	0.078 + 0.009*SL
	t_{PHL}	0.072	0.058 + 0.007*SL	0.059 + 0.007*SL	0.062 + 0.007*SL
F to Y	t_R	0.134	0.094 + 0.020*SL	0.093 + 0.020*SL	0.091 + 0.020*SL
	t_F	0.106	0.078 + 0.014*SL	0.078 + 0.014*SL	0.074 + 0.014*SL
	t_{PLH}	0.100	0.081 + 0.009*SL	0.082 + 0.009*SL	0.083 + 0.009*SL
	t_{PHL}	0.072	0.058 + 0.007*SL	0.059 + 0.007*SL	0.061 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

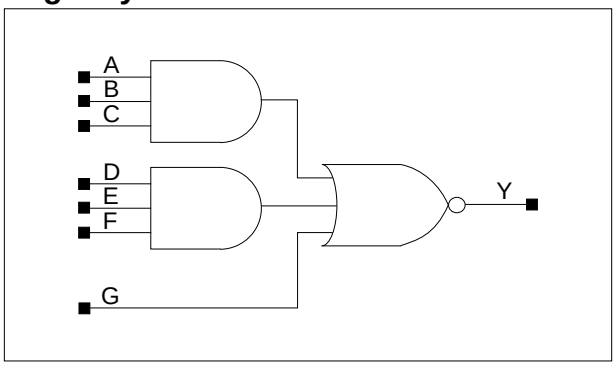
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao33d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.025 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.115	0.109 + 0.003*SL	0.112 + 0.002*SL	0.114 + 0.002*SL
	t_{PHL}	0.099	0.093 + 0.003*SL	0.097 + 0.002*SL	0.101 + 0.002*SL
B to Y	t_R	0.034	0.025 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.121	0.115 + 0.003*SL	0.118 + 0.002*SL	0.120 + 0.002*SL
	t_{PHL}	0.101	0.095 + 0.003*SL	0.099 + 0.002*SL	0.103 + 0.002*SL
C to Y	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.126 + 0.002*SL
	t_{PHL}	0.101	0.095 + 0.003*SL	0.099 + 0.002*SL	0.103 + 0.002*SL
D to Y	t_R	0.034	0.025 + 0.004*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.134	0.128 + 0.003*SL	0.131 + 0.002*SL	0.133 + 0.002*SL
	t_{PHL}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.120 + 0.002*SL
E to Y	t_R	0.033	0.023 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.029	0.020 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.140	0.134 + 0.003*SL	0.137 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.120	0.114 + 0.003*SL	0.118 + 0.002*SL	0.122 + 0.002*SL
F to Y	t_R	0.035	0.026 + 0.005*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.146	0.140 + 0.003*SL	0.143 + 0.002*SL	0.145 + 0.002*SL
	t_{PHL}	0.119	0.113 + 0.003*SL	0.116 + 0.002*SL	0.121 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)						
ao331						
A	B	C	D	E	F	G
1.0	1.1	1.0	1.0	1.0	1.1	1.0
ao331d2						
A	B	C	D	E	F	G
1.0	1.1	1.1	1.0	1.0	1.1	1.0

Gate Count	
ao331	*ao331d2*
3.33	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao331

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.183	0.123 + 0.030*SL	0.120 + 0.031*SL	0.122 + 0.031*SL
	t_F	0.108	0.077 + 0.016*SL	0.070 + 0.017*SL	0.063 + 0.018*SL
	t_{PLH}	0.084	0.057 + 0.013*SL	0.056 + 0.014*SL	0.057 + 0.014*SL
	t_{PHL}	0.062	0.044 + 0.009*SL	0.045 + 0.009*SL	0.046 + 0.009*SL
B to Y	t_R	0.193	0.134 + 0.030*SL	0.130 + 0.031*SL	0.132 + 0.031*SL
	t_F	0.105	0.073 + 0.016*SL	0.069 + 0.017*SL	0.063 + 0.018*SL
	t_{PLH}	0.089	0.062 + 0.014*SL	0.062 + 0.014*SL	0.063 + 0.014*SL
	t_{PHL}	0.064	0.046 + 0.009*SL	0.048 + 0.009*SL	0.050 + 0.009*SL
C to Y	t_R	0.203	0.143 + 0.030*SL	0.140 + 0.031*SL	0.142 + 0.031*SL
	t_F	0.103	0.070 + 0.017*SL	0.067 + 0.017*SL	0.062 + 0.018*SL
	t_{PLH}	0.095	0.068 + 0.014*SL	0.068 + 0.014*SL	0.069 + 0.014*SL
	t_{PHL}	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.050 + 0.009*SL
D to Y	t_R	0.189	0.129 + 0.030*SL	0.128 + 0.030*SL	0.125 + 0.031*SL
	t_F	0.126	0.092 + 0.017*SL	0.090 + 0.017*SL	0.085 + 0.018*SL
	t_{PLH}	0.124	0.096 + 0.014*SL	0.097 + 0.014*SL	0.099 + 0.014*SL
	t_{PHL}	0.086	0.068 + 0.009*SL	0.069 + 0.009*SL	0.071 + 0.009*SL
E to Y	t_R	0.199	0.139 + 0.030*SL	0.137 + 0.030*SL	0.135 + 0.031*SL
	t_F	0.125	0.090 + 0.017*SL	0.089 + 0.018*SL	0.085 + 0.018*SL
	t_{PLH}	0.130	0.102 + 0.014*SL	0.103 + 0.014*SL	0.104 + 0.014*SL
	t_{PHL}	0.089	0.071 + 0.009*SL	0.072 + 0.009*SL	0.074 + 0.009*SL
F to Y	t_R	0.209	0.149 + 0.030*SL	0.147 + 0.030*SL	0.145 + 0.031*SL
	t_F	0.123	0.089 + 0.017*SL	0.087 + 0.018*SL	0.086 + 0.018*SL
	t_{PLH}	0.136	0.109 + 0.014*SL	0.109 + 0.014*SL	0.111 + 0.014*SL
	t_{PHL}	0.089	0.071 + 0.009*SL	0.073 + 0.009*SL	0.074 + 0.009*SL
G to Y	t_R	0.209	0.149 + 0.030*SL	0.147 + 0.031*SL	0.145 + 0.031*SL
	t_F	0.126	0.100 + 0.013*SL	0.098 + 0.014*SL	0.093 + 0.014*SL
	t_{PLH}	0.149	0.121 + 0.014*SL	0.122 + 0.014*SL	0.124 + 0.014*SL
	t_{PHL}	0.084	0.068 + 0.008*SL	0.070 + 0.007*SL	0.075 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao331d2

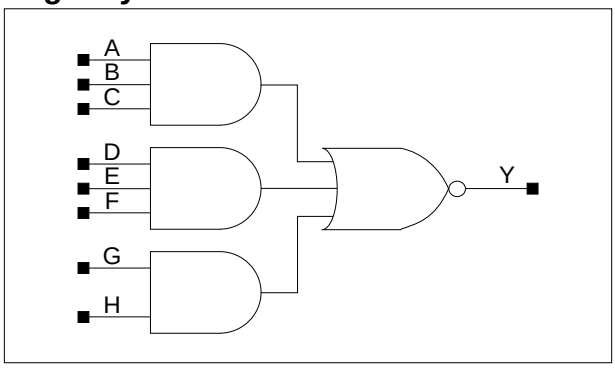
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.133	0.127 + 0.003*SL	0.130 + 0.002*SL	0.133 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.109 + 0.002*SL	0.113 + 0.002*SL
B to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.034	0.026 + 0.004*SL	0.026 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.140	0.134 + 0.003*SL	0.137 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.111	0.104 + 0.003*SL	0.109 + 0.002*SL	0.111 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.147	0.140 + 0.003*SL	0.144 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.110	0.104 + 0.003*SL	0.108 + 0.002*SL	0.112 + 0.002*SL
D to Y	t_R	0.038	0.029 + 0.005*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.173	0.166 + 0.003*SL	0.170 + 0.002*SL	0.172 + 0.002*SL
	t_{PHL}	0.137	0.131 + 0.003*SL	0.134 + 0.002*SL	0.139 + 0.002*SL
E to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.180	0.173 + 0.003*SL	0.177 + 0.002*SL	0.180 + 0.002*SL
	t_{PHL}	0.140	0.133 + 0.003*SL	0.137 + 0.002*SL	0.142 + 0.002*SL
F to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.187	0.181 + 0.003*SL	0.184 + 0.002*SL	0.187 + 0.002*SL
	t_{PHL}	0.140	0.133 + 0.003*SL	0.137 + 0.002*SL	0.142 + 0.002*SL
G to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.200	0.194 + 0.003*SL	0.198 + 0.002*SL	0.200 + 0.002*SL
	t_{PHL}	0.119	0.113 + 0.003*SL	0.116 + 0.002*SL	0.120 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ao332/ao332d2

Two 3-ANDs and 2-AND into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	x	x	x	x	x	0
x	x	x	1	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)							
ao332							
A	B	C	D	E	F	G	H
1.0	1.0	1.0	1.0	1.1	1.1	1.0	1.0
ao332d2							
A	B	C	D	E	F	G	H
1.0	1.1	1.1	1.0	1.1	1.1	1.0	1.0

Gate Count	
ao332	*ao332d2*
3.67	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao332

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.187	0.127 + 0.030*SL	0.123 + 0.031*SL	0.126 + 0.031*SL
	t_F	0.117	0.085 + 0.016*SL	0.079 + 0.017*SL	0.071 + 0.018*SL
	t_{PLH}	0.085	0.058 + 0.013*SL	0.057 + 0.014*SL	0.058 + 0.014*SL
	t_{PHL}	0.065	0.047 + 0.009*SL	0.047 + 0.009*SL	0.050 + 0.009*SL
B to Y	t_R	0.197	0.137 + 0.030*SL	0.133 + 0.031*SL	0.136 + 0.031*SL
	t_F	0.114	0.081 + 0.017*SL	0.078 + 0.017*SL	0.072 + 0.018*SL
	t_{PLH}	0.090	0.063 + 0.014*SL	0.062 + 0.014*SL	0.063 + 0.014*SL
	t_{PHL}	0.067	0.049 + 0.009*SL	0.050 + 0.009*SL	0.053 + 0.009*SL
C to Y	t_R	0.206	0.146 + 0.030*SL	0.143 + 0.031*SL	0.146 + 0.031*SL
	t_F	0.112	0.078 + 0.017*SL	0.077 + 0.017*SL	0.072 + 0.018*SL
	t_{PLH}	0.096	0.068 + 0.014*SL	0.069 + 0.014*SL	0.070 + 0.014*SL
	t_{PHL}	0.067	0.049 + 0.009*SL	0.050 + 0.009*SL	0.053 + 0.009*SL
D to Y	t_R	0.202	0.141 + 0.030*SL	0.140 + 0.030*SL	0.138 + 0.031*SL
	t_F	0.141	0.106 + 0.017*SL	0.105 + 0.017*SL	0.100 + 0.018*SL
	t_{PLH}	0.131	0.103 + 0.014*SL	0.104 + 0.014*SL	0.106 + 0.014*SL
	t_{PHL}	0.089	0.071 + 0.009*SL	0.073 + 0.009*SL	0.075 + 0.009*SL
E to Y	t_R	0.212	0.151 + 0.030*SL	0.150 + 0.031*SL	0.149 + 0.031*SL
	t_F	0.140	0.106 + 0.017*SL	0.103 + 0.018*SL	0.100 + 0.018*SL
	t_{PLH}	0.137	0.109 + 0.014*SL	0.110 + 0.014*SL	0.111 + 0.014*SL
	t_{PHL}	0.092	0.074 + 0.009*SL	0.075 + 0.009*SL	0.078 + 0.009*SL
F to Y	t_R	0.221	0.160 + 0.030*SL	0.160 + 0.031*SL	0.158 + 0.031*SL
	t_F	0.139	0.105 + 0.017*SL	0.103 + 0.018*SL	0.100 + 0.018*SL
	t_{PLH}	0.143	0.115 + 0.014*SL	0.116 + 0.014*SL	0.117 + 0.014*SL
	t_{PHL}	0.092	0.074 + 0.009*SL	0.076 + 0.009*SL	0.078 + 0.009*SL
G to Y	t_R	0.212	0.152 + 0.030*SL	0.151 + 0.030*SL	0.149 + 0.031*SL
	t_F	0.151	0.121 + 0.015*SL	0.119 + 0.016*SL	0.115 + 0.016*SL
	t_{PLH}	0.156	0.128 + 0.014*SL	0.129 + 0.014*SL	0.130 + 0.014*SL
	t_{PHL}	0.093	0.075 + 0.009*SL	0.078 + 0.008*SL	0.083 + 0.008*SL
H to Y	t_R	0.221	0.160 + 0.030*SL	0.159 + 0.031*SL	0.158 + 0.031*SL
	t_F	0.150	0.119 + 0.015*SL	0.118 + 0.016*SL	0.115 + 0.016*SL
	t_{PLH}	0.161	0.134 + 0.014*SL	0.134 + 0.014*SL	0.136 + 0.014*SL
	t_{PHL}	0.094	0.076 + 0.009*SL	0.079 + 0.008*SL	0.085 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

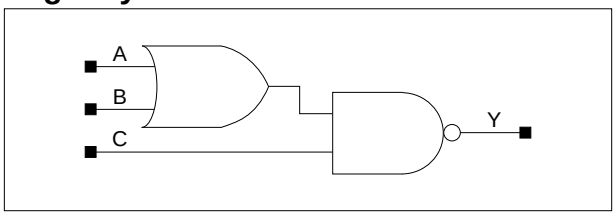
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ao332d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.133	0.127 + 0.003*SL	0.130 + 0.002*SL	0.133 + 0.002*SL
	t_{PHL}	0.115	0.109 + 0.003*SL	0.112 + 0.002*SL	0.117 + 0.002*SL
B to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.140	0.134 + 0.003*SL	0.137 + 0.002*SL	0.140 + 0.002*SL
	t_{PHL}	0.117	0.111 + 0.003*SL	0.115 + 0.002*SL	0.119 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.147	0.141 + 0.003*SL	0.144 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.117	0.111 + 0.003*SL	0.115 + 0.002*SL	0.119 + 0.002*SL
D to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.180	0.174 + 0.003*SL	0.177 + 0.002*SL	0.180 + 0.002*SL
	t_{PHL}	0.141	0.135 + 0.003*SL	0.138 + 0.002*SL	0.143 + 0.002*SL
E to Y	t_R	0.040	0.031 + 0.005*SL	0.030 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.025 + 0.003*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.187	0.181 + 0.003*SL	0.184 + 0.002*SL	0.187 + 0.002*SL
	t_{PHL}	0.144	0.137 + 0.003*SL	0.141 + 0.002*SL	0.146 + 0.002*SL
F to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.025 + 0.003*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.195	0.188 + 0.003*SL	0.192 + 0.002*SL	0.195 + 0.002*SL
	t_{PHL}	0.144	0.138 + 0.003*SL	0.142 + 0.002*SL	0.146 + 0.002*SL
G to Y	t_R	0.040	0.031 + 0.004*SL	0.030 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.035	0.028 + 0.003*SL	0.026 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.206	0.200 + 0.003*SL	0.204 + 0.002*SL	0.206 + 0.002*SL
	t_{PHL}	0.148	0.141 + 0.003*SL	0.145 + 0.002*SL	0.151 + 0.002*SL
H to Y	t_R	0.039	0.031 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.035	0.029 + 0.003*SL	0.026 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.213	0.207 + 0.003*SL	0.210 + 0.002*SL	0.213 + 0.002*SL
	t_{PHL}	0.149	0.143 + 0.003*SL	0.147 + 0.002*SL	0.152 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	1
x	x	0	1
Others States			0

Cell Data

Input Load (SL)								
oa21			*oa21d2*			*oa21d4*		
A	B	C	A	B	C	A	B	C
1.1	1.2	1.1	2.2	2.4	2.3	1.2	1.2	1.2
Gate Count								
oa21			*oa21d2*			*oa21d4*		
1.67			3.00			3.67		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.056 + 0.018*SL	0.048 + 0.020*SL	0.038 + 0.020*SL
	t_F	0.054	0.037 + 0.009*SL	0.034 + 0.009*SL	0.023 + 0.010*SL
	t_{PLH}	0.055	0.037 + 0.009*SL	0.038 + 0.009*SL	0.037 + 0.009*SL
	t_{PHL}	0.035	0.022 + 0.006*SL	0.028 + 0.005*SL	0.028 + 0.005*SL
B to Y	t_R	0.087	0.051 + 0.018*SL	0.043 + 0.020*SL	0.038 + 0.020*SL
	t_F	0.061	0.044 + 0.009*SL	0.042 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.059	0.040 + 0.009*SL	0.041 + 0.009*SL	0.041 + 0.009*SL
	t_{PHL}	0.039	0.027 + 0.006*SL	0.031 + 0.005*SL	0.032 + 0.005*SL
C to Y	t_R	0.074	0.057 + 0.009*SL	0.053 + 0.010*SL	0.041 + 0.010*SL
	t_F	0.055	0.038 + 0.009*SL	0.036 + 0.009*SL	0.027 + 0.010*SL
	t_{PLH}	0.043	0.033 + 0.005*SL	0.036 + 0.004*SL	0.036 + 0.005*SL
	t_{PHL}	0.042	0.031 + 0.006*SL	0.034 + 0.005*SL	0.035 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

oa21/oa21d2/oa21d4

2-OR into 2-NAND with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa21d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.056 + 0.009*SL	0.053 + 0.010*SL	0.039 + 0.010*SL
	t_F	0.045	0.036 + 0.005*SL	0.036 + 0.005*SL	0.024 + 0.005*SL
	t_{PLH}	0.046	0.036 + 0.005*SL	0.038 + 0.004*SL	0.037 + 0.005*SL
	t_{PHL}	0.028	0.021 + 0.004*SL	0.026 + 0.003*SL	0.028 + 0.002*SL
B to Y	t_R	0.069	0.052 + 0.009*SL	0.046 + 0.010*SL	0.039 + 0.010*SL
	t_F	0.052	0.045 + 0.004*SL	0.041 + 0.005*SL	0.030 + 0.005*SL
	t_{PLH}	0.050	0.040 + 0.005*SL	0.042 + 0.005*SL	0.042 + 0.005*SL
	t_{PHL}	0.034	0.027 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
C to Y	t_R	0.066	0.059 + 0.004*SL	0.055 + 0.005*SL	0.042 + 0.005*SL
	t_F	0.045	0.037 + 0.004*SL	0.034 + 0.005*SL	0.028 + 0.005*SL
	t_{PLH}	0.038	0.032 + 0.003*SL	0.035 + 0.002*SL	0.036 + 0.002*SL
	t_{PHL}	0.037	0.031 + 0.003*SL	0.033 + 0.003*SL	0.036 + 0.002*SL

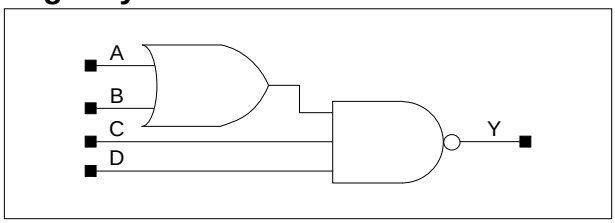
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa21d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.002*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.084	0.080 + 0.002*SL	0.083 + 0.001*SL	0.091 + 0.001*SL
B to Y	t_R	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.108 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.097 + 0.001*SL
C to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.095	0.092 + 0.002*SL	0.094 + 0.001*SL	0.099 + 0.001*SL
	t_{PHL}	0.092	0.089 + 0.002*SL	0.091 + 0.001*SL	0.100 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)											
oa211				*oa211d2*				*oa211d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.2	1.0	1.1	2.1	2.5	2.2	2.1	1.1	1.2	1.1	1.1

Gate Count		
oa211	*oa211d2*	*oa211d4*
2.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.066 + 0.018*SL	0.058 + 0.020*SL	0.050 + 0.020*SL
	t_F	0.075	0.052 + 0.012*SL	0.045 + 0.014*SL	0.036 + 0.014*SL
	t_{PLH}	0.061	0.043 + 0.009*SL	0.043 + 0.009*SL	0.042 + 0.009*SL
	t_{PHL}	0.047	0.032 + 0.007*SL	0.034 + 0.007*SL	0.034 + 0.007*SL
B to Y	t_R	0.097	0.059 + 0.019*SL	0.054 + 0.020*SL	0.050 + 0.020*SL
	t_F	0.083	0.057 + 0.013*SL	0.056 + 0.013*SL	0.046 + 0.014*SL
	t_{PLH}	0.065	0.046 + 0.009*SL	0.047 + 0.009*SL	0.047 + 0.009*SL
	t_{PHL}	0.052	0.038 + 0.007*SL	0.039 + 0.007*SL	0.040 + 0.007*SL
C to Y	t_R	0.088	0.067 + 0.011*SL	0.063 + 0.012*SL	0.051 + 0.012*SL
	t_F	0.081	0.056 + 0.013*SL	0.051 + 0.014*SL	0.045 + 0.014*SL
	t_{PLH}	0.052	0.041 + 0.006*SL	0.042 + 0.005*SL	0.042 + 0.005*SL
	t_{PHL}	0.059	0.044 + 0.007*SL	0.045 + 0.007*SL	0.046 + 0.007*SL
D to Y	t_R	0.096	0.080 + 0.008*SL	0.066 + 0.012*SL	0.056 + 0.012*SL
	t_F	0.079	0.054 + 0.013*SL	0.049 + 0.014*SL	0.045 + 0.014*SL
	t_{PLH}	0.054	0.043 + 0.006*SL	0.044 + 0.005*SL	0.045 + 0.005*SL
	t_{PHL}	0.059	0.044 + 0.007*SL	0.045 + 0.007*SL	0.046 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa211d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.080	0.063 + 0.009*SL	0.058 + 0.010*SL	0.045 + 0.010*SL
	t_F	0.061	0.049 + 0.006*SL	0.047 + 0.007*SL	0.034 + 0.007*SL
	t_{PLH}	0.049	0.040 + 0.005*SL	0.041 + 0.004*SL	0.040 + 0.005*SL
	t_{PHL}	0.037	0.029 + 0.004*SL	0.032 + 0.003*SL	0.032 + 0.003*SL
B to Y	t_R	0.073	0.055 + 0.009*SL	0.052 + 0.010*SL	0.045 + 0.010*SL
	t_F	0.070	0.057 + 0.006*SL	0.056 + 0.007*SL	0.045 + 0.007*SL
	t_{PLH}	0.053	0.043 + 0.005*SL	0.045 + 0.005*SL	0.045 + 0.005*SL
	t_{PHL}	0.044	0.036 + 0.004*SL	0.038 + 0.003*SL	0.038 + 0.003*SL
C to Y	t_R	0.077	0.063 + 0.007*SL	0.069 + 0.006*SL	0.050 + 0.006*SL
	t_F	0.065	0.051 + 0.007*SL	0.052 + 0.007*SL	0.043 + 0.007*SL
	t_{PLH}	0.045	0.039 + 0.003*SL	0.041 + 0.003*SL	0.041 + 0.003*SL
	t_{PHL}	0.050	0.043 + 0.004*SL	0.044 + 0.003*SL	0.046 + 0.003*SL
D to Y	t_R	0.079	0.068 + 0.005*SL	0.067 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.063	0.051 + 0.006*SL	0.048 + 0.007*SL	0.042 + 0.007*SL
	t_{PLH}	0.048	0.042 + 0.003*SL	0.043 + 0.003*SL	0.043 + 0.003*SL
	t_{PHL}	0.050	0.043 + 0.004*SL	0.044 + 0.003*SL	0.045 + 0.003*SL

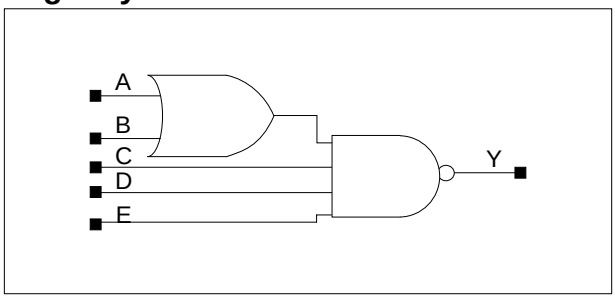
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa211d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.028 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.113	0.109 + 0.002*SL	0.111 + 0.001*SL	0.117 + 0.001*SL
	t_{PHL}	0.099	0.095 + 0.002*SL	0.098 + 0.001*SL	0.106 + 0.001*SL
B to Y	t_R	0.035	0.030 + 0.003*SL	0.031 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.028 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.116	0.112 + 0.002*SL	0.115 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.106	0.102 + 0.002*SL	0.105 + 0.001*SL	0.114 + 0.001*SL
C to Y	t_R	0.038	0.031 + 0.003*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.103	0.100 + 0.002*SL	0.102 + 0.001*SL	0.105 + 0.001*SL
	t_{PHL}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.119 + 0.001*SL
D to Y	t_R	0.038	0.032 + 0.003*SL	0.036 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.109 + 0.001*SL
	t_{PHL}	0.112	0.108 + 0.002*SL	0.111 + 0.001*SL	0.119 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
oa2111					*oa2111d2*					*oa2111*	*oa2111d2*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	0.9	0.9	1.0	2.1	2.4	2.0	2.0	1.8	2.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa2111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.068 + 0.018*SL	0.060 + 0.020*SL	0.052 + 0.020*SL
	t_F	0.095	0.062 + 0.016*SL	0.057 + 0.018*SL	0.049 + 0.018*SL
	t_{PLH}	0.061	0.043 + 0.009*SL	0.044 + 0.009*SL	0.043 + 0.009*SL
	t_{PHL}	0.055	0.037 + 0.009*SL	0.038 + 0.009*SL	0.038 + 0.009*SL
B to Y	t_R	0.099	0.062 + 0.019*SL	0.056 + 0.020*SL	0.052 + 0.020*SL
	t_F	0.106	0.072 + 0.017*SL	0.068 + 0.018*SL	0.061 + 0.018*SL
	t_{PLH}	0.065	0.047 + 0.009*SL	0.048 + 0.009*SL	0.048 + 0.009*SL
	t_{PHL}	0.062	0.044 + 0.009*SL	0.045 + 0.009*SL	0.045 + 0.009*SL
C to Y	t_R	0.109	0.081 + 0.014*SL	0.074 + 0.016*SL	0.065 + 0.016*SL
	t_F	0.103	0.069 + 0.017*SL	0.067 + 0.018*SL	0.062 + 0.018*SL
	t_{PLH}	0.063	0.049 + 0.007*SL	0.049 + 0.007*SL	0.050 + 0.007*SL
	t_{PHL}	0.070	0.052 + 0.009*SL	0.053 + 0.009*SL	0.054 + 0.009*SL
D to Y	t_R	0.114	0.086 + 0.014*SL	0.080 + 0.016*SL	0.071 + 0.016*SL
	t_F	0.102	0.067 + 0.018*SL	0.065 + 0.018*SL	0.062 + 0.018*SL
	t_{PLH}	0.067	0.052 + 0.007*SL	0.053 + 0.007*SL	0.054 + 0.007*SL
	t_{PHL}	0.073	0.055 + 0.009*SL	0.056 + 0.009*SL	0.057 + 0.009*SL
E to Y	t_R	0.120	0.092 + 0.014*SL	0.085 + 0.016*SL	0.077 + 0.016*SL
	t_F	0.101	0.066 + 0.018*SL	0.064 + 0.018*SL	0.062 + 0.018*SL
	t_{PLH}	0.069	0.055 + 0.007*SL	0.056 + 0.007*SL	0.057 + 0.007*SL
	t_{PHL}	0.074	0.056 + 0.009*SL	0.057 + 0.009*SL	0.058 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

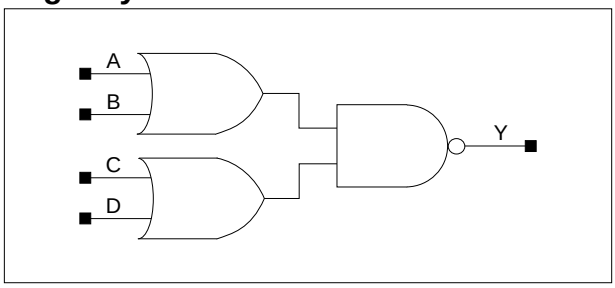
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa2111d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.066 + 0.008*SL	0.060 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.077	0.060 + 0.008*SL	0.059 + 0.009*SL	0.048 + 0.009*SL
	t_{PLH}	0.051	0.042 + 0.005*SL	0.042 + 0.004*SL	0.042 + 0.005*SL
	t_{PHL}	0.045	0.035 + 0.005*SL	0.036 + 0.004*SL	0.037 + 0.004*SL
B to Y	t_R	0.078	0.060 + 0.009*SL	0.056 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.090	0.073 + 0.008*SL	0.071 + 0.009*SL	0.060 + 0.009*SL
	t_{PLH}	0.055	0.045 + 0.005*SL	0.047 + 0.005*SL	0.047 + 0.005*SL
	t_{PHL}	0.052	0.043 + 0.005*SL	0.044 + 0.004*SL	0.044 + 0.004*SL
C to Y	t_R	0.098	0.087 + 0.006*SL	0.078 + 0.008*SL	0.065 + 0.008*SL
	t_F	0.086	0.071 + 0.008*SL	0.066 + 0.009*SL	0.061 + 0.009*SL
	t_{PLH}	0.056	0.048 + 0.004*SL	0.049 + 0.004*SL	0.050 + 0.004*SL
	t_{PHL}	0.062	0.053 + 0.005*SL	0.053 + 0.004*SL	0.055 + 0.004*SL
D to Y	t_R	0.100	0.086 + 0.007*SL	0.082 + 0.008*SL	0.072 + 0.008*SL
	t_F	0.084	0.067 + 0.008*SL	0.065 + 0.009*SL	0.061 + 0.009*SL
	t_{PLH}	0.059	0.052 + 0.004*SL	0.052 + 0.004*SL	0.054 + 0.004*SL
	t_{PHL}	0.064	0.055 + 0.005*SL	0.056 + 0.004*SL	0.057 + 0.004*SL
E to Y	t_R	0.106	0.092 + 0.007*SL	0.089 + 0.008*SL	0.077 + 0.008*SL
	t_F	0.083	0.066 + 0.008*SL	0.064 + 0.009*SL	0.061 + 0.009*SL
	t_{PLH}	0.061	0.054 + 0.004*SL	0.054 + 0.004*SL	0.056 + 0.004*SL
	t_{PHL}	0.064	0.055 + 0.005*SL	0.056 + 0.004*SL	0.057 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
Other States				0

Cell Data

Input Load (SL)											
oa22				*oa22d2*				*oa22d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.2	1.1	1.2	2.2	2.4	2.2	2.5	1.2	1.2	1.1	1.2

Gate Count		
oa22	*oa22d2*	*oa22d4*
2.00	3.67	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.080 + 0.018*SL	0.072 + 0.020*SL	0.062 + 0.020*SL
	t_F	0.060	0.043 + 0.009*SL	0.041 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.059	0.040 + 0.009*SL	0.040 + 0.009*SL	0.042 + 0.009*SL
	t_{PHL}	0.041	0.029 + 0.006*SL	0.033 + 0.005*SL	0.033 + 0.005*SL
B to Y	t_R	0.111	0.075 + 0.018*SL	0.067 + 0.020*SL	0.061 + 0.020*SL
	t_F	0.066	0.049 + 0.009*SL	0.046 + 0.009*SL	0.037 + 0.010*SL
	t_{PLH}	0.062	0.043 + 0.010*SL	0.044 + 0.009*SL	0.046 + 0.009*SL
	t_{PHL}	0.045	0.034 + 0.005*SL	0.036 + 0.005*SL	0.037 + 0.005*SL
C to Y	t_R	0.130	0.092 + 0.019*SL	0.087 + 0.020*SL	0.079 + 0.020*SL
	t_F	0.056	0.038 + 0.009*SL	0.035 + 0.009*SL	0.028 + 0.010*SL
	t_{PLH}	0.069	0.051 + 0.009*SL	0.051 + 0.009*SL	0.053 + 0.009*SL
	t_{PHL}	0.045	0.034 + 0.006*SL	0.036 + 0.005*SL	0.038 + 0.005*SL
D to Y	t_R	0.126	0.088 + 0.019*SL	0.083 + 0.020*SL	0.079 + 0.020*SL
	t_F	0.061	0.042 + 0.010*SL	0.042 + 0.010*SL	0.036 + 0.010*SL
	t_{PLH}	0.074	0.056 + 0.009*SL	0.056 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.049	0.038 + 0.005*SL	0.040 + 0.005*SL	0.042 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa22d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.078 + 0.009*SL	0.074 + 0.010*SL	0.060 + 0.010*SL
	t_F	0.050	0.041 + 0.004*SL	0.040 + 0.005*SL	0.030 + 0.005*SL
	t_{PLH}	0.048	0.039 + 0.005*SL	0.040 + 0.005*SL	0.041 + 0.005*SL
	t_{PHL}	0.034	0.028 + 0.003*SL	0.031 + 0.002*SL	0.033 + 0.002*SL
B to Y	t_R	0.091	0.073 + 0.009*SL	0.068 + 0.010*SL	0.060 + 0.010*SL
	t_F	0.058	0.051 + 0.004*SL	0.048 + 0.005*SL	0.037 + 0.005*SL
	t_{PLH}	0.052	0.042 + 0.005*SL	0.044 + 0.005*SL	0.046 + 0.005*SL
	t_{PHL}	0.039	0.033 + 0.003*SL	0.035 + 0.002*SL	0.037 + 0.002*SL
C to Y	t_R	0.110	0.092 + 0.009*SL	0.089 + 0.010*SL	0.077 + 0.010*SL
	t_F	0.046	0.038 + 0.004*SL	0.035 + 0.005*SL	0.028 + 0.005*SL
	t_{PLH}	0.059	0.050 + 0.005*SL	0.050 + 0.005*SL	0.052 + 0.005*SL
	t_{PHL}	0.039	0.033 + 0.003*SL	0.035 + 0.002*SL	0.037 + 0.002*SL
D to Y	t_R	0.105	0.087 + 0.009*SL	0.083 + 0.010*SL	0.077 + 0.010*SL
	t_F	0.051	0.040 + 0.005*SL	0.044 + 0.005*SL	0.035 + 0.005*SL
	t_{PLH}	0.064	0.055 + 0.005*SL	0.054 + 0.005*SL	0.057 + 0.005*SL
	t_{PHL}	0.043	0.037 + 0.003*SL	0.039 + 0.002*SL	0.041 + 0.002*SL

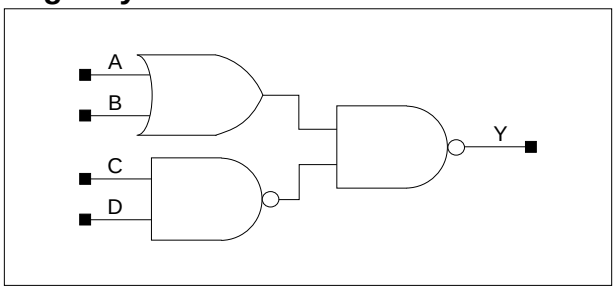
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa22d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.032 + 0.002*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.115	0.111 + 0.002*SL	0.114 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.090	0.087 + 0.002*SL	0.089 + 0.001*SL	0.098 + 0.001*SL
B to Y	t_R	0.037	0.033 + 0.002*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.119	0.115 + 0.002*SL	0.117 + 0.001*SL	0.123 + 0.001*SL
	t_{PHL}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.103 + 0.001*SL
C to Y	t_R	0.039	0.035 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.129	0.126 + 0.002*SL	0.128 + 0.001*SL	0.133 + 0.001*SL
	t_{PHL}	0.095	0.091 + 0.002*SL	0.094 + 0.001*SL	0.102 + 0.001*SL
D to Y	t_R	0.039	0.035 + 0.002*SL	0.033 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.133	0.130 + 0.002*SL	0.132 + 0.001*SL	0.137 + 0.001*SL
	t_{PHL}	0.100	0.097 + 0.002*SL	0.099 + 0.001*SL	0.108 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)												Gate Count		
oa22a				*oa22d2a*				*oa22d4a*				*oa22a*	*oa22d2a*	*oa22d4a*
A	B	C	D	A	B	C	D	A	B	C	D			
1.1	1.2	1.2	1.2	2.3	2.3	1.1	1.2	1.1	1.2	1.2	1.2	2.33	3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa22a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.056 + 0.018*SL	0.048 + 0.020*SL	0.039 + 0.020*SL
	t_F	0.054	0.037 + 0.009*SL	0.034 + 0.009*SL	0.024 + 0.010*SL
	t_{PLH}	0.055	0.037 + 0.009*SL	0.038 + 0.009*SL	0.037 + 0.009*SL
	t_{PHL}	0.035	0.022 + 0.006*SL	0.028 + 0.005*SL	0.028 + 0.005*SL
B to Y	t_R	0.087	0.051 + 0.018*SL	0.044 + 0.020*SL	0.038 + 0.020*SL
	t_F	0.061	0.044 + 0.009*SL	0.042 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.059	0.040 + 0.009*SL	0.041 + 0.009*SL	0.041 + 0.009*SL
	t_{PHL}	0.039	0.027 + 0.006*SL	0.031 + 0.005*SL	0.032 + 0.005*SL
C to Y	t_R	0.064	0.045 + 0.010*SL	0.044 + 0.010*SL	0.038 + 0.010*SL
	t_F	0.048	0.029 + 0.010*SL	0.029 + 0.010*SL	0.026 + 0.010*SL
	t_{PLH}	0.062	0.053 + 0.005*SL	0.054 + 0.005*SL	0.055 + 0.005*SL
	t_{PHL}	0.068	0.057 + 0.005*SL	0.059 + 0.005*SL	0.060 + 0.005*SL
D to Y	t_R	0.064	0.044 + 0.010*SL	0.044 + 0.010*SL	0.038 + 0.010*SL
	t_F	0.050	0.030 + 0.010*SL	0.030 + 0.010*SL	0.026 + 0.010*SL
	t_{PLH}	0.063	0.053 + 0.005*SL	0.054 + 0.005*SL	0.055 + 0.005*SL
	t_{PHL}	0.072	0.061 + 0.005*SL	0.063 + 0.005*SL	0.064 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa22d2a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.056 + 0.009*SL	0.053 + 0.010*SL	0.039 + 0.010*SL
	t_F	0.046	0.037 + 0.005*SL	0.037 + 0.005*SL	0.025 + 0.005*SL
	t_{PLH}	0.046	0.036 + 0.005*SL	0.038 + 0.004*SL	0.037 + 0.005*SL
	t_{PHL}	0.029	0.022 + 0.004*SL	0.026 + 0.003*SL	0.029 + 0.002*SL
B to Y	t_R	0.069	0.051 + 0.009*SL	0.047 + 0.010*SL	0.039 + 0.010*SL
	t_F	0.053	0.046 + 0.004*SL	0.043 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.049	0.039 + 0.005*SL	0.041 + 0.005*SL	0.042 + 0.005*SL
	t_{PHL}	0.034	0.027 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
C to Y	t_R	0.059	0.049 + 0.005*SL	0.048 + 0.005*SL	0.042 + 0.005*SL
	t_F	0.043	0.032 + 0.005*SL	0.034 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.069	0.064 + 0.003*SL	0.065 + 0.002*SL	0.067 + 0.002*SL
	t_{PHL}	0.073	0.068 + 0.003*SL	0.069 + 0.003*SL	0.072 + 0.002*SL
D to Y	t_R	0.060	0.052 + 0.004*SL	0.048 + 0.005*SL	0.042 + 0.005*SL
	t_F	0.043	0.034 + 0.004*SL	0.032 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.069	0.064 + 0.003*SL	0.065 + 0.002*SL	0.067 + 0.002*SL
	t_{PHL}	0.077	0.071 + 0.003*SL	0.073 + 0.003*SL	0.075 + 0.002*SL

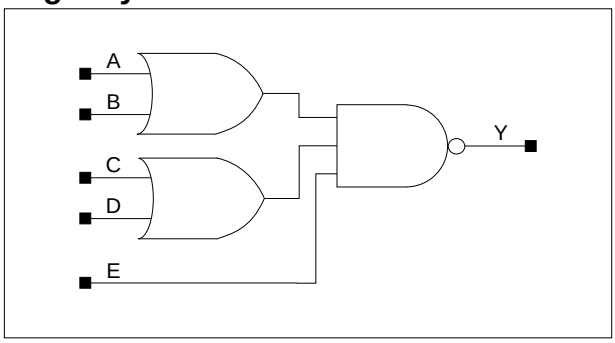
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa22d4a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.002*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.106	0.103 + 0.002*SL	0.105 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.084	0.080 + 0.002*SL	0.083 + 0.001*SL	0.091 + 0.001*SL
B to Y	t_R	0.034	0.029 + 0.002*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.026 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.109	0.106 + 0.002*SL	0.108 + 0.001*SL	0.113 + 0.001*SL
	t_{PHL}	0.089	0.086 + 0.002*SL	0.089 + 0.001*SL	0.097 + 0.001*SL
C to Y	t_R	0.032	0.027 + 0.002*SL	0.027 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.114	0.111 + 0.002*SL	0.113 + 0.001*SL	0.118 + 0.001*SL
	t_{PHL}	0.118	0.114 + 0.002*SL	0.117 + 0.001*SL	0.126 + 0.001*SL
D to Y	t_R	0.032	0.027 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.115	0.111 + 0.002*SL	0.113 + 0.001*SL	0.118 + 0.001*SL
	t_{PHL}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.129 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
oa221					*oa221d2*					*oa221d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.1	1.1	1.1	1.2	1.1	2.1	2.2	2.3	2.3	2.1	1.1	1.2	1.1	1.2	1.1
Gate Count														
oa221					*oa221d2*					*oa221d4*				
3.00					4.67					4.67				

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa221

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.125	0.089 + 0.018*SL	0.082 + 0.020*SL	0.073 + 0.020*SL
	t_F	0.086	0.061 + 0.013*SL	0.057 + 0.014*SL	0.047 + 0.014*SL
	t_{PLH}	0.064	0.045 + 0.009*SL	0.046 + 0.009*SL	0.047 + 0.009*SL
	t_{PHL}	0.054	0.040 + 0.007*SL	0.040 + 0.007*SL	0.041 + 0.007*SL
B to Y	t_R	0.121	0.083 + 0.019*SL	0.078 + 0.020*SL	0.073 + 0.020*SL
	t_F	0.095	0.070 + 0.013*SL	0.066 + 0.014*SL	0.059 + 0.014*SL
	t_{PLH}	0.068	0.050 + 0.009*SL	0.049 + 0.009*SL	0.052 + 0.009*SL
	t_{PHL}	0.059	0.045 + 0.007*SL	0.046 + 0.007*SL	0.046 + 0.007*SL
C to Y	t_R	0.143	0.106 + 0.019*SL	0.099 + 0.020*SL	0.093 + 0.020*SL
	t_F	0.083	0.057 + 0.013*SL	0.054 + 0.014*SL	0.048 + 0.014*SL
	t_{PLH}	0.076	0.057 + 0.009*SL	0.057 + 0.009*SL	0.059 + 0.009*SL
	t_{PHL}	0.063	0.048 + 0.007*SL	0.050 + 0.007*SL	0.051 + 0.007*SL
D to Y	t_R	0.139	0.099 + 0.020*SL	0.097 + 0.020*SL	0.093 + 0.020*SL
	t_F	0.092	0.064 + 0.014*SL	0.064 + 0.014*SL	0.058 + 0.014*SL
	t_{PLH}	0.079	0.060 + 0.009*SL	0.062 + 0.009*SL	0.064 + 0.009*SL
	t_{PHL}	0.068	0.054 + 0.007*SL	0.055 + 0.007*SL	0.056 + 0.007*SL
E to Y	t_R	0.106	0.085 + 0.010*SL	0.084 + 0.011*SL	0.073 + 0.011*SL
	t_F	0.090	0.063 + 0.013*SL	0.061 + 0.014*SL	0.057 + 0.014*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.047 + 0.005*SL	0.049 + 0.005*SL
	t_{PHL}	0.072	0.057 + 0.007*SL	0.058 + 0.007*SL	0.060 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa221d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.090 + 0.009*SL	0.087 + 0.010*SL	0.072 + 0.010*SL
	t_F	0.072	0.061 + 0.006*SL	0.056 + 0.007*SL	0.047 + 0.007*SL
	t_{PLH}	0.052	0.043 + 0.004*SL	0.042 + 0.005*SL	0.044 + 0.005*SL
	t_{PHL}	0.046	0.038 + 0.004*SL	0.039 + 0.003*SL	0.040 + 0.003*SL
B to Y	t_R	0.101	0.081 + 0.010*SL	0.081 + 0.010*SL	0.072 + 0.010*SL
	t_F	0.081	0.068 + 0.006*SL	0.067 + 0.007*SL	0.058 + 0.007*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.049 + 0.005*SL	0.051 + 0.005*SL
	t_{PHL}	0.052	0.045 + 0.004*SL	0.046 + 0.003*SL	0.047 + 0.003*SL
C to Y	t_R	0.123	0.105 + 0.009*SL	0.102 + 0.010*SL	0.090 + 0.010*SL
	t_F	0.069	0.056 + 0.006*SL	0.054 + 0.007*SL	0.046 + 0.007*SL
	t_{PLH}	0.063	0.054 + 0.005*SL	0.054 + 0.005*SL	0.056 + 0.005*SL
	t_{PHL}	0.054	0.047 + 0.004*SL	0.048 + 0.003*SL	0.050 + 0.003*SL
D to Y	t_R	0.117	0.099 + 0.009*SL	0.096 + 0.010*SL	0.089 + 0.010*SL
	t_F	0.077	0.063 + 0.007*SL	0.064 + 0.007*SL	0.057 + 0.007*SL
	t_{PLH}	0.070	0.060 + 0.005*SL	0.061 + 0.005*SL	0.063 + 0.005*SL
	t_{PHL}	0.061	0.053 + 0.004*SL	0.054 + 0.003*SL	0.056 + 0.003*SL
E to Y	t_R	0.089	0.084 + 0.003*SL	0.072 + 0.005*SL	0.061 + 0.006*SL
	t_F	0.076	0.063 + 0.006*SL	0.060 + 0.007*SL	0.057 + 0.007*SL
	t_{PLH}	0.050	0.045 + 0.003*SL	0.046 + 0.003*SL	0.046 + 0.003*SL
	t_{PHL}	0.063	0.055 + 0.004*SL	0.056 + 0.003*SL	0.058 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa221d4

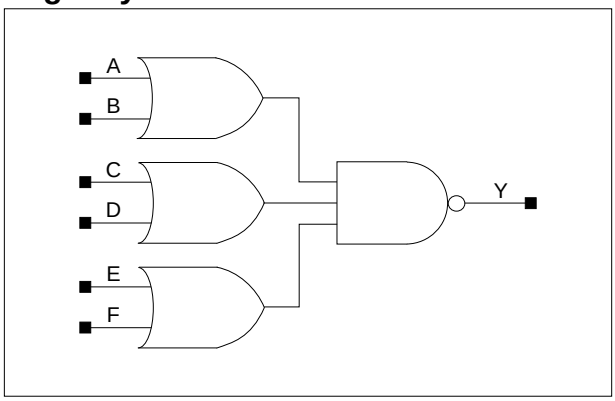
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.032 + 0.002*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.124	0.121 + 0.002*SL	0.123 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.118 + 0.001*SL
B to Y	t_R	0.038	0.033 + 0.002*SL	0.034 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.033	0.028 + 0.002*SL	0.030 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.128	0.124 + 0.002*SL	0.127 + 0.001*SL	0.132 + 0.001*SL
	t_{PHL}	0.117	0.113 + 0.002*SL	0.116 + 0.001*SL	0.125 + 0.001*SL
C to Y	t_R	0.039	0.034 + 0.002*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.143 + 0.001*SL
	t_{PHL}	0.118	0.115 + 0.002*SL	0.117 + 0.001*SL	0.126 + 0.001*SL
D to Y	t_R	0.040	0.035 + 0.002*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.142	0.139 + 0.002*SL	0.141 + 0.001*SL	0.147 + 0.001*SL
	t_{PHL}	0.126	0.122 + 0.002*SL	0.125 + 0.001*SL	0.134 + 0.001*SL
E to Y	t_R	0.035	0.031 + 0.002*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.117	0.113 + 0.002*SL	0.116 + 0.001*SL	0.121 + 0.001*SL
	t_{PHL}	0.128	0.124 + 0.002*SL	0.127 + 0.001*SL	0.136 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

oa222/oa222d2/oa222d4

Three 2-ORs into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
oa222						*oa222*
A	B	C	D	E	F	
1.1	1.2	1.1	1.2	1.1	1.2	3.33
oa222d2						*oa222d2*
A	B	C	D	E	F	
2.2	2.4	2.1	2.5	2.2	2.5	5.67
oa222d4						*oa222d4*
A	B	C	D	E	F	
1.1	1.2	1.1	1.2	1.1	1.2	5.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.158	0.122 + 0.018*SL	0.114 + 0.020*SL	0.105 + 0.020*SL
	t_F	0.097	0.071 + 0.013*SL	0.069 + 0.014*SL	0.062 + 0.014*SL
	t_{PLH}	0.068	0.049 + 0.009*SL	0.049 + 0.009*SL	0.053 + 0.009*SL
	t_{PHL}	0.064	0.049 + 0.007*SL	0.050 + 0.007*SL	0.052 + 0.007*SL
B to Y	t_R	0.154	0.116 + 0.019*SL	0.111 + 0.020*SL	0.105 + 0.020*SL
	t_F	0.106	0.080 + 0.013*SL	0.078 + 0.014*SL	0.072 + 0.014*SL
	t_{PLH}	0.072	0.054 + 0.009*SL	0.053 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.069	0.055 + 0.007*SL	0.055 + 0.007*SL	0.057 + 0.007*SL
C to Y	t_R	0.172	0.136 + 0.018*SL	0.129 + 0.020*SL	0.122 + 0.020*SL
	t_F	0.096	0.070 + 0.013*SL	0.067 + 0.014*SL	0.063 + 0.014*SL
	t_{PLH}	0.078	0.059 + 0.010*SL	0.060 + 0.009*SL	0.064 + 0.009*SL
	t_{PHL}	0.071	0.056 + 0.007*SL	0.058 + 0.007*SL	0.059 + 0.007*SL
D to Y	t_R	0.168	0.129 + 0.020*SL	0.126 + 0.020*SL	0.121 + 0.020*SL
	t_F	0.105	0.078 + 0.013*SL	0.076 + 0.014*SL	0.072 + 0.014*SL
	t_{PLH}	0.082	0.063 + 0.010*SL	0.065 + 0.009*SL	0.068 + 0.009*SL
	t_{PHL}	0.076	0.062 + 0.007*SL	0.063 + 0.007*SL	0.065 + 0.007*SL
E to Y	t_R	0.177	0.140 + 0.019*SL	0.134 + 0.020*SL	0.129 + 0.020*SL
	t_F	0.089	0.062 + 0.014*SL	0.060 + 0.014*SL	0.059 + 0.014*SL
	t_{PLH}	0.087	0.068 + 0.010*SL	0.069 + 0.009*SL	0.073 + 0.009*SL
	t_{PHL}	0.073	0.059 + 0.007*SL	0.060 + 0.007*SL	0.061 + 0.007*SL
F to Y	t_R	0.174	0.135 + 0.020*SL	0.133 + 0.020*SL	0.129 + 0.020*SL
	t_F	0.103	0.077 + 0.013*SL	0.074 + 0.014*SL	0.072 + 0.014*SL
	t_{PLH}	0.096	0.077 + 0.010*SL	0.078 + 0.009*SL	0.083 + 0.009*SL
	t_{PHL}	0.081	0.066 + 0.007*SL	0.067 + 0.007*SL	0.069 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa222d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.127	0.109 + 0.009*SL	0.105 + 0.010*SL	0.093 + 0.010*SL
	t_F	0.079	0.065 + 0.007*SL	0.065 + 0.007*SL	0.056 + 0.007*SL
	t_{PLH}	0.056	0.047 + 0.005*SL	0.047 + 0.005*SL	0.050 + 0.005*SL
	t_{PHL}	0.053	0.045 + 0.004*SL	0.046 + 0.003*SL	0.047 + 0.003*SL
B to Y	t_R	0.121	0.103 + 0.009*SL	0.099 + 0.010*SL	0.092 + 0.010*SL
	t_F	0.088	0.075 + 0.006*SL	0.074 + 0.007*SL	0.066 + 0.007*SL
	t_{PLH}	0.061	0.052 + 0.005*SL	0.051 + 0.005*SL	0.056 + 0.005*SL
	t_{PHL}	0.058	0.051 + 0.004*SL	0.052 + 0.003*SL	0.053 + 0.003*SL
C to Y	t_R	0.139	0.121 + 0.009*SL	0.118 + 0.010*SL	0.108 + 0.010*SL
	t_F	0.076	0.063 + 0.007*SL	0.062 + 0.007*SL	0.056 + 0.007*SL
	t_{PLH}	0.067	0.057 + 0.005*SL	0.058 + 0.005*SL	0.061 + 0.005*SL
	t_{PHL}	0.060	0.052 + 0.004*SL	0.054 + 0.003*SL	0.055 + 0.003*SL
D to Y	t_R	0.135	0.115 + 0.010*SL	0.114 + 0.010*SL	0.108 + 0.010*SL
	t_F	0.086	0.072 + 0.007*SL	0.072 + 0.007*SL	0.065 + 0.007*SL
	t_{PLH}	0.072	0.063 + 0.005*SL	0.063 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.066	0.059 + 0.004*SL	0.059 + 0.003*SL	0.061 + 0.003*SL
E to Y	t_R	0.155	0.136 + 0.009*SL	0.134 + 0.010*SL	0.124 + 0.010*SL
	t_F	0.075	0.061 + 0.007*SL	0.060 + 0.007*SL	0.055 + 0.007*SL
	t_{PLH}	0.076	0.066 + 0.005*SL	0.067 + 0.005*SL	0.072 + 0.005*SL
	t_{PHL}	0.064	0.056 + 0.004*SL	0.057 + 0.003*SL	0.059 + 0.003*SL
F to Y	t_R	0.150	0.131 + 0.010*SL	0.129 + 0.010*SL	0.125 + 0.010*SL
	t_F	0.083	0.070 + 0.007*SL	0.069 + 0.007*SL	0.065 + 0.007*SL
	t_{PLH}	0.081	0.071 + 0.005*SL	0.072 + 0.005*SL	0.077 + 0.005*SL
	t_{PHL}	0.070	0.063 + 0.004*SL	0.063 + 0.003*SL	0.065 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa222d4

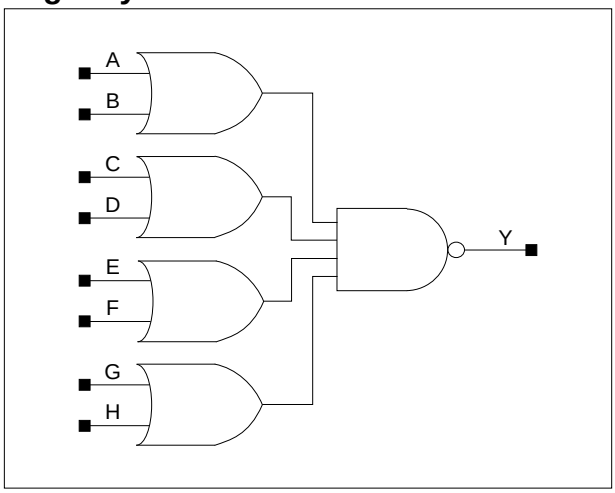
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.036 + 0.002*SL	0.035 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.030 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.133	0.129 + 0.002*SL	0.132 + 0.001*SL	0.138 + 0.001*SL
	t_{PHL}	0.119	0.115 + 0.002*SL	0.118 + 0.001*SL	0.127 + 0.001*SL
B to Y	t_R	0.041	0.036 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.030 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.136	0.133 + 0.002*SL	0.135 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.125	0.122 + 0.002*SL	0.125 + 0.001*SL	0.134 + 0.001*SL
C to Y	t_R	0.041	0.037 + 0.002*SL	0.036 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.146	0.142 + 0.002*SL	0.145 + 0.001*SL	0.151 + 0.001*SL
	t_{PHL}	0.126	0.123 + 0.002*SL	0.126 + 0.001*SL	0.134 + 0.001*SL
D to Y	t_R	0.042	0.038 + 0.002*SL	0.037 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.034	0.030 + 0.002*SL	0.030 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.151	0.147 + 0.002*SL	0.150 + 0.001*SL	0.155 + 0.001*SL
	t_{PHL}	0.134	0.130 + 0.002*SL	0.133 + 0.001*SL	0.142 + 0.001*SL
E to Y	t_R	0.043	0.040 + 0.002*SL	0.037 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.029 + 0.002*SL	0.023 + 0.002*SL
	t_{PLH}	0.158	0.154 + 0.002*SL	0.156 + 0.001*SL	0.162 + 0.001*SL
	t_{PHL}	0.131	0.127 + 0.002*SL	0.130 + 0.001*SL	0.139 + 0.001*SL
F to Y	t_R	0.043	0.040 + 0.001*SL	0.037 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.162	0.158 + 0.002*SL	0.161 + 0.001*SL	0.167 + 0.001*SL
	t_{PHL}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.146 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

oa2222/oa2222d2/oa2222d4

Four 2-ORs into 4-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
oa2222								*oa2222*
A	B	C	D	E	F	G	H	
1.1	1.2	1.1	1.2	1.1	1.2	1.1	1.2	4.00
oa2222d2								*oa2222d2*
A	B	C	D	E	F	G	H	
1.1	1.2	1.1	1.2	1.1	1.2	1.1	1.2	5.33
oa2222d4								*oa2222d4*
A	B	C	D	E	F	G	H	
1.1	1.2	1.1	1.2	1.1	1.2	1.1	1.2	6.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.179	0.142 + 0.019*SL	0.136 + 0.020*SL	0.129 + 0.020*SL
	t_F	0.115	0.084 + 0.015*SL	0.082 + 0.016*SL	0.077 + 0.016*SL
	t_{PLH}	0.076	0.056 + 0.010*SL	0.058 + 0.009*SL	0.063 + 0.009*SL
	t_{PHL}	0.071	0.055 + 0.008*SL	0.055 + 0.008*SL	0.056 + 0.008*SL
B to Y	t_R	0.176	0.137 + 0.019*SL	0.134 + 0.020*SL	0.129 + 0.020*SL
	t_F	0.125	0.096 + 0.015*SL	0.091 + 0.016*SL	0.087 + 0.016*SL
	t_{PLH}	0.081	0.062 + 0.010*SL	0.062 + 0.009*SL	0.068 + 0.009*SL
	t_{PHL}	0.077	0.061 + 0.008*SL	0.062 + 0.008*SL	0.062 + 0.008*SL
C to Y	t_R	0.197	0.159 + 0.019*SL	0.154 + 0.020*SL	0.148 + 0.020*SL
	t_F	0.114	0.084 + 0.015*SL	0.080 + 0.016*SL	0.078 + 0.016*SL
	t_{PLH}	0.089	0.070 + 0.009*SL	0.070 + 0.009*SL	0.076 + 0.009*SL
	t_{PHL}	0.082	0.066 + 0.008*SL	0.067 + 0.008*SL	0.068 + 0.008*SL
D to Y	t_R	0.193	0.154 + 0.020*SL	0.151 + 0.020*SL	0.148 + 0.020*SL
	t_F	0.124	0.093 + 0.015*SL	0.091 + 0.016*SL	0.088 + 0.016*SL
	t_{PLH}	0.093	0.074 + 0.010*SL	0.074 + 0.009*SL	0.080 + 0.009*SL
	t_{PHL}	0.088	0.072 + 0.008*SL	0.072 + 0.008*SL	0.074 + 0.008*SL
E to Y	t_R	0.210	0.172 + 0.019*SL	0.168 + 0.020*SL	0.162 + 0.020*SL
	t_F	0.111	0.079 + 0.016*SL	0.079 + 0.016*SL	0.077 + 0.016*SL
	t_{PLH}	0.099	0.079 + 0.010*SL	0.081 + 0.009*SL	0.086 + 0.009*SL
	t_{PHL}	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.073 + 0.008*SL
F to Y	t_R	0.207	0.168 + 0.020*SL	0.165 + 0.020*SL	0.163 + 0.020*SL
	t_F	0.123	0.092 + 0.015*SL	0.089 + 0.016*SL	0.088 + 0.016*SL
	t_{PLH}	0.104	0.084 + 0.010*SL	0.086 + 0.009*SL	0.092 + 0.009*SL
	t_{PHL}	0.094	0.078 + 0.008*SL	0.079 + 0.008*SL	0.080 + 0.008*SL
G to Y	t_R	0.227	0.188 + 0.019*SL	0.185 + 0.020*SL	0.180 + 0.020*SL
	t_F	0.140	0.103 + 0.018*SL	0.103 + 0.018*SL	0.103 + 0.018*SL
	t_{PLH}	0.109	0.089 + 0.010*SL	0.091 + 0.009*SL	0.097 + 0.009*SL
	t_{PHL}	0.111	0.093 + 0.009*SL	0.094 + 0.009*SL	0.096 + 0.009*SL
H to Y	t_R	0.225	0.185 + 0.020*SL	0.183 + 0.020*SL	0.180 + 0.020*SL
	t_F	0.152	0.116 + 0.018*SL	0.115 + 0.018*SL	0.115 + 0.018*SL
	t_{PLH}	0.114	0.095 + 0.010*SL	0.096 + 0.009*SL	0.102 + 0.009*SL
	t_{PHL}	0.119	0.101 + 0.009*SL	0.102 + 0.009*SL	0.104 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa2222d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.031	0.022 + 0.005*SL	0.026 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.131	0.125 + 0.003*SL	0.129 + 0.002*SL	0.131 + 0.002*SL
	t_{PHL}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.120 + 0.002*SL
B to Y	t_R	0.039	0.031 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.135	0.129 + 0.003*SL	0.133 + 0.002*SL	0.135 + 0.002*SL
	t_{PHL}	0.125	0.119 + 0.003*SL	0.123 + 0.002*SL	0.127 + 0.002*SL
C to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.145	0.138 + 0.003*SL	0.142 + 0.002*SL	0.145 + 0.002*SL
	t_{PHL}	0.128	0.122 + 0.003*SL	0.126 + 0.002*SL	0.130 + 0.002*SL
D to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.024 + 0.003*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.149	0.142 + 0.003*SL	0.146 + 0.002*SL	0.149 + 0.002*SL
	t_{PHL}	0.136	0.130 + 0.003*SL	0.133 + 0.002*SL	0.138 + 0.002*SL
E to Y	t_R	0.041	0.033 + 0.004*SL	0.031 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.156	0.150 + 0.003*SL	0.154 + 0.002*SL	0.156 + 0.002*SL
	t_{PHL}	0.134	0.128 + 0.003*SL	0.132 + 0.002*SL	0.136 + 0.002*SL
F to Y	t_R	0.042	0.034 + 0.004*SL	0.031 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.161	0.154 + 0.003*SL	0.158 + 0.002*SL	0.161 + 0.002*SL
	t_{PHL}	0.142	0.136 + 0.003*SL	0.140 + 0.002*SL	0.144 + 0.002*SL
G to Y	t_R	0.042	0.035 + 0.004*SL	0.032 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.024 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.166	0.159 + 0.003*SL	0.163 + 0.002*SL	0.166 + 0.002*SL
	t_{PHL}	0.160	0.154 + 0.003*SL	0.158 + 0.002*SL	0.163 + 0.002*SL
H to Y	t_R	0.041	0.031 + 0.005*SL	0.032 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.025 + 0.004*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.171	0.164 + 0.003*SL	0.168 + 0.002*SL	0.171 + 0.002*SL
	t_{PHL}	0.170	0.164 + 0.003*SL	0.167 + 0.002*SL	0.172 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa2222d4

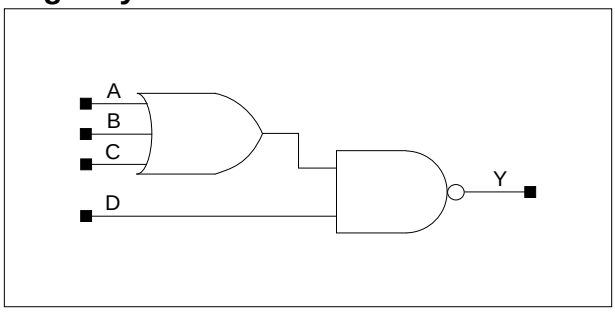
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.032 + 0.002*SL	0.031 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.027	0.024 + 0.001*SL	0.022 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.138	0.134 + 0.002*SL	0.136 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.122	0.119 + 0.002*SL	0.121 + 0.001*SL	0.127 + 0.001*SL
B to Y	t_R	0.035	0.031 + 0.002*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.024 + 0.002*SL	0.015 + 0.002*SL
	t_{PLH}	0.141	0.138 + 0.002*SL	0.140 + 0.001*SL	0.144 + 0.001*SL
	t_{PHL}	0.130	0.126 + 0.002*SL	0.129 + 0.001*SL	0.135 + 0.001*SL
C to Y	t_R	0.038	0.033 + 0.002*SL	0.034 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.027	0.024 + 0.002*SL	0.023 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.151	0.147 + 0.002*SL	0.150 + 0.001*SL	0.154 + 0.001*SL
	t_{PHL}	0.133	0.130 + 0.002*SL	0.132 + 0.001*SL	0.138 + 0.001*SL
D to Y	t_R	0.038	0.033 + 0.003*SL	0.034 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.028	0.025 + 0.001*SL	0.023 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.155	0.152 + 0.002*SL	0.154 + 0.001*SL	0.158 + 0.001*SL
	t_{PHL}	0.141	0.137 + 0.002*SL	0.140 + 0.001*SL	0.146 + 0.001*SL
E to Y	t_R	0.039	0.036 + 0.002*SL	0.034 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.027	0.025 + 0.001*SL	0.022 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.162	0.158 + 0.002*SL	0.161 + 0.001*SL	0.165 + 0.001*SL
	t_{PHL}	0.139	0.135 + 0.002*SL	0.138 + 0.001*SL	0.144 + 0.001*SL
F to Y	t_R	0.039	0.035 + 0.002*SL	0.033 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.017 + 0.002*SL
	t_{PLH}	0.167	0.163 + 0.002*SL	0.165 + 0.001*SL	0.170 + 0.001*SL
	t_{PHL}	0.146	0.143 + 0.002*SL	0.145 + 0.001*SL	0.152 + 0.001*SL
G to Y	t_R	0.039	0.034 + 0.002*SL	0.034 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.027 + 0.001*SL	0.024 + 0.002*SL	0.018 + 0.002*SL
	t_{PLH}	0.173	0.169 + 0.002*SL	0.172 + 0.001*SL	0.177 + 0.001*SL
	t_{PHL}	0.167	0.164 + 0.002*SL	0.166 + 0.001*SL	0.173 + 0.001*SL
H to Y	t_R	0.040	0.035 + 0.002*SL	0.035 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.177	0.174 + 0.002*SL	0.176 + 0.001*SL	0.181 + 0.001*SL
	t_{PHL}	0.176	0.172 + 0.002*SL	0.175 + 0.001*SL	0.182 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

oa31/oa31d2/oa31d4

3-OR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)												Gate Count		
oa31				*oa31d2*				*oa31d4*				*oa31*	*oa31d2*	*oa31d4*
A	B	C	D	A	B	C	D	A	B	C	D			
1.0	1.1	1.1	1.0	1.9	2.3	2.5	1.9	1.0	1.1	1.1	1.0	2.00	3.67	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.138	0.081 + 0.028*SL	0.073 + 0.030*SL	0.069 + 0.031*SL
	t_F	0.064	0.043 + 0.011*SL	0.036 + 0.012*SL	0.026 + 0.013*SL
	t_{PLH}	0.073	0.045 + 0.014*SL	0.045 + 0.014*SL	0.045 + 0.014*SL
	t_{PHL}	0.044	0.030 + 0.007*SL	0.033 + 0.006*SL	0.033 + 0.006*SL
B to Y	t_R	0.135	0.076 + 0.029*SL	0.072 + 0.030*SL	0.069 + 0.031*SL
	t_F	0.074	0.053 + 0.011*SL	0.046 + 0.012*SL	0.035 + 0.013*SL
	t_{PLH}	0.084	0.056 + 0.014*SL	0.057 + 0.014*SL	0.058 + 0.014*SL
	t_{PHL}	0.050	0.037 + 0.007*SL	0.038 + 0.006*SL	0.039 + 0.006*SL
C to Y	t_R	0.133	0.074 + 0.030*SL	0.070 + 0.030*SL	0.069 + 0.031*SL
	t_F	0.080	0.058 + 0.011*SL	0.053 + 0.012*SL	0.044 + 0.013*SL
	t_{PLH}	0.088	0.061 + 0.014*SL	0.061 + 0.014*SL	0.062 + 0.014*SL
	t_{PHL}	0.053	0.039 + 0.007*SL	0.041 + 0.007*SL	0.043 + 0.006*SL
D to Y	t_R	0.081	0.062 + 0.010*SL	0.057 + 0.011*SL	0.045 + 0.011*SL
	t_F	0.076	0.054 + 0.011*SL	0.048 + 0.013*SL	0.043 + 0.013*SL
	t_{PLH}	0.048	0.037 + 0.005*SL	0.039 + 0.005*SL	0.038 + 0.005*SL
	t_{PHL}	0.057	0.043 + 0.007*SL	0.045 + 0.007*SL	0.048 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa31d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.107	0.079 + 0.014*SL	0.075 + 0.015*SL	0.066 + 0.015*SL
	t_F	0.052	0.042 + 0.005*SL	0.038 + 0.006*SL	0.026 + 0.006*SL
	t_{PLH}	0.058	0.044 + 0.007*SL	0.044 + 0.007*SL	0.044 + 0.007*SL
	t_{PHL}	0.036	0.028 + 0.004*SL	0.032 + 0.003*SL	0.033 + 0.003*SL
B to Y	t_R	0.104	0.076 + 0.014*SL	0.071 + 0.015*SL	0.066 + 0.015*SL
	t_F	0.061	0.049 + 0.006*SL	0.048 + 0.006*SL	0.035 + 0.006*SL
	t_{PLH}	0.069	0.055 + 0.007*SL	0.056 + 0.007*SL	0.057 + 0.007*SL
	t_{PHL}	0.043	0.035 + 0.004*SL	0.038 + 0.003*SL	0.038 + 0.003*SL
C to Y	t_R	0.101	0.072 + 0.014*SL	0.069 + 0.015*SL	0.067 + 0.015*SL
	t_F	0.069	0.058 + 0.006*SL	0.056 + 0.006*SL	0.045 + 0.006*SL
	t_{PLH}	0.074	0.060 + 0.007*SL	0.061 + 0.007*SL	0.062 + 0.007*SL
	t_{PHL}	0.046	0.038 + 0.004*SL	0.040 + 0.003*SL	0.043 + 0.003*SL
D to Y	t_R	0.074	0.062 + 0.006*SL	0.065 + 0.005*SL	0.046 + 0.006*SL
	t_F	0.062	0.048 + 0.007*SL	0.051 + 0.006*SL	0.043 + 0.006*SL
	t_{PLH}	0.042	0.035 + 0.003*SL	0.038 + 0.003*SL	0.038 + 0.003*SL
	t_{PHL}	0.050	0.042 + 0.004*SL	0.044 + 0.003*SL	0.047 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa31d4

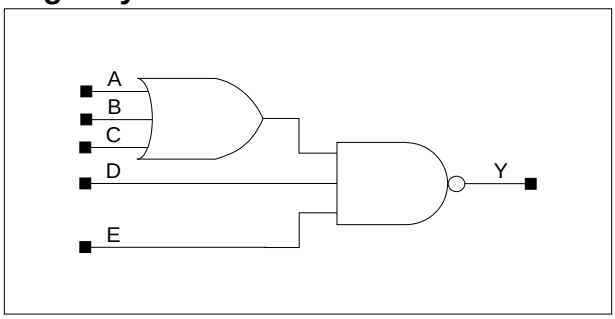
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.034 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.027 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.129	0.125 + 0.002*SL	0.128 + 0.001*SL	0.134 + 0.001*SL
	t_{PHL}	0.095	0.092 + 0.002*SL	0.095 + 0.001*SL	0.103 + 0.001*SL
B to Y	t_R	0.039	0.034 + 0.002*SL	0.034 + 0.002*SL	0.020 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.027 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.141	0.137 + 0.002*SL	0.139 + 0.001*SL	0.145 + 0.001*SL
	t_{PHL}	0.103	0.099 + 0.002*SL	0.102 + 0.001*SL	0.110 + 0.001*SL
C to Y	t_R	0.037	0.032 + 0.002*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.031	0.028 + 0.001*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.145	0.141 + 0.002*SL	0.144 + 0.001*SL	0.150 + 0.001*SL
	t_{PHL}	0.107	0.104 + 0.002*SL	0.106 + 0.001*SL	0.115 + 0.001*SL
D to Y	t_R	0.036	0.031 + 0.002*SL	0.031 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.103	0.099 + 0.002*SL	0.101 + 0.001*SL	0.106 + 0.001*SL
	t_{PHL}	0.111	0.108 + 0.002*SL	0.111 + 0.001*SL	0.119 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

oa311/oa311d2

3-OR into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)					Input Load (SL)				
oa311					*oa311d2*				
A	B	C	D	E	A	B	C	D	E
1.1	1.1	1.2	1.0	1.1	1.1	1.2	1.2	1.1	1.1
Gate Count									
oa311					*oa311d2*				
2.33					3.67				

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa311

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.157	0.099 + 0.029*SL	0.094 + 0.030*SL	0.091 + 0.031*SL
	t_F	0.079	0.055 + 0.012*SL	0.049 + 0.014*SL	0.041 + 0.014*SL
	t_{PLH}	0.083	0.056 + 0.014*SL	0.056 + 0.014*SL	0.056 + 0.014*SL
	t_{PHL}	0.050	0.035 + 0.007*SL	0.037 + 0.007*SL	0.036 + 0.007*SL
B to Y	t_R	0.155	0.096 + 0.030*SL	0.093 + 0.030*SL	0.091 + 0.031*SL
	t_F	0.088	0.063 + 0.013*SL	0.059 + 0.014*SL	0.051 + 0.014*SL
	t_{PLH}	0.095	0.067 + 0.014*SL	0.068 + 0.014*SL	0.069 + 0.014*SL
	t_{PHL}	0.055	0.041 + 0.007*SL	0.042 + 0.007*SL	0.042 + 0.007*SL
C to Y	t_R	0.154	0.095 + 0.030*SL	0.092 + 0.031*SL	0.091 + 0.031*SL
	t_F	0.098	0.073 + 0.013*SL	0.068 + 0.014*SL	0.060 + 0.014*SL
	t_{PLH}	0.099	0.071 + 0.014*SL	0.072 + 0.014*SL	0.073 + 0.014*SL
	t_{PHL}	0.058	0.044 + 0.007*SL	0.045 + 0.007*SL	0.047 + 0.007*SL
D to Y	t_R	0.099	0.082 + 0.008*SL	0.069 + 0.012*SL	0.059 + 0.012*SL
	t_F	0.094	0.068 + 0.013*SL	0.066 + 0.014*SL	0.059 + 0.014*SL
	t_{PLH}	0.056	0.045 + 0.005*SL	0.045 + 0.005*SL	0.046 + 0.005*SL
	t_{PHL}	0.067	0.052 + 0.007*SL	0.053 + 0.007*SL	0.056 + 0.007*SL
E to Y	t_R	0.103	0.086 + 0.009*SL	0.074 + 0.012*SL	0.063 + 0.012*SL
	t_F	0.092	0.066 + 0.013*SL	0.062 + 0.014*SL	0.059 + 0.014*SL
	t_{PLH}	0.058	0.047 + 0.005*SL	0.047 + 0.005*SL	0.048 + 0.005*SL
	t_{PHL}	0.066	0.052 + 0.007*SL	0.053 + 0.007*SL	0.055 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa311d2

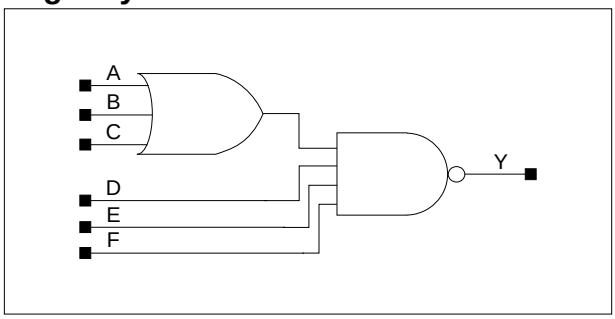
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.127 + 0.002*SL
	t_{PHL}	0.091	0.085 + 0.003*SL	0.089 + 0.002*SL	0.093 + 0.002*SL
B to Y	t_R	0.036	0.026 + 0.005*SL	0.026 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.139	0.132 + 0.003*SL	0.136 + 0.002*SL	0.138 + 0.002*SL
	t_{PHL}	0.099	0.093 + 0.003*SL	0.096 + 0.002*SL	0.100 + 0.002*SL
C to Y	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.143	0.136 + 0.003*SL	0.140 + 0.002*SL	0.142 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.105 + 0.002*SL
D to Y	t_R	0.039	0.029 + 0.005*SL	0.032 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.028	0.020 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.098	0.092 + 0.003*SL	0.094 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.108 + 0.002*SL	0.112 + 0.002*SL
E to Y	t_R	0.032	0.023 + 0.005*SL	0.022 + 0.005*SL	0.013 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.020 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.102 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.108 + 0.002*SL	0.112 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

oa3111/oa3111d2

3-OR into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)											
oa3111						*oa3111d2*					
A	B	C	D	E	F	A	B	C	D	E	F
1.1	1.1	1.2	1.0	1.0	0.9	1.1	1.1	1.1	0.9	1.0	1.0

Gate Count	
oa3111	*oa3111d2*
2.67	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa3111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.161	0.102 + 0.029*SL	0.098 + 0.030*SL	0.095 + 0.031*SL
	t_F	0.101	0.068 + 0.017*SL	0.062 + 0.018*SL	0.056 + 0.018*SL
	t_{PLH}	0.085	0.058 + 0.014*SL	0.057 + 0.014*SL	0.058 + 0.014*SL
	t_{PHL}	0.058	0.040 + 0.009*SL	0.041 + 0.009*SL	0.040 + 0.009*SL
B to Y	t_R	0.159	0.099 + 0.030*SL	0.097 + 0.030*SL	0.095 + 0.031*SL
	t_F	0.113	0.080 + 0.017*SL	0.075 + 0.018*SL	0.069 + 0.018*SL
	t_{PLH}	0.096	0.069 + 0.014*SL	0.069 + 0.014*SL	0.071 + 0.014*SL
	t_{PHL}	0.065	0.047 + 0.009*SL	0.048 + 0.009*SL	0.048 + 0.009*SL
C to Y	t_R	0.158	0.098 + 0.030*SL	0.095 + 0.031*SL	0.095 + 0.031*SL
	t_F	0.125	0.092 + 0.017*SL	0.087 + 0.018*SL	0.081 + 0.018*SL
	t_{PLH}	0.101	0.073 + 0.014*SL	0.074 + 0.014*SL	0.075 + 0.014*SL
	t_{PHL}	0.070	0.052 + 0.009*SL	0.053 + 0.009*SL	0.055 + 0.009*SL
D to Y	t_R	0.117	0.089 + 0.014*SL	0.081 + 0.016*SL	0.075 + 0.016*SL
	t_F	0.123	0.088 + 0.017*SL	0.085 + 0.018*SL	0.082 + 0.018*SL
	t_{PLH}	0.068	0.054 + 0.007*SL	0.054 + 0.007*SL	0.055 + 0.007*SL
	t_{PHL}	0.081	0.063 + 0.009*SL	0.064 + 0.009*SL	0.067 + 0.009*SL
E to Y	t_R	0.122	0.094 + 0.014*SL	0.088 + 0.016*SL	0.081 + 0.016*SL
	t_F	0.121	0.086 + 0.017*SL	0.084 + 0.018*SL	0.081 + 0.018*SL
	t_{PLH}	0.072	0.058 + 0.007*SL	0.058 + 0.007*SL	0.059 + 0.007*SL
	t_{PHL}	0.085	0.066 + 0.009*SL	0.067 + 0.009*SL	0.070 + 0.009*SL
F to Y	t_R	0.128	0.098 + 0.015*SL	0.094 + 0.016*SL	0.087 + 0.016*SL
	t_F	0.120	0.084 + 0.018*SL	0.083 + 0.018*SL	0.081 + 0.018*SL
	t_{PLH}	0.075	0.061 + 0.007*SL	0.061 + 0.007*SL	0.063 + 0.007*SL
	t_{PHL}	0.085	0.067 + 0.009*SL	0.068 + 0.009*SL	0.070 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

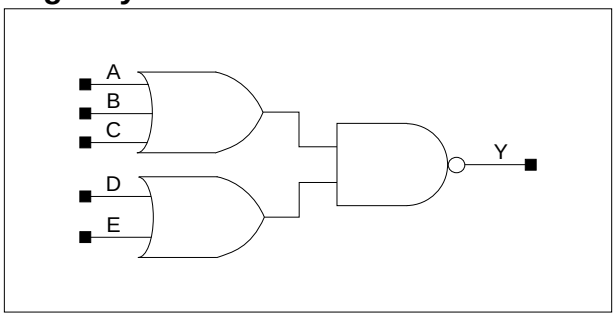
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa3111d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.129	0.123 + 0.003*SL	0.126 + 0.002*SL	0.128 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.104 + 0.002*SL
B to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.141	0.135 + 0.003*SL	0.138 + 0.002*SL	0.140 + 0.002*SL
	t_{PHL}	0.112	0.106 + 0.003*SL	0.109 + 0.002*SL	0.113 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.025 + 0.004*SL	0.025 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.145	0.139 + 0.003*SL	0.142 + 0.002*SL	0.144 + 0.002*SL
	t_{PHL}	0.118	0.112 + 0.003*SL	0.115 + 0.002*SL	0.120 + 0.002*SL
D to Y	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.025 + 0.004*SL	0.025 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.116	0.110 + 0.003*SL	0.112 + 0.002*SL	0.114 + 0.002*SL
	t_{PHL}	0.129	0.123 + 0.003*SL	0.127 + 0.002*SL	0.131 + 0.002*SL
E to Y	t_R	0.036	0.027 + 0.004*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.033	0.026 + 0.003*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.120	0.115 + 0.003*SL	0.117 + 0.002*SL	0.119 + 0.002*SL
	t_{PHL}	0.133	0.127 + 0.003*SL	0.130 + 0.002*SL	0.134 + 0.002*SL
F to Y	t_R	0.036	0.026 + 0.005*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.124	0.119 + 0.003*SL	0.121 + 0.002*SL	0.123 + 0.002*SL
	t_{PHL}	0.133	0.127 + 0.003*SL	0.131 + 0.002*SL	0.135 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	0	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
oa32					*oa32d2*					*oa32*	*oa32d2*
A	B	C	D	E	A	B	C	D	E		
0.9	1.0	1.0	1.1	1.2	1.0	1.0	1.1	1.1	1.2	2.67	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa32

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.176	0.119 + 0.028*SL	0.111 + 0.030*SL	0.107 + 0.031*SL
	t_F	0.078	0.054 + 0.012*SL	0.048 + 0.014*SL	0.039 + 0.014*SL
	t_{PLH}	0.079	0.052 + 0.014*SL	0.051 + 0.014*SL	0.055 + 0.014*SL
	t_{PHL}	0.057	0.043 + 0.007*SL	0.044 + 0.007*SL	0.044 + 0.007*SL
B to Y	t_R	0.172	0.113 + 0.029*SL	0.110 + 0.030*SL	0.107 + 0.031*SL
	t_F	0.087	0.062 + 0.012*SL	0.057 + 0.014*SL	0.050 + 0.014*SL
	t_{PLH}	0.091	0.063 + 0.014*SL	0.064 + 0.014*SL	0.069 + 0.014*SL
	t_{PHL}	0.063	0.049 + 0.007*SL	0.049 + 0.007*SL	0.050 + 0.007*SL
C to Y	t_R	0.171	0.112 + 0.030*SL	0.108 + 0.030*SL	0.107 + 0.031*SL
	t_F	0.097	0.072 + 0.012*SL	0.066 + 0.014*SL	0.058 + 0.014*SL
	t_{PLH}	0.096	0.067 + 0.014*SL	0.069 + 0.014*SL	0.073 + 0.014*SL
	t_{PHL}	0.066	0.052 + 0.007*SL	0.053 + 0.007*SL	0.055 + 0.007*SL
D to Y	t_R	0.136	0.099 + 0.018*SL	0.092 + 0.020*SL	0.085 + 0.020*SL
	t_F	0.082	0.056 + 0.013*SL	0.053 + 0.014*SL	0.049 + 0.014*SL
	t_{PLH}	0.072	0.053 + 0.009*SL	0.054 + 0.009*SL	0.056 + 0.009*SL
	t_{PHL}	0.063	0.048 + 0.008*SL	0.050 + 0.007*SL	0.052 + 0.007*SL
E to Y	t_R	0.131	0.092 + 0.020*SL	0.090 + 0.020*SL	0.085 + 0.020*SL
	t_F	0.092	0.066 + 0.013*SL	0.062 + 0.014*SL	0.058 + 0.014*SL
	t_{PLH}	0.076	0.057 + 0.009*SL	0.058 + 0.009*SL	0.060 + 0.009*SL
	t_{PHL}	0.068	0.054 + 0.007*SL	0.055 + 0.007*SL	0.057 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

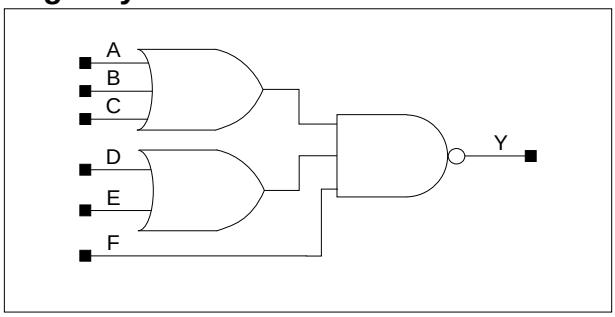
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa32d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.024 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.117	0.111 + 0.003*SL	0.115 + 0.002*SL	0.117 + 0.002*SL
	t_{PHL}	0.102	0.095 + 0.003*SL	0.099 + 0.002*SL	0.105 + 0.002*SL
B to Y	t_R	0.039	0.030 + 0.005*SL	0.029 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.129	0.123 + 0.003*SL	0.126 + 0.002*SL	0.129 + 0.002*SL
	t_{PHL}	0.110	0.103 + 0.003*SL	0.107 + 0.002*SL	0.113 + 0.002*SL
C to Y	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.025 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.133	0.127 + 0.003*SL	0.131 + 0.002*SL	0.133 + 0.002*SL
	t_{PHL}	0.115	0.109 + 0.003*SL	0.113 + 0.002*SL	0.119 + 0.002*SL
D to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.113	0.107 + 0.003*SL	0.110 + 0.002*SL	0.113 + 0.002*SL
	t_{PHL}	0.109	0.103 + 0.003*SL	0.107 + 0.002*SL	0.113 + 0.002*SL
E to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.117	0.111 + 0.003*SL	0.114 + 0.002*SL	0.117 + 0.002*SL
	t_{PHL}	0.117	0.110 + 0.003*SL	0.114 + 0.002*SL	0.120 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)											
oa321						*oa321d2*					
A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.1	1.1	1.1	1.2	1.1	1.0	1.1	1.1	1.1	1.2	0.8

Gate Count	
oa321	*oa321d2*
3.33	4.33

oa321

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.188	0.131 + 0.029*SL	0.125 + 0.030*SL	0.120 + 0.031*SL
	t_F	0.092	0.063 + 0.015*SL	0.060 + 0.015*SL	0.053 + 0.016*SL
	t_{PLH}	0.086	0.057 + 0.014*SL	0.059 + 0.014*SL	0.062 + 0.014*SL
	t_{PHL}	0.062	0.047 + 0.008*SL	0.047 + 0.008*SL	0.048 + 0.008*SL
B to Y	t_R	0.185	0.126 + 0.030*SL	0.123 + 0.030*SL	0.120 + 0.031*SL
	t_F	0.103	0.075 + 0.014*SL	0.070 + 0.015*SL	0.064 + 0.016*SL
	t_{PLH}	0.097	0.068 + 0.014*SL	0.070 + 0.014*SL	0.075 + 0.014*SL
	t_{PHL}	0.069	0.053 + 0.008*SL	0.053 + 0.008*SL	0.054 + 0.008*SL
C to Y	t_R	0.184	0.125 + 0.030*SL	0.121 + 0.030*SL	0.120 + 0.031*SL
	t_F	0.114	0.086 + 0.014*SL	0.081 + 0.015*SL	0.075 + 0.016*SL
	t_{PLH}	0.102	0.074 + 0.014*SL	0.075 + 0.014*SL	0.080 + 0.014*SL
	t_{PHL}	0.073	0.057 + 0.008*SL	0.058 + 0.008*SL	0.060 + 0.008*SL
D to Y	t_R	0.146	0.109 + 0.019*SL	0.103 + 0.020*SL	0.097 + 0.020*SL
	t_F	0.101	0.072 + 0.015*SL	0.068 + 0.016*SL	0.064 + 0.016*SL
	t_{PLH}	0.078	0.060 + 0.009*SL	0.060 + 0.009*SL	0.062 + 0.009*SL
	t_{PHL}	0.073	0.057 + 0.008*SL	0.059 + 0.008*SL	0.061 + 0.008*SL
E to Y	t_R	0.142	0.103 + 0.020*SL	0.100 + 0.020*SL	0.096 + 0.020*SL
	t_F	0.111	0.082 + 0.015*SL	0.078 + 0.016*SL	0.075 + 0.016*SL
	t_{PLH}	0.082	0.063 + 0.009*SL	0.064 + 0.009*SL	0.067 + 0.009*SL
	t_{PHL}	0.080	0.063 + 0.008*SL	0.065 + 0.008*SL	0.067 + 0.008*SL
F to Y	t_R	0.107	0.093 + 0.007*SL	0.083 + 0.010*SL	0.070 + 0.010*SL
	t_F	0.109	0.078 + 0.015*SL	0.077 + 0.016*SL	0.075 + 0.016*SL
	t_{PLH}	0.055	0.045 + 0.005*SL	0.046 + 0.005*SL	0.047 + 0.005*SL
	t_{PHL}	0.083	0.066 + 0.008*SL	0.068 + 0.008*SL	0.070 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

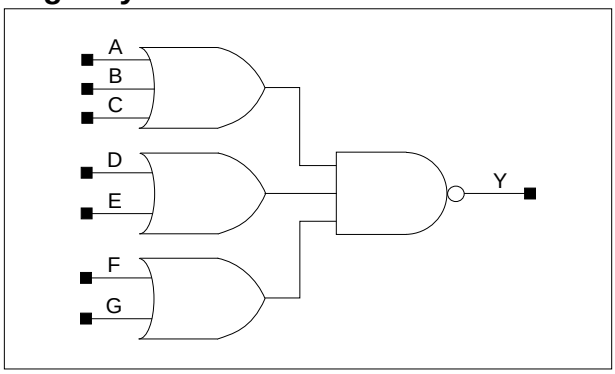
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa321d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.019 + 0.005*SL	0.026 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.131	0.124 + 0.003*SL	0.128 + 0.002*SL	0.131 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.104 + 0.002*SL
B to Y	t_R	0.038	0.029 + 0.004*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.143	0.137 + 0.003*SL	0.141 + 0.002*SL	0.143 + 0.002*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.109 + 0.002*SL	0.113 + 0.002*SL
C to Y	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.023 + 0.003*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.148	0.142 + 0.003*SL	0.145 + 0.002*SL	0.148 + 0.002*SL
	t_{PHL}	0.117	0.111 + 0.003*SL	0.115 + 0.002*SL	0.119 + 0.002*SL
D to Y	t_R	0.038	0.029 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.124	0.118 + 0.003*SL	0.121 + 0.002*SL	0.124 + 0.002*SL
	t_{PHL}	0.116	0.110 + 0.003*SL	0.113 + 0.002*SL	0.118 + 0.002*SL
E to Y	t_R	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.022 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.128	0.122 + 0.003*SL	0.125 + 0.002*SL	0.128 + 0.002*SL
	t_{PHL}	0.124	0.118 + 0.003*SL	0.121 + 0.002*SL	0.126 + 0.002*SL
F to Y	t_R	0.045	0.037 + 0.004*SL	0.034 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.029	0.022 + 0.003*SL	0.021 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.165	0.158 + 0.003*SL	0.163 + 0.002*SL	0.166 + 0.002*SL
	t_{PHL}	0.126	0.120 + 0.003*SL	0.123 + 0.002*SL	0.128 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	x	x	1
x	x	x	x	x	0	0	1
Other States							0

Cell Data

Input Load (SL)						
oa322						
A	B	C	D	E	F	G
0.9	1.0	1.0	1.1	1.2	1.1	1.2
oa322d2						
A	B	C	D	E	F	G
1.0	1.0	1.1	1.1	1.2	1.1	1.2

Gate Count	
oa322	*oa322d2*
3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.224	0.166 + 0.029*SL	0.160 + 0.030*SL	0.156 + 0.031*SL
	t_F	0.109	0.077 + 0.016*SL	0.075 + 0.017*SL	0.070 + 0.017*SL
	t_{PLH}	0.092	0.063 + 0.014*SL	0.065 + 0.014*SL	0.071 + 0.014*SL
	t_{PHL}	0.075	0.059 + 0.008*SL	0.059 + 0.008*SL	0.060 + 0.008*SL
B to Y	t_R	0.221	0.162 + 0.030*SL	0.158 + 0.030*SL	0.156 + 0.031*SL
	t_F	0.121	0.089 + 0.016*SL	0.086 + 0.017*SL	0.082 + 0.017*SL
	t_{PLH}	0.105	0.076 + 0.015*SL	0.078 + 0.014*SL	0.085 + 0.014*SL
	t_{PHL}	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.068 + 0.008*SL
C to Y	t_R	0.220	0.161 + 0.030*SL	0.157 + 0.030*SL	0.156 + 0.031*SL
	t_F	0.133	0.101 + 0.016*SL	0.098 + 0.017*SL	0.094 + 0.017*SL
	t_{PLH}	0.110	0.080 + 0.015*SL	0.082 + 0.014*SL	0.090 + 0.014*SL
	t_{PHL}	0.088	0.070 + 0.009*SL	0.072 + 0.008*SL	0.074 + 0.008*SL
D to Y	t_R	0.169	0.132 + 0.019*SL	0.126 + 0.020*SL	0.120 + 0.020*SL
	t_F	0.119	0.087 + 0.016*SL	0.085 + 0.017*SL	0.082 + 0.017*SL
	t_{PLH}	0.082	0.062 + 0.010*SL	0.064 + 0.009*SL	0.067 + 0.009*SL
	t_{PHL}	0.087	0.069 + 0.009*SL	0.071 + 0.008*SL	0.074 + 0.008*SL
E to Y	t_R	0.165	0.126 + 0.020*SL	0.124 + 0.020*SL	0.120 + 0.020*SL
	t_F	0.130	0.097 + 0.016*SL	0.095 + 0.017*SL	0.094 + 0.017*SL
	t_{PLH}	0.085	0.066 + 0.010*SL	0.068 + 0.009*SL	0.071 + 0.009*SL
	t_{PHL}	0.093	0.076 + 0.009*SL	0.077 + 0.008*SL	0.079 + 0.008*SL
F to Y	t_R	0.185	0.147 + 0.019*SL	0.143 + 0.020*SL	0.137 + 0.020*SL
	t_F	0.118	0.085 + 0.017*SL	0.084 + 0.017*SL	0.082 + 0.017*SL
	t_{PLH}	0.093	0.074 + 0.009*SL	0.074 + 0.009*SL	0.079 + 0.009*SL
	t_{PHL}	0.092	0.075 + 0.009*SL	0.076 + 0.008*SL	0.079 + 0.008*SL
G to Y	t_R	0.182	0.142 + 0.020*SL	0.141 + 0.020*SL	0.137 + 0.020*SL
	t_F	0.129	0.096 + 0.017*SL	0.095 + 0.017*SL	0.094 + 0.017*SL
	t_{PLH}	0.097	0.078 + 0.010*SL	0.079 + 0.009*SL	0.083 + 0.009*SL
	t_{PHL}	0.099	0.081 + 0.009*SL	0.083 + 0.008*SL	0.085 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa322d2

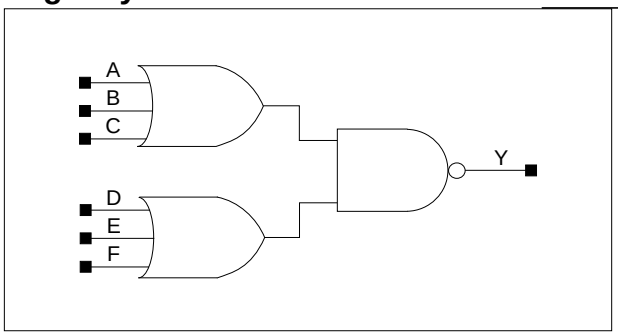
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.032 + 0.005*SL	0.032 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.147	0.140 + 0.003*SL	0.144 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.121	0.115 + 0.003*SL	0.118 + 0.002*SL	0.123 + 0.002*SL
B to Y	t_R	0.041	0.032 + 0.005*SL	0.032 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.158	0.152 + 0.003*SL	0.156 + 0.002*SL	0.159 + 0.002*SL
	t_{PHL}	0.129	0.123 + 0.003*SL	0.127 + 0.002*SL	0.132 + 0.002*SL
C to Y	t_R	0.043	0.035 + 0.004*SL	0.032 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.163	0.156 + 0.003*SL	0.160 + 0.002*SL	0.163 + 0.002*SL
	t_{PHL}	0.136	0.130 + 0.003*SL	0.133 + 0.002*SL	0.138 + 0.002*SL
D to Y	t_R	0.039	0.031 + 0.004*SL	0.030 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.030	0.023 + 0.003*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.134	0.128 + 0.003*SL	0.131 + 0.002*SL	0.134 + 0.002*SL
	t_{PHL}	0.133	0.127 + 0.003*SL	0.130 + 0.002*SL	0.135 + 0.002*SL
E to Y	t_R	0.038	0.029 + 0.004*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.024 + 0.003*SL	0.022 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.139	0.132 + 0.003*SL	0.136 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.142	0.135 + 0.003*SL	0.139 + 0.002*SL	0.144 + 0.002*SL
F to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.145	0.139 + 0.003*SL	0.142 + 0.002*SL	0.145 + 0.002*SL
	t_{PHL}	0.137	0.131 + 0.003*SL	0.135 + 0.002*SL	0.139 + 0.002*SL
G to Y	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.031	0.024 + 0.003*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.149	0.143 + 0.003*SL	0.146 + 0.002*SL	0.148 + 0.002*SL
	t_{PHL}	0.146	0.140 + 0.003*SL	0.143 + 0.002*SL	0.148 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

oa33/oa33d2

Two 3-ORs into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
Other States						0

Cell Data

Input Load (SL)					
oa33					
A	B	C	D	E	F
0.9	1.0	1.0	0.9	1.0	1.0
oa33d2					
A	B	C	D	E	F
1.1	1.2	1.2	1.1	1.2	1.2

Gate Count	
oa33	*oa33d2*
3.00	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

oa33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.201	0.145 + 0.028*SL	0.136 + 0.030*SL	0.128 + 0.031*SL
	t_F	0.093	0.062 + 0.015*SL	0.059 + 0.016*SL	0.052 + 0.017*SL
	t_{PLH}	0.074	0.046 + 0.014*SL	0.047 + 0.014*SL	0.049 + 0.014*SL
	t_{PHL}	0.065	0.048 + 0.009*SL	0.049 + 0.008*SL	0.051 + 0.008*SL
B to Y	t_R	0.198	0.141 + 0.029*SL	0.134 + 0.030*SL	0.128 + 0.031*SL
	t_F	0.103	0.073 + 0.015*SL	0.068 + 0.016*SL	0.064 + 0.017*SL
	t_{PLH}	0.086	0.057 + 0.015*SL	0.059 + 0.014*SL	0.062 + 0.014*SL
	t_{PHL}	0.072	0.055 + 0.009*SL	0.056 + 0.008*SL	0.059 + 0.008*SL
C to Y	t_R	0.196	0.138 + 0.029*SL	0.133 + 0.030*SL	0.128 + 0.031*SL
	t_F	0.115	0.084 + 0.015*SL	0.080 + 0.016*SL	0.075 + 0.017*SL
	t_{PLH}	0.091	0.063 + 0.014*SL	0.063 + 0.014*SL	0.066 + 0.014*SL
	t_{PHL}	0.077	0.059 + 0.009*SL	0.061 + 0.008*SL	0.064 + 0.008*SL
D to Y	t_R	0.189	0.131 + 0.029*SL	0.125 + 0.030*SL	0.122 + 0.031*SL
	t_F	0.090	0.060 + 0.015*SL	0.055 + 0.016*SL	0.052 + 0.017*SL
	t_{PLH}	0.090	0.062 + 0.014*SL	0.063 + 0.014*SL	0.067 + 0.014*SL
	t_{PHL}	0.072	0.054 + 0.009*SL	0.056 + 0.008*SL	0.059 + 0.008*SL
E to Y	t_R	0.186	0.126 + 0.030*SL	0.124 + 0.030*SL	0.122 + 0.031*SL
	t_F	0.100	0.068 + 0.016*SL	0.068 + 0.016*SL	0.064 + 0.017*SL
	t_{PLH}	0.103	0.074 + 0.014*SL	0.076 + 0.014*SL	0.080 + 0.014*SL
	t_{PHL}	0.079	0.062 + 0.009*SL	0.064 + 0.008*SL	0.066 + 0.008*SL
F to Y	t_R	0.185	0.126 + 0.030*SL	0.123 + 0.031*SL	0.122 + 0.031*SL
	t_F	0.112	0.081 + 0.015*SL	0.076 + 0.017*SL	0.075 + 0.017*SL
	t_{PLH}	0.107	0.078 + 0.014*SL	0.079 + 0.014*SL	0.084 + 0.014*SL
	t_{PHL}	0.084	0.066 + 0.009*SL	0.068 + 0.008*SL	0.072 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

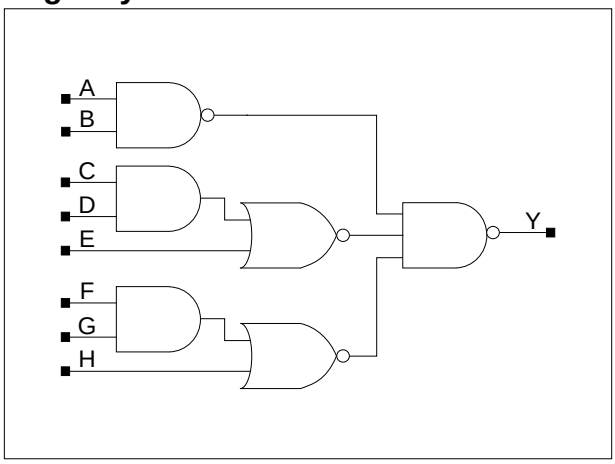
oa33d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.042	0.034 + 0.004*SL	0.032 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.031	0.021 + 0.005*SL	0.026 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.134	0.128 + 0.003*SL	0.132 + 0.002*SL	0.135 + 0.002*SL
	t_{PHL}	0.087	0.081 + 0.003*SL	0.083 + 0.002*SL	0.087 + 0.002*SL
B to Y	t_R	0.042	0.034 + 0.004*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.146	0.139 + 0.003*SL	0.143 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.093	0.087 + 0.003*SL	0.091 + 0.002*SL	0.094 + 0.002*SL
C to Y	t_R	0.041	0.032 + 0.004*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.027	0.020 + 0.004*SL	0.019 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.150	0.144 + 0.003*SL	0.148 + 0.002*SL	0.151 + 0.002*SL
	t_{PHL}	0.097	0.091 + 0.003*SL	0.094 + 0.002*SL	0.098 + 0.002*SL
D to Y	t_R	0.040	0.031 + 0.005*SL	0.031 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.026	0.018 + 0.004*SL	0.019 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.161	0.154 + 0.003*SL	0.158 + 0.002*SL	0.161 + 0.002*SL
	t_{PHL}	0.094	0.088 + 0.003*SL	0.091 + 0.002*SL	0.095 + 0.002*SL
E to Y	t_R	0.040	0.031 + 0.005*SL	0.031 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.173	0.166 + 0.003*SL	0.170 + 0.002*SL	0.173 + 0.002*SL
	t_{PHL}	0.099	0.093 + 0.003*SL	0.097 + 0.002*SL	0.100 + 0.002*SL
F to Y	t_R	0.041	0.033 + 0.004*SL	0.031 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.027	0.018 + 0.004*SL	0.020 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.178	0.171 + 0.003*SL	0.175 + 0.002*SL	0.178 + 0.002*SL
	t_{PHL}	0.103	0.097 + 0.003*SL	0.101 + 0.002*SL	0.104 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	x	x	x	1
x	x	x	x	x	1	1	x	1
x	x	x	x	x	x	x	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
scg1								*scg1*
A	B	C	D	E	F	G	H	
1.1	1.2	1.0	1.0	1.0	1.0	1.0	1.0	5.33
scg1d2								*scg1d2*
A	B	C	D	E	F	G	H	
1.2	1.2	1.0	1.0	1.0	1.0	1.0	1.0	6.33

scg1/scg1d2

2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.036 + 0.015*SL	0.032 + 0.016*SL	0.029 + 0.016*SL
	t_F	0.060	0.033 + 0.014*SL	0.033 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.066	0.051 + 0.007*SL	0.053 + 0.007*SL	0.053 + 0.007*SL
	t_{PHL}	0.067	0.052 + 0.007*SL	0.054 + 0.007*SL	0.054 + 0.007*SL
B to Y	t_R	0.065	0.036 + 0.015*SL	0.031 + 0.016*SL	0.029 + 0.016*SL
	t_F	0.061	0.036 + 0.013*SL	0.032 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.067	0.052 + 0.007*SL	0.054 + 0.007*SL	0.054 + 0.007*SL
	t_{PHL}	0.071	0.056 + 0.007*SL	0.058 + 0.007*SL	0.058 + 0.007*SL
C to Y	t_R	0.075	0.045 + 0.015*SL	0.042 + 0.016*SL	0.036 + 0.016*SL
	t_F	0.065	0.039 + 0.013*SL	0.035 + 0.014*SL	0.031 + 0.014*SL
	t_{PLH}	0.087	0.072 + 0.007*SL	0.074 + 0.007*SL	0.074 + 0.007*SL
	t_{PHL}	0.086	0.070 + 0.008*SL	0.074 + 0.007*SL	0.076 + 0.007*SL
D to Y	t_R	0.075	0.046 + 0.015*SL	0.041 + 0.016*SL	0.037 + 0.016*SL
	t_F	0.065	0.039 + 0.013*SL	0.037 + 0.014*SL	0.031 + 0.014*SL
	t_{PLH}	0.086	0.072 + 0.007*SL	0.073 + 0.007*SL	0.074 + 0.007*SL
	t_{PHL}	0.090	0.074 + 0.008*SL	0.077 + 0.007*SL	0.080 + 0.007*SL
E to Y	t_R	0.074	0.044 + 0.015*SL	0.041 + 0.016*SL	0.036 + 0.016*SL
	t_F	0.066	0.040 + 0.013*SL	0.038 + 0.014*SL	0.032 + 0.014*SL
	t_{PLH}	0.087	0.072 + 0.007*SL	0.074 + 0.007*SL	0.074 + 0.007*SL
	t_{PHL}	0.098	0.083 + 0.008*SL	0.087 + 0.007*SL	0.089 + 0.007*SL
F to Y	t_R	0.081	0.050 + 0.015*SL	0.048 + 0.016*SL	0.043 + 0.016*SL
	t_F	0.063	0.036 + 0.013*SL	0.034 + 0.014*SL	0.030 + 0.014*SL
	t_{PLH}	0.090	0.075 + 0.007*SL	0.077 + 0.007*SL	0.078 + 0.007*SL
	t_{PHL}	0.087	0.072 + 0.008*SL	0.075 + 0.007*SL	0.077 + 0.007*SL
G to Y	t_R	0.081	0.051 + 0.015*SL	0.048 + 0.016*SL	0.043 + 0.016*SL
	t_F	0.062	0.035 + 0.014*SL	0.035 + 0.014*SL	0.031 + 0.014*SL
	t_{PLH}	0.090	0.075 + 0.007*SL	0.077 + 0.007*SL	0.078 + 0.007*SL
	t_{PHL}	0.091	0.076 + 0.008*SL	0.079 + 0.007*SL	0.081 + 0.007*SL
H to Y	t_R	0.080	0.049 + 0.016*SL	0.047 + 0.016*SL	0.042 + 0.016*SL
	t_F	0.064	0.037 + 0.013*SL	0.035 + 0.014*SL	0.030 + 0.014*SL
	t_{PLH}	0.091	0.076 + 0.007*SL	0.077 + 0.007*SL	0.078 + 0.007*SL
	t_{PHL}	0.101	0.086 + 0.008*SL	0.088 + 0.007*SL	0.091 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg1d2

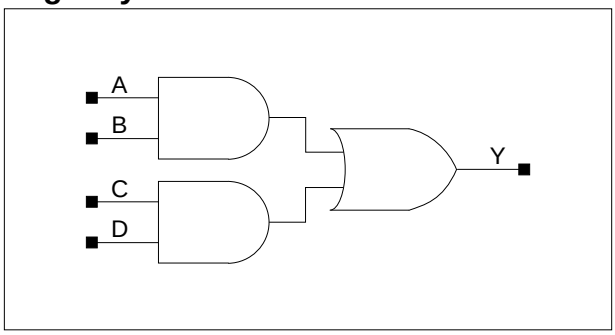
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.050	0.036 + 0.007*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_F	0.045	0.033 + 0.006*SL	0.030 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.064	0.056 + 0.004*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PHL}	0.062	0.055 + 0.004*SL	0.056 + 0.003*SL	0.057 + 0.003*SL
B to Y	t_R	0.053	0.042 + 0.006*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_F	0.046	0.033 + 0.007*SL	0.032 + 0.007*SL	0.027 + 0.007*SL
	t_{PLH}	0.064	0.056 + 0.004*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PHL}	0.065	0.058 + 0.004*SL	0.059 + 0.003*SL	0.061 + 0.003*SL
C to Y	t_R	0.062	0.048 + 0.007*SL	0.046 + 0.008*SL	0.036 + 0.008*SL
	t_F	0.051	0.038 + 0.007*SL	0.037 + 0.007*SL	0.032 + 0.007*SL
	t_{PLH}	0.089	0.080 + 0.004*SL	0.083 + 0.004*SL	0.085 + 0.004*SL
	t_{PHL}	0.087	0.078 + 0.004*SL	0.082 + 0.004*SL	0.087 + 0.003*SL
D to Y	t_R	0.061	0.046 + 0.008*SL	0.045 + 0.008*SL	0.035 + 0.008*SL
	t_F	0.052	0.037 + 0.007*SL	0.039 + 0.007*SL	0.033 + 0.007*SL
	t_{PLH}	0.088	0.080 + 0.004*SL	0.082 + 0.004*SL	0.085 + 0.004*SL
	t_{PHL}	0.090	0.081 + 0.005*SL	0.085 + 0.004*SL	0.091 + 0.003*SL
E to Y	t_R	0.060	0.046 + 0.007*SL	0.042 + 0.008*SL	0.034 + 0.008*SL
	t_F	0.053	0.041 + 0.006*SL	0.038 + 0.007*SL	0.033 + 0.007*SL
	t_{PLH}	0.086	0.078 + 0.004*SL	0.080 + 0.004*SL	0.081 + 0.004*SL
	t_{PHL}	0.100	0.091 + 0.004*SL	0.095 + 0.004*SL	0.101 + 0.003*SL
F to Y	t_R	0.068	0.053 + 0.007*SL	0.052 + 0.008*SL	0.042 + 0.008*SL
	t_F	0.049	0.035 + 0.007*SL	0.035 + 0.007*SL	0.031 + 0.007*SL
	t_{PLH}	0.091	0.083 + 0.004*SL	0.085 + 0.004*SL	0.087 + 0.004*SL
	t_{PHL}	0.088	0.079 + 0.004*SL	0.082 + 0.004*SL	0.088 + 0.003*SL
G to Y	t_R	0.067	0.051 + 0.008*SL	0.051 + 0.008*SL	0.042 + 0.008*SL
	t_F	0.049	0.037 + 0.006*SL	0.035 + 0.007*SL	0.032 + 0.007*SL
	t_{PLH}	0.090	0.082 + 0.004*SL	0.084 + 0.004*SL	0.087 + 0.004*SL
	t_{PHL}	0.091	0.082 + 0.004*SL	0.086 + 0.004*SL	0.091 + 0.003*SL
H to Y	t_R	0.064	0.048 + 0.008*SL	0.048 + 0.008*SL	0.040 + 0.008*SL
	t_F	0.050	0.036 + 0.007*SL	0.037 + 0.007*SL	0.032 + 0.007*SL
	t_{PLH}	0.089	0.081 + 0.004*SL	0.082 + 0.004*SL	0.084 + 0.004*SL
	t_{PHL}	0.101	0.093 + 0.004*SL	0.096 + 0.004*SL	0.101 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg2/scg2d2/scg2d4

Two 2-ANDs into 2-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)												Gate Count		
scg2				*scg2d2*				*scg2d4*				*scg2*	*scg2d2*	*scg2d4*
A	B	C	D	A	B	C	D	A	B	C	D			
1.1	1.1	1.0	1.1	1.1	1.1	1.1	1.1	1.0	1.1	1.1	1.1	2.67	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.028 + 0.009*SL	0.025 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.044	0.027 + 0.009*SL	0.031 + 0.008*SL	0.024 + 0.008*SL
	t_{PLH}	0.066	0.055 + 0.006*SL	0.059 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.080	0.067 + 0.006*SL	0.074 + 0.005*SL	0.082 + 0.004*SL
B to Y	t_R	0.048	0.033 + 0.008*SL	0.024 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.044	0.028 + 0.008*SL	0.030 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.066	0.054 + 0.006*SL	0.059 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.084	0.072 + 0.006*SL	0.079 + 0.005*SL	0.087 + 0.004*SL
C to Y	t_R	0.050	0.031 + 0.009*SL	0.029 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.044	0.025 + 0.009*SL	0.032 + 0.007*SL	0.024 + 0.008*SL
	t_{PLH}	0.079	0.067 + 0.006*SL	0.072 + 0.005*SL	0.075 + 0.005*SL
	t_{PHL}	0.094	0.082 + 0.006*SL	0.089 + 0.005*SL	0.096 + 0.004*SL
D to Y	t_R	0.049	0.029 + 0.010*SL	0.030 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.045	0.028 + 0.009*SL	0.032 + 0.008*SL	0.025 + 0.008*SL
	t_{PLH}	0.079	0.067 + 0.006*SL	0.072 + 0.005*SL	0.076 + 0.004*SL
	t_{PHL}	0.099	0.087 + 0.006*SL	0.094 + 0.005*SL	0.102 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.026 + 0.005*SL	0.029 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.040	0.031 + 0.005*SL	0.034 + 0.004*SL	0.031 + 0.004*SL
	t_{PLH}	0.065	0.058 + 0.003*SL	0.062 + 0.002*SL	0.067 + 0.002*SL
	t_{PHL}	0.080	0.073 + 0.004*SL	0.078 + 0.002*SL	0.091 + 0.002*SL
B to Y	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.041	0.031 + 0.005*SL	0.036 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.065	0.058 + 0.003*SL	0.062 + 0.002*SL	0.068 + 0.002*SL
	t_{PHL}	0.085	0.077 + 0.004*SL	0.083 + 0.002*SL	0.096 + 0.002*SL
C to Y	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.040	0.030 + 0.005*SL	0.035 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.078	0.071 + 0.004*SL	0.075 + 0.002*SL	0.081 + 0.002*SL
	t_{PHL}	0.096	0.088 + 0.004*SL	0.093 + 0.002*SL	0.106 + 0.002*SL
D to Y	t_R	0.043	0.034 + 0.005*SL	0.034 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.041	0.032 + 0.005*SL	0.036 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.078	0.071 + 0.004*SL	0.075 + 0.002*SL	0.081 + 0.002*SL
	t_{PHL}	0.101	0.093 + 0.004*SL	0.098 + 0.002*SL	0.112 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg2d4

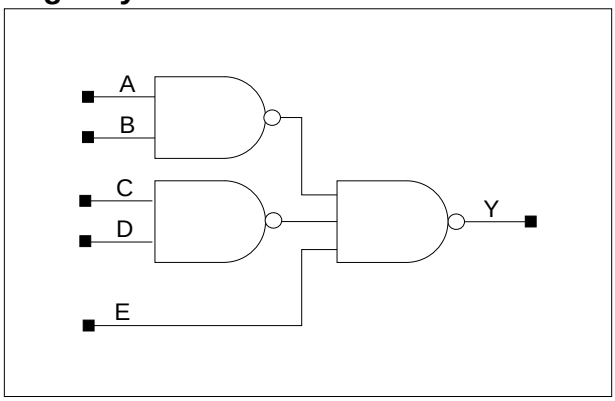
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.042	0.037 + 0.002*SL	0.037 + 0.002*SL	0.028 + 0.003*SL
	t_F	0.050	0.045 + 0.002*SL	0.047 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.077	0.073 + 0.002*SL	0.076 + 0.001*SL	0.086 + 0.001*SL
	t_{PHL}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.117 + 0.001*SL
B to Y	t_R	0.046	0.040 + 0.003*SL	0.044 + 0.002*SL	0.029 + 0.003*SL
	t_F	0.052	0.047 + 0.002*SL	0.049 + 0.002*SL	0.046 + 0.002*SL
	t_{PLH}	0.076	0.072 + 0.002*SL	0.075 + 0.001*SL	0.086 + 0.001*SL
	t_{PHL}	0.103	0.098 + 0.002*SL	0.102 + 0.001*SL	0.122 + 0.001*SL
C to Y	t_R	0.045	0.040 + 0.003*SL	0.042 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.050	0.045 + 0.002*SL	0.047 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.090	0.086 + 0.002*SL	0.089 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.114	0.109 + 0.002*SL	0.113 + 0.001*SL	0.133 + 0.001*SL
D to Y	t_R	0.046	0.042 + 0.002*SL	0.041 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.052	0.047 + 0.002*SL	0.049 + 0.002*SL	0.046 + 0.002*SL
	t_{PLH}	0.091	0.086 + 0.002*SL	0.090 + 0.001*SL	0.101 + 0.001*SL
	t_{PHL}	0.118	0.114 + 0.002*SL	0.118 + 0.001*SL	0.139 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg3/scg3d2/scg3d4

Two 2-NANDs into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
scg3					*scg3d2*					*scg3d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.2	1.2	1.2	1.2	1.0	1.1	1.2	1.1	1.2	2.5	1.1	1.2	1.1	1.2	3.8

Gate Count		
scg3	*scg3d2*	*scg3d4*
3.33	4.67	7.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.036 + 0.015*SL	0.031 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.060	0.033 + 0.013*SL	0.031 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.067	0.052 + 0.007*SL	0.054 + 0.007*SL	0.054 + 0.007*SL
	t_{PHL}	0.067	0.053 + 0.007*SL	0.055 + 0.007*SL	0.055 + 0.007*SL
B to Y	t_R	0.065	0.036 + 0.014*SL	0.030 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.060	0.035 + 0.013*SL	0.030 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.068	0.053 + 0.007*SL	0.054 + 0.007*SL	0.055 + 0.007*SL
	t_{PHL}	0.071	0.057 + 0.007*SL	0.058 + 0.007*SL	0.059 + 0.007*SL
C to Y	t_R	0.071	0.041 + 0.015*SL	0.037 + 0.016*SL	0.034 + 0.016*SL
	t_F	0.059	0.032 + 0.014*SL	0.030 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.070	0.056 + 0.007*SL	0.056 + 0.007*SL	0.057 + 0.007*SL
	t_{PHL}	0.071	0.056 + 0.007*SL	0.058 + 0.007*SL	0.058 + 0.007*SL
D to Y	t_R	0.071	0.041 + 0.015*SL	0.036 + 0.016*SL	0.034 + 0.016*SL
	t_F	0.060	0.033 + 0.013*SL	0.031 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.071	0.056 + 0.007*SL	0.057 + 0.007*SL	0.058 + 0.007*SL
	t_{PHL}	0.075	0.060 + 0.007*SL	0.062 + 0.007*SL	0.062 + 0.007*SL
E to Y	t_R	0.085	0.057 + 0.014*SL	0.052 + 0.016*SL	0.040 + 0.016*SL
	t_F	0.063	0.038 + 0.013*SL	0.033 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.056	0.042 + 0.007*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.045	0.029 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.050	0.036 + 0.007*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_F	0.046	0.033 + 0.007*SL	0.032 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.064	0.056 + 0.004*SL	0.058 + 0.004*SL	0.060 + 0.004*SL
	t_{PHL}	0.064	0.056 + 0.004*SL	0.058 + 0.003*SL	0.059 + 0.003*SL
B to Y	t_R	0.053	0.042 + 0.006*SL	0.032 + 0.008*SL	0.025 + 0.008*SL
	t_F	0.045	0.032 + 0.007*SL	0.031 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.065	0.057 + 0.004*SL	0.058 + 0.004*SL	0.060 + 0.004*SL
	t_{PHL}	0.067	0.059 + 0.004*SL	0.061 + 0.003*SL	0.063 + 0.003*SL
C to Y	t_R	0.056	0.042 + 0.007*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_F	0.044	0.030 + 0.007*SL	0.031 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.070	0.062 + 0.004*SL	0.063 + 0.004*SL	0.064 + 0.004*SL
	t_{PHL}	0.069	0.061 + 0.004*SL	0.063 + 0.003*SL	0.065 + 0.003*SL
D to Y	t_R	0.059	0.048 + 0.005*SL	0.038 + 0.008*SL	0.032 + 0.008*SL
	t_F	0.044	0.030 + 0.007*SL	0.031 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.070	0.062 + 0.004*SL	0.063 + 0.004*SL	0.064 + 0.004*SL
	t_{PHL}	0.072	0.064 + 0.004*SL	0.066 + 0.003*SL	0.069 + 0.003*SL
E to Y	t_R	0.068	0.054 + 0.007*SL	0.051 + 0.008*SL	0.036 + 0.008*SL
	t_F	0.047	0.033 + 0.007*SL	0.034 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.047	0.040 + 0.004*SL	0.041 + 0.004*SL	0.041 + 0.004*SL
	t_{PHL}	0.036	0.027 + 0.004*SL	0.030 + 0.003*SL	0.033 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

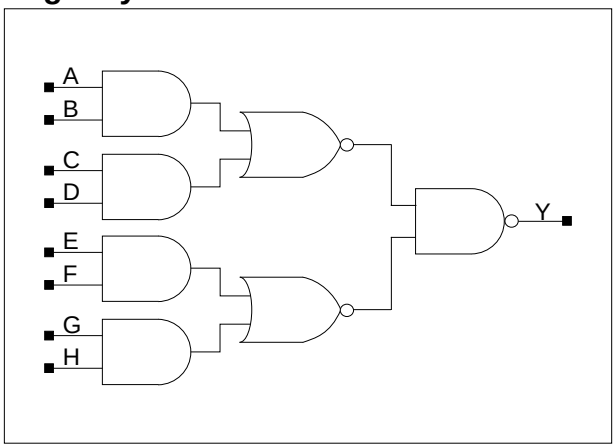
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg3d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.049	0.041 + 0.004*SL	0.042 + 0.004*SL	0.032 + 0.004*SL
	t_F	0.048	0.044 + 0.002*SL	0.037 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.076	0.072 + 0.002*SL	0.074 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.073	0.068 + 0.002*SL	0.070 + 0.002*SL	0.074 + 0.002*SL
B to Y	t_R	0.055	0.053 + 0.001*SL	0.041 + 0.004*SL	0.031 + 0.004*SL
	t_F	0.046	0.039 + 0.004*SL	0.040 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.075	0.071 + 0.002*SL	0.073 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.076	0.071 + 0.002*SL	0.073 + 0.002*SL	0.077 + 0.002*SL
C to Y	t_R	0.056	0.049 + 0.003*SL	0.047 + 0.004*SL	0.038 + 0.004*SL
	t_F	0.043	0.036 + 0.004*SL	0.037 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.081	0.077 + 0.002*SL	0.078 + 0.002*SL	0.081 + 0.002*SL
	t_{PHL}	0.079	0.074 + 0.002*SL	0.076 + 0.002*SL	0.082 + 0.002*SL
D to Y	t_R	0.057	0.050 + 0.004*SL	0.049 + 0.004*SL	0.038 + 0.004*SL
	t_F	0.045	0.037 + 0.004*SL	0.039 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.081	0.076 + 0.002*SL	0.078 + 0.002*SL	0.082 + 0.002*SL
	t_{PHL}	0.082	0.077 + 0.002*SL	0.079 + 0.002*SL	0.085 + 0.002*SL
E to Y	t_R	0.064	0.057 + 0.004*SL	0.057 + 0.004*SL	0.039 + 0.004*SL
	t_F	0.043	0.036 + 0.004*SL	0.037 + 0.003*SL	0.031 + 0.004*SL
	t_{PLH}	0.046	0.041 + 0.002*SL	0.043 + 0.002*SL	0.043 + 0.002*SL
	t_{PHL}	0.035	0.030 + 0.002*SL	0.033 + 0.002*SL	0.038 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	1	x	x	1
x	x	x	x	x	x	1	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
scg4								*scg4*
A	B	C	D	E	F	G	H	
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	5.00
scg4d2								*scg4d2*
A	B	C	D	E	F	G	H	
1.0	1.1	1.1	1.1	1.1	1.1	1.4	1.1	5.67
scg4d4								*scg4d4*
A	B	C	D	E	F	G	H	
1.0	1.1	1.1	1.1	1.0	1.1	1.1	1.1	7.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.052	0.032 + 0.010*SL	0.031 + 0.010*SL	0.024 + 0.011*SL
	t_F	0.055	0.036 + 0.009*SL	0.036 + 0.009*SL	0.031 + 0.010*SL
	t_{PLH}	0.072	0.061 + 0.005*SL	0.064 + 0.005*SL	0.065 + 0.005*SL
	t_{PHL}	0.085	0.072 + 0.006*SL	0.077 + 0.005*SL	0.082 + 0.005*SL
B to Y	t_R	0.054	0.036 + 0.009*SL	0.030 + 0.010*SL	0.024 + 0.011*SL
	t_F	0.057	0.037 + 0.010*SL	0.039 + 0.009*SL	0.032 + 0.010*SL
	t_{PLH}	0.071	0.060 + 0.006*SL	0.063 + 0.005*SL	0.065 + 0.005*SL
	t_{PHL}	0.090	0.077 + 0.006*SL	0.082 + 0.005*SL	0.087 + 0.005*SL
C to Y	t_R	0.056	0.038 + 0.009*SL	0.032 + 0.010*SL	0.027 + 0.011*SL
	t_F	0.055	0.036 + 0.009*SL	0.035 + 0.010*SL	0.031 + 0.010*SL
	t_{PLH}	0.086	0.075 + 0.006*SL	0.078 + 0.005*SL	0.080 + 0.005*SL
	t_{PHL}	0.101	0.088 + 0.006*SL	0.093 + 0.005*SL	0.098 + 0.005*SL
D to Y	t_R	0.058	0.040 + 0.009*SL	0.035 + 0.010*SL	0.028 + 0.011*SL
	t_F	0.057	0.037 + 0.010*SL	0.039 + 0.009*SL	0.032 + 0.010*SL
	t_{PLH}	0.085	0.074 + 0.006*SL	0.078 + 0.005*SL	0.081 + 0.005*SL
	t_{PHL}	0.106	0.093 + 0.007*SL	0.098 + 0.005*SL	0.103 + 0.005*SL
E to Y	t_R	0.057	0.038 + 0.010*SL	0.034 + 0.010*SL	0.028 + 0.011*SL
	t_F	0.051	0.032 + 0.010*SL	0.033 + 0.010*SL	0.029 + 0.010*SL
	t_{PLH}	0.074	0.063 + 0.005*SL	0.066 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.086	0.074 + 0.006*SL	0.078 + 0.005*SL	0.083 + 0.005*SL
F to Y	t_R	0.060	0.043 + 0.009*SL	0.035 + 0.010*SL	0.029 + 0.011*SL
	t_F	0.053	0.033 + 0.010*SL	0.036 + 0.009*SL	0.029 + 0.010*SL
	t_{PLH}	0.074	0.063 + 0.005*SL	0.066 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.091	0.078 + 0.006*SL	0.083 + 0.005*SL	0.088 + 0.005*SL
G to Y	t_R	0.061	0.041 + 0.010*SL	0.040 + 0.010*SL	0.032 + 0.011*SL
	t_F	0.054	0.035 + 0.010*SL	0.036 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.088	0.077 + 0.006*SL	0.080 + 0.005*SL	0.082 + 0.005*SL
	t_{PHL}	0.100	0.088 + 0.006*SL	0.091 + 0.005*SL	0.097 + 0.005*SL
H to Y	t_R	0.061	0.043 + 0.009*SL	0.038 + 0.010*SL	0.032 + 0.011*SL
	t_F	0.053	0.033 + 0.010*SL	0.033 + 0.010*SL	0.030 + 0.010*SL
	t_{PLH}	0.087	0.076 + 0.006*SL	0.080 + 0.005*SL	0.082 + 0.005*SL
	t_{PHL}	0.106	0.094 + 0.006*SL	0.098 + 0.005*SL	0.103 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.037 + 0.004*SL	0.034 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.048	0.038 + 0.005*SL	0.038 + 0.005*SL	0.034 + 0.005*SL
	t_{PLH}	0.071	0.065 + 0.003*SL	0.068 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.085	0.077 + 0.004*SL	0.081 + 0.003*SL	0.091 + 0.002*SL
B to Y	t_R	0.044	0.035 + 0.004*SL	0.032 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.050	0.039 + 0.005*SL	0.042 + 0.005*SL	0.035 + 0.005*SL
	t_{PLH}	0.071	0.065 + 0.003*SL	0.068 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.090	0.082 + 0.004*SL	0.086 + 0.003*SL	0.096 + 0.002*SL
C to Y	t_R	0.047	0.037 + 0.005*SL	0.037 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.048	0.037 + 0.005*SL	0.040 + 0.005*SL	0.034 + 0.005*SL
	t_{PLH}	0.084	0.078 + 0.003*SL	0.081 + 0.003*SL	0.086 + 0.002*SL
	t_{PHL}	0.100	0.093 + 0.004*SL	0.097 + 0.003*SL	0.107 + 0.002*SL
D to Y	t_R	0.049	0.040 + 0.005*SL	0.038 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.049	0.038 + 0.006*SL	0.042 + 0.005*SL	0.035 + 0.005*SL
	t_{PLH}	0.084	0.078 + 0.003*SL	0.081 + 0.003*SL	0.086 + 0.002*SL
	t_{PHL}	0.105	0.097 + 0.004*SL	0.101 + 0.003*SL	0.112 + 0.002*SL
E to Y	t_R	0.048	0.037 + 0.005*SL	0.038 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.044	0.033 + 0.006*SL	0.036 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.076	0.070 + 0.003*SL	0.073 + 0.002*SL	0.076 + 0.002*SL
	t_{PHL}	0.090	0.083 + 0.004*SL	0.087 + 0.003*SL	0.097 + 0.002*SL
F to Y	t_R	0.048	0.037 + 0.005*SL	0.038 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.050	0.043 + 0.003*SL	0.038 + 0.005*SL	0.035 + 0.005*SL
	t_{PLH}	0.076	0.070 + 0.003*SL	0.073 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.093	0.086 + 0.004*SL	0.090 + 0.003*SL	0.100 + 0.002*SL
G to Y	t_R	0.054	0.045 + 0.005*SL	0.043 + 0.005*SL	0.033 + 0.005*SL
	t_F	0.045	0.033 + 0.006*SL	0.037 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.089	0.082 + 0.003*SL	0.085 + 0.003*SL	0.090 + 0.002*SL
	t_{PHL}	0.105	0.097 + 0.004*SL	0.101 + 0.003*SL	0.111 + 0.002*SL
H to Y	t_R	0.054	0.044 + 0.005*SL	0.044 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.046	0.035 + 0.005*SL	0.038 + 0.005*SL	0.033 + 0.005*SL
	t_{PLH}	0.089	0.083 + 0.003*SL	0.086 + 0.003*SL	0.092 + 0.002*SL
	t_{PHL}	0.110	0.102 + 0.004*SL	0.107 + 0.003*SL	0.117 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

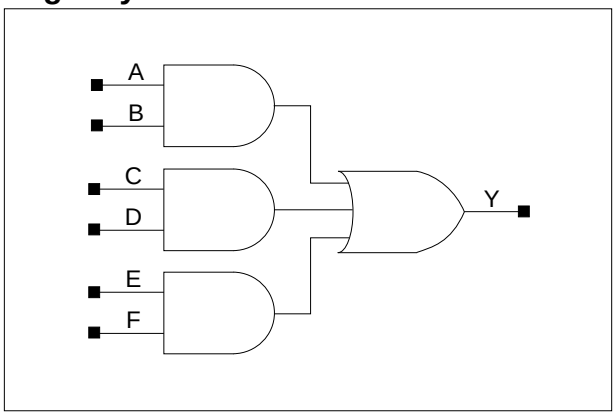
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg4d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.044 + 0.003*SL	0.047 + 0.002*SL	0.037 + 0.003*SL
	t_F	0.064	0.059 + 0.002*SL	0.059 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.088	0.085 + 0.002*SL	0.087 + 0.001*SL	0.096 + 0.001*SL
	t_{PHL}	0.108	0.104 + 0.002*SL	0.107 + 0.002*SL	0.123 + 0.001*SL
B to Y	t_R	0.052	0.047 + 0.002*SL	0.046 + 0.003*SL	0.038 + 0.003*SL
	t_F	0.066	0.061 + 0.003*SL	0.062 + 0.002*SL	0.054 + 0.002*SL
	t_{PLH}	0.089	0.085 + 0.002*SL	0.087 + 0.001*SL	0.097 + 0.001*SL
	t_{PHL}	0.113	0.109 + 0.002*SL	0.112 + 0.002*SL	0.128 + 0.001*SL
C to Y	t_R	0.057	0.053 + 0.002*SL	0.052 + 0.002*SL	0.039 + 0.003*SL
	t_F	0.063	0.058 + 0.003*SL	0.060 + 0.002*SL	0.052 + 0.002*SL
	t_{PLH}	0.102	0.098 + 0.002*SL	0.100 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.124	0.120 + 0.002*SL	0.122 + 0.002*SL	0.138 + 0.001*SL
D to Y	t_R	0.057	0.052 + 0.002*SL	0.052 + 0.002*SL	0.040 + 0.003*SL
	t_F	0.066	0.062 + 0.002*SL	0.062 + 0.002*SL	0.054 + 0.002*SL
	t_{PLH}	0.103	0.099 + 0.002*SL	0.102 + 0.001*SL	0.112 + 0.001*SL
	t_{PHL}	0.129	0.125 + 0.002*SL	0.128 + 0.002*SL	0.144 + 0.001*SL
E to Y	t_R	0.054	0.049 + 0.003*SL	0.049 + 0.003*SL	0.042 + 0.003*SL
	t_F	0.055	0.051 + 0.002*SL	0.051 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.093	0.089 + 0.002*SL	0.091 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.113	0.108 + 0.002*SL	0.111 + 0.002*SL	0.128 + 0.001*SL
F to Y	t_R	0.055	0.050 + 0.002*SL	0.050 + 0.003*SL	0.042 + 0.003*SL
	t_F	0.057	0.053 + 0.002*SL	0.052 + 0.002*SL	0.049 + 0.002*SL
	t_{PLH}	0.093	0.089 + 0.002*SL	0.091 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.117	0.113 + 0.002*SL	0.116 + 0.002*SL	0.133 + 0.001*SL
G to Y	t_R	0.059	0.054 + 0.002*SL	0.054 + 0.003*SL	0.046 + 0.003*SL
	t_F	0.054	0.051 + 0.002*SL	0.048 + 0.002*SL	0.049 + 0.002*SL
	t_{PLH}	0.106	0.102 + 0.002*SL	0.104 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.129	0.125 + 0.002*SL	0.127 + 0.002*SL	0.144 + 0.001*SL
H to Y	t_R	0.061	0.056 + 0.002*SL	0.055 + 0.002*SL	0.046 + 0.003*SL
	t_F	0.057	0.052 + 0.002*SL	0.051 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.107	0.103 + 0.002*SL	0.105 + 0.001*SL	0.115 + 0.001*SL
	t_{PHL}	0.133	0.129 + 0.002*SL	0.132 + 0.002*SL	0.149 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	1
x	x	1	1	x	x	1
x	x	x	x	1	1	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
scg5						*scg5*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.1	3.67
scg5d2						*scg5d2*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.0	4.00
scg5d4						*scg5d4*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.1	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.032 + 0.009*SL	0.030 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.055	0.038 + 0.009*SL	0.041 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.076	0.064 + 0.006*SL	0.070 + 0.005*SL	0.073 + 0.004*SL
	t_{PHL}	0.097	0.082 + 0.007*SL	0.091 + 0.005*SL	0.106 + 0.004*SL
B to Y	t_R	0.050	0.033 + 0.009*SL	0.028 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.057	0.038 + 0.010*SL	0.046 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.076	0.064 + 0.006*SL	0.069 + 0.005*SL	0.073 + 0.004*SL
	t_{PHL}	0.102	0.087 + 0.007*SL	0.096 + 0.005*SL	0.112 + 0.004*SL
C to Y	t_R	0.054	0.037 + 0.009*SL	0.033 + 0.010*SL	0.024 + 0.010*SL
	t_F	0.058	0.042 + 0.008*SL	0.043 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.094	0.081 + 0.006*SL	0.088 + 0.005*SL	0.092 + 0.004*SL
	t_{PHL}	0.128	0.113 + 0.007*SL	0.122 + 0.005*SL	0.137 + 0.004*SL
D to Y	t_R	0.056	0.037 + 0.010*SL	0.038 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.060	0.042 + 0.009*SL	0.047 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.093	0.080 + 0.006*SL	0.087 + 0.005*SL	0.092 + 0.004*SL
	t_{PHL}	0.133	0.118 + 0.007*SL	0.128 + 0.005*SL	0.143 + 0.004*SL
E to Y	t_R	0.059	0.041 + 0.009*SL	0.040 + 0.010*SL	0.029 + 0.010*SL
	t_F	0.057	0.037 + 0.010*SL	0.046 + 0.007*SL	0.040 + 0.008*SL
	t_{PLH}	0.105	0.091 + 0.007*SL	0.098 + 0.005*SL	0.105 + 0.005*SL
	t_{PHL}	0.140	0.125 + 0.007*SL	0.135 + 0.005*SL	0.150 + 0.004*SL
F to Y	t_R	0.058	0.039 + 0.009*SL	0.038 + 0.010*SL	0.029 + 0.010*SL
	t_F	0.059	0.040 + 0.009*SL	0.047 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.106	0.092 + 0.007*SL	0.099 + 0.005*SL	0.106 + 0.005*SL
	t_{PHL}	0.146	0.131 + 0.008*SL	0.141 + 0.005*SL	0.157 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.035 + 0.004*SL	0.033 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.055	0.044 + 0.005*SL	0.050 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.078	0.071 + 0.004*SL	0.076 + 0.003*SL	0.084 + 0.002*SL
	t_{PHL}	0.103	0.094 + 0.005*SL	0.101 + 0.003*SL	0.123 + 0.002*SL
B to Y	t_R	0.044	0.034 + 0.005*SL	0.036 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.058	0.047 + 0.005*SL	0.053 + 0.004*SL	0.053 + 0.004*SL
	t_{PLH}	0.078	0.071 + 0.004*SL	0.076 + 0.003*SL	0.084 + 0.002*SL
	t_{PHL}	0.108	0.099 + 0.005*SL	0.106 + 0.003*SL	0.129 + 0.002*SL
C to Y	t_R	0.047	0.037 + 0.005*SL	0.038 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.055	0.046 + 0.005*SL	0.049 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.095	0.088 + 0.004*SL	0.093 + 0.003*SL	0.103 + 0.002*SL
	t_{PHL}	0.134	0.125 + 0.004*SL	0.132 + 0.003*SL	0.154 + 0.002*SL
D to Y	t_R	0.048	0.037 + 0.005*SL	0.040 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.058	0.048 + 0.005*SL	0.054 + 0.004*SL	0.053 + 0.004*SL
	t_{PLH}	0.096	0.088 + 0.004*SL	0.094 + 0.003*SL	0.103 + 0.002*SL
	t_{PHL}	0.139	0.130 + 0.005*SL	0.137 + 0.003*SL	0.160 + 0.002*SL
E to Y	t_R	0.053	0.043 + 0.005*SL	0.045 + 0.005*SL	0.033 + 0.005*SL
	t_F	0.057	0.048 + 0.005*SL	0.050 + 0.004*SL	0.053 + 0.004*SL
	t_{PLH}	0.106	0.098 + 0.004*SL	0.104 + 0.003*SL	0.116 + 0.002*SL
	t_{PHL}	0.147	0.138 + 0.005*SL	0.145 + 0.003*SL	0.167 + 0.002*SL
F to Y	t_R	0.053	0.044 + 0.004*SL	0.042 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.059	0.050 + 0.004*SL	0.051 + 0.004*SL	0.054 + 0.004*SL
	t_{PLH}	0.108	0.100 + 0.004*SL	0.105 + 0.003*SL	0.117 + 0.002*SL
	t_{PHL}	0.153	0.144 + 0.005*SL	0.151 + 0.003*SL	0.174 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Switching Characteristics

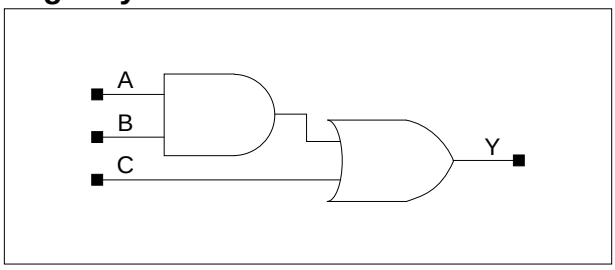
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg5d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.045 + 0.003*SL	0.048 + 0.002*SL	0.039 + 0.002*SL
	t_F	0.074	0.070 + 0.002*SL	0.070 + 0.002*SL	0.075 + 0.002*SL
	t_{PLH}	0.095	0.091 + 0.002*SL	0.094 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.135	0.130 + 0.003*SL	0.134 + 0.002*SL	0.163 + 0.001*SL
B to Y	t_R	0.053	0.048 + 0.002*SL	0.048 + 0.002*SL	0.038 + 0.002*SL
	t_F	0.079	0.075 + 0.002*SL	0.075 + 0.002*SL	0.078 + 0.002*SL
	t_{PLH}	0.095	0.091 + 0.002*SL	0.094 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.140	0.134 + 0.003*SL	0.139 + 0.002*SL	0.169 + 0.001*SL
C to Y	t_R	0.057	0.053 + 0.002*SL	0.052 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.075	0.070 + 0.003*SL	0.073 + 0.002*SL	0.076 + 0.002*SL
	t_{PLH}	0.112	0.107 + 0.002*SL	0.111 + 0.001*SL	0.128 + 0.001*SL
	t_{PHL}	0.166	0.160 + 0.003*SL	0.165 + 0.002*SL	0.194 + 0.001*SL
D to Y	t_R	0.057	0.053 + 0.002*SL	0.050 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.079	0.075 + 0.002*SL	0.075 + 0.002*SL	0.078 + 0.002*SL
	t_{PLH}	0.113	0.109 + 0.002*SL	0.112 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.171	0.166 + 0.003*SL	0.170 + 0.002*SL	0.200 + 0.001*SL
E to Y	t_R	0.062	0.057 + 0.002*SL	0.058 + 0.002*SL	0.048 + 0.002*SL
	t_F	0.076	0.074 + 0.001*SL	0.070 + 0.002*SL	0.076 + 0.002*SL
	t_{PLH}	0.124	0.120 + 0.002*SL	0.123 + 0.001*SL	0.142 + 0.001*SL
	t_{PHL}	0.179	0.174 + 0.003*SL	0.178 + 0.002*SL	0.207 + 0.001*SL
F to Y	t_R	0.062	0.058 + 0.002*SL	0.056 + 0.002*SL	0.046 + 0.002*SL
	t_F	0.077	0.073 + 0.002*SL	0.073 + 0.002*SL	0.078 + 0.002*SL
	t_{PLH}	0.126	0.121 + 0.002*SL	0.125 + 0.001*SL	0.143 + 0.001*SL
	t_{PHL}	0.185	0.180 + 0.003*SL	0.184 + 0.002*SL	0.214 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	1
x	x	1	1
Other States			0

Cell Data

Input Load (SL)								
scg6			*scg6d2*			*scg6d4*		
A	B	C	A	B	C	A	B	C
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Gate Count		
scg6	*scg6d2*	*scg6d4*
2.00	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.028 + 0.009*SL	0.024 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.042	0.026 + 0.008*SL	0.028 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.067	0.056 + 0.005*SL	0.059 + 0.005*SL	0.060 + 0.004*SL
	t_{PHL}	0.070	0.059 + 0.006*SL	0.064 + 0.004*SL	0.070 + 0.004*SL
B to Y	t_R	0.048	0.035 + 0.007*SL	0.021 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.042	0.025 + 0.008*SL	0.027 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.066	0.055 + 0.005*SL	0.059 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.074	0.062 + 0.006*SL	0.068 + 0.004*SL	0.074 + 0.004*SL
C to Y	t_R	0.047	0.032 + 0.008*SL	0.023 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.043	0.026 + 0.009*SL	0.030 + 0.008*SL	0.022 + 0.008*SL
	t_{PLH}	0.068	0.057 + 0.005*SL	0.060 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.084	0.072 + 0.006*SL	0.078 + 0.004*SL	0.084 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

2-AND into 2-OR with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg6d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.037	0.028 + 0.005*SL	0.031 + 0.004*SL	0.026 + 0.004*SL
	t_{PLH}	0.070	0.063 + 0.003*SL	0.067 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.074	0.067 + 0.004*SL	0.072 + 0.002*SL	0.084 + 0.002*SL
B to Y	t_R	0.038	0.030 + 0.004*SL	0.028 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.039	0.030 + 0.004*SL	0.032 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.070	0.063 + 0.003*SL	0.067 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.078	0.071 + 0.004*SL	0.076 + 0.002*SL	0.088 + 0.002*SL
C to Y	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.038	0.028 + 0.005*SL	0.032 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.069	0.063 + 0.003*SL	0.067 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.089	0.082 + 0.004*SL	0.087 + 0.002*SL	0.099 + 0.002*SL

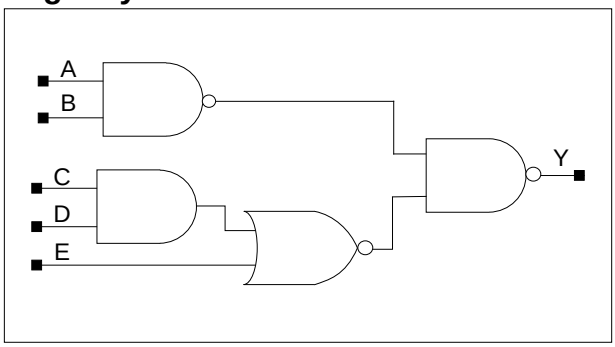
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg6d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.048	0.043 + 0.002*SL	0.042 + 0.002*SL	0.033 + 0.003*SL
	t_F	0.049	0.045 + 0.002*SL	0.045 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.086	0.082 + 0.002*SL	0.085 + 0.001*SL	0.098 + 0.001*SL
	t_{PHL}	0.094	0.090 + 0.002*SL	0.093 + 0.001*SL	0.112 + 0.001*SL
B to Y	t_R	0.048	0.042 + 0.003*SL	0.044 + 0.002*SL	0.033 + 0.003*SL
	t_F	0.050	0.046 + 0.002*SL	0.047 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.087	0.083 + 0.002*SL	0.085 + 0.001*SL	0.098 + 0.001*SL
	t_{PHL}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.116 + 0.001*SL
C to Y	t_R	0.041	0.036 + 0.003*SL	0.037 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.050	0.045 + 0.002*SL	0.047 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.080	0.076 + 0.002*SL	0.079 + 0.001*SL	0.087 + 0.001*SL
	t_{PHL}	0.109	0.105 + 0.002*SL	0.108 + 0.001*SL	0.128 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	1	1
Other States					0

Cell Data

Input Load (SL)														
scg7					*scg7d2*					*scg7d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.2	1.1	1.0	1.0	1.0	1.1	1.2	1.0	1.0	1.0	1.1	1.2	1.0	1.0	1.0

Gate Count		
scg7	*scg7d2*	*scg7d4*
3.33	4.00	5.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.047	0.027 + 0.010*SL	0.025 + 0.010*SL	0.018 + 0.011*SL
	t_F	0.045	0.026 + 0.010*SL	0.026 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.056	0.046 + 0.005*SL	0.047 + 0.005*SL	0.048 + 0.005*SL
	t_{PHL}	0.060	0.049 + 0.005*SL	0.051 + 0.005*SL	0.052 + 0.005*SL
B to Y	t_R	0.047	0.027 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.011*SL
	t_F	0.045	0.026 + 0.009*SL	0.026 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.056	0.046 + 0.005*SL	0.048 + 0.005*SL	0.048 + 0.005*SL
	t_{PHL}	0.063	0.052 + 0.005*SL	0.055 + 0.005*SL	0.056 + 0.005*SL
C to Y	t_R	0.060	0.046 + 0.007*SL	0.033 + 0.010*SL	0.027 + 0.011*SL
	t_F	0.046	0.027 + 0.010*SL	0.028 + 0.010*SL	0.023 + 0.010*SL
	t_{PLH}	0.074	0.064 + 0.005*SL	0.066 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.076	0.064 + 0.006*SL	0.068 + 0.005*SL	0.071 + 0.005*SL
D to Y	t_R	0.055	0.035 + 0.010*SL	0.033 + 0.010*SL	0.026 + 0.011*SL
	t_F	0.048	0.029 + 0.010*SL	0.030 + 0.009*SL	0.023 + 0.010*SL
	t_{PLH}	0.074	0.063 + 0.005*SL	0.066 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.080	0.068 + 0.006*SL	0.072 + 0.005*SL	0.076 + 0.005*SL
E to Y	t_R	0.054	0.035 + 0.009*SL	0.030 + 0.011*SL	0.025 + 0.011*SL
	t_F	0.047	0.026 + 0.010*SL	0.029 + 0.010*SL	0.023 + 0.010*SL
	t_{PLH}	0.075	0.064 + 0.005*SL	0.066 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.090	0.078 + 0.006*SL	0.082 + 0.005*SL	0.086 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg7d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.029 + 0.005*SL	0.030 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.023 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.058 + 0.002*SL
	t_{PHL}	0.062	0.055 + 0.003*SL	0.058 + 0.003*SL	0.061 + 0.002*SL
B to Y	t_R	0.040	0.031 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.022 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.058 + 0.002*SL
	t_{PHL}	0.065	0.059 + 0.003*SL	0.061 + 0.003*SL	0.064 + 0.002*SL
C to Y	t_R	0.050	0.040 + 0.005*SL	0.040 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.043	0.032 + 0.005*SL	0.034 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.081	0.075 + 0.003*SL	0.078 + 0.002*SL	0.082 + 0.002*SL
	t_{PHL}	0.084	0.077 + 0.004*SL	0.080 + 0.003*SL	0.088 + 0.002*SL
D to Y	t_R	0.050	0.042 + 0.004*SL	0.038 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.044	0.033 + 0.005*SL	0.035 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.081	0.075 + 0.003*SL	0.078 + 0.002*SL	0.082 + 0.002*SL
	t_{PHL}	0.087	0.080 + 0.004*SL	0.084 + 0.003*SL	0.092 + 0.002*SL
E to Y	t_R	0.047	0.039 + 0.004*SL	0.036 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.036 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.079	0.073 + 0.003*SL	0.075 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.097	0.090 + 0.004*SL	0.094 + 0.003*SL	0.102 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg7d4

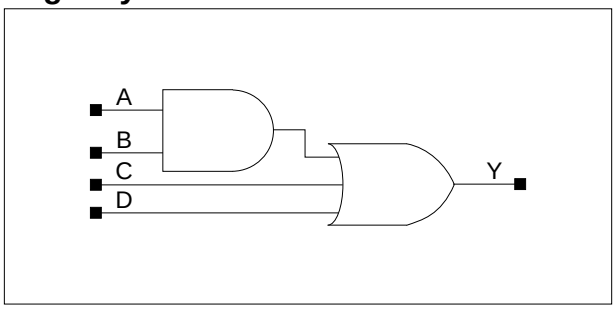
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.038 + 0.003*SL	0.039 + 0.003*SL	0.029 + 0.003*SL
	t_F	0.041	0.038 + 0.001*SL	0.034 + 0.002*SL	0.029 + 0.002*SL
	t_{PLH}	0.073	0.069 + 0.002*SL	0.071 + 0.001*SL	0.078 + 0.001*SL
	t_{PHL}	0.073	0.069 + 0.002*SL	0.072 + 0.001*SL	0.079 + 0.001*SL
B to Y	t_R	0.044	0.039 + 0.003*SL	0.039 + 0.003*SL	0.030 + 0.003*SL
	t_F	0.040	0.036 + 0.002*SL	0.035 + 0.002*SL	0.031 + 0.002*SL
	t_{PLH}	0.072	0.068 + 0.002*SL	0.071 + 0.001*SL	0.077 + 0.001*SL
	t_{PHL}	0.076	0.073 + 0.002*SL	0.075 + 0.001*SL	0.082 + 0.001*SL
C to Y	t_R	0.059	0.054 + 0.003*SL	0.056 + 0.002*SL	0.045 + 0.003*SL
	t_F	0.054	0.050 + 0.002*SL	0.049 + 0.002*SL	0.042 + 0.002*SL
	t_{PLH}	0.102	0.099 + 0.002*SL	0.101 + 0.001*SL	0.111 + 0.001*SL
	t_{PHL}	0.106	0.102 + 0.002*SL	0.105 + 0.001*SL	0.119 + 0.001*SL
D to Y	t_R	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.046 + 0.003*SL
	t_F	0.056	0.052 + 0.002*SL	0.050 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.103	0.099 + 0.002*SL	0.101 + 0.001*SL	0.111 + 0.001*SL
	t_{PHL}	0.110	0.105 + 0.002*SL	0.108 + 0.001*SL	0.123 + 0.001*SL
E to Y	t_R	0.052	0.046 + 0.003*SL	0.047 + 0.002*SL	0.035 + 0.003*SL
	t_F	0.054	0.049 + 0.003*SL	0.050 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.093	0.089 + 0.002*SL	0.091 + 0.001*SL	0.097 + 0.001*SL
	t_{PHL}	0.120	0.116 + 0.002*SL	0.119 + 0.001*SL	0.134 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg8/scg8d2

2-AND into 3-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	x	1
x	x	x	1	1
	Other States			0

Cell Data

Input Load (SL)								Gate Count	
scg8				*scg8d2*				*scg8*	*scg8d2*
A	B	C	D	A	B	C	D		
1.0	1.0	0.9	1.0	1.0	1.0	0.9	1.0	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.048	0.034 + 0.007*SL	0.023 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.050	0.031 + 0.009*SL	0.038 + 0.008*SL	0.036 + 0.008*SL
	t_{PLH}	0.069	0.058 + 0.006*SL	0.062 + 0.005*SL	0.064 + 0.004*SL
	t_{PHL}	0.086	0.073 + 0.007*SL	0.081 + 0.005*SL	0.093 + 0.004*SL
B to Y	t_R	0.044	0.024 + 0.010*SL	0.025 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.052	0.034 + 0.009*SL	0.040 + 0.008*SL	0.035 + 0.008*SL
	t_{PLH}	0.069	0.058 + 0.006*SL	0.062 + 0.005*SL	0.064 + 0.004*SL
	t_{PHL}	0.092	0.078 + 0.007*SL	0.086 + 0.005*SL	0.099 + 0.004*SL
C to Y	t_R	0.046	0.028 + 0.009*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.053	0.034 + 0.009*SL	0.042 + 0.008*SL	0.037 + 0.008*SL
	t_{PLH}	0.079	0.068 + 0.006*SL	0.071 + 0.005*SL	0.073 + 0.004*SL
	t_{PHL}	0.113	0.099 + 0.007*SL	0.108 + 0.005*SL	0.121 + 0.004*SL
D to Y	t_R	0.052	0.036 + 0.008*SL	0.028 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.053	0.036 + 0.009*SL	0.040 + 0.008*SL	0.036 + 0.008*SL
	t_{PLH}	0.083	0.072 + 0.006*SL	0.076 + 0.005*SL	0.078 + 0.004*SL
	t_{PHL}	0.118	0.104 + 0.007*SL	0.112 + 0.005*SL	0.126 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg8d2

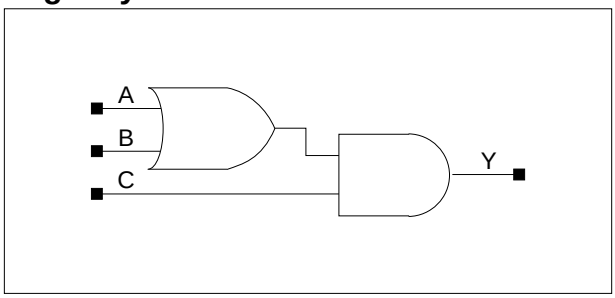
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.027 + 0.006*SL	0.031 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.051	0.042 + 0.004*SL	0.044 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.072	0.066 + 0.003*SL	0.070 + 0.002*SL	0.076 + 0.002*SL
	t_{PHL}	0.094	0.086 + 0.004*SL	0.092 + 0.003*SL	0.111 + 0.002*SL
B to Y	t_R	0.042	0.034 + 0.004*SL	0.030 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.052	0.042 + 0.005*SL	0.046 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.072	0.065 + 0.004*SL	0.070 + 0.002*SL	0.076 + 0.002*SL
	t_{PHL}	0.099	0.091 + 0.004*SL	0.097 + 0.003*SL	0.117 + 0.002*SL
C to Y	t_R	0.043	0.034 + 0.004*SL	0.033 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.054	0.045 + 0.005*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.080	0.073 + 0.003*SL	0.078 + 0.002*SL	0.082 + 0.002*SL
	t_{PHL}	0.121	0.112 + 0.004*SL	0.119 + 0.003*SL	0.139 + 0.002*SL
D to Y	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.054	0.046 + 0.004*SL	0.046 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.085	0.078 + 0.004*SL	0.083 + 0.002*SL	0.088 + 0.002*SL
	t_{PHL}	0.126	0.117 + 0.004*SL	0.124 + 0.003*SL	0.144 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg9/scg9d2/scg9d4

2-OR into 2-AND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	0
x	x	0	0
Other States			1

Cell Data

Input Load (SL)								
scg9			*scg9d2*			*scg9d4*		
A	B	C	A	B	C	A	B	C
1.1	1.1	1.1	1.0	1.1	1.1	1.1	1.1	1.1

Gate Count		
scg9	*scg9d2*	*scg9d4*
2.00	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg9

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.042	0.023 + 0.010*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.041	0.026 + 0.008*SL	0.026 + 0.008*SL	0.020 + 0.008*SL
	t_{PLH}	0.059	0.049 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.004*SL
	t_{PHL}	0.074	0.062 + 0.006*SL	0.068 + 0.004*SL	0.073 + 0.004*SL
B to Y	t_R	0.043	0.024 + 0.009*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.041	0.024 + 0.009*SL	0.027 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.066	0.055 + 0.005*SL	0.058 + 0.005*SL	0.060 + 0.004*SL
	t_{PHL}	0.077	0.065 + 0.006*SL	0.071 + 0.004*SL	0.076 + 0.004*SL
C to Y	t_R	0.047	0.032 + 0.008*SL	0.022 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.038	0.023 + 0.007*SL	0.022 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.068	0.057 + 0.005*SL	0.061 + 0.005*SL	0.063 + 0.004*SL
	t_{PHL}	0.064	0.053 + 0.006*SL	0.058 + 0.004*SL	0.062 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg9d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.022 + 0.008*SL	0.034 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.037	0.027 + 0.005*SL	0.032 + 0.004*SL	0.027 + 0.004*SL
	t_{PLH}	0.061	0.055 + 0.003*SL	0.058 + 0.002*SL	0.062 + 0.002*SL
	t_{PHL}	0.078	0.070 + 0.004*SL	0.075 + 0.002*SL	0.087 + 0.002*SL
B to Y	t_R	0.038	0.031 + 0.004*SL	0.027 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.039	0.031 + 0.004*SL	0.033 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.067	0.060 + 0.003*SL	0.064 + 0.002*SL	0.068 + 0.002*SL
	t_{PHL}	0.081	0.074 + 0.004*SL	0.079 + 0.002*SL	0.090 + 0.002*SL
C to Y	t_R	0.036	0.026 + 0.005*SL	0.027 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.026 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.070	0.063 + 0.003*SL	0.067 + 0.002*SL	0.071 + 0.002*SL
	t_{PHL}	0.064	0.057 + 0.003*SL	0.062 + 0.002*SL	0.069 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg9d4

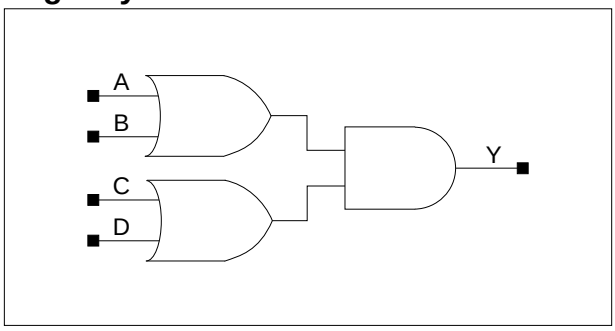
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.034 + 0.003*SL	0.036 + 0.002*SL	0.025 + 0.003*SL
	t_F	0.049	0.044 + 0.002*SL	0.046 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.074	0.070 + 0.002*SL	0.073 + 0.001*SL	0.082 + 0.001*SL
	t_{PHL}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.116 + 0.001*SL
B to Y	t_R	0.043	0.038 + 0.003*SL	0.039 + 0.002*SL	0.028 + 0.003*SL
	t_F	0.049	0.044 + 0.002*SL	0.046 + 0.002*SL	0.042 + 0.002*SL
	t_{PLH}	0.079	0.075 + 0.002*SL	0.078 + 0.001*SL	0.088 + 0.001*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.120 + 0.001*SL
C to Y	t_R	0.042	0.038 + 0.002*SL	0.037 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.035	0.030 + 0.003*SL	0.033 + 0.002*SL	0.028 + 0.002*SL
	t_{PLH}	0.082	0.078 + 0.002*SL	0.081 + 0.001*SL	0.092 + 0.001*SL
	t_{PHL}	0.073	0.069 + 0.002*SL	0.072 + 0.001*SL	0.085 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg10/scg10d2/scg10d4

Two 2-ORs into 2-AND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)											
scg10				*scg10d2*				*scg10d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	1.1	1.1	1.0	1.1	1.0	1.1	1.0	1.1	1.0	1.1

Gate Count		
scg10	*scg10d2*	*scg10d4*
3.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg10

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.044	0.026 + 0.009*SL	0.021 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.048	0.030 + 0.009*SL	0.036 + 0.007*SL	0.029 + 0.008*SL
	t_{PLH}	0.067	0.056 + 0.005*SL	0.060 + 0.005*SL	0.061 + 0.004*SL
	t_{PHL}	0.080	0.067 + 0.007*SL	0.075 + 0.005*SL	0.085 + 0.004*SL
B to Y	t_R	0.046	0.028 + 0.009*SL	0.025 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.050	0.033 + 0.008*SL	0.037 + 0.007*SL	0.030 + 0.008*SL
	t_{PLH}	0.073	0.062 + 0.006*SL	0.066 + 0.005*SL	0.068 + 0.004*SL
	t_{PHL}	0.083	0.070 + 0.007*SL	0.079 + 0.005*SL	0.089 + 0.004*SL
C to Y	t_R	0.044	0.025 + 0.009*SL	0.024 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.050	0.034 + 0.008*SL	0.036 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.071	0.060 + 0.005*SL	0.064 + 0.005*SL	0.066 + 0.004*SL
	t_{PHL}	0.092	0.078 + 0.007*SL	0.087 + 0.005*SL	0.098 + 0.004*SL
D to Y	t_R	0.047	0.030 + 0.008*SL	0.025 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.051	0.034 + 0.009*SL	0.039 + 0.007*SL	0.032 + 0.008*SL
	t_{PLH}	0.078	0.066 + 0.006*SL	0.071 + 0.005*SL	0.073 + 0.004*SL
	t_{PHL}	0.096	0.082 + 0.007*SL	0.091 + 0.005*SL	0.102 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg10d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.025 + 0.006*SL	0.030 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.044	0.035 + 0.004*SL	0.036 + 0.004*SL	0.036 + 0.004*SL
	t_{PLH}	0.072	0.065 + 0.003*SL	0.069 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.083	0.074 + 0.004*SL	0.081 + 0.003*SL	0.097 + 0.002*SL
B to Y	t_R	0.041	0.031 + 0.005*SL	0.032 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.045	0.035 + 0.005*SL	0.040 + 0.004*SL	0.037 + 0.004*SL
	t_{PLH}	0.078	0.071 + 0.004*SL	0.075 + 0.002*SL	0.082 + 0.002*SL
	t_{PHL}	0.087	0.079 + 0.004*SL	0.085 + 0.003*SL	0.101 + 0.002*SL
C to Y	t_R	0.040	0.029 + 0.005*SL	0.031 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.040 + 0.004*SL	0.039 + 0.004*SL
	t_{PLH}	0.076	0.069 + 0.003*SL	0.073 + 0.002*SL	0.079 + 0.002*SL
	t_{PHL}	0.092	0.083 + 0.004*SL	0.090 + 0.003*SL	0.108 + 0.002*SL
D to Y	t_R	0.042	0.032 + 0.005*SL	0.034 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.042 + 0.004*SL	0.040 + 0.004*SL
	t_{PLH}	0.083	0.076 + 0.004*SL	0.080 + 0.002*SL	0.086 + 0.002*SL
	t_{PHL}	0.097	0.088 + 0.004*SL	0.095 + 0.003*SL	0.112 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg10d4

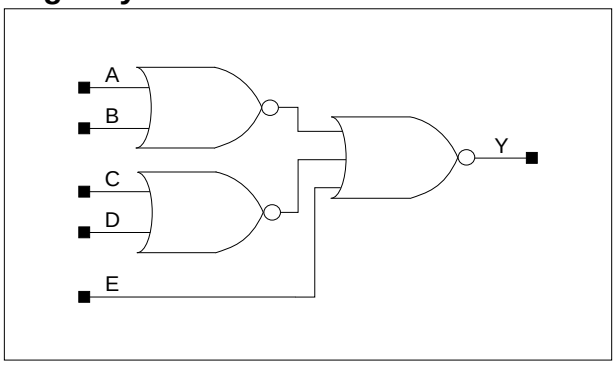
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.040 + 0.003*SL	0.041 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.055	0.052 + 0.002*SL	0.051 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.084	0.080 + 0.002*SL	0.083 + 0.001*SL	0.095 + 0.001*SL
	t_{PHL}	0.101	0.096 + 0.002*SL	0.100 + 0.001*SL	0.123 + 0.001*SL
B to Y	t_R	0.047	0.041 + 0.003*SL	0.043 + 0.002*SL	0.032 + 0.003*SL
	t_F	0.056	0.051 + 0.003*SL	0.054 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.091	0.087 + 0.002*SL	0.090 + 0.001*SL	0.103 + 0.001*SL
	t_{PHL}	0.106	0.101 + 0.002*SL	0.105 + 0.001*SL	0.129 + 0.001*SL
C to Y	t_R	0.044	0.037 + 0.004*SL	0.042 + 0.002*SL	0.029 + 0.003*SL
	t_F	0.060	0.055 + 0.003*SL	0.058 + 0.002*SL	0.056 + 0.002*SL
	t_{PLH}	0.090	0.086 + 0.002*SL	0.088 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.111	0.105 + 0.003*SL	0.110 + 0.001*SL	0.135 + 0.001*SL
D to Y	t_R	0.046	0.040 + 0.003*SL	0.043 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.061	0.057 + 0.002*SL	0.058 + 0.002*SL	0.055 + 0.002*SL
	t_{PLH}	0.095	0.091 + 0.002*SL	0.094 + 0.001*SL	0.107 + 0.001*SL
	t_{PHL}	0.115	0.110 + 0.003*SL	0.114 + 0.001*SL	0.139 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg11/scg11d2

Two 2-NORs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	0
x	x	0	0	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
scg11					*scg11d2*					*scg11*	*scg11d2*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	1.1	1.1	1.0	1.1	1.1	1.0	1.1	2.2	3.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.048 + 0.030*SL	0.046 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.053	0.027 + 0.013*SL	0.028 + 0.013*SL	0.020 + 0.013*SL
	t_{PLH}	0.076	0.048 + 0.014*SL	0.049 + 0.014*SL	0.050 + 0.014*SL
	t_{PHL}	0.082	0.066 + 0.008*SL	0.071 + 0.007*SL	0.074 + 0.007*SL
B to Y	t_R	0.109	0.050 + 0.030*SL	0.046 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.053	0.029 + 0.012*SL	0.028 + 0.013*SL	0.020 + 0.013*SL
	t_{PLH}	0.081	0.053 + 0.014*SL	0.054 + 0.014*SL	0.055 + 0.014*SL
	t_{PHL}	0.086	0.070 + 0.008*SL	0.075 + 0.007*SL	0.078 + 0.007*SL
C to Y	t_R	0.108	0.048 + 0.030*SL	0.047 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.061	0.036 + 0.012*SL	0.035 + 0.013*SL	0.028 + 0.013*SL
	t_{PLH}	0.088	0.060 + 0.014*SL	0.061 + 0.014*SL	0.061 + 0.014*SL
	t_{PHL}	0.085	0.070 + 0.008*SL	0.074 + 0.007*SL	0.076 + 0.007*SL
D to Y	t_R	0.108	0.048 + 0.030*SL	0.047 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.061	0.036 + 0.012*SL	0.036 + 0.013*SL	0.029 + 0.013*SL
	t_{PLH}	0.093	0.065 + 0.014*SL	0.066 + 0.014*SL	0.066 + 0.014*SL
	t_{PHL}	0.089	0.074 + 0.008*SL	0.078 + 0.007*SL	0.080 + 0.007*SL
E to Y	t_R	0.111	0.052 + 0.029*SL	0.048 + 0.030*SL	0.046 + 0.031*SL
	t_F	0.070	0.045 + 0.012*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_{PLH}	0.077	0.049 + 0.014*SL	0.050 + 0.014*SL	0.050 + 0.014*SL
	t_{PHL}	0.051	0.037 + 0.007*SL	0.039 + 0.007*SL	0.041 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg11d2

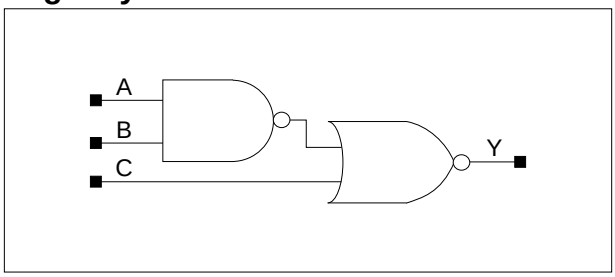
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.045 + 0.014*SL	0.042 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.043	0.029 + 0.007*SL	0.033 + 0.006*SL	0.025 + 0.006*SL
	t_{PLH}	0.064	0.050 + 0.007*SL	0.051 + 0.007*SL	0.052 + 0.007*SL
	t_{PHL}	0.083	0.073 + 0.005*SL	0.079 + 0.004*SL	0.087 + 0.003*SL
B to Y	t_R	0.075	0.046 + 0.014*SL	0.042 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.044	0.031 + 0.007*SL	0.032 + 0.006*SL	0.024 + 0.006*SL
	t_{PLH}	0.069	0.055 + 0.007*SL	0.055 + 0.007*SL	0.056 + 0.007*SL
	t_{PHL}	0.087	0.077 + 0.005*SL	0.083 + 0.004*SL	0.090 + 0.003*SL
C to Y	t_R	0.075	0.045 + 0.015*SL	0.044 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.053	0.041 + 0.006*SL	0.041 + 0.006*SL	0.033 + 0.006*SL
	t_{PLH}	0.080	0.066 + 0.007*SL	0.067 + 0.007*SL	0.068 + 0.007*SL
	t_{PHL}	0.091	0.082 + 0.005*SL	0.086 + 0.003*SL	0.093 + 0.003*SL
D to Y	t_R	0.076	0.047 + 0.014*SL	0.044 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.053	0.041 + 0.006*SL	0.041 + 0.006*SL	0.033 + 0.006*SL
	t_{PLH}	0.084	0.070 + 0.007*SL	0.072 + 0.007*SL	0.073 + 0.007*SL
	t_{PHL}	0.095	0.086 + 0.005*SL	0.090 + 0.003*SL	0.097 + 0.003*SL
E to Y	t_R	0.078	0.049 + 0.014*SL	0.046 + 0.015*SL	0.041 + 0.015*SL
	t_F	0.057	0.043 + 0.007*SL	0.046 + 0.006*SL	0.031 + 0.006*SL
	t_{PLH}	0.062	0.048 + 0.007*SL	0.049 + 0.007*SL	0.050 + 0.007*SL
	t_{PHL}	0.043	0.035 + 0.004*SL	0.038 + 0.003*SL	0.041 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg12/scg12d2/scg12d4

2-NAND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	0	1
Other States			0

Cell Data

Input Load (SL)									Gate Count		
scg12			*scg12d2*			*scg12d4*			*scg12*	*scg12d2*	*scg12d4*
A	B	C	A	B	C	A	B	C			
0.9	0.9	1.1	0.9	0.9	2.3	0.9	1.0	4.5	2.00	2.67	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.035 + 0.020*SL	0.032 + 0.020*SL	0.030 + 0.020*SL
	t_F	0.038	0.023 + 0.008*SL	0.024 + 0.007*SL	0.020 + 0.008*SL
	t_{PLH}	0.062	0.044 + 0.009*SL	0.045 + 0.009*SL	0.045 + 0.009*SL
	t_{PHL}	0.073	0.063 + 0.005*SL	0.067 + 0.004*SL	0.070 + 0.004*SL
B to Y	t_R	0.075	0.036 + 0.019*SL	0.032 + 0.020*SL	0.030 + 0.020*SL
	t_F	0.042	0.026 + 0.008*SL	0.030 + 0.007*SL	0.020 + 0.008*SL
	t_{PLH}	0.064	0.045 + 0.009*SL	0.047 + 0.009*SL	0.047 + 0.009*SL
	t_{PHL}	0.080	0.069 + 0.005*SL	0.074 + 0.004*SL	0.078 + 0.004*SL
C to Y	t_R	0.080	0.043 + 0.018*SL	0.036 + 0.020*SL	0.030 + 0.020*SL
	t_F	0.050	0.040 + 0.005*SL	0.033 + 0.007*SL	0.023 + 0.007*SL
	t_{PLH}	0.054	0.035 + 0.010*SL	0.037 + 0.009*SL	0.037 + 0.009*SL
	t_{PHL}	0.033	0.023 + 0.005*SL	0.029 + 0.004*SL	0.030 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg12d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.054	0.035 + 0.010*SL	0.034 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.039	0.031 + 0.004*SL	0.033 + 0.004*SL	0.027 + 0.004*SL
	t_{PLH}	0.060	0.050 + 0.005*SL	0.051 + 0.005*SL	0.052 + 0.005*SL
	t_{PHL}	0.080	0.073 + 0.003*SL	0.077 + 0.002*SL	0.086 + 0.002*SL
B to Y	t_R	0.054	0.035 + 0.009*SL	0.032 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.041	0.032 + 0.004*SL	0.035 + 0.003*SL	0.028 + 0.004*SL
	t_{PLH}	0.060	0.051 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.005*SL
	t_{PHL}	0.086	0.079 + 0.003*SL	0.084 + 0.002*SL	0.094 + 0.002*SL
C to Y	t_R	0.059	0.041 + 0.009*SL	0.037 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.042	0.037 + 0.003*SL	0.035 + 0.003*SL	0.022 + 0.004*SL
	t_{PLH}	0.043	0.032 + 0.005*SL	0.036 + 0.005*SL	0.037 + 0.005*SL
	t_{PHL}	0.027	0.020 + 0.003*SL	0.025 + 0.002*SL	0.030 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg12d4

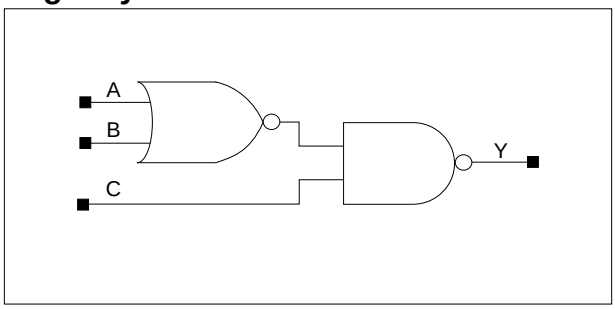
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.052	0.044 + 0.004*SL	0.040 + 0.005*SL	0.032 + 0.005*SL
	t_F	0.042	0.038 + 0.002*SL	0.039 + 0.002*SL	0.033 + 0.002*SL
	t_{PLH}	0.072	0.066 + 0.003*SL	0.068 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.085	0.081 + 0.002*SL	0.084 + 0.001*SL	0.098 + 0.001*SL
B to Y	t_R	0.052	0.042 + 0.005*SL	0.041 + 0.005*SL	0.032 + 0.005*SL
	t_F	0.043	0.040 + 0.002*SL	0.040 + 0.002*SL	0.036 + 0.002*SL
	t_{PLH}	0.072	0.066 + 0.003*SL	0.068 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.089	0.085 + 0.002*SL	0.089 + 0.001*SL	0.103 + 0.001*SL
C to Y	t_R	0.053	0.045 + 0.004*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.040	0.035 + 0.002*SL	0.038 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.039	0.033 + 0.003*SL	0.036 + 0.002*SL	0.040 + 0.002*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.023 + 0.001*SL	0.030 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg13/scg13d2/scg13d4

2-NOR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	1	0
Other States			1

Cell Data

Input Load (SL)								
scg13			*scg13d2*			*scg13d4*		
A	B	C	A	B	C	A	B	C
1.1	1.1	1.2	1.1	1.1	2.4	1.0	1.1	4.8
Gate Count								
scg13			*scg13d2*			*scg13d4*		
2.00			2.67			4.33		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.044	0.025 + 0.010*SL	0.021 + 0.011*SL	0.018 + 0.011*SL
	t_F	0.049	0.031 + 0.009*SL	0.030 + 0.009*SL	0.024 + 0.010*SL
	t_{PLH}	0.052	0.042 + 0.005*SL	0.044 + 0.005*SL	0.044 + 0.005*SL
	t_{PHL}	0.073	0.061 + 0.006*SL	0.065 + 0.005*SL	0.068 + 0.005*SL
B to Y	t_R	0.044	0.023 + 0.010*SL	0.021 + 0.011*SL	0.018 + 0.011*SL
	t_F	0.048	0.029 + 0.009*SL	0.028 + 0.010*SL	0.024 + 0.010*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.049 + 0.005*SL	0.049 + 0.005*SL
	t_{PHL}	0.077	0.065 + 0.006*SL	0.069 + 0.005*SL	0.072 + 0.005*SL
C to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.026 + 0.011*SL
	t_F	0.050	0.032 + 0.009*SL	0.030 + 0.009*SL	0.022 + 0.010*SL
	t_{PLH}	0.039	0.028 + 0.006*SL	0.032 + 0.005*SL	0.032 + 0.005*SL
	t_{PHL}	0.034	0.021 + 0.006*SL	0.026 + 0.005*SL	0.029 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg13d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.027 + 0.004*SL	0.023 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.036 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.054	0.049 + 0.003*SL	0.050 + 0.002*SL	0.052 + 0.002*SL
	t_{PHL}	0.079	0.072 + 0.004*SL	0.075 + 0.003*SL	0.082 + 0.002*SL
B to Y	t_R	0.037	0.026 + 0.005*SL	0.027 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.046	0.036 + 0.005*SL	0.038 + 0.005*SL	0.030 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.056 + 0.002*SL
	t_{PHL}	0.082	0.075 + 0.004*SL	0.079 + 0.003*SL	0.086 + 0.002*SL
C to Y	t_R	0.052	0.044 + 0.004*SL	0.040 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.040	0.030 + 0.005*SL	0.032 + 0.005*SL	0.024 + 0.005*SL
	t_{PLH}	0.033	0.026 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
	t_{PHL}	0.027	0.020 + 0.004*SL	0.024 + 0.003*SL	0.030 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg13d4

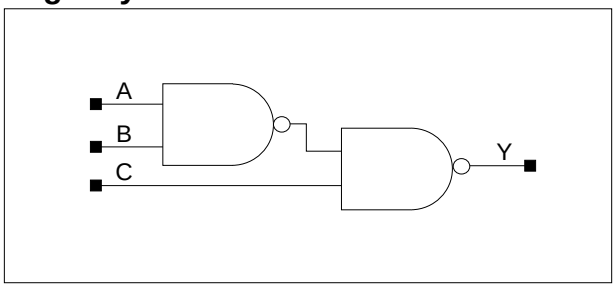
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.038 + 0.001*SL	0.033 + 0.003*SL	0.023 + 0.003*SL
	t_F	0.056	0.052 + 0.002*SL	0.052 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.066	0.062 + 0.002*SL	0.064 + 0.001*SL	0.067 + 0.001*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.099 + 0.001*SL	0.113 + 0.001*SL
B to Y	t_R	0.044	0.042 + 0.001*SL	0.035 + 0.003*SL	0.023 + 0.003*SL
	t_F	0.056	0.052 + 0.002*SL	0.052 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.069	0.065 + 0.002*SL	0.068 + 0.001*SL	0.071 + 0.001*SL
	t_{PHL}	0.105	0.101 + 0.002*SL	0.103 + 0.001*SL	0.117 + 0.001*SL
C to Y	t_R	0.048	0.044 + 0.002*SL	0.042 + 0.002*SL	0.027 + 0.003*SL
	t_F	0.036	0.031 + 0.003*SL	0.032 + 0.002*SL	0.031 + 0.002*SL
	t_{PLH}	0.029	0.026 + 0.002*SL	0.028 + 0.001*SL	0.032 + 0.001*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.023 + 0.001*SL	0.032 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg14/scg14d2/scg14d4

2-NAND into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	0	1	0
Other States			1

Cell Data

Input Load (SL)								
scg14			*scg14d2*			*scg14d4*		
A	B	C	A	B	C	A	B	C
1.1	1.2	1.2	1.1	1.2	2.5	1.1	1.1	4.8

Gate Count		
scg14	*scg14d2*	*scg14d4*
2.00	3.00	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg14

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.048	0.028 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.011*SL
	t_F	0.045	0.026 + 0.009*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.057	0.046 + 0.005*SL	0.048 + 0.005*SL	0.049 + 0.005*SL
	t_{PHL}	0.061	0.050 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.005*SL
B to Y	t_R	0.046	0.026 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.011*SL
	t_F	0.044	0.024 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.057	0.047 + 0.005*SL	0.049 + 0.005*SL	0.050 + 0.005*SL
	t_{PHL}	0.064	0.053 + 0.005*SL	0.056 + 0.005*SL	0.057 + 0.005*SL
C to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.026 + 0.011*SL
	t_F	0.050	0.032 + 0.009*SL	0.030 + 0.009*SL	0.021 + 0.010*SL
	t_{PLH}	0.040	0.029 + 0.006*SL	0.033 + 0.005*SL	0.033 + 0.005*SL
	t_{PHL}	0.034	0.022 + 0.006*SL	0.027 + 0.005*SL	0.029 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg14d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.037	0.028 + 0.004*SL	0.027 + 0.005*SL	0.021 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.057 + 0.002*SL
	t_{PHL}	0.061	0.055 + 0.003*SL	0.058 + 0.003*SL	0.060 + 0.002*SL
B to Y	t_R	0.040	0.031 + 0.005*SL	0.029 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.037	0.028 + 0.005*SL	0.028 + 0.005*SL	0.020 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.055 + 0.002*SL	0.058 + 0.002*SL
	t_{PHL}	0.065	0.059 + 0.003*SL	0.061 + 0.003*SL	0.064 + 0.002*SL
C to Y	t_R	0.052	0.044 + 0.004*SL	0.040 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.039	0.032 + 0.004*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_{PLH}	0.033	0.027 + 0.003*SL	0.031 + 0.002*SL	0.032 + 0.002*SL
	t_{PHL}	0.027	0.020 + 0.004*SL	0.024 + 0.003*SL	0.029 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg14d4

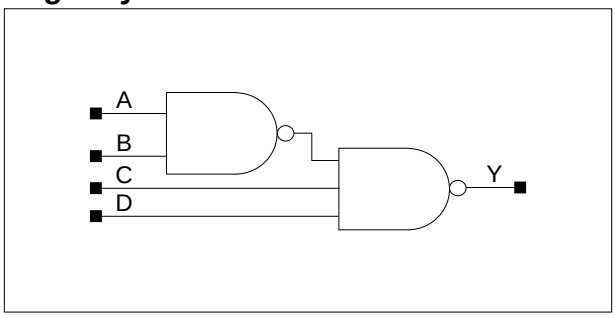
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.038 + 0.003*SL	0.038 + 0.003*SL	0.029 + 0.003*SL
	t_F	0.040	0.037 + 0.001*SL	0.033 + 0.002*SL	0.027 + 0.002*SL
	t_{PLH}	0.072	0.069 + 0.002*SL	0.071 + 0.001*SL	0.077 + 0.001*SL
	t_{PHL}	0.073	0.069 + 0.002*SL	0.071 + 0.001*SL	0.078 + 0.001*SL
B to Y	t_R	0.047	0.045 + 0.001*SL	0.039 + 0.003*SL	0.029 + 0.003*SL
	t_F	0.040	0.035 + 0.003*SL	0.036 + 0.002*SL	0.028 + 0.002*SL
	t_{PLH}	0.072	0.068 + 0.002*SL	0.070 + 0.001*SL	0.077 + 0.001*SL
	t_{PHL}	0.076	0.073 + 0.002*SL	0.075 + 0.001*SL	0.081 + 0.001*SL
C to Y	t_R	0.048	0.044 + 0.002*SL	0.043 + 0.002*SL	0.027 + 0.003*SL
	t_F	0.036	0.030 + 0.003*SL	0.031 + 0.002*SL	0.026 + 0.002*SL
	t_{PLH}	0.030	0.026 + 0.002*SL	0.029 + 0.001*SL	0.032 + 0.001*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.023 + 0.001*SL	0.030 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg15/scg15d2/scg15d4

2-NAND into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	1	1	0
x	0	1	1	0
Other States				1

Cell Data

Input Load (SL)											
scg15				*scg15d2*				*scg15d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.2	1.2	1.0	1.0	1.1	1.2	2.1	2.2	1.1	1.1	4.0	4.3

Gate Count		
scg15	*scg15d2*	*scg15d4*
2.67	3.67	6.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg15

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.064	0.033 + 0.016*SL	0.032 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.060	0.034 + 0.013*SL	0.032 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.065	0.051 + 0.007*SL	0.052 + 0.007*SL	0.053 + 0.007*SL
	t_{PHL}	0.066	0.052 + 0.007*SL	0.053 + 0.007*SL	0.053 + 0.007*SL
B to Y	t_R	0.065	0.034 + 0.015*SL	0.031 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.061	0.035 + 0.013*SL	0.032 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.066	0.051 + 0.007*SL	0.053 + 0.007*SL	0.053 + 0.007*SL
	t_{PHL}	0.070	0.055 + 0.007*SL	0.057 + 0.007*SL	0.057 + 0.007*SL
C to Y	t_R	0.080	0.053 + 0.014*SL	0.045 + 0.016*SL	0.034 + 0.016*SL
	t_F	0.066	0.042 + 0.012*SL	0.036 + 0.014*SL	0.027 + 0.014*SL
	t_{PLH}	0.054	0.039 + 0.007*SL	0.040 + 0.007*SL	0.040 + 0.007*SL
	t_{PHL}	0.044	0.029 + 0.008*SL	0.033 + 0.007*SL	0.034 + 0.007*SL
D to Y	t_R	0.086	0.057 + 0.014*SL	0.052 + 0.016*SL	0.040 + 0.016*SL
	t_F	0.061	0.034 + 0.014*SL	0.034 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.057	0.043 + 0.007*SL	0.043 + 0.007*SL	0.043 + 0.007*SL
	t_{PHL}	0.045	0.030 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg15d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.049	0.033 + 0.008*SL	0.034 + 0.008*SL	0.026 + 0.008*SL
	t_F	0.047	0.034 + 0.006*SL	0.033 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.064	0.056 + 0.004*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PHL}	0.064	0.056 + 0.004*SL	0.058 + 0.003*SL	0.059 + 0.003*SL
B to Y	t_R	0.051	0.036 + 0.007*SL	0.034 + 0.008*SL	0.026 + 0.008*SL
	t_F	0.045	0.031 + 0.007*SL	0.032 + 0.007*SL	0.027 + 0.007*SL
	t_{PLH}	0.064	0.056 + 0.004*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PHL}	0.067	0.059 + 0.004*SL	0.061 + 0.003*SL	0.062 + 0.003*SL
C to Y	t_R	0.064	0.051 + 0.007*SL	0.047 + 0.008*SL	0.031 + 0.008*SL
	t_F	0.050	0.039 + 0.006*SL	0.034 + 0.007*SL	0.027 + 0.007*SL
	t_{PLH}	0.044	0.036 + 0.004*SL	0.038 + 0.003*SL	0.038 + 0.004*SL
	t_{PHL}	0.035	0.026 + 0.004*SL	0.030 + 0.003*SL	0.032 + 0.003*SL
D to Y	t_R	0.069	0.055 + 0.007*SL	0.052 + 0.008*SL	0.037 + 0.008*SL
	t_F	0.046	0.033 + 0.007*SL	0.033 + 0.007*SL	0.026 + 0.007*SL
	t_{PLH}	0.048	0.040 + 0.004*SL	0.042 + 0.003*SL	0.042 + 0.004*SL
	t_{PHL}	0.035	0.027 + 0.004*SL	0.030 + 0.003*SL	0.032 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg15d4

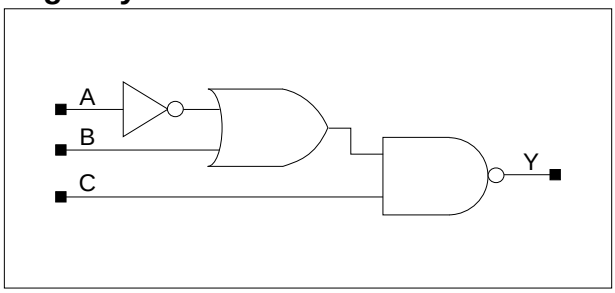
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.051	0.044 + 0.003*SL	0.043 + 0.004*SL	0.032 + 0.004*SL
	t_F	0.045	0.039 + 0.003*SL	0.037 + 0.003*SL	0.031 + 0.004*SL
	t_{PLH}	0.076	0.072 + 0.002*SL	0.074 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.073	0.068 + 0.002*SL	0.070 + 0.002*SL	0.074 + 0.002*SL
B to Y	t_R	0.055	0.053 + 0.001*SL	0.042 + 0.004*SL	0.032 + 0.004*SL
	t_F	0.046	0.039 + 0.004*SL	0.040 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.076	0.071 + 0.002*SL	0.073 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.076	0.072 + 0.002*SL	0.074 + 0.002*SL	0.078 + 0.002*SL
C to Y	t_R	0.056	0.050 + 0.003*SL	0.047 + 0.004*SL	0.033 + 0.004*SL
	t_F	0.046	0.039 + 0.004*SL	0.040 + 0.003*SL	0.030 + 0.004*SL
	t_{PLH}	0.040	0.035 + 0.002*SL	0.037 + 0.002*SL	0.038 + 0.002*SL
	t_{PHL}	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.034 + 0.002*SL
D to Y	t_R	0.064	0.056 + 0.004*SL	0.056 + 0.004*SL	0.038 + 0.004*SL
	t_F	0.043	0.034 + 0.005*SL	0.039 + 0.003*SL	0.029 + 0.004*SL
	t_{PLH}	0.045	0.041 + 0.002*SL	0.043 + 0.002*SL	0.043 + 0.002*SL
	t_{PHL}	0.034	0.029 + 0.002*SL	0.031 + 0.002*SL	0.035 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg16/scg16d2/scg16d4

2-OR with one Inverted Input into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	1	1	0
Other States			1

Cell Data

Input Load (SL)								
scg16			*scg16d2*			*scg16d4*		
A	B	C	A	B	C	A	B	C
0.7	1.2	1.2	0.7	2.3	2.5	0.7	1.2	1.2
Gate Count								
scg16			*scg16d2*			*scg16d4*		
2.00			3.33			4.33		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.044 + 0.019*SL	0.040 + 0.020*SL	0.040 + 0.020*SL
	t_F	0.049	0.031 + 0.009*SL	0.028 + 0.010*SL	0.023 + 0.010*SL
	t_{PLH}	0.069	0.051 + 0.009*SL	0.051 + 0.009*SL	0.052 + 0.009*SL
	t_{PHL}	0.073	0.062 + 0.006*SL	0.064 + 0.005*SL	0.066 + 0.005*SL
B to Y	t_R	0.089	0.052 + 0.019*SL	0.046 + 0.020*SL	0.040 + 0.020*SL
	t_F	0.061	0.044 + 0.009*SL	0.042 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.060	0.041 + 0.009*SL	0.043 + 0.009*SL	0.043 + 0.009*SL
	t_{PHL}	0.039	0.028 + 0.006*SL	0.031 + 0.005*SL	0.032 + 0.005*SL
C to Y	t_R	0.075	0.059 + 0.008*SL	0.053 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.056	0.039 + 0.009*SL	0.036 + 0.009*SL	0.027 + 0.010*SL
	t_{PLH}	0.043	0.033 + 0.005*SL	0.036 + 0.005*SL	0.035 + 0.005*SL
	t_{PHL}	0.042	0.031 + 0.006*SL	0.034 + 0.005*SL	0.035 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg16d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.049 + 0.009*SL	0.045 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.050	0.040 + 0.005*SL	0.041 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.072	0.063 + 0.005*SL	0.063 + 0.005*SL	0.064 + 0.005*SL
	t_{PHL}	0.084	0.078 + 0.003*SL	0.081 + 0.003*SL	0.086 + 0.002*SL
B to Y	t_R	0.071	0.054 + 0.009*SL	0.048 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.053	0.046 + 0.003*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.050	0.040 + 0.005*SL	0.042 + 0.005*SL	0.044 + 0.005*SL
	t_{PHL}	0.033	0.026 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
C to Y	t_R	0.066	0.059 + 0.003*SL	0.054 + 0.005*SL	0.042 + 0.005*SL
	t_F	0.047	0.039 + 0.004*SL	0.036 + 0.005*SL	0.029 + 0.005*SL
	t_{PLH}	0.037	0.031 + 0.003*SL	0.034 + 0.002*SL	0.035 + 0.002*SL
	t_{PHL}	0.036	0.030 + 0.003*SL	0.032 + 0.003*SL	0.035 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg16d4

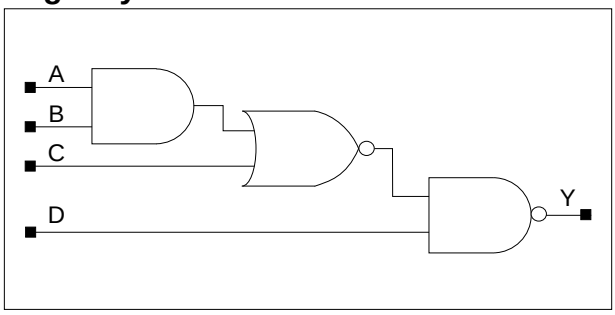
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.029 + 0.002*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.120	0.116 + 0.002*SL	0.118 + 0.001*SL	0.123 + 0.001*SL
	t_{PHL}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.129 + 0.001*SL
B to Y	t_R	0.033	0.027 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.023 + 0.002*SL	0.025 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.089	0.085 + 0.002*SL	0.088 + 0.001*SL	0.096 + 0.001*SL
C to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.023 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.094	0.091 + 0.002*SL	0.093 + 0.001*SL	0.098 + 0.001*SL
	t_{PHL}	0.092	0.088 + 0.002*SL	0.091 + 0.001*SL	0.099 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg17/scg17d2/scg17d4

2-AND into 2-NOR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	1	0
x	0	0	1	0
Other States				1

Cell Data

Input Load (SL)											
scg17				*scg17d2*				*scg17d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.0	1.1	1.0	1.0	1.0	2.5	1.0	1.0	1.0	4.8

Gate Count		
scg17	*scg17d2*	*scg17d4*
2.67	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg17

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.055	0.040 + 0.008*SL	0.029 + 0.010*SL	0.021 + 0.011*SL
	t_F	0.050	0.032 + 0.009*SL	0.030 + 0.010*SL	0.025 + 0.010*SL
	t_{PLH}	0.071	0.060 + 0.006*SL	0.063 + 0.005*SL	0.065 + 0.005*SL
	t_{PHL}	0.075	0.062 + 0.006*SL	0.067 + 0.005*SL	0.070 + 0.005*SL
B to Y	t_R	0.051	0.032 + 0.009*SL	0.028 + 0.010*SL	0.021 + 0.011*SL
	t_F	0.050	0.030 + 0.010*SL	0.033 + 0.009*SL	0.025 + 0.010*SL
	t_{PLH}	0.071	0.060 + 0.006*SL	0.063 + 0.005*SL	0.064 + 0.005*SL
	t_{PHL}	0.078	0.065 + 0.006*SL	0.070 + 0.005*SL	0.074 + 0.005*SL
C to Y	t_R	0.052	0.036 + 0.008*SL	0.025 + 0.011*SL	0.020 + 0.011*SL
	t_F	0.052	0.032 + 0.010*SL	0.034 + 0.009*SL	0.026 + 0.010*SL
	t_{PLH}	0.072	0.062 + 0.005*SL	0.064 + 0.005*SL	0.065 + 0.005*SL
	t_{PHL}	0.088	0.076 + 0.006*SL	0.081 + 0.005*SL	0.085 + 0.005*SL
D to Y	t_R	0.061	0.043 + 0.009*SL	0.039 + 0.010*SL	0.026 + 0.011*SL
	t_F	0.049	0.032 + 0.008*SL	0.027 + 0.010*SL	0.022 + 0.010*SL
	t_{PLH}	0.039	0.028 + 0.006*SL	0.032 + 0.005*SL	0.032 + 0.005*SL
	t_{PHL}	0.034	0.021 + 0.006*SL	0.026 + 0.005*SL	0.029 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg17d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.038 + 0.004*SL	0.033 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.045	0.034 + 0.006*SL	0.037 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.077	0.071 + 0.003*SL	0.074 + 0.002*SL	0.079 + 0.002*SL
	t_{PHL}	0.080	0.073 + 0.004*SL	0.077 + 0.003*SL	0.085 + 0.002*SL
B to Y	t_R	0.050	0.044 + 0.003*SL	0.036 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.047	0.038 + 0.004*SL	0.037 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.077	0.069 + 0.004*SL	0.074 + 0.002*SL	0.078 + 0.002*SL
	t_{PHL}	0.084	0.076 + 0.004*SL	0.080 + 0.003*SL	0.089 + 0.002*SL
C to Y	t_R	0.042	0.032 + 0.005*SL	0.032 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.046	0.036 + 0.005*SL	0.038 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.074	0.068 + 0.003*SL	0.071 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.094	0.086 + 0.004*SL	0.090 + 0.003*SL	0.099 + 0.002*SL
D to Y	t_R	0.052	0.044 + 0.004*SL	0.040 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.040	0.031 + 0.004*SL	0.029 + 0.005*SL	0.024 + 0.005*SL
	t_{PLH}	0.033	0.026 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
	t_{PHL}	0.027	0.020 + 0.004*SL	0.024 + 0.003*SL	0.030 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg17d4

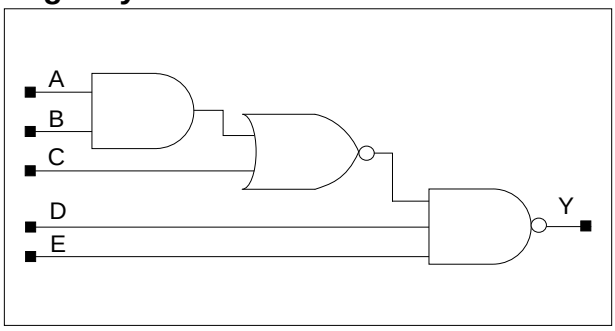
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.056	0.052 + 0.002*SL	0.050 + 0.002*SL	0.039 + 0.003*SL
	t_F	0.057	0.052 + 0.002*SL	0.053 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.107 + 0.001*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.114 + 0.001*SL
B to Y	t_R	0.056	0.052 + 0.002*SL	0.050 + 0.002*SL	0.041 + 0.003*SL
	t_F	0.058	0.054 + 0.002*SL	0.054 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.107 + 0.001*SL
	t_{PHL}	0.104	0.100 + 0.002*SL	0.103 + 0.001*SL	0.118 + 0.001*SL
C to Y	t_R	0.049	0.044 + 0.002*SL	0.043 + 0.002*SL	0.031 + 0.003*SL
	t_F	0.059	0.054 + 0.003*SL	0.056 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.088	0.085 + 0.002*SL	0.087 + 0.001*SL	0.093 + 0.001*SL
	t_{PHL}	0.115	0.111 + 0.002*SL	0.114 + 0.001*SL	0.129 + 0.001*SL
D to Y	t_R	0.048	0.044 + 0.002*SL	0.042 + 0.002*SL	0.027 + 0.003*SL
	t_F	0.036	0.030 + 0.003*SL	0.032 + 0.002*SL	0.030 + 0.002*SL
	t_{PLH}	0.030	0.026 + 0.002*SL	0.028 + 0.001*SL	0.032 + 0.001*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.023 + 0.001*SL	0.032 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

scg18/scg18d2/scg18d4

2-AND into 2-NOR into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	0	1	1	0
x	0	0	1	1	0
Other States					1

Cell Data

Input Load (SL)														
scg18					*scg18d2*					*scg18d4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	2.0	2.2	1.0	1.0	1.0	4.1	3.9

Gate Count		
scg18	*scg18d2*	*scg18d4*
3.00	4.00	6.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg18

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.038 + 0.015*SL	0.034 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.066	0.040 + 0.013*SL	0.037 + 0.014*SL	0.030 + 0.014*SL
	t_{PLH}	0.081	0.066 + 0.008*SL	0.068 + 0.007*SL	0.069 + 0.007*SL
	t_{PHL}	0.081	0.065 + 0.008*SL	0.069 + 0.007*SL	0.071 + 0.007*SL
B to Y	t_R	0.067	0.037 + 0.015*SL	0.033 + 0.016*SL	0.029 + 0.016*SL
	t_F	0.066	0.040 + 0.013*SL	0.038 + 0.014*SL	0.032 + 0.014*SL
	t_{PLH}	0.081	0.066 + 0.008*SL	0.068 + 0.007*SL	0.069 + 0.007*SL
	t_{PHL}	0.084	0.069 + 0.008*SL	0.072 + 0.007*SL	0.075 + 0.007*SL
C to Y	t_R	0.067	0.038 + 0.015*SL	0.032 + 0.016*SL	0.028 + 0.016*SL
	t_F	0.067	0.042 + 0.012*SL	0.037 + 0.014*SL	0.031 + 0.014*SL
	t_{PLH}	0.082	0.068 + 0.007*SL	0.069 + 0.007*SL	0.070 + 0.007*SL
	t_{PHL}	0.095	0.079 + 0.008*SL	0.083 + 0.007*SL	0.085 + 0.007*SL
D to Y	t_R	0.078	0.049 + 0.014*SL	0.044 + 0.016*SL	0.032 + 0.016*SL
	t_F	0.066	0.041 + 0.012*SL	0.036 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.052	0.038 + 0.007*SL	0.039 + 0.007*SL	0.039 + 0.007*SL
	t_{PHL}	0.044	0.028 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL
E to Y	t_R	0.084	0.056 + 0.014*SL	0.051 + 0.016*SL	0.039 + 0.016*SL
	t_F	0.061	0.034 + 0.014*SL	0.034 + 0.014*SL	0.028 + 0.014*SL
	t_{PLH}	0.056	0.042 + 0.007*SL	0.042 + 0.007*SL	0.042 + 0.007*SL
	t_{PHL}	0.044	0.029 + 0.008*SL	0.032 + 0.007*SL	0.033 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg18d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.056	0.042 + 0.007*SL	0.039 + 0.008*SL	0.030 + 0.008*SL
	t_F	0.054	0.040 + 0.007*SL	0.041 + 0.007*SL	0.033 + 0.007*SL
	t_{PLH}	0.082	0.074 + 0.004*SL	0.076 + 0.004*SL	0.079 + 0.004*SL
	t_{PHL}	0.081	0.072 + 0.004*SL	0.075 + 0.004*SL	0.080 + 0.003*SL
B to Y	t_R	0.054	0.038 + 0.008*SL	0.038 + 0.008*SL	0.029 + 0.008*SL
	t_F	0.054	0.039 + 0.007*SL	0.041 + 0.007*SL	0.034 + 0.007*SL
	t_{PLH}	0.082	0.073 + 0.004*SL	0.076 + 0.004*SL	0.079 + 0.004*SL
	t_{PHL}	0.085	0.076 + 0.004*SL	0.079 + 0.004*SL	0.084 + 0.003*SL
C to Y	t_R	0.051	0.036 + 0.008*SL	0.035 + 0.008*SL	0.027 + 0.008*SL
	t_F	0.055	0.042 + 0.007*SL	0.041 + 0.007*SL	0.034 + 0.007*SL
	t_{PLH}	0.080	0.072 + 0.004*SL	0.074 + 0.004*SL	0.076 + 0.004*SL
	t_{PHL}	0.094	0.085 + 0.005*SL	0.089 + 0.004*SL	0.094 + 0.003*SL
D to Y	t_R	0.064	0.051 + 0.007*SL	0.047 + 0.008*SL	0.031 + 0.008*SL
	t_F	0.051	0.038 + 0.006*SL	0.037 + 0.007*SL	0.029 + 0.007*SL
	t_{PLH}	0.044	0.036 + 0.004*SL	0.038 + 0.003*SL	0.038 + 0.004*SL
	t_{PHL}	0.035	0.026 + 0.005*SL	0.030 + 0.004*SL	0.033 + 0.003*SL
E to Y	t_R	0.069	0.055 + 0.007*SL	0.052 + 0.008*SL	0.037 + 0.008*SL
	t_F	0.047	0.032 + 0.007*SL	0.035 + 0.007*SL	0.028 + 0.007*SL
	t_{PLH}	0.048	0.040 + 0.004*SL	0.042 + 0.004*SL	0.042 + 0.004*SL
	t_{PHL}	0.036	0.027 + 0.004*SL	0.031 + 0.003*SL	0.033 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

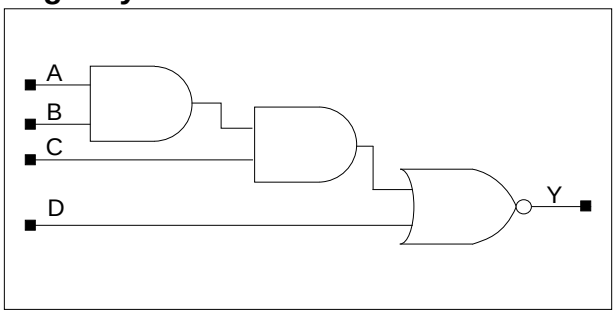
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg18d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.062	0.055 + 0.004*SL	0.054 + 0.004*SL	0.041 + 0.004*SL
	t_F	0.061	0.054 + 0.003*SL	0.054 + 0.003*SL	0.045 + 0.003*SL
	t_{PLH}	0.101	0.096 + 0.002*SL	0.098 + 0.002*SL	0.106 + 0.002*SL
	t_{PHL}	0.098	0.093 + 0.003*SL	0.096 + 0.002*SL	0.107 + 0.002*SL
B to Y	t_R	0.062	0.055 + 0.004*SL	0.054 + 0.004*SL	0.041 + 0.004*SL
	t_F	0.062	0.056 + 0.003*SL	0.055 + 0.003*SL	0.045 + 0.003*SL
	t_{PLH}	0.101	0.096 + 0.002*SL	0.098 + 0.002*SL	0.106 + 0.002*SL
	t_{PHL}	0.102	0.096 + 0.003*SL	0.099 + 0.002*SL	0.111 + 0.002*SL
C to Y	t_R	0.055	0.049 + 0.003*SL	0.046 + 0.004*SL	0.033 + 0.004*SL
	t_F	0.062	0.055 + 0.003*SL	0.055 + 0.003*SL	0.045 + 0.003*SL
	t_{PLH}	0.093	0.088 + 0.002*SL	0.090 + 0.002*SL	0.094 + 0.002*SL
	t_{PHL}	0.112	0.107 + 0.003*SL	0.110 + 0.002*SL	0.122 + 0.002*SL
D to Y	t_R	0.057	0.051 + 0.003*SL	0.047 + 0.004*SL	0.033 + 0.004*SL
	t_F	0.047	0.039 + 0.004*SL	0.041 + 0.003*SL	0.034 + 0.004*SL
	t_{PLH}	0.040	0.035 + 0.002*SL	0.037 + 0.002*SL	0.038 + 0.002*SL
	t_{PHL}	0.031	0.026 + 0.003*SL	0.029 + 0.002*SL	0.036 + 0.002*SL
E to Y	t_R	0.065	0.057 + 0.004*SL	0.057 + 0.004*SL	0.039 + 0.004*SL
	t_F	0.043	0.036 + 0.003*SL	0.036 + 0.003*SL	0.035 + 0.004*SL
	t_{PLH}	0.045	0.041 + 0.002*SL	0.043 + 0.002*SL	0.043 + 0.002*SL
	t_{PHL}	0.035	0.030 + 0.002*SL	0.032 + 0.002*SL	0.038 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
scg19				*scg19d2*				*scg19*	*scg19d2*
A	B	C	D	A	B	C	D		
1.2	1.2	1.0	1.0	1.1	1.2	1.9	2.2	3.00	4.33

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg19

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.079	0.039 + 0.020*SL	0.036 + 0.020*SL	0.037 + 0.020*SL
	t_F	0.059	0.029 + 0.015*SL	0.027 + 0.016*SL	0.025 + 0.016*SL
	t_{PLH}	0.091	0.073 + 0.009*SL	0.074 + 0.009*SL	0.074 + 0.009*SL
	t_{PHL}	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.073 + 0.008*SL
B to Y	t_R	0.079	0.040 + 0.020*SL	0.037 + 0.020*SL	0.036 + 0.020*SL
	t_F	0.059	0.029 + 0.015*SL	0.026 + 0.016*SL	0.025 + 0.016*SL
	t_{PLH}	0.095	0.076 + 0.009*SL	0.077 + 0.009*SL	0.077 + 0.009*SL
	t_{PHL}	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.073 + 0.008*SL
C to Y	t_R	0.095	0.058 + 0.018*SL	0.052 + 0.020*SL	0.041 + 0.020*SL
	t_F	0.067	0.039 + 0.014*SL	0.033 + 0.015*SL	0.025 + 0.016*SL
	t_{PLH}	0.054	0.036 + 0.009*SL	0.037 + 0.009*SL	0.036 + 0.009*SL
	t_{PHL}	0.048	0.031 + 0.009*SL	0.034 + 0.008*SL	0.035 + 0.008*SL
D to Y	t_R	0.089	0.052 + 0.019*SL	0.046 + 0.020*SL	0.041 + 0.020*SL
	t_F	0.064	0.046 + 0.009*SL	0.044 + 0.010*SL	0.032 + 0.010*SL
	t_{PLH}	0.064	0.045 + 0.009*SL	0.046 + 0.009*SL	0.046 + 0.009*SL
	t_{PHL}	0.048	0.036 + 0.006*SL	0.038 + 0.005*SL	0.039 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

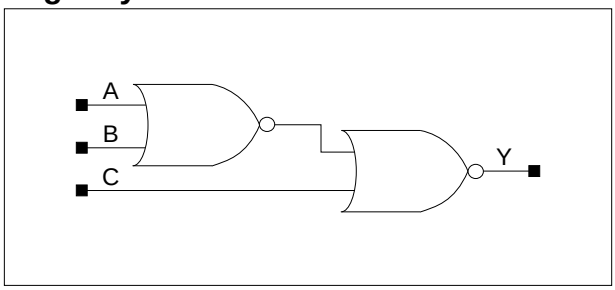
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg19d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.060	0.041 + 0.010*SL	0.040 + 0.010*SL	0.036 + 0.010*SL
	t_F	0.046	0.030 + 0.008*SL	0.031 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.088	0.079 + 0.005*SL	0.080 + 0.005*SL	0.080 + 0.005*SL
	t_{PHL}	0.086	0.077 + 0.004*SL	0.079 + 0.004*SL	0.081 + 0.004*SL
B to Y	t_R	0.061	0.041 + 0.010*SL	0.040 + 0.010*SL	0.037 + 0.010*SL
	t_F	0.046	0.030 + 0.008*SL	0.031 + 0.008*SL	0.025 + 0.008*SL
	t_{PLH}	0.093	0.083 + 0.005*SL	0.084 + 0.005*SL	0.085 + 0.005*SL
	t_{PHL}	0.087	0.078 + 0.004*SL	0.080 + 0.004*SL	0.081 + 0.004*SL
C to Y	t_R	0.077	0.061 + 0.008*SL	0.055 + 0.010*SL	0.041 + 0.010*SL
	t_F	0.051	0.036 + 0.008*SL	0.036 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.044	0.034 + 0.005*SL	0.036 + 0.004*SL	0.036 + 0.005*SL
	t_{PHL}	0.039	0.029 + 0.005*SL	0.033 + 0.004*SL	0.036 + 0.004*SL
D to Y	t_R	0.070	0.053 + 0.009*SL	0.048 + 0.010*SL	0.041 + 0.010*SL
	t_F	0.053	0.044 + 0.004*SL	0.043 + 0.005*SL	0.032 + 0.005*SL
	t_{PLH}	0.054	0.044 + 0.005*SL	0.046 + 0.005*SL	0.047 + 0.005*SL
	t_{PHL}	0.042	0.035 + 0.003*SL	0.038 + 0.003*SL	0.039 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	x	0	1
x	1	0	1
Other States			0

Cell Data

Input Load (SL)								
scg20			*scg20d2*			*scg20d4*		
A	B	C	A	B	C	A	B	C
1.1	1.1	1.1	1.1	1.1	2.5	1.0	1.1	4.6
Gate Count								
scg20			*scg20d2*			*scg20d4*		
2.00			3.00			4.67		

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg20

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.034 + 0.020*SL	0.032 + 0.020*SL	0.031 + 0.020*SL
	t_F	0.041	0.026 + 0.007*SL	0.027 + 0.007*SL	0.022 + 0.008*SL
	t_{PLH}	0.065	0.047 + 0.009*SL	0.048 + 0.009*SL	0.048 + 0.009*SL
	t_{PHL}	0.070	0.060 + 0.005*SL	0.065 + 0.004*SL	0.069 + 0.004*SL
B to Y	t_R	0.074	0.035 + 0.020*SL	0.033 + 0.020*SL	0.031 + 0.020*SL
	t_F	0.039	0.024 + 0.008*SL	0.026 + 0.007*SL	0.020 + 0.008*SL
	t_{PLH}	0.070	0.051 + 0.009*SL	0.053 + 0.009*SL	0.053 + 0.009*SL
	t_{PHL}	0.073	0.063 + 0.005*SL	0.068 + 0.004*SL	0.072 + 0.004*SL
C to Y	t_R	0.081	0.045 + 0.018*SL	0.037 + 0.020*SL	0.031 + 0.020*SL
	t_F	0.050	0.040 + 0.005*SL	0.033 + 0.007*SL	0.023 + 0.007*SL
	t_{PLH}	0.055	0.036 + 0.010*SL	0.038 + 0.009*SL	0.038 + 0.009*SL
	t_{PHL}	0.034	0.023 + 0.005*SL	0.029 + 0.004*SL	0.030 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg20d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.053	0.034 + 0.010*SL	0.032 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.037	0.029 + 0.004*SL	0.030 + 0.004*SL	0.027 + 0.004*SL
	t_{PLH}	0.060	0.051 + 0.005*SL	0.051 + 0.005*SL	0.052 + 0.005*SL
	t_{PHL}	0.075	0.068 + 0.003*SL	0.073 + 0.002*SL	0.082 + 0.002*SL
B to Y	t_R	0.054	0.036 + 0.009*SL	0.032 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.038	0.030 + 0.004*SL	0.031 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.064	0.055 + 0.005*SL	0.056 + 0.005*SL	0.056 + 0.005*SL
	t_{PHL}	0.078	0.072 + 0.003*SL	0.076 + 0.002*SL	0.086 + 0.002*SL
C to Y	t_R	0.058	0.041 + 0.009*SL	0.036 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.043	0.037 + 0.003*SL	0.035 + 0.003*SL	0.023 + 0.004*SL
	t_{PLH}	0.043	0.033 + 0.005*SL	0.036 + 0.005*SL	0.037 + 0.005*SL
	t_{PHL}	0.027	0.021 + 0.003*SL	0.026 + 0.002*SL	0.030 + 0.002*SL

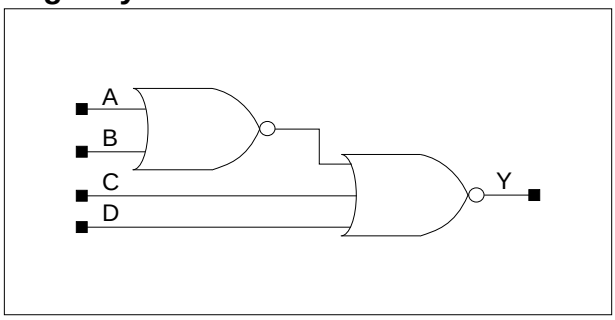
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg20d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.054	0.049 + 0.002*SL	0.038 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.050	0.046 + 0.002*SL	0.046 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.068	0.063 + 0.003*SL	0.064 + 0.002*SL	0.065 + 0.002*SL
	t_{PHL}	0.097	0.093 + 0.002*SL	0.096 + 0.001*SL	0.114 + 0.001*SL
B to Y	t_R	0.050	0.042 + 0.004*SL	0.037 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.049	0.045 + 0.002*SL	0.046 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.072	0.067 + 0.003*SL	0.068 + 0.002*SL	0.070 + 0.002*SL
	t_{PHL}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.118 + 0.001*SL
C to Y	t_R	0.052	0.044 + 0.004*SL	0.041 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.040	0.036 + 0.002*SL	0.038 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.039	0.033 + 0.003*SL	0.036 + 0.002*SL	0.038 + 0.002*SL
	t_{PHL}	0.024	0.020 + 0.002*SL	0.023 + 0.001*SL	0.030 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	0	0	1
x	1	0	0	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
scg21				*scg21d2*				*scg21*	*scg21d2*
A	B	C	D	A	B	C	D		
1.1	1.2	1.0	1.0	1.1	1.2	2.0	2.1	2.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.048 + 0.030*SL	0.046 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.053	0.028 + 0.012*SL	0.027 + 0.013*SL	0.020 + 0.013*SL
	t_{PLH}	0.071	0.043 + 0.014*SL	0.045 + 0.014*SL	0.046 + 0.014*SL
	t_{PHL}	0.080	0.065 + 0.008*SL	0.070 + 0.007*SL	0.072 + 0.007*SL
B to Y	t_R	0.109	0.049 + 0.030*SL	0.046 + 0.031*SL	0.046 + 0.031*SL
	t_F	0.053	0.027 + 0.013*SL	0.028 + 0.013*SL	0.021 + 0.013*SL
	t_{PLH}	0.076	0.048 + 0.014*SL	0.049 + 0.014*SL	0.050 + 0.014*SL
	t_{PHL}	0.083	0.067 + 0.008*SL	0.072 + 0.007*SL	0.075 + 0.007*SL
C to Y	t_R	0.114	0.057 + 0.029*SL	0.050 + 0.030*SL	0.046 + 0.031*SL
	t_F	0.063	0.040 + 0.011*SL	0.036 + 0.012*SL	0.023 + 0.013*SL
	t_{PLH}	0.073	0.045 + 0.014*SL	0.046 + 0.014*SL	0.047 + 0.014*SL
	t_{PHL}	0.049	0.034 + 0.007*SL	0.037 + 0.007*SL	0.038 + 0.007*SL
D to Y	t_R	0.110	0.051 + 0.029*SL	0.047 + 0.030*SL	0.046 + 0.031*SL
	t_F	0.070	0.047 + 0.012*SL	0.044 + 0.012*SL	0.033 + 0.013*SL
	t_{PLH}	0.078	0.050 + 0.014*SL	0.051 + 0.014*SL	0.051 + 0.014*SL
	t_{PHL}	0.052	0.037 + 0.007*SL	0.040 + 0.007*SL	0.042 + 0.007*SL

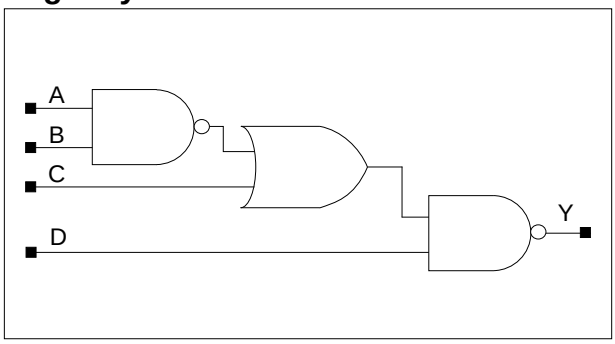
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

scg21d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.046 + 0.015*SL	0.043 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.044	0.030 + 0.007*SL	0.034 + 0.006*SL	0.025 + 0.006*SL
	t_{PLH}	0.061	0.047 + 0.007*SL	0.048 + 0.007*SL	0.049 + 0.007*SL
	t_{PHL}	0.084	0.074 + 0.005*SL	0.080 + 0.004*SL	0.087 + 0.003*SL
B to Y	t_R	0.076	0.048 + 0.014*SL	0.044 + 0.015*SL	0.043 + 0.015*SL
	t_F	0.045	0.031 + 0.007*SL	0.034 + 0.006*SL	0.025 + 0.006*SL
	t_{PLH}	0.065	0.051 + 0.007*SL	0.052 + 0.007*SL	0.053 + 0.007*SL
	t_{PHL}	0.087	0.077 + 0.005*SL	0.083 + 0.003*SL	0.090 + 0.003*SL
C to Y	t_R	0.082	0.055 + 0.014*SL	0.048 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.051	0.040 + 0.006*SL	0.039 + 0.006*SL	0.023 + 0.006*SL
	t_{PLH}	0.057	0.042 + 0.007*SL	0.044 + 0.007*SL	0.045 + 0.007*SL
	t_{PHL}	0.040	0.031 + 0.004*SL	0.035 + 0.003*SL	0.037 + 0.003*SL
D to Y	t_R	0.078	0.049 + 0.015*SL	0.046 + 0.015*SL	0.042 + 0.015*SL
	t_F	0.057	0.044 + 0.007*SL	0.047 + 0.006*SL	0.031 + 0.006*SL
	t_{PLH}	0.062	0.048 + 0.007*SL	0.049 + 0.007*SL	0.050 + 0.007*SL
	t_{PHL}	0.044	0.035 + 0.004*SL	0.039 + 0.003*SL	0.041 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)											
scg22				*scg22d2*				*scg22d4*			
A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.2	1.1	1.1	1.2	2.3	2.5	1.0	1.0	1.2	1.2

Gate Count		
scg22	*scg22d2*	*scg22d4*
2.33	3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.084	0.044 + 0.020*SL	0.041 + 0.020*SL	0.040 + 0.020*SL
	t_F	0.047	0.029 + 0.009*SL	0.025 + 0.010*SL	0.021 + 0.010*SL
	t_{PLH}	0.072	0.053 + 0.009*SL	0.054 + 0.009*SL	0.055 + 0.009*SL
	t_{PHL}	0.067	0.056 + 0.005*SL	0.058 + 0.005*SL	0.059 + 0.005*SL
B to Y	t_R	0.084	0.044 + 0.020*SL	0.042 + 0.020*SL	0.040 + 0.020*SL
	t_F	0.047	0.029 + 0.009*SL	0.027 + 0.010*SL	0.023 + 0.010*SL
	t_{PLH}	0.073	0.054 + 0.009*SL	0.055 + 0.009*SL	0.056 + 0.009*SL
	t_{PHL}	0.071	0.060 + 0.006*SL	0.063 + 0.005*SL	0.064 + 0.005*SL
C to Y	t_R	0.089	0.052 + 0.019*SL	0.046 + 0.020*SL	0.040 + 0.020*SL
	t_F	0.061	0.044 + 0.009*SL	0.042 + 0.009*SL	0.030 + 0.010*SL
	t_{PLH}	0.060	0.041 + 0.009*SL	0.043 + 0.009*SL	0.044 + 0.009*SL
	t_{PHL}	0.039	0.028 + 0.006*SL	0.032 + 0.005*SL	0.032 + 0.005*SL
D to Y	t_R	0.075	0.059 + 0.008*SL	0.054 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.056	0.039 + 0.009*SL	0.036 + 0.009*SL	0.027 + 0.010*SL
	t_{PLH}	0.043	0.033 + 0.005*SL	0.036 + 0.005*SL	0.035 + 0.005*SL
	t_{PHL}	0.042	0.031 + 0.006*SL	0.034 + 0.005*SL	0.035 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

2-NAND into 2-OR into 2-NAND with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

scg22d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.049 + 0.009*SL	0.046 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.040	0.031 + 0.005*SL	0.030 + 0.005*SL	0.024 + 0.005*SL
	t_{PLH}	0.074	0.064 + 0.005*SL	0.065 + 0.005*SL	0.066 + 0.005*SL
	t_{PHL}	0.065	0.059 + 0.003*SL	0.061 + 0.003*SL	0.064 + 0.002*SL
B to Y	t_R	0.067	0.048 + 0.010*SL	0.046 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.025 + 0.005*SL
	t_{PLH}	0.074	0.064 + 0.005*SL	0.065 + 0.005*SL	0.067 + 0.005*SL
	t_{PHL}	0.069	0.063 + 0.003*SL	0.065 + 0.003*SL	0.067 + 0.002*SL
C to Y	t_R	0.071	0.054 + 0.009*SL	0.048 + 0.010*SL	0.042 + 0.010*SL
	t_F	0.053	0.046 + 0.003*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_{PLH}	0.051	0.040 + 0.005*SL	0.043 + 0.005*SL	0.044 + 0.005*SL
	t_{PHL}	0.033	0.026 + 0.003*SL	0.030 + 0.002*SL	0.032 + 0.002*SL
D to Y	t_R	0.055	0.047 + 0.004*SL	0.044 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.048	0.039 + 0.005*SL	0.039 + 0.005*SL	0.028 + 0.005*SL
	t_{PLH}	0.038	0.032 + 0.003*SL	0.035 + 0.002*SL	0.035 + 0.002*SL
	t_{PHL}	0.036	0.030 + 0.003*SL	0.032 + 0.003*SL	0.035 + 0.002*SL

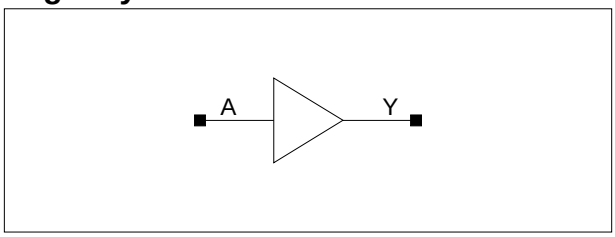
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

scg22d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.029 + 0.003*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.018 + 0.002*SL
	t_{PLH}	0.122	0.118 + 0.002*SL	0.121 + 0.001*SL	0.126 + 0.001*SL
	t_{PHL}	0.115	0.111 + 0.002*SL	0.114 + 0.001*SL	0.122 + 0.001*SL
B to Y	t_R	0.033	0.029 + 0.002*SL	0.027 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.023 + 0.002*SL	0.025 + 0.002*SL	0.018 + 0.002*SL
	t_{PLH}	0.123	0.119 + 0.002*SL	0.122 + 0.001*SL	0.127 + 0.001*SL
	t_{PHL}	0.119	0.116 + 0.002*SL	0.119 + 0.001*SL	0.127 + 0.001*SL
C to Y	t_R	0.033	0.027 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.108 + 0.001*SL	0.113 + 0.001*SL
	t_{PHL}	0.089	0.085 + 0.002*SL	0.088 + 0.001*SL	0.096 + 0.001*SL
D to Y	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.024 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.094	0.090 + 0.002*SL	0.093 + 0.001*SL	0.097 + 0.001*SL
	t_{PHL}	0.091	0.087 + 0.002*SL	0.090 + 0.001*SL	0.098 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
dl1d2	*dl1d2*
A	
0.7	4.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

dl1d2

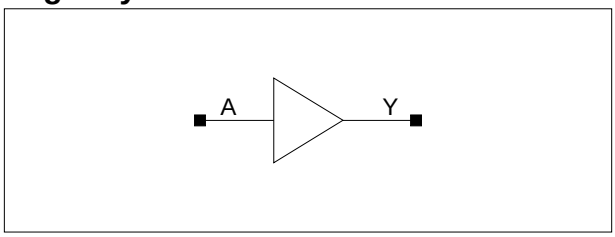
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.032 + 0.005*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.040	0.032 + 0.004*SL	0.035 + 0.004*SL	0.023 + 0.004*SL
	t_{PLH}	0.986	0.980 + 0.003*SL	0.984 + 0.002*SL	0.988 + 0.002*SL
	t_{PHL}	1.035	1.028 + 0.004*SL	1.033 + 0.002*SL	1.041 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

dl2d2

2ns Delay Cell with 2X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
dl2d2	*dl2d2*
A	
0.7	5.33

Switching Characteristics

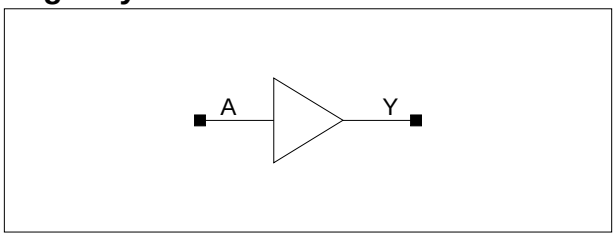
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

dl2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.047	0.039 + 0.004*SL	0.036 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.051	0.044 + 0.003*SL	0.044 + 0.003*SL	0.028 + 0.004*SL
	t_{PLH}	1.684	1.677 + 0.003*SL	1.682 + 0.002*SL	1.686 + 0.002*SL
	t_{PHL}	1.870	1.863 + 0.004*SL	1.869 + 0.002*SL	1.879 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
dl5d2	*dl5d2*
A	
0.7	7.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

dl5d2

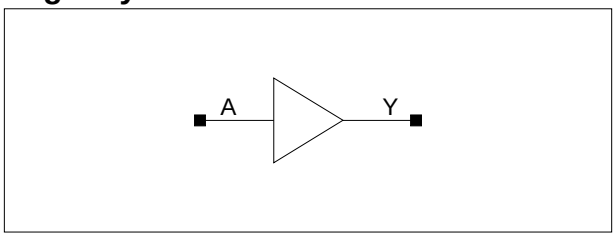
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.045	0.035 + 0.005*SL	0.036 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.050	0.041 + 0.004*SL	0.045 + 0.003*SL	0.028 + 0.004*SL
	t_{PLH}	4.305	4.298 + 0.003*SL	4.302 + 0.002*SL	4.307 + 0.002*SL
	t_{PHL}	4.498	4.490 + 0.004*SL	4.496 + 0.002*SL	4.507 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

dl10d2

10ns Delay Cell with 2X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
dl10d2	*dl10d2*
A	
0.7	10.00

Switching Characteristics

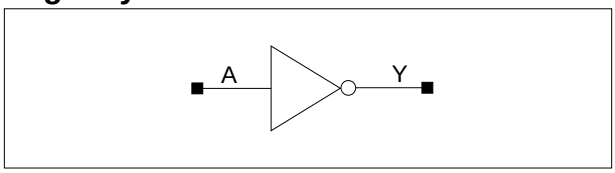
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

dl10d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.046	0.037 + 0.005*SL	0.038 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.054	0.047 + 0.003*SL	0.047 + 0.003*SL	0.033 + 0.004*SL
	t_{PLH}	8.527	8.520 + 0.004*SL	8.525 + 0.002*SL	8.530 + 0.002*SL
	t_{PHL}	8.961	8.953 + 0.004*SL	8.960 + 0.002*SL	8.972 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)							
iv	*ivd2*	*ivd3*	*ivd4*	*ivd6*	*ivd8*	*ivd16*	*ivd24*
A	A	A	A	A	A	A	A
1.0	2.0	3.0	4.0	6.0	8.3	17.3	26.7
Gate Count							
iv	*ivd2*	*ivd3*	*ivd4*	*ivd6*	*ivd8*	*ivd16*	*ivd24*
1.00	1.33	1.67	2.00	3.00	3.67	7.00	10.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

iv

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.052	0.037 + 0.008*SL	0.029 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.047	0.034 + 0.007*SL	0.027 + 0.008*SL	0.015 + 0.009*SL
	t_{PLH}	0.031	0.019 + 0.006*SL	0.026 + 0.004*SL	0.027 + 0.004*SL
	t_{PHL}	0.031	0.018 + 0.007*SL	0.026 + 0.005*SL	0.027 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ivd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.043	0.034 + 0.004*SL	0.033 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.037	0.029 + 0.004*SL	0.029 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.023	0.015 + 0.004*SL	0.022 + 0.002*SL	0.026 + 0.002*SL
	t_{PHL}	0.023	0.015 + 0.004*SL	0.021 + 0.002*SL	0.026 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ivd3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.034 + 0.003*SL	0.034 + 0.003*SL	0.016 + 0.003*SL
	t_F	0.036	0.028 + 0.004*SL	0.032 + 0.003*SL	0.014 + 0.003*SL
	t_{PLH}	0.021	0.016 + 0.003*SL	0.020 + 0.002*SL	0.026 + 0.001*SL
	t_{PHL}	0.021	0.015 + 0.003*SL	0.020 + 0.002*SL	0.026 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 47, *Group3 : 47 < SL

ivd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.032 + 0.003*SL	0.034 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.033	0.027 + 0.003*SL	0.031 + 0.002*SL	0.014 + 0.002*SL
	t_{PLH}	0.019	0.015 + 0.002*SL	0.019 + 0.001*SL	0.026 + 0.001*SL
	t_{PHL}	0.019	0.014 + 0.002*SL	0.018 + 0.001*SL	0.026 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ivd6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.032 + 0.002*SL	0.034 + 0.001*SL	0.017 + 0.002*SL
	t_F	0.031	0.027 + 0.002*SL	0.030 + 0.001*SL	0.015 + 0.001*SL
	t_{PLH}	0.018	0.015 + 0.002*SL	0.018 + 0.001*SL	0.026 + 0.001*SL
	t_{PHL}	0.017	0.014 + 0.002*SL	0.017 + 0.001*SL	0.026 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 90, *Group3 : 90 < SL

ivd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.032 + 0.002*SL	0.034 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.030	0.027 + 0.002*SL	0.030 + 0.001*SL	0.015 + 0.001*SL
	t_{PLH}	0.017	0.015 + 0.001*SL	0.017 + 0.001*SL	0.026 + 0.001*SL
	t_{PHL}	0.017	0.014 + 0.001*SL	0.017 + 0.001*SL	0.026 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

ivd16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.032 + 0.001*SL	0.033 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.029	0.027 + 0.001*SL	0.029 + 0.001*SL	0.016 + 0.001*SL
	t_{PLH}	0.016	0.015 + 0.001*SL	0.016 + 0.000*SL	0.027 + 0.000*SL
	t_{PHL}	0.016	0.014 + 0.001*SL	0.016 + 0.000*SL	0.027 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 232, *Group3 : 232 < SL

ivd24

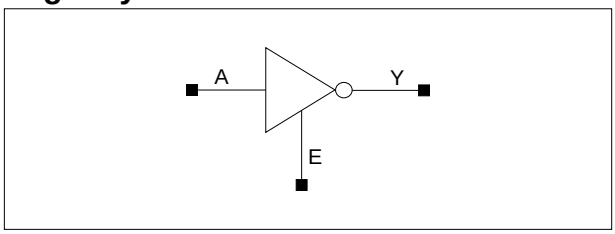
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.032 + 0.001*SL	0.033 + 0.000*SL	0.017 + 0.000*SL
	t_F	0.029	0.027 + 0.001*SL	0.029 + 0.000*SL	0.016 + 0.000*SL
	t_{PLH}	0.017	0.016 + 0.000*SL	0.017 + 0.000*SL	0.027 + 0.000*SL
	t_{PHL}	0.016	0.015 + 0.000*SL	0.016 + 0.000*SL	0.027 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 345, *Group3 : 345 < SL

ivt/ivtd2/ivtd4/ivtd8/ivtd16

Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)										Output Load (SL)				
ivt		*ivtd2*		*ivtd4*		*ivtd8*		*ivtd16*		*ivt*	*ivtd2*	*ivtd4*	*ivtd8*	*ivtd16*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
1.0	1.6	1.0	1.6	1.1	2.1	1.0	3.5	1.0	3.5	0.9	1.3	2.7	5.4	10.8

Gate Count				
ivt	*ivtd2*	*ivtd4*	*ivtd8*	*ivtd16*
3.67	4.00	4.67	7.67	11.00

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ivt

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.040	0.021 + 0.010*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.034	0.018 + 0.008*SL	0.018 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.078	0.067 + 0.005*SL	0.070 + 0.005*SL	0.071 + 0.004*SL
	t_{PHL}	0.077	0.067 + 0.005*SL	0.070 + 0.004*SL	0.073 + 0.004*SL
E to Y	t_R	0.039	0.020 + 0.010*SL	0.019 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.033	0.015 + 0.009*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.053	0.042 + 0.005*SL	0.045 + 0.004*SL	0.045 + 0.004*SL
	t_{PHL}	0.069	0.059 + 0.005*SL	0.063 + 0.004*SL	0.065 + 0.004*SL
	t_{PLZ}	0.083	0.083 + 0.000*SL	0.083 + 0.000*SL	0.083 + 0.000*SL
	t_{PHZ}	0.065	0.065 + 0.000*SL	0.065 + 0.000*SL	0.065 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ivtd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.031	0.023 + 0.004*SL	0.020 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.021 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.077	0.071 + 0.003*SL	0.074 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.075	0.069 + 0.003*SL	0.072 + 0.002*SL	0.077 + 0.002*SL
E to Y	t_R	0.032	0.020 + 0.006*SL	0.023 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.025	0.016 + 0.004*SL	0.018 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.052	0.046 + 0.003*SL	0.049 + 0.002*SL	0.052 + 0.002*SL
	t_{PHL}	0.066	0.059 + 0.003*SL	0.064 + 0.002*SL	0.069 + 0.002*SL
	t_{PLZ}	0.089	0.089 + 0.000*SL	0.089 + 0.000*SL	0.089 + 0.000*SL
	t_{PHZ}	0.076	0.076 + 0.000*SL	0.076 + 0.000*SL	0.076 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ivtd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.027 + 0.004*SL	0.032 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.028 + 0.001*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.079	0.075 + 0.002*SL	0.077 + 0.001*SL	0.083 + 0.001*SL
	t_{PHL}	0.081	0.078 + 0.002*SL	0.079 + 0.001*SL	0.086 + 0.001*SL
E to Y	t_R	0.029	0.024 + 0.002*SL	0.024 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.023	0.018 + 0.002*SL	0.021 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.049	0.046 + 0.002*SL	0.049 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.069	0.065 + 0.002*SL	0.069 + 0.001*SL	0.079 + 0.001*SL
	t_{PLZ}	0.086	0.086 + 0.000*SL	0.086 + 0.000*SL	0.086 + 0.000*SL
	t_{PHZ}	0.093	0.092 + 0.000*SL	0.093 + 0.000*SL	0.095 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ivtd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.026 + 0.001*SL	0.027 + 0.001*SL	0.018 + 0.001*SL
	t_F	0.030	0.029 + 0.001*SL	0.027 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.092	0.090 + 0.001*SL	0.092 + 0.001*SL	0.099 + 0.001*SL
	t_{PHL}	0.092	0.090 + 0.001*SL	0.091 + 0.001*SL	0.099 + 0.001*SL
E to Y	t_R	0.026	0.023 + 0.002*SL	0.025 + 0.001*SL	0.017 + 0.001*SL
	t_F	0.021	0.018 + 0.001*SL	0.020 + 0.001*SL	0.021 + 0.001*SL
	t_{PLH}	0.047	0.045 + 0.001*SL	0.047 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.078	0.076 + 0.001*SL	0.078 + 0.001*SL	0.090 + 0.001*SL
	t_{PLZ}	0.103	0.103 + 0.000*SL	0.103 + 0.000*SL	0.103 + 0.000*SL
	t_{PHZ}	0.093	0.092 + 0.000*SL	0.093 + 0.000*SL	0.095 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

ivtd16

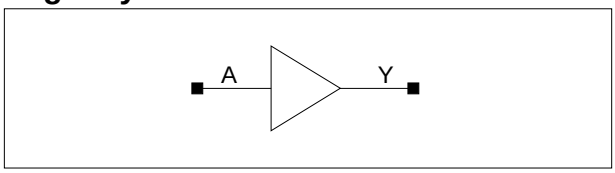
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.037	0.035 + 0.001*SL	0.036 + 0.001*SL	0.028 + 0.001*SL
	t_F	0.049	0.048 + 0.000*SL	0.048 + 0.000*SL	0.033 + 0.000*SL
	t_{PLH}	0.107	0.106 + 0.001*SL	0.107 + 0.000*SL	0.123 + 0.000*SL
	t_{PHL}	0.111	0.110 + 0.000*SL	0.110 + 0.000*SL	0.119 + 0.000*SL
E to Y	t_R	0.036	0.036 + 0.000*SL	0.033 + 0.001*SL	0.027 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.028 + 0.001*SL	0.030 + 0.000*SL
	t_{PLH}	0.060	0.059 + 0.001*SL	0.060 + 0.000*SL	0.076 + 0.000*SL
	t_{PHL}	0.089	0.087 + 0.001*SL	0.089 + 0.000*SL	0.108 + 0.000*SL
	t_{PLZ}	0.119	0.118 + 0.000*SL	0.119 + 0.000*SL	0.119 + 0.000*SL
	t_{PHZ}	0.134	0.133 + 0.000*SL	0.134 + 0.000*SL	0.138 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 232, *Group3 : 232 < SL

nid/nid2/nid3/nid4/nid6/nid8/nid16/nid24

Non-Inverting Buffer with 1X/2X/3X/4X/6X/8X/16X/24X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)							
nid	*nid2*	*nid3*	*nid4*	*nid6*	*nid8*	*nid16*	*nid24*
A	A	A	A	A	A	A	A
0.9	1.0	1.0	1.0	1.8	1.8	3.6	5.5
Gate Count							
nid	*nid2*	*nid3*	*nid4*	*nid6*	*nid8*	*nid16*	*nid24*
1.33	1.67	2.00	2.67	3.67	4.67	8.67	12.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nid

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.042	0.023 + 0.009*SL	0.021 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.041	0.021 + 0.010*SL	0.019 + 0.010*SL	0.013 + 0.011*SL
	t_{PLH}	0.060	0.050 + 0.005*SL	0.052 + 0.004*SL	0.052 + 0.004*SL
	t_{PHL}	0.054	0.042 + 0.006*SL	0.044 + 0.005*SL	0.045 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nid2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.033	0.019 + 0.007*SL	0.028 + 0.005*SL	0.013 + 0.005*SL
	t_{PLH}	0.059	0.053 + 0.003*SL	0.056 + 0.002*SL	0.057 + 0.002*SL
	t_{PHL}	0.053	0.046 + 0.003*SL	0.049 + 0.003*SL	0.052 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nid3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.038	0.034 + 0.002*SL	0.030 + 0.003*SL	0.018 + 0.003*SL
	t_F	0.031	0.025 + 0.003*SL	0.024 + 0.003*SL	0.017 + 0.004*SL
	t_{PLH}	0.065	0.060 + 0.002*SL	0.063 + 0.002*SL	0.068 + 0.001*SL
	t_{PHL}	0.059	0.054 + 0.003*SL	0.057 + 0.002*SL	0.061 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 47, *Group3 : 47 < SL

nid4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.041	0.035 + 0.003*SL	0.039 + 0.002*SL	0.022 + 0.003*SL
	t_F	0.033	0.030 + 0.002*SL	0.027 + 0.002*SL	0.018 + 0.003*SL
	t_{PLH}	0.069	0.065 + 0.002*SL	0.068 + 0.001*SL	0.075 + 0.001*SL
	t_{PHL}	0.063	0.059 + 0.002*SL	0.062 + 0.001*SL	0.068 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nid6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.028 + 0.002*SL	0.029 + 0.002*SL	0.018 + 0.002*SL
	t_F	0.028	0.023 + 0.003*SL	0.027 + 0.002*SL	0.016 + 0.002*SL
	t_{PLH}	0.061	0.058 + 0.001*SL	0.060 + 0.001*SL	0.066 + 0.001*SL
	t_{PHL}	0.054	0.052 + 0.001*SL	0.053 + 0.001*SL	0.058 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 90, *Group3 : 90 < SL

nid8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.036 + 0.001*SL	0.037 + 0.001*SL	0.023 + 0.001*SL
	t_F	0.030	0.026 + 0.002*SL	0.030 + 0.001*SL	0.019 + 0.001*SL
	t_{PLH}	0.066	0.064 + 0.001*SL	0.065 + 0.001*SL	0.072 + 0.001*SL
	t_{PHL}	0.060	0.058 + 0.001*SL	0.059 + 0.001*SL	0.067 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

nid16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.032 + 0.002*SL	0.037 + 0.001*SL	0.022 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.027 + 0.001*SL	0.018 + 0.001*SL
	t_{PLH}	0.065	0.064 + 0.000*SL	0.064 + 0.000*SL	0.072 + 0.000*SL
	t_{PHL}	0.059	0.058 + 0.001*SL	0.059 + 0.000*SL	0.066 + 0.000*SL

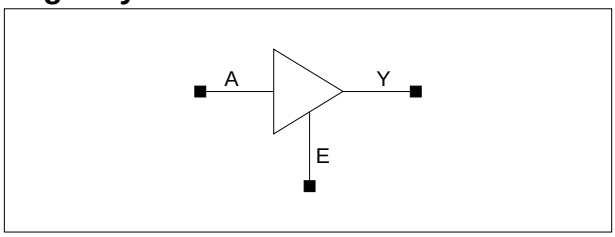
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 232, *Group3 : 232 < SL

nid24

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.033 + 0.001*SL	0.037 + 0.000*SL	0.023 + 0.000*SL
	t_F	0.028	0.026 + 0.001*SL	0.028 + 0.000*SL	0.019 + 0.000*SL
	t_{PLH}	0.065	0.064 + 0.000*SL	0.064 + 0.000*SL	0.073 + 0.000*SL
	t_{PHL}	0.059	0.058 + 0.000*SL	0.059 + 0.000*SL	0.067 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 345, *Group3 : 345 < SL

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)										Output Load (SL)				
nit		*nitd2*		*nitd4*		*nitd8*		*nitd16*		*nit*	*nitd2*	*nitd4*	*nitd8*	*nitd16*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
1.8	1.6	1.8	1.6	2.2	2.0	4.2	3.3	4.4	3.5	0.9	1.4	2.7	5.4	10.8

Gate Count				
nit	*nitd2*	*nitd4*	*nitd8*	*nitd16*
3.33	3.67	4.33	7.33	10.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nit

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.039	0.021 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.023 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.051	0.041 + 0.005*SL	0.043 + 0.005*SL	0.044 + 0.004*SL
	t_{PHL}	0.055	0.045 + 0.005*SL	0.049 + 0.004*SL	0.051 + 0.004*SL
E to Y	t_R	0.039	0.019 + 0.010*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.033	0.015 + 0.009*SL	0.019 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.052	0.042 + 0.005*SL	0.045 + 0.004*SL	0.045 + 0.004*SL
	t_{PHL}	0.069	0.059 + 0.005*SL	0.063 + 0.004*SL	0.065 + 0.004*SL
	t_{PLZ}	0.083	0.083 + 0.000*SL	0.083 + 0.000*SL	0.083 + 0.000*SL
	t_{PHZ}	0.065	0.064 + 0.000*SL	0.065 + 0.000*SL	0.065 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

nitd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.032	0.022 + 0.005*SL	0.024 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.032	0.022 + 0.005*SL	0.027 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.052	0.046 + 0.003*SL	0.049 + 0.002*SL	0.051 + 0.002*SL
	t_{PHL}	0.054	0.048 + 0.003*SL	0.050 + 0.002*SL	0.055 + 0.002*SL
E to Y	t_R	0.031	0.021 + 0.005*SL	0.021 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.025	0.015 + 0.005*SL	0.018 + 0.004*SL	0.014 + 0.004*SL
	t_{PLH}	0.052	0.045 + 0.003*SL	0.049 + 0.002*SL	0.052 + 0.002*SL
	t_{PHL}	0.065	0.058 + 0.003*SL	0.063 + 0.002*SL	0.068 + 0.002*SL
	t_{PLZ}	0.088	0.088 + 0.000*SL	0.088 + 0.000*SL	0.089 + 0.000*SL
	t_{PHZ}	0.076	0.076 + 0.000*SL	0.076 + 0.000*SL	0.076 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

nitd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.029	0.024 + 0.003*SL	0.024 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.033	0.030 + 0.002*SL	0.029 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.051	0.047 + 0.002*SL	0.050 + 0.001*SL	0.055 + 0.001*SL
	t_{PHL}	0.060	0.057 + 0.002*SL	0.059 + 0.001*SL	0.065 + 0.001*SL
E to Y	t_R	0.029	0.023 + 0.003*SL	0.025 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.023	0.018 + 0.002*SL	0.020 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.049	0.045 + 0.002*SL	0.048 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.069	0.064 + 0.002*SL	0.068 + 0.001*SL	0.078 + 0.001*SL
	t_{PLZ}	0.085	0.085 + 0.000*SL	0.086 + 0.000*SL	0.086 + 0.000*SL
	t_{PHZ}	0.093	0.093 + 0.000*SL	0.094 + 0.000*SL	0.096 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

nitd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.027	0.024 + 0.001*SL	0.025 + 0.001*SL	0.015 + 0.001*SL
	t_F	0.032	0.031 + 0.000*SL	0.030 + 0.001*SL	0.020 + 0.001*SL
	t_{PLH}	0.048	0.046 + 0.001*SL	0.048 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.057	0.056 + 0.001*SL	0.057 + 0.001*SL	0.063 + 0.001*SL
E to Y	t_R	0.027	0.024 + 0.001*SL	0.025 + 0.001*SL	0.015 + 0.001*SL
	t_F	0.020	0.018 + 0.001*SL	0.019 + 0.001*SL	0.020 + 0.001*SL
	t_{PLH}	0.047	0.045 + 0.001*SL	0.046 + 0.001*SL	0.054 + 0.001*SL
	t_{PHL}	0.076	0.074 + 0.001*SL	0.076 + 0.001*SL	0.088 + 0.001*SL
	t_{PLZ}	0.102	0.102 + 0.000*SL	0.102 + 0.000*SL	0.103 + 0.000*SL
	t_{PHZ}	0.092	0.092 + 0.000*SL	0.093 + 0.000*SL	0.095 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

nitd16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.034	0.033 + 0.001*SL	0.033 + 0.001*SL	0.027 + 0.001*SL
	t_F	0.048	0.047 + 0.000*SL	0.046 + 0.000*SL	0.031 + 0.000*SL
	t_{PLH}	0.063	0.061 + 0.001*SL	0.063 + 0.000*SL	0.077 + 0.000*SL
	t_{PHL}	0.075	0.074 + 0.000*SL	0.075 + 0.000*SL	0.083 + 0.000*SL
E to Y	t_R	0.037	0.035 + 0.001*SL	0.036 + 0.001*SL	0.027 + 0.001*SL
	t_F	0.027	0.026 + 0.001*SL	0.027 + 0.001*SL	0.030 + 0.000*SL
	t_{PLH}	0.060	0.059 + 0.001*SL	0.060 + 0.000*SL	0.076 + 0.000*SL
	t_{PHL}	0.087	0.086 + 0.001*SL	0.087 + 0.000*SL	0.106 + 0.000*SL
	t_{PLZ}	0.119	0.119 + 0.000*SL	0.119 + 0.000*SL	0.120 + 0.000*SL
	t_{PHZ}	0.134	0.133 + 0.000*SL	0.134 + 0.000*SL	0.139 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 232, *Group3 : 232 < SL

FLIP-FLOPS

Cell List

Cell Name	Function Description
fd1	D Flip-Flop with 1X Drive
fd1d2	D Flip-Flop with 2X Drive
fd1d4	D Flip-Flop with 4X Drive
fd1s	D Flip-Flop with Scan, 1X Drive
fd1sd2	D Flip-Flop with Scan, 2X Drive
fd1sd4	D Flip-Flop with Scan, 4X Drive
fd1sq	D Flip-Flop with Scan, Q Output Only, 1X Drive
fd1sqd2	D Flip-Flop with Scan, Q Output Only, 2X Drive
fd1sqd4	D Flip-Flop with Scan, Q Output Only, 4X Drive
fd1q	D Flip-Flop with Q Output Only, 1X Drive
fd1qd2	D Flip-Flop with Q Output Only, 2X Drive
fd1qd4	D Flip-Flop with Q Output Only, 4X Drive
fd2	D Flip-Flop with Reset, 1X Drive
fd2d2	D Flip-Flop with Reset, 2X Drive
fd2d4	D Flip-Flop with Reset, 4X Drive
fd2s	D Flip-Flop with Reset, Scan, 1X Drive
fd2sd2	D Flip-Flop with Reset, Scan, 2X Drive
fd2sd4	D Flip-Flop with Reset, Scan, 4X Drive
fd2sq	D Flip-Flop with Reset, Scan, Q Output Only, 1X Drive
fd2sqd2	D Flip-Flop with Reset, Scan, Q Output Only, 2X Drive
fd2sqd4	D Flip-Flop with Reset, Scan, Q Output Only, 4X Drive
fd2q	D Flip-Flop with Reset, Q Output Only, 1X Drive
fd2qd2	D Flip-Flop with Reset, Q Output Only, 2X Drive
fd2qd4	D Flip-Flop with Reset, Q Output Only, 4X Drive
fd3	D Flip-Flop with Set, 1X Drive
fd3d2	D Flip-Flop with Set, 2X Drive
fd3s	D Flip-Flop with Set, Scan, 1X Drive
fd3sd2	D Flip-Flop with Set, Scan, 2X Drive
fd3sq	D Flip-Flop with Set, Scan, Q Output Only, 1X Drive
fd3sqd2	D Flip-Flop with Set, Scan, Q Output Only, 2X Drive
fd3q	D Flip-Flop with Set, Q Output Only, 1X Drive
fd3qd2	D Flip-Flop with Set, Q Output Only, 2X Drive
fd4	D Flip-Flop with Reset, Set, 1X Drive
fd4d2	D Flip-Flop with Reset, Set, 2X Drive
fd4s	D Flip-Flop with Reset, Set, Scan, 1X Drive
fd4sd2	D Flip-Flop with Reset, Set, Scan, 2X Drive
fd4sq	D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X Drive
fd4sqd2	D Flip-Flop with Reset, Set, Scan, Q Output Only, 2X Drive

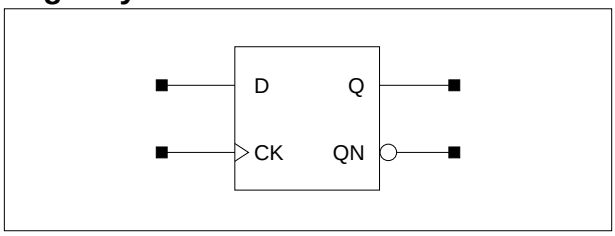
Cell List (Continued)

Cell Name	Function Description
fd4q	D Flip-Flop with Reset, Set, Q Output Only, 1X Drive
fd4qd2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
fd5	D Flip-Flop with Negative Edge Trigger, 1X Drive
fd5d2	D Flip-Flop with Negative Edge Trigger, 2X Drive
fd5s	D Flip-Flop with Negative Edge Trigger, Scan, 1X Drive
fd5sd2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
fd6	D Flip-Flop with Negative Edge Trigger, Reset, 1X Drive
fd6d2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
fd6s	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X Drive
fd6sd2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
fd7	D Flip-Flop with Negative Edge Trigger, Set, 1X Drive
fd7d2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
fd7s	D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X Drive
fd7sd2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
fd8	D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X Drive
fd8d2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
fd8s	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X Drive
fd8sd2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
fds2	D Flip-Flop with Synchronous Clear, 1X Drive
fds2d2	D Flip-Flop with Synchronous Clear, 2X Drive
fds2s	D Flip-Flop with Synchronous Clear, Scan, 1X Drive
fds2sd2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
fds3	D Flip-Flop with Synchronous Set, 1X Drive
fds3d2	D Flip-Flop with Synchronous Set, 2X Drive
fds3s	D Flip-Flop with Synchronous Set, Scan, 1X Drive
fds3sd2	D Flip-Flop with Synchronous Set, Scan, 2x Drive
fj2	JK Flip-Flop with Reset, 1X Drive
fj2d2	JK Flip-Flop with Reset, 2X Drive
fj2s	JK Flip-Flop with Reset, Scan, 1X Drive
fj2sd2	JK Flip-Flop with Reset, Scan, 2X Drive
fj4	JK Flip-Flop with Reset, Set, 1X Drive
fj4d2	JK Flip-Flop with Reset, Set, 2X Drive
fj4s	JK Flip-Flop with Reset, Set, Scan, 1X Drive
fj4sd2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
ft2	Toggle Flip-Flop with Reset, 1X Drive
ft2d2	Toggle Flip-Flop with Reset, 2X Drive

fd1/fd1d2/fd1d4

D Flip-Flop with 1X/2X/4X Drive

Logic Symbol



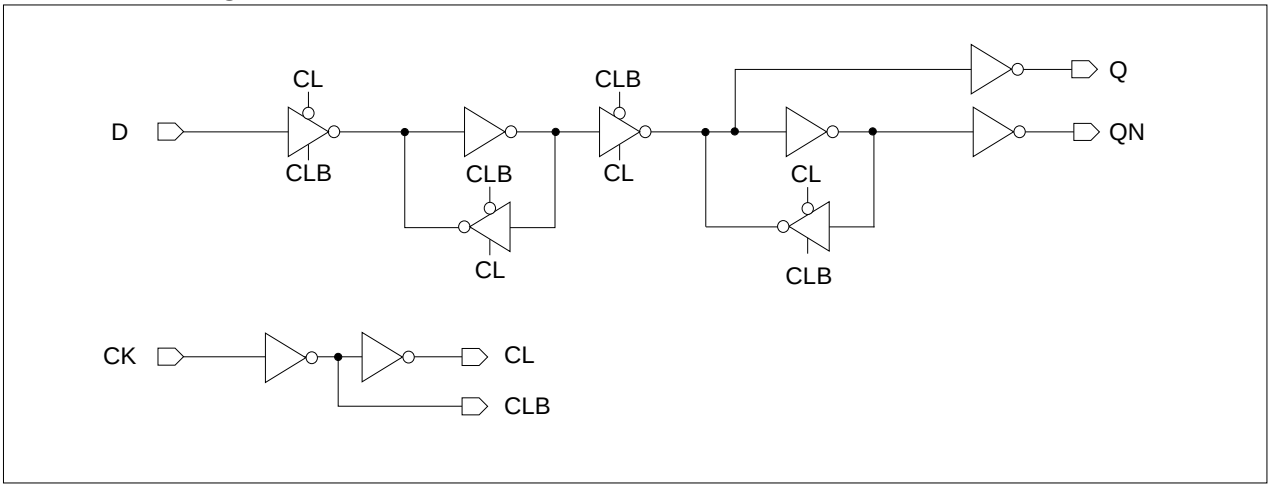
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count		
fd1		*fd1d2*		*fd1d4*		*fd1*	*fd1d2*	*fd1d4*
D	CK	D	CK	D	CK			
0.7	1.1	0.7	1.1	0.7	1.0	6.33	7.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd1	fd1d2	fd1d4
Input Setup Time (D to CK)	t_{SU}	0.051	0.051	0.052
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.100	0.100	0.100
Pulse Width High (CK)	t_{PWH}	0.069	0.092	0.066

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.048	0.028 + 0.010*SL	0.029 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.050	0.032 + 0.009*SL	0.040 + 0.007*SL	0.033 + 0.008*SL
	t_{PLH}	0.110	0.097 + 0.006*SL	0.103 + 0.005*SL	0.108 + 0.004*SL
	t_{PHL}	0.101	0.086 + 0.007*SL	0.096 + 0.005*SL	0.108 + 0.004*SL
CK to QN	t_R	0.043	0.027 + 0.008*SL	0.019 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.020 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.125	0.115 + 0.005*SL	0.117 + 0.005*SL	0.118 + 0.004*SL
	t_{PHL}	0.138	0.128 + 0.005*SL	0.132 + 0.004*SL	0.134 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd1d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.049	0.041 + 0.004*SL	0.041 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.111	0.103 + 0.004*SL	0.108 + 0.003*SL	0.117 + 0.002*SL
	t_{PHL}	0.105	0.096 + 0.004*SL	0.103 + 0.003*SL	0.123 + 0.002*SL
CK to QN	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.142	0.136 + 0.003*SL	0.140 + 0.002*SL	0.142 + 0.002*SL
	t_{PHL}	0.150	0.143 + 0.003*SL	0.148 + 0.002*SL	0.153 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd1d4

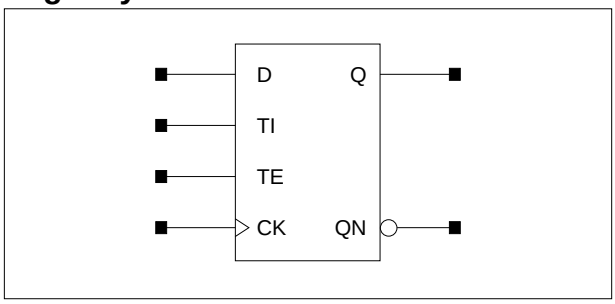
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.031	0.028 + 0.002*SL	0.026 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.164	0.161 + 0.002*SL	0.163 + 0.001*SL	0.168 + 0.001*SL
	t_{PHL}	0.151	0.147 + 0.002*SL	0.150 + 0.001*SL	0.158 + 0.001*SL
CK to QN	t_R	0.035	0.030 + 0.002*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.135	0.131 + 0.002*SL	0.134 + 0.001*SL	0.138 + 0.001*SL
	t_{PHL}	0.141	0.138 + 0.002*SL	0.141 + 0.001*SL	0.149 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

fd1s/fd1sd2/fd1sd4

D Flip-Flop with Scan, 1X/2X/4X Drive

Logic Symbol



Truth Table

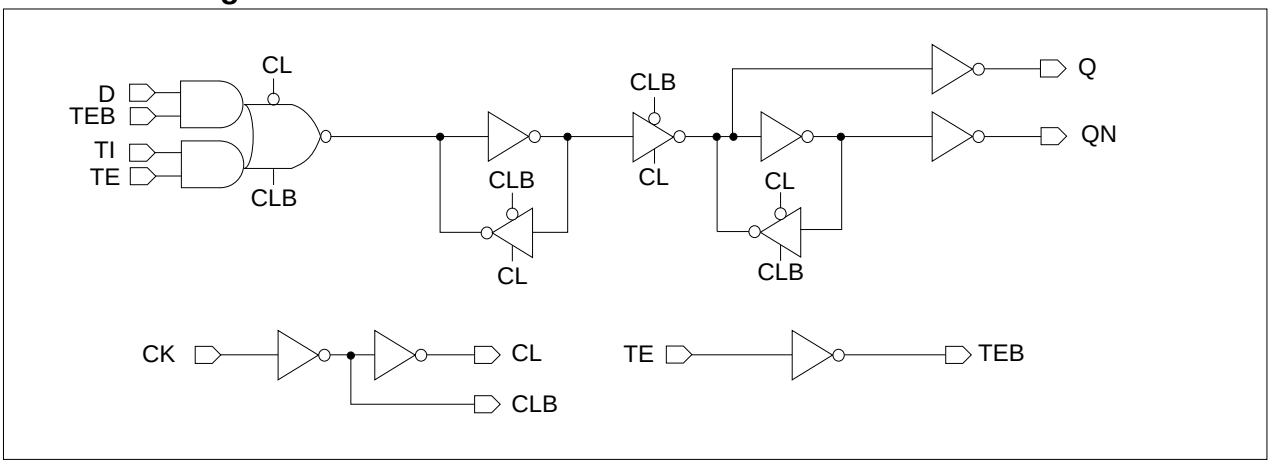
D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0
x	x	x	↓	Q(n)	QN(n)

Cell Data

Input Load (SL)											
fd1s				*fd1sd2*				*fd1sd4*			
D	CK	TI	TE	D	CK	TI	TE	D	CK	TI	TE
0.5	1.0	0.6	1.1	0.5	1.0	0.6	1.1	0.5	1.0	0.6	1.1

Gate Count		
fd1s	*fd1sd2*	*fd1sd4*
8.67	9.33	11.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd1s	fd1sd2	fd1sd4
Input Setup Time (D to CK)	t_{SU}	0.146	0.144	0.151
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TI to CK)	t_{SU}	0.172	0.170	0.177
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.171	0.169	0.177
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.173	0.171	0.176
Pulse Width High (CK)	t_{PWH}	0.067	0.091	0.070

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd1s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.026 + 0.010*SL	0.025 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.048	0.029 + 0.009*SL	0.037 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.109	0.097 + 0.006*SL	0.102 + 0.005*SL	0.106 + 0.004*SL
	t_{PHL}	0.098	0.084 + 0.007*SL	0.093 + 0.005*SL	0.105 + 0.004*SL
CK to QN	t_R	0.043	0.025 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.020 + 0.008*SL	0.019 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.122	0.112 + 0.005*SL	0.115 + 0.005*SL	0.115 + 0.004*SL
	t_{PHL}	0.137	0.127 + 0.005*SL	0.131 + 0.004*SL	0.133 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd1sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.028 + 0.005*SL	0.029 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.047	0.038 + 0.004*SL	0.040 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.004*SL	0.106 + 0.003*SL	0.114 + 0.002*SL
	t_{PHL}	0.104	0.096 + 0.004*SL	0.102 + 0.003*SL	0.122 + 0.002*SL
CK to QN	t_R	0.038	0.028 + 0.005*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.144	0.138 + 0.003*SL	0.142 + 0.002*SL	0.144 + 0.002*SL
	t_{PHL}	0.150	0.144 + 0.003*SL	0.148 + 0.002*SL	0.154 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd1sd4

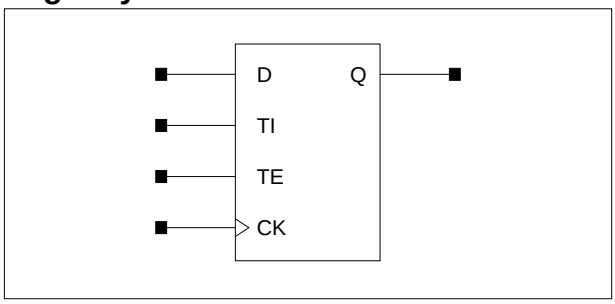
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.032	0.027 + 0.002*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.168	0.165 + 0.002*SL	0.167 + 0.001*SL	0.172 + 0.001*SL
	t_{PHL}	0.156	0.152 + 0.002*SL	0.155 + 0.001*SL	0.163 + 0.001*SL
CK to QN	t_R	0.037	0.033 + 0.002*SL	0.031 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.140	0.137 + 0.002*SL	0.139 + 0.001*SL	0.144 + 0.001*SL
	t_{PHL}	0.146	0.142 + 0.002*SL	0.145 + 0.001*SL	0.153 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

fd1sq/fd1sqd2/fd1sqd4

D Flip-Flop with Scan, Q Output Only, 1X/2X/4X Drive

Logic Symbol



Truth Table

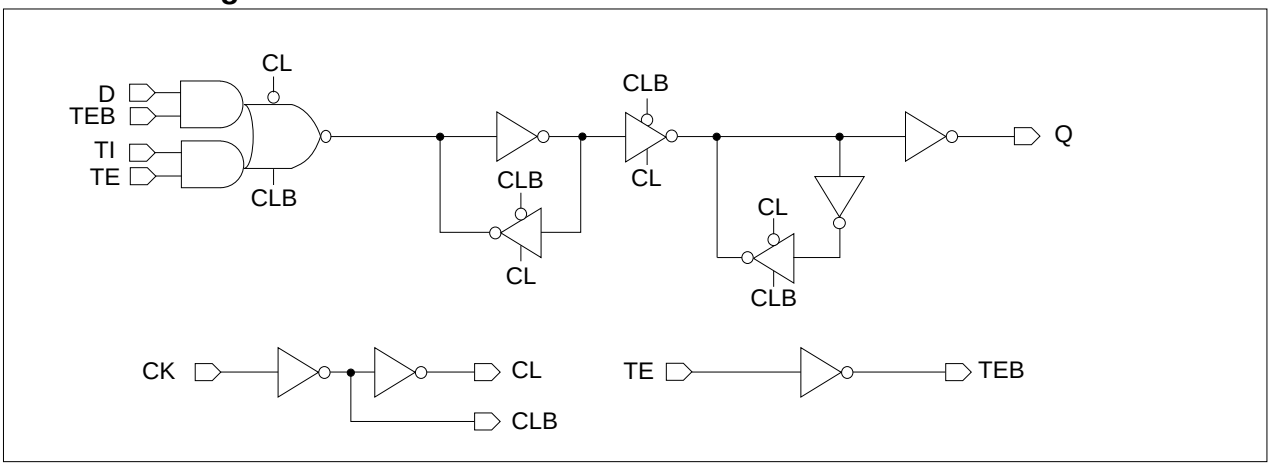
D	TI	TE	CK	Q (n+1)
0	x	0	↑	0
1	x	0	↑	1
x	0	1	↑	0
x	1	1	↑	1
x	x	x	↓	Q(n)

Cell Data

Input Load (SL)											
fd1sq				*fd1sqd2*				*fd1sqd4*			
D	CK	TI	TE	D	CK	TI	TE	D	CK	TI	TE
0.5	1.0	0.6	1.1	0.5	1.0	0.6	1.1	0.5	1.0	0.6	1.1

Gate Count		
fd1sq	*fd1sqd2*	*fd1sqd4*
8.33	8.67	9.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd1sq	fd1sqd2	fd1sqd4
Input Setup Time (D to CK)	t_{SU}	0.144	0.143	0.145
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TI to CK)	t_{SU}	0.170	0.167	0.170
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.169	0.166	0.169
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.172	0.172	0.172
Pulse Width High (CK)	t_{PWH}	0.055	0.073	0.048

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd1sq

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.025 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.047	0.029 + 0.009*SL	0.035 + 0.007*SL	0.027 + 0.008*SL
	t_{PLH}	0.105	0.093 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.092	0.079 + 0.007*SL	0.087 + 0.005*SL	0.096 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd1sqd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.039	0.030 + 0.005*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.038 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.106	0.099 + 0.004*SL	0.103 + 0.002*SL	0.110 + 0.002*SL
	t_{PHL}	0.100	0.091 + 0.004*SL	0.098 + 0.003*SL	0.114 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd1sqd4

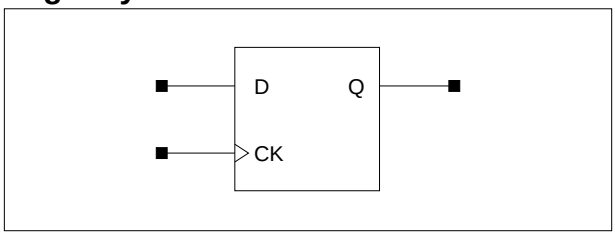
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.153	0.150 + 0.002*SL	0.152 + 0.001*SL	0.157 + 0.001*SL
	t_{PHL}	0.133	0.130 + 0.002*SL	0.132 + 0.001*SL	0.141 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

fd1q/fd1qd2/fd1qd4

D Flip-Flop with Q Output Only, 1X/2X/4X Drive

Logic Symbol



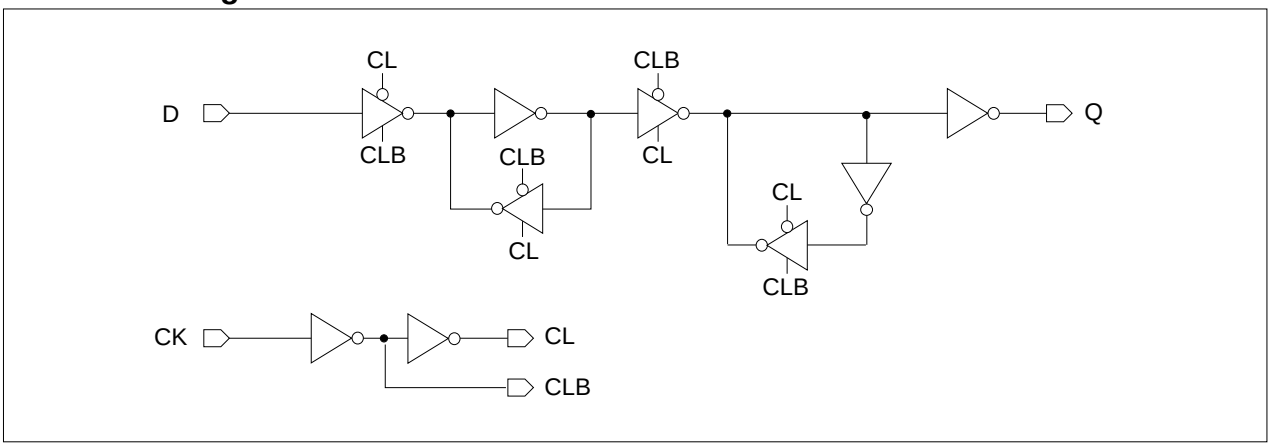
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)					
fd1q		*fd1qd2*		*fd1qd4*	
D	CK	D	CK	D	CK
0.7	1.0	0.7	1.1	0.7	1.0
Gate Count					
fd1q		*fd1qd2*		*fd1qd4*	
5.67		6.33		7.33	

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd1q	fd1qd2	fd1qd4
Input Setup Time (D to CK)	t_{SU}	0.052	0.052	0.052
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.100	0.101	0.101
Pulse Width High (CK)	t_{PWH}	0.056	0.072	0.047

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd1q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.045	0.025 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.047	0.029 + 0.009*SL	0.035 + 0.008*SL	0.029 + 0.008*SL
	t_{PLH}	0.104	0.093 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.092	0.079 + 0.007*SL	0.087 + 0.005*SL	0.096 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd1qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.041	0.031 + 0.005*SL	0.031 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.046	0.037 + 0.005*SL	0.040 + 0.004*SL	0.038 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.003*SL	0.105 + 0.002*SL	0.112 + 0.002*SL
	t_{PHL}	0.100	0.092 + 0.004*SL	0.098 + 0.003*SL	0.114 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd1qd4

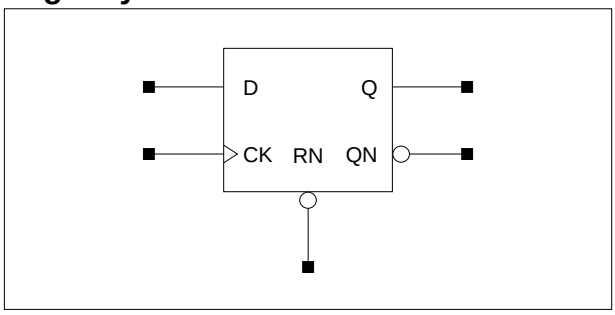
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.032	0.026 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.026 + 0.002*SL	0.019 + 0.002*SL
	t_{PLH}	0.153	0.149 + 0.002*SL	0.151 + 0.001*SL	0.156 + 0.001*SL
	t_{PHL}	0.131	0.128 + 0.002*SL	0.130 + 0.001*SL	0.139 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

fd2/fd2d2/fd2d4

D Flip-Flop with Reset, 1X/2X/4X Drive

Logic Symbol



Truth Table

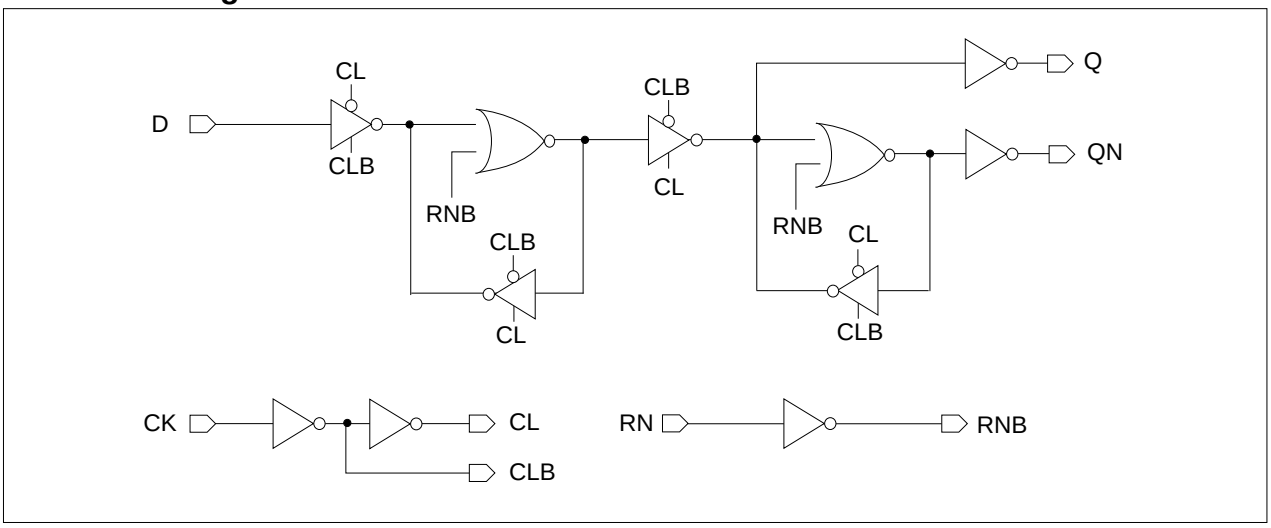
D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								
fd2			*fd2d2*			*fd2d4*		
D	CK	RN	D	CK	RN	D	CK	RN
0.7	1.0	1.0	0.7	1.0	1.0	0.7	1.0	1.0

Gate Count		
fd2	*fd2d2*	*fd2d4*
7.67	8.67	11.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd2	fd2d2	fd2d4
Input Setup Time (D to CK)	t_{SU}	0.052	0.051	0.052
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.096	0.097	0.096
Pulse Width High (CK)	t_{PWH}	0.070	0.094	0.069
Pulse Width Low (RN)	t_{PWL}	0.159	0.192	0.166
Recovery Time (RN to CK)	t_{RC}	0.030	0.028	0.029
Removal Time (RN to CK)	t_{RM}	0.010	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.026 + 0.010*SL	0.026 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.050	0.032 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.110	0.098 + 0.006*SL	0.103 + 0.005*SL	0.107 + 0.005*SL
	t_{PHL}	0.101	0.086 + 0.007*SL	0.096 + 0.005*SL	0.108 + 0.004*SL
RN to Q	t_F	0.094	0.074 + 0.010*SL	0.082 + 0.008*SL	0.088 + 0.008*SL
	t_{PHL}	0.290	0.272 + 0.009*SL	0.284 + 0.006*SL	0.313 + 0.005*SL
CK to QN	t_R	0.043	0.026 + 0.009*SL	0.020 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.042	0.027 + 0.008*SL	0.027 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.127	0.117 + 0.005*SL	0.120 + 0.005*SL	0.120 + 0.004*SL
	t_{PHL}	0.154	0.143 + 0.006*SL	0.148 + 0.004*SL	0.154 + 0.004*SL
RN to QN	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.014 + 0.010*SL
	t_{PLH}	0.090	0.080 + 0.005*SL	0.082 + 0.005*SL	0.083 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.049	0.041 + 0.004*SL	0.041 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.112	0.105 + 0.004*SL	0.110 + 0.002*SL	0.117 + 0.002*SL
	t_{PHL}	0.106	0.097 + 0.004*SL	0.104 + 0.003*SL	0.124 + 0.002*SL
RN to Q	t_F	0.118	0.111 + 0.004*SL	0.110 + 0.004*SL	0.119 + 0.004*SL
	t_{PHL}	0.341	0.330 + 0.006*SL	0.338 + 0.004*SL	0.374 + 0.003*SL
CK to QN	t_R	0.038	0.029 + 0.005*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.040	0.031 + 0.005*SL	0.034 + 0.004*SL	0.028 + 0.004*SL
	t_{PLH}	0.148	0.142 + 0.003*SL	0.145 + 0.002*SL	0.148 + 0.002*SL
	t_{PHL}	0.172	0.165 + 0.004*SL	0.170 + 0.002*SL	0.182 + 0.002*SL
RN to QN	t_R	0.033	0.024 + 0.004*SL	0.022 + 0.005*SL	0.015 + 0.005*SL
	t_{PLH}	0.091	0.085 + 0.003*SL	0.088 + 0.002*SL	0.090 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

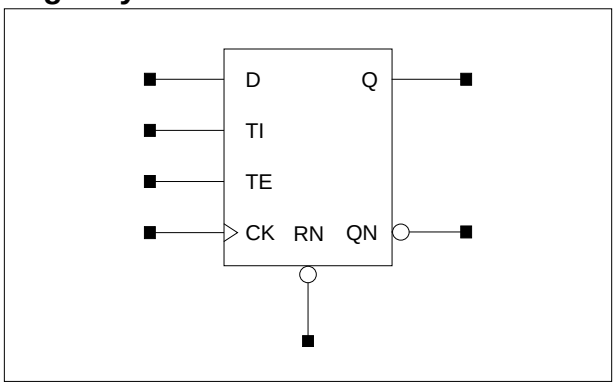
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.034	0.030 + 0.002*SL	0.028 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.183	0.180 + 0.002*SL	0.182 + 0.001*SL	0.187 + 0.001*SL
	t_{PHL}	0.154	0.151 + 0.002*SL	0.154 + 0.001*SL	0.161 + 0.001*SL
RN to Q	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PHL}	0.118	0.114 + 0.002*SL	0.117 + 0.001*SL	0.125 + 0.001*SL
CK to QN	t_R	0.035	0.031 + 0.002*SL	0.031 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.142 + 0.001*SL
	t_{PHL}	0.143	0.140 + 0.002*SL	0.143 + 0.001*SL	0.150 + 0.001*SL
RN to QN	t_R	0.053	0.048 + 0.002*SL	0.049 + 0.002*SL	0.031 + 0.002*SL
	t_{PLH}	0.350	0.346 + 0.002*SL	0.350 + 0.001*SL	0.359 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

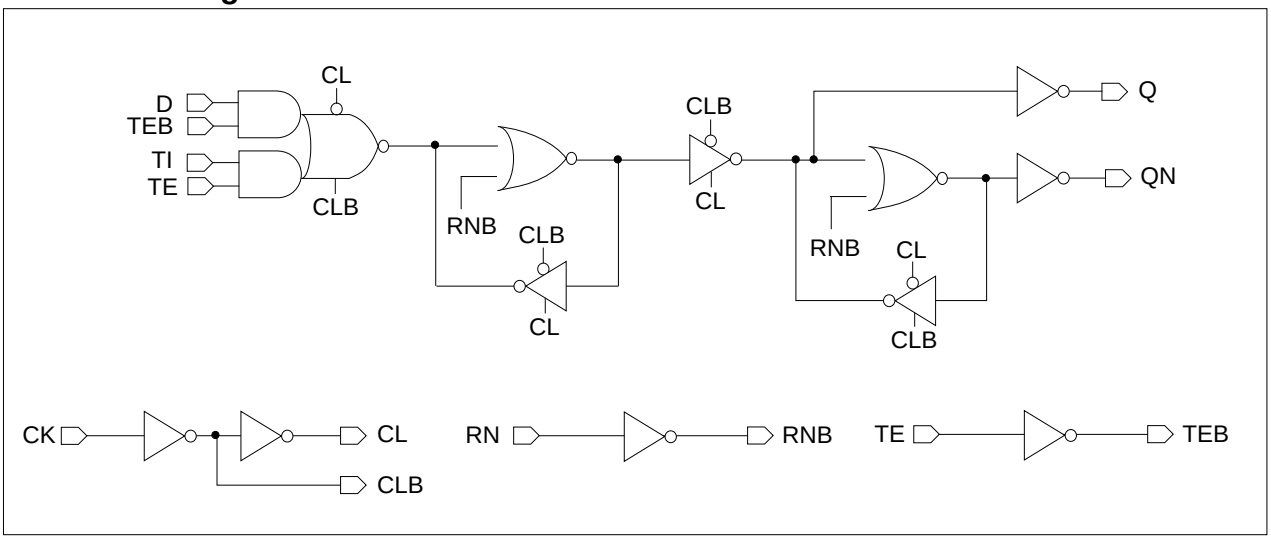
D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1
x	x	x	↓	1	Q(n)	QN(n)

Cell Data

Input Load (SL)														
fd2s					*fd2sd2*					*fd2sd4*				
D	CK	RN	TI	TE	D	CK	RN	TI	TE	D	CK	RN	TI	TE
0.5	1.0	1.0	0.6	1.1	0.5	1.0	1.0	0.6	1.1	0.5	1.0	1.0	0.6	1.1

Gate Count		
fd2s	*fd2sd2*	*fd2sd4*
10.00	10.67	13.33

Schematic Diagram



fd2s/fd2sd2/fd2sd4

D Flip-Flop with Reset, Scan, 1X/2X/4X Drive

Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd2s	fd2sd2	fd2sd4
Input Setup Time (D to CK)	t_{SU}	0.137	0.148	0.142
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TI to CK)	t_{SU}	0.163	0.174	0.167
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.161	0.173	0.167
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.172	0.181	0.178
Pulse Width High (CK)	t_{PWH}	0.073	0.097	0.070
Pulse Width Low (RN)	t_{PWL}	0.170	0.206	0.170
Recovery Time (RN to CK)	t_{RC}	0.030	0.027	0.031
Removal Time (RN to CK)	t_{RM}	0.010	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.047	0.027 + 0.010*SL	0.027 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.052	0.035 + 0.008*SL	0.039 + 0.008*SL	0.034 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.104	0.090 + 0.007*SL	0.099 + 0.005*SL	0.112 + 0.004*SL
RN to Q	t_F	0.096	0.079 + 0.009*SL	0.082 + 0.008*SL	0.090 + 0.008*SL
	t_{PHL}	0.292	0.273 + 0.009*SL	0.285 + 0.006*SL	0.314 + 0.005*SL
CK to QN	t_R	0.043	0.026 + 0.009*SL	0.021 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.042	0.026 + 0.008*SL	0.026 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.130	0.120 + 0.005*SL	0.123 + 0.005*SL	0.123 + 0.004*SL
	t_{PHL}	0.155	0.143 + 0.006*SL	0.149 + 0.004*SL	0.155 + 0.004*SL
RN to QN	t_R	0.040	0.022 + 0.009*SL	0.017 + 0.010*SL	0.013 + 0.010*SL
	t_{PLH}	0.090	0.080 + 0.005*SL	0.082 + 0.005*SL	0.083 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.051	0.043 + 0.004*SL	0.043 + 0.004*SL	0.044 + 0.004*SL
	t_{PLH}	0.113	0.105 + 0.004*SL	0.110 + 0.002*SL	0.118 + 0.002*SL
	t_{PHL}	0.109	0.100 + 0.004*SL	0.107 + 0.003*SL	0.128 + 0.002*SL
RN to Q	t_F	0.119	0.112 + 0.004*SL	0.110 + 0.004*SL	0.121 + 0.004*SL
	t_{PHL}	0.337	0.326 + 0.006*SL	0.334 + 0.004*SL	0.370 + 0.003*SL
CK to QN	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.040	0.032 + 0.004*SL	0.034 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.152	0.145 + 0.003*SL	0.149 + 0.002*SL	0.152 + 0.002*SL
	t_{PHL}	0.173	0.166 + 0.004*SL	0.171 + 0.002*SL	0.183 + 0.002*SL
RN to QN	t_R	0.033	0.024 + 0.004*SL	0.022 + 0.005*SL	0.014 + 0.005*SL
	t_{PLH}	0.090	0.084 + 0.003*SL	0.087 + 0.002*SL	0.090 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd2sd4

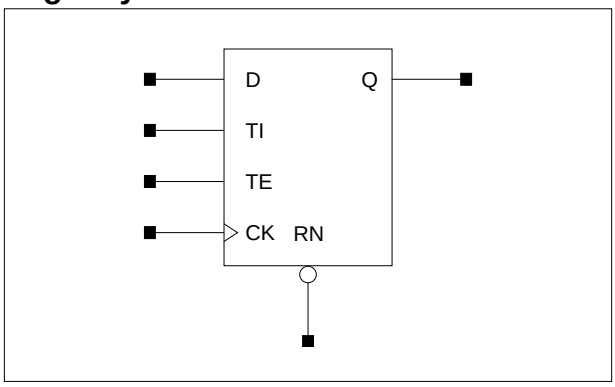
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.034	0.029 + 0.002*SL	0.030 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.185	0.181 + 0.002*SL	0.184 + 0.001*SL	0.189 + 0.001*SL
	t_{PHL}	0.157	0.154 + 0.002*SL	0.156 + 0.001*SL	0.164 + 0.001*SL
RN to Q	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.019 + 0.002*SL
	t_{PHL}	0.119	0.116 + 0.002*SL	0.118 + 0.001*SL	0.127 + 0.001*SL
CK to QN	t_R	0.037	0.033 + 0.002*SL	0.032 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.027 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.139	0.135 + 0.002*SL	0.137 + 0.001*SL	0.142 + 0.001*SL
	t_{PHL}	0.142	0.138 + 0.002*SL	0.141 + 0.001*SL	0.150 + 0.001*SL
RN to QN	t_R	0.053	0.048 + 0.003*SL	0.050 + 0.002*SL	0.031 + 0.002*SL
	t_{PLH}	0.340	0.336 + 0.002*SL	0.339 + 0.001*SL	0.349 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

fd2sq/fd2sqd2/fd2sqd4

D Flip-Flop with Reset, Scan, Q Output Only, 1X/2X/4X Drive

Logic Symbol



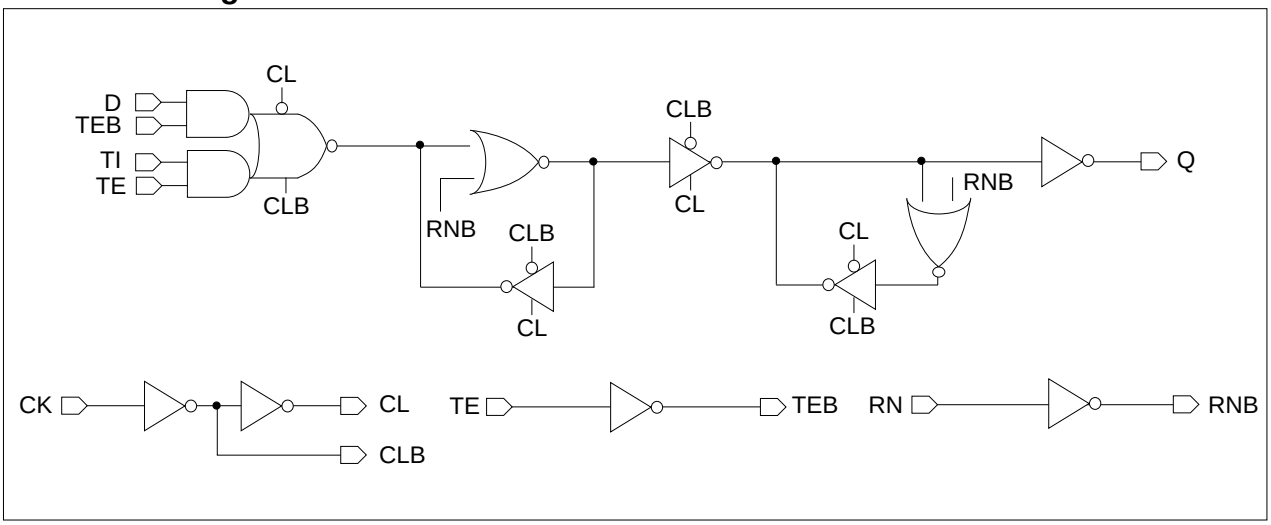
Truth Table

D	TI	TE	CK	RN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	0
x	x	x	↓	1	Q(n)

Cell Data

Input Load (SL)														
fd2sq					*fd2sqd2*					*fd2sqd4*				
D	CK	RN	TI	TE	D	CK	RN	TI	TE	D	CK	RN	TI	TE
0.5	1.0	1.0	0.6	1.1	0.5	1.0	1.0	0.6	1.1	0.5	1.0	1.0	0.6	1.1
Gate Count														
fd2sq					*fd2sqd2*					*fd2sqd4*				
9.33					10.00					11.00				

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd2sq	fd2sqd2	fd2sqd4
Input Setup Time (D to CK)	t_{SU}	0.145	0.147	0.148
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TI to CK)	t_{SU}	0.172	0.173	0.173
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.168	0.172	0.173
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.178	0.177	0.180
Pulse Width High (CK)	t_{PWH}	0.057	0.072	0.050
Pulse Width Low (RN)	t_{PWL}	0.123	0.160	0.120
Recovery Time (RN to CK)	t_{RC}	0.022	0.024	0.027
Removal Time (RN to CK)	t_{RM}	0.010	0.010	0.010

fd2sq/fd2sqd2/fd2sqd4

D Flip-Flop with Reset, Scan, Q Output Only, 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2sq

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.045	0.024 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.049	0.031 + 0.009*SL	0.036 + 0.007*SL	0.029 + 0.008*SL
	t_{PLH}	0.107	0.095 + 0.006*SL	0.099 + 0.005*SL	0.103 + 0.004*SL
	t_{PHL}	0.096	0.082 + 0.007*SL	0.091 + 0.005*SL	0.100 + 0.004*SL
RN to Q	t_F	0.089	0.071 + 0.009*SL	0.076 + 0.008*SL	0.081 + 0.008*SL
	t_{PHL}	0.246	0.228 + 0.009*SL	0.240 + 0.006*SL	0.266 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd2sqd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.028 + 0.005*SL	0.028 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.045	0.036 + 0.005*SL	0.039 + 0.004*SL	0.037 + 0.004*SL
	t_{PLH}	0.107	0.100 + 0.003*SL	0.104 + 0.002*SL	0.111 + 0.002*SL
	t_{PHL}	0.101	0.093 + 0.004*SL	0.099 + 0.003*SL	0.116 + 0.002*SL
RN to Q	t_F	0.111	0.104 + 0.003*SL	0.102 + 0.004*SL	0.110 + 0.004*SL
	t_{PHL}	0.283	0.272 + 0.005*SL	0.280 + 0.004*SL	0.314 + 0.002*SL

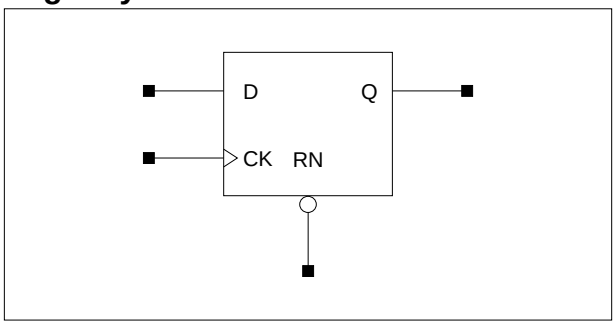
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd2sqd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.033	0.028 + 0.003*SL	0.029 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.167	0.164 + 0.002*SL	0.166 + 0.001*SL	0.171 + 0.001*SL
	t_{PHL}	0.136	0.132 + 0.002*SL	0.135 + 0.001*SL	0.143 + 0.001*SL
RN to Q	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PHL}	0.118	0.115 + 0.002*SL	0.117 + 0.001*SL	0.126 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



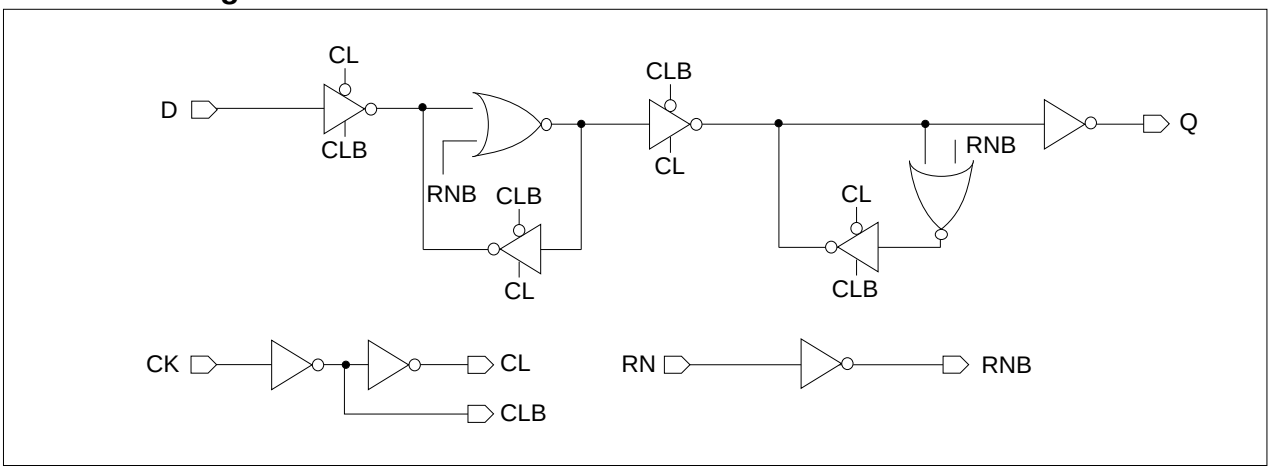
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)									Gate Count		
fd2q			*fd2qd2*			*fd2qd4*			*fd2q*	*fd2qd2*	*fd2qd4*
D	CK	RN	D	CK	RN	D	CK	RN			
0.7	1.0	1.0	0.7	1.0	1.0	0.7	1.0	1.0	7.33	7.67	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		fd2q	fd2qd2	fd2qd4
Input Setup Time (D to CK)	t_{SU}	0.052	0.051	0.052
Input Hold Time (D to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.096	0.095	0.096
Pulse Width High (CK)	t_{PWH}	0.055	0.071	0.047
Pulse Width Low (RN)	t_{PWL}	0.121	0.157	0.113
Recovery Time (RN to CK)	t_{RC}	0.026	0.026	0.029
Removal Time (RN to CK)	t_{RM}	0.010	0.010	0.010

fd2q/fd2qd2/fd2qd4

D Flip-Flop with Reset, Q Output Only, 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd2q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.024 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.048	0.030 + 0.009*SL	0.035 + 0.007*SL	0.028 + 0.008*SL
	t_{PLH}	0.106	0.095 + 0.006*SL	0.098 + 0.005*SL	0.102 + 0.004*SL
	t_{PHL}	0.093	0.079 + 0.007*SL	0.088 + 0.005*SL	0.097 + 0.004*SL
RN to Q	t_F	0.089	0.072 + 0.008*SL	0.075 + 0.008*SL	0.080 + 0.008*SL
	t_{PHL}	0.248	0.230 + 0.009*SL	0.242 + 0.006*SL	0.267 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd2qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.028 + 0.005*SL	0.028 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.046	0.037 + 0.004*SL	0.039 + 0.004*SL	0.037 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.003*SL	0.105 + 0.002*SL	0.111 + 0.002*SL
	t_{PHL}	0.099	0.090 + 0.004*SL	0.097 + 0.003*SL	0.113 + 0.002*SL
RN to Q	t_F	0.112	0.105 + 0.003*SL	0.102 + 0.004*SL	0.110 + 0.004*SL
	t_{PHL}	0.287	0.277 + 0.005*SL	0.284 + 0.003*SL	0.318 + 0.002*SL

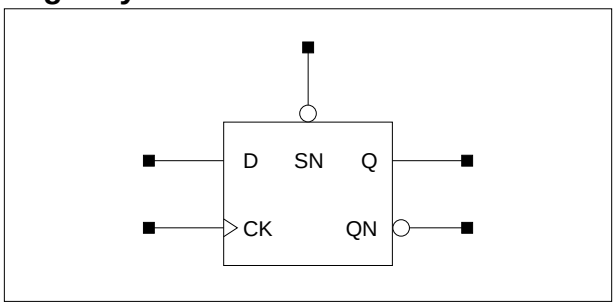
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd2qd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.034	0.028 + 0.003*SL	0.030 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.030	0.025 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.169	0.165 + 0.002*SL	0.168 + 0.001*SL	0.172 + 0.001*SL
	t_{PHL}	0.136	0.132 + 0.002*SL	0.135 + 0.001*SL	0.143 + 0.001*SL
RN to Q	t_F	0.029	0.026 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PHL}	0.125	0.121 + 0.002*SL	0.124 + 0.001*SL	0.132 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



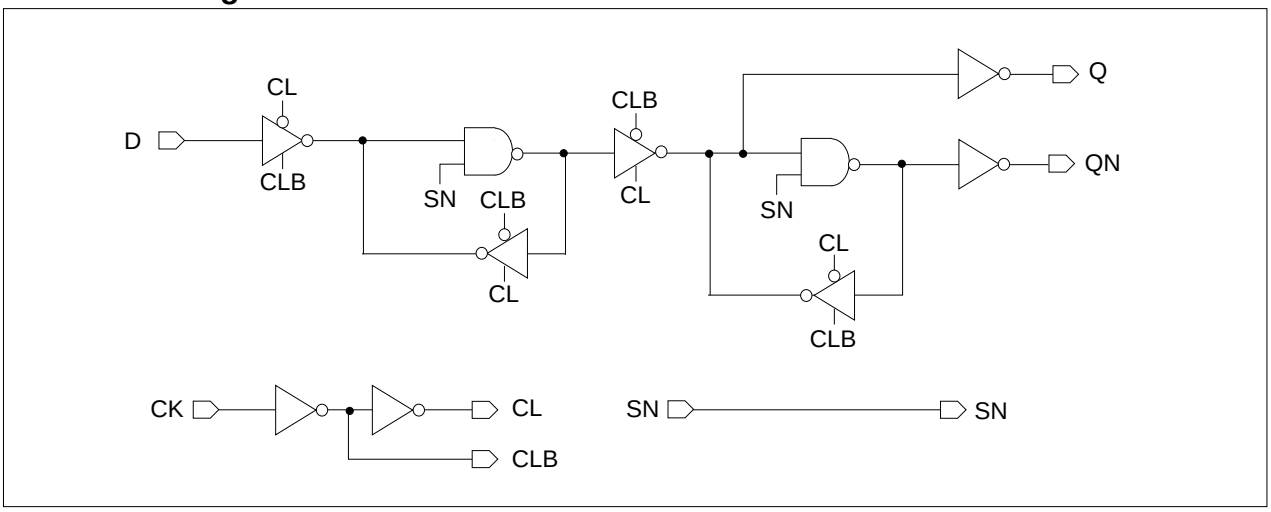
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
fd3			*fd3d2*			*fd3*	*fd3d2*
D	CK	SN	D	CK	SN		
0.7	1.0	2.0	0.7	1.0	2.2	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd3	fd3d2
Input Setup Time (D to CK)	t_{SU}	0.051	0.051
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.101	0.101
Pulse Width High (CK)	t_{PWH}	0.070	0.094
Pulse Width Low (SN)	t_{PWL}	0.107	0.131
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.072	0.071

fd3/fd3d2

D Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.026 + 0.010*SL	0.027 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.048	0.031 + 0.009*SL	0.035 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.109	0.098 + 0.006*SL	0.102 + 0.005*SL	0.106 + 0.004*SL
	t_{PHL}	0.097	0.083 + 0.007*SL	0.091 + 0.005*SL	0.104 + 0.004*SL
SN to Q	t_R	0.072	0.053 + 0.010*SL	0.054 + 0.009*SL	0.045 + 0.010*SL
	t_{PLH}	0.181	0.166 + 0.008*SL	0.175 + 0.005*SL	0.189 + 0.005*SL
CK to QN	t_R	0.047	0.030 + 0.009*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.037	0.022 + 0.007*SL	0.020 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.131	0.120 + 0.005*SL	0.124 + 0.005*SL	0.126 + 0.004*SL
	t_{PHL}	0.143	0.132 + 0.005*SL	0.136 + 0.004*SL	0.139 + 0.004*SL
SN to QN	t_F	0.038	0.022 + 0.008*SL	0.022 + 0.008*SL	0.018 + 0.008*SL
	t_{PHL}	0.067	0.056 + 0.005*SL	0.060 + 0.004*SL	0.064 + 0.004*SL

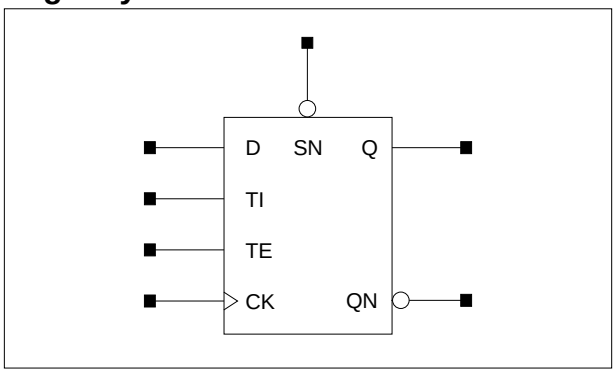
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd3d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.039 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.112	0.105 + 0.004*SL	0.110 + 0.003*SL	0.118 + 0.002*SL
	t_{PHL}	0.105	0.096 + 0.004*SL	0.103 + 0.003*SL	0.123 + 0.002*SL
SN to Q	t_R	0.077	0.068 + 0.004*SL	0.066 + 0.005*SL	0.063 + 0.005*SL
	t_{PLH}	0.207	0.198 + 0.005*SL	0.204 + 0.003*SL	0.227 + 0.002*SL
CK to QN	t_R	0.041	0.032 + 0.004*SL	0.030 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.031	0.022 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.149	0.142 + 0.003*SL	0.146 + 0.002*SL	0.151 + 0.002*SL
	t_{PHL}	0.151	0.145 + 0.003*SL	0.149 + 0.002*SL	0.155 + 0.002*SL
SN to QN	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.018 + 0.004*SL
	t_{PHL}	0.063	0.057 + 0.003*SL	0.060 + 0.002*SL	0.066 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



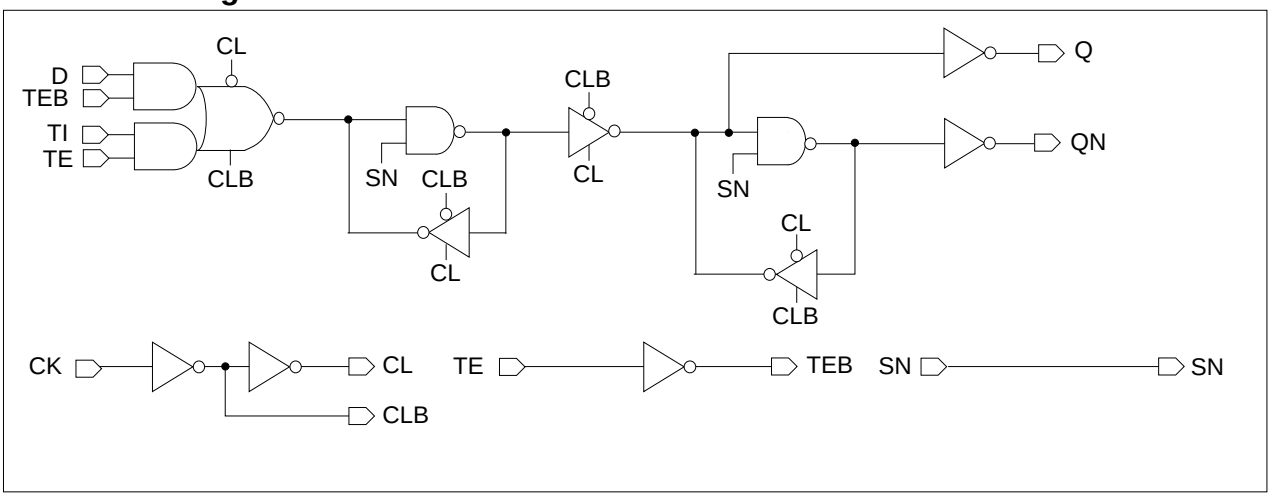
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
fd3s					*fd3sd2*					*fd3s*	*fd3sd2*
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.5	1.0	2.2	0.5	1.1	0.5	1.0	2.2	0.6	1.1	9.00	9.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd3s	fd3sd2
Input Setup Time (D to CK)	t_{SU}	0.158	0.164
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.187	0.191
Pulse Width High (CK)	t_{PWH}	0.072	0.095
Pulse Width Low (SN)	t_{PWL}	0.108	0.134
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.064	0.064
Input Setup Time (TI to CK)	t_{SU}	0.183	0.190
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.180	0.187
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd3s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.047	0.028 + 0.010*SL	0.027 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.050	0.032 + 0.009*SL	0.039 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.105 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.102	0.088 + 0.007*SL	0.097 + 0.005*SL	0.110 + 0.004*SL
SN to Q	t_R	0.073	0.052 + 0.011*SL	0.057 + 0.009*SL	0.045 + 0.010*SL
	t_{PLH}	0.182	0.166 + 0.008*SL	0.176 + 0.005*SL	0.190 + 0.005*SL
CK to QN	t_R	0.045	0.027 + 0.009*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.035	0.019 + 0.008*SL	0.021 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.132	0.121 + 0.005*SL	0.124 + 0.005*SL	0.125 + 0.004*SL
	t_{PHL}	0.140	0.129 + 0.005*SL	0.133 + 0.004*SL	0.135 + 0.004*SL
SN to QN	t_F	0.036	0.020 + 0.008*SL	0.020 + 0.008*SL	0.016 + 0.008*SL
	t_{PHL}	0.062	0.052 + 0.005*SL	0.055 + 0.004*SL	0.058 + 0.004*SL

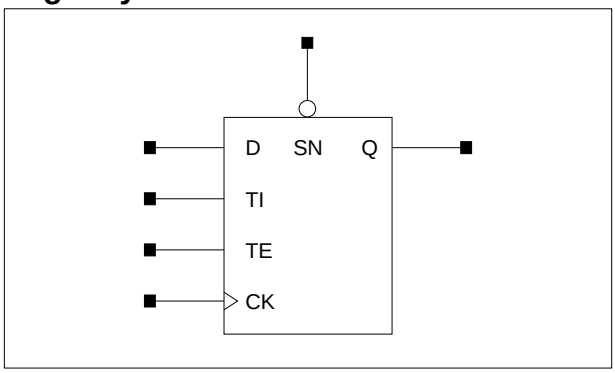
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd3sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.041	0.032 + 0.005*SL	0.031 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.048	0.039 + 0.005*SL	0.041 + 0.004*SL	0.044 + 0.004*SL
	t_{PLH}	0.113	0.106 + 0.004*SL	0.110 + 0.003*SL	0.119 + 0.002*SL
	t_{PHL}	0.107	0.099 + 0.004*SL	0.105 + 0.003*SL	0.126 + 0.002*SL
SN to Q	t_R	0.076	0.065 + 0.006*SL	0.069 + 0.005*SL	0.063 + 0.005*SL
	t_{PLH}	0.209	0.200 + 0.005*SL	0.207 + 0.003*SL	0.229 + 0.002*SL
CK to QN	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.024 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.151	0.144 + 0.003*SL	0.148 + 0.002*SL	0.152 + 0.002*SL
	t_{PHL}	0.152	0.145 + 0.003*SL	0.150 + 0.002*SL	0.155 + 0.002*SL
SN to QN	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.017 + 0.004*SL
	t_{PHL}	0.062	0.056 + 0.003*SL	0.060 + 0.002*SL	0.065 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



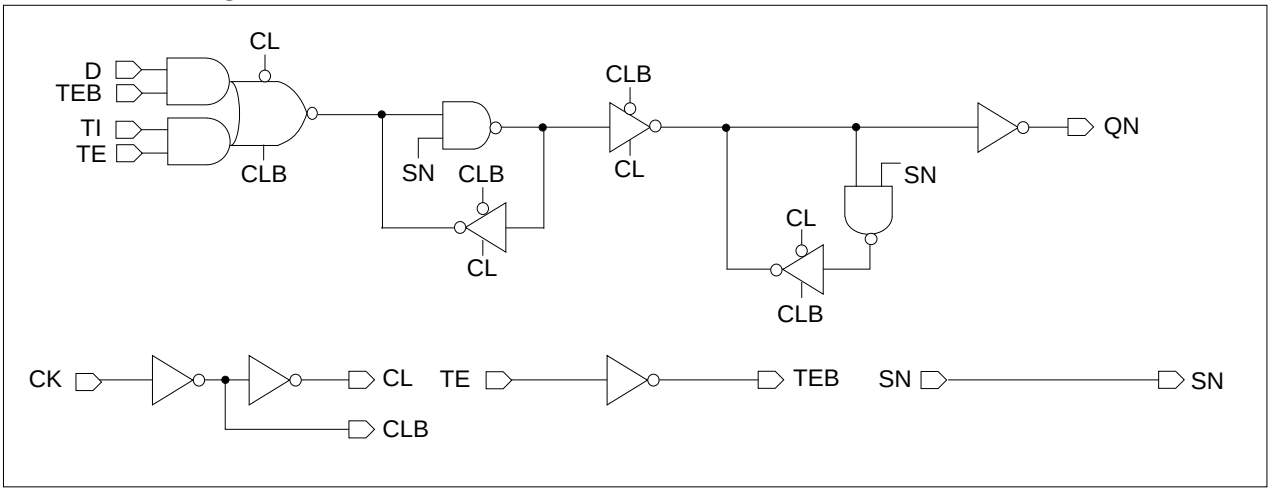
Truth Table

D	TI	TE	CK	SN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	1
x	x	x	↓	1	Q (n)

Cell Data

Input Load (SL)										Gate Count	
fd3sq					*fd3sqd2*					*fd3sq*	*fd3sqd2*
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.5	1.0	1.7	0.6	1.1	0.5	1.0	1.7	0.6	1.1	8.33	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd3sq	fd3sqd2
Input Setup Time (D to CK)	t_{SU}	0.161	0.160
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.190	0.190
Pulse Width High (CK)	t_{PWH}	0.060	0.079
Pulse Width Low (SN)	t_{PWL}	0.084	0.102
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.064	0.064
Input Setup Time (TI to CK)	t_{SU}	0.188	0.186
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.185	0.185
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010

fd3sq/fd3sqd2

D Flip-Flop with Set, Scan, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd3sq

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.024 + 0.010*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.045	0.028 + 0.009*SL	0.032 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.105	0.094 + 0.006*SL	0.098 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.092	0.079 + 0.006*SL	0.086 + 0.005*SL	0.096 + 0.004*SL
SN to Q	t_R	0.068	0.050 + 0.009*SL	0.048 + 0.010*SL	0.040 + 0.010*SL
	t_{PLH}	0.158	0.143 + 0.007*SL	0.152 + 0.005*SL	0.163 + 0.005*SL

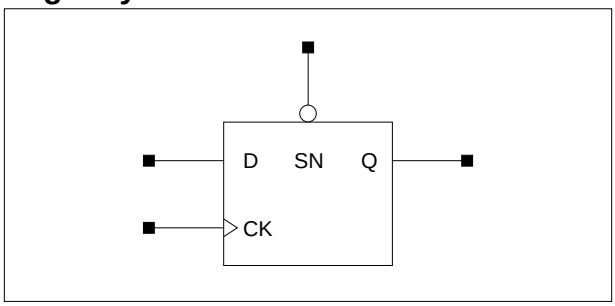
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd3sqd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.027 + 0.005*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.043	0.034 + 0.004*SL	0.037 + 0.004*SL	0.036 + 0.004*SL
	t_{PLH}	0.107	0.100 + 0.003*SL	0.104 + 0.002*SL	0.111 + 0.002*SL
	t_{PHL}	0.098	0.090 + 0.004*SL	0.096 + 0.003*SL	0.112 + 0.002*SL
SN to Q	t_R	0.072	0.062 + 0.005*SL	0.063 + 0.005*SL	0.056 + 0.005*SL
	t_{PLH}	0.175	0.166 + 0.005*SL	0.173 + 0.003*SL	0.193 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



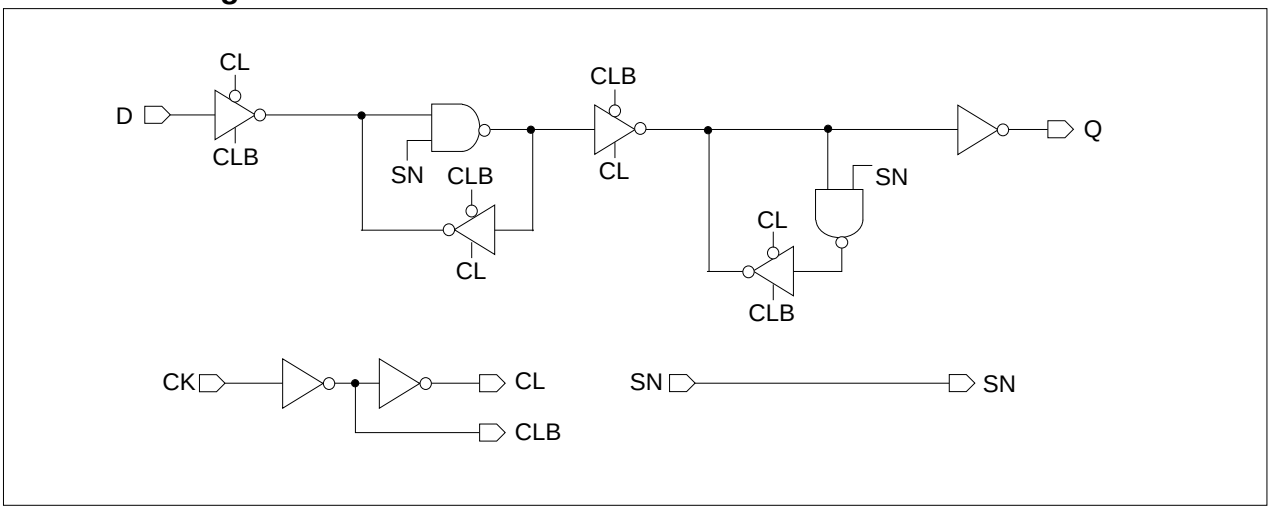
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
fd3q			*fd3qd2*			*fd3q*	*fd3qd2*
D	CK	SN	D	CK	SN		
0.7	1.0	1.6	0.7	1.0	1.6	6.33	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd3q	fd3qd2
Input Setup Time (D to CK)	t_{SU}	0.051	0.051
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.102	0.101
Pulse Width High (CK)	t_{PWH}	0.060	0.079
Pulse Width Low (SN)	t_{PWL}	0.083	0.099
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.071	0.070

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd3q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.024 + 0.010*SL	0.026 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.045	0.028 + 0.009*SL	0.031 + 0.008*SL	0.028 + 0.008*SL
	t_{PLH}	0.105	0.093 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.090	0.077 + 0.006*SL	0.085 + 0.005*SL	0.095 + 0.004*SL
SN to Q	t_R	0.069	0.050 + 0.010*SL	0.050 + 0.009*SL	0.040 + 0.010*SL
	t_{PLH}	0.160	0.145 + 0.007*SL	0.154 + 0.005*SL	0.165 + 0.005*SL

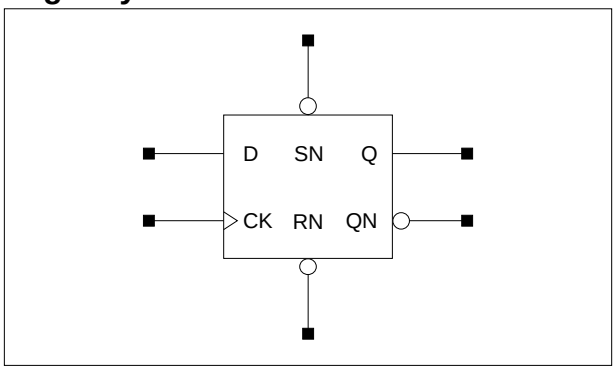
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd3qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.044	0.033 + 0.005*SL	0.039 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.106	0.099 + 0.004*SL	0.103 + 0.002*SL	0.109 + 0.002*SL
	t_{PHL}	0.096	0.088 + 0.004*SL	0.094 + 0.003*SL	0.110 + 0.002*SL
SN to Q	t_R	0.071	0.060 + 0.005*SL	0.063 + 0.005*SL	0.055 + 0.005*SL
	t_{PLH}	0.175	0.166 + 0.004*SL	0.172 + 0.003*SL	0.192 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



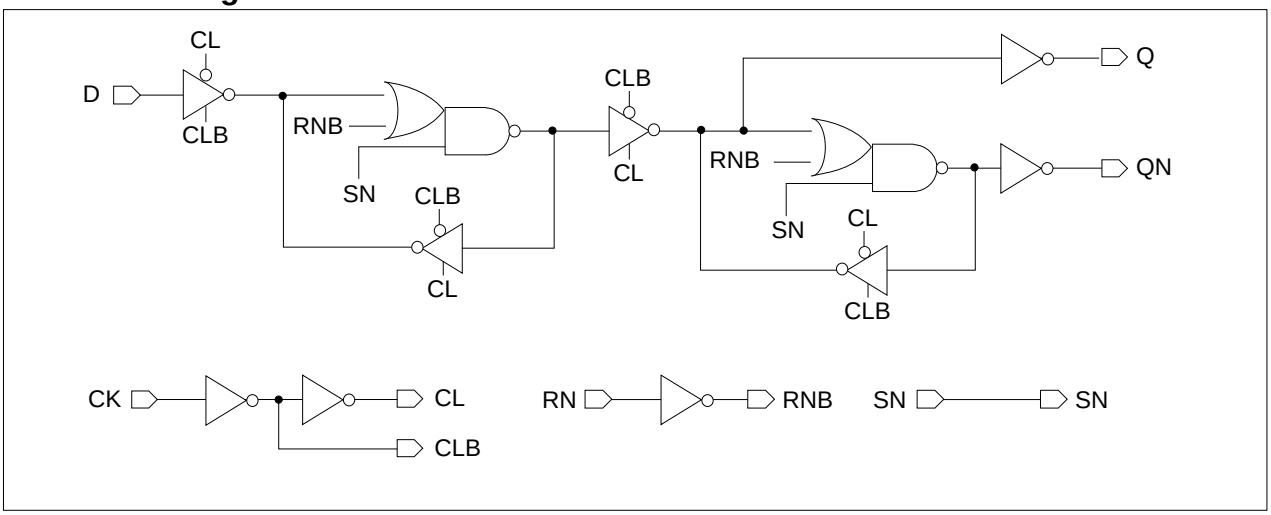
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
fd4				*fd4d2*				*fd4*	*fd4d2*
D	CK	RN	SN	D	CK	RN	SN		
0.7	1.0	1.0	2.1	0.7	1.0	1.0	2.1	9.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd4	fd4d2
Input Setup Time (D to CK)	t_{SU}	0.054	0.054
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.103	0.103
Pulse Width High (CK)	t_{PWH}	0.076	0.101
Pulse Width Low (RN)	t_{PWL}	0.163	0.202
Pulse Width Low (SN)	t_{PWL}	0.102	0.127
Recovery Time (RN to CK)	t_{RC}	0.030	0.030
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.071	0.071
Removal Time (SN to RN)	t_{RM}	0.010	0.010
Recovery Time (SN to RN)	t_{RC}	0.084	0.084

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.027 + 0.010*SL	0.026 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.050	0.034 + 0.008*SL	0.035 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.107 + 0.005*SL
	t_{PHL}	0.100	0.086 + 0.007*SL	0.095 + 0.005*SL	0.107 + 0.004*SL
RN to Q	t_F	0.096	0.079 + 0.009*SL	0.081 + 0.008*SL	0.090 + 0.008*SL
	t_{PHL}	0.305	0.286 + 0.009*SL	0.298 + 0.006*SL	0.327 + 0.005*SL
SN to Q	t_R	0.075	0.055 + 0.010*SL	0.056 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.097	0.080 + 0.008*SL	0.081 + 0.008*SL	0.090 + 0.008*SL
	t_{PLH}	0.185	0.169 + 0.008*SL	0.179 + 0.005*SL	0.194 + 0.005*SL
	t_{PHL}	0.278	0.259 + 0.009*SL	0.271 + 0.006*SL	0.300 + 0.005*SL
CK to QN	t_R	0.049	0.030 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.046	0.029 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.142	0.130 + 0.006*SL	0.135 + 0.005*SL	0.137 + 0.004*SL
	t_{PHL}	0.165	0.153 + 0.006*SL	0.160 + 0.005*SL	0.167 + 0.004*SL
RN to QN	t_R	0.046	0.027 + 0.009*SL	0.024 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.103	0.092 + 0.006*SL	0.096 + 0.005*SL	0.099 + 0.005*SL
SN to QN	t_R	0.047	0.028 + 0.010*SL	0.027 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.074	0.063 + 0.006*SL	0.067 + 0.005*SL	0.069 + 0.005*SL
	t_{PHL}	0.067	0.057 + 0.005*SL	0.061 + 0.004*SL	0.063 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd4d2

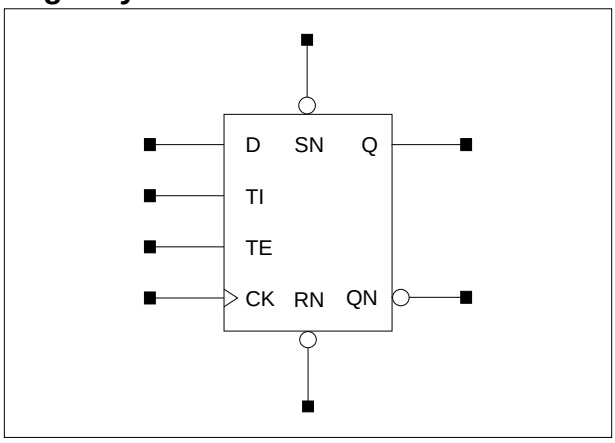
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.042	0.034 + 0.004*SL	0.030 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.046	0.037 + 0.004*SL	0.039 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.112	0.105 + 0.004*SL	0.110 + 0.002*SL	0.116 + 0.002*SL
	t_{PHL}	0.105	0.097 + 0.004*SL	0.103 + 0.003*SL	0.122 + 0.002*SL
RN to Q	t_F	0.119	0.111 + 0.004*SL	0.110 + 0.004*SL	0.120 + 0.004*SL
	t_{PHL}	0.356	0.344 + 0.006*SL	0.353 + 0.004*SL	0.389 + 0.003*SL
SN to Q	t_R	0.078	0.070 + 0.004*SL	0.067 + 0.005*SL	0.066 + 0.005*SL
	t_F	0.118	0.110 + 0.004*SL	0.109 + 0.004*SL	0.120 + 0.004*SL
	t_{PLH}	0.213	0.203 + 0.005*SL	0.210 + 0.003*SL	0.233 + 0.002*SL
	t_{PHL}	0.328	0.317 + 0.006*SL	0.325 + 0.004*SL	0.361 + 0.003*SL
CK to QN	t_R	0.044	0.035 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.044	0.035 + 0.004*SL	0.037 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.165	0.158 + 0.004*SL	0.163 + 0.002*SL	0.170 + 0.002*SL
	t_{PHL}	0.185	0.177 + 0.004*SL	0.183 + 0.003*SL	0.198 + 0.002*SL
RN to QN	t_R	0.041	0.032 + 0.005*SL	0.032 + 0.005*SL	0.022 + 0.005*SL
	t_{PLH}	0.106	0.098 + 0.004*SL	0.103 + 0.002*SL	0.109 + 0.002*SL
SN to QN	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.032	0.023 + 0.004*SL	0.025 + 0.004*SL	0.020 + 0.004*SL
	t_{PLH}	0.077	0.069 + 0.004*SL	0.074 + 0.002*SL	0.081 + 0.002*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.066 + 0.002*SL	0.073 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd4s/fd4sd2

D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Logic Symbol



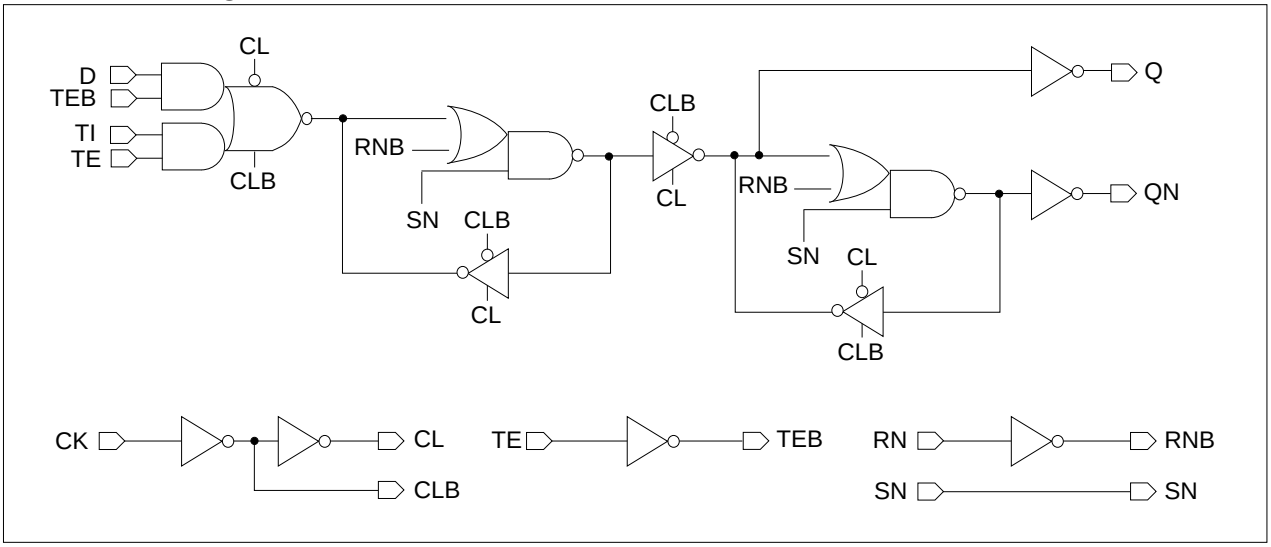
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	1	0
x	x	x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
fd4s						*fd4sd2*						*fd4s*	*fd4sd2*
D	CK	RN	SN	TI	TE	D	CK	RN	SN	TI	TE		
0.5	1.0	1.0	2.1	0.6	1.1	0.5	1.0	1.0	2.1	0.6	1.1	11.33	11.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd4s	fd4sd2
Input Setup Time (D to CK)	t_{SU}	0.149	0.150
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.182	0.183
Pulse Width High (CK)	t_{PWH}	0.077	0.102
Pulse Width Low (RN)	t_{PWL}	0.161	0.202
Pulse Width Low (SN)	t_{PWL}	0.101	0.127
Recovery Time (RN to CK)	t_{RC}	0.030	0.029
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.063	0.063
Input Setup Time (TI to CK)	t_{SU}	0.174	0.176
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.174	0.174
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010
Recovery Time (SN to RN)	t_{RC}	0.080	0.080
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd4s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.027 + 0.010*SL	0.025 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.049	0.033 + 0.008*SL	0.035 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.110	0.098 + 0.006*SL	0.103 + 0.005*SL	0.107 + 0.005*SL
	t_{PHL}	0.103	0.089 + 0.007*SL	0.098 + 0.005*SL	0.110 + 0.004*SL
RN to Q	t_F	0.095	0.078 + 0.009*SL	0.080 + 0.008*SL	0.089 + 0.008*SL
	t_{PHL}	0.303	0.284 + 0.009*SL	0.297 + 0.006*SL	0.325 + 0.005*SL
SN to Q	t_R	0.074	0.055 + 0.010*SL	0.055 + 0.010*SL	0.048 + 0.010*SL
	t_F	0.096	0.078 + 0.009*SL	0.081 + 0.008*SL	0.089 + 0.008*SL
	t_{PLH}	0.183	0.168 + 0.008*SL	0.177 + 0.005*SL	0.192 + 0.005*SL
	t_{PHL}	0.275	0.256 + 0.009*SL	0.268 + 0.006*SL	0.296 + 0.005*SL
CK to QN	t_R	0.048	0.030 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.047	0.030 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.145	0.133 + 0.006*SL	0.138 + 0.005*SL	0.140 + 0.004*SL
	t_{PHL}	0.165	0.152 + 0.006*SL	0.159 + 0.005*SL	0.167 + 0.004*SL
RN to QN	t_R	0.047	0.029 + 0.009*SL	0.024 + 0.010*SL	0.020 + 0.010*SL
	t_{PLH}	0.104	0.092 + 0.006*SL	0.097 + 0.005*SL	0.099 + 0.005*SL
SN to QN	t_R	0.046	0.027 + 0.009*SL	0.025 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.074	0.063 + 0.006*SL	0.067 + 0.005*SL	0.069 + 0.005*SL
	t_{PHL}	0.067	0.056 + 0.005*SL	0.060 + 0.004*SL	0.063 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd4sd2

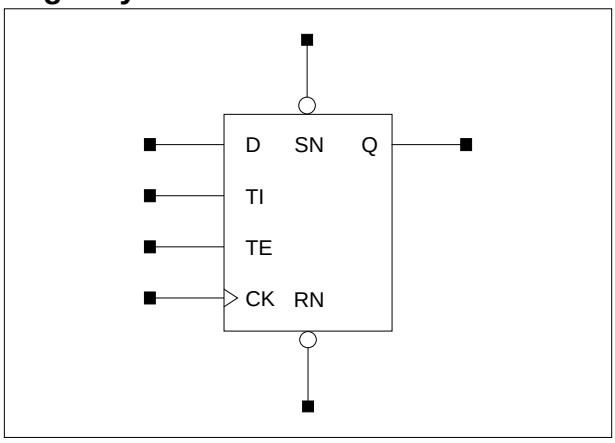
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.041	0.032 + 0.004*SL	0.030 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.046	0.037 + 0.005*SL	0.040 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.112	0.105 + 0.004*SL	0.109 + 0.002*SL	0.116 + 0.002*SL
	t_{PHL}	0.109	0.100 + 0.004*SL	0.107 + 0.003*SL	0.126 + 0.002*SL
RN to Q	t_F	0.117	0.109 + 0.004*SL	0.109 + 0.004*SL	0.118 + 0.004*SL
	t_{PHL}	0.355	0.344 + 0.006*SL	0.352 + 0.004*SL	0.388 + 0.003*SL
SN to Q	t_R	0.078	0.069 + 0.005*SL	0.069 + 0.005*SL	0.065 + 0.005*SL
	t_F	0.117	0.109 + 0.004*SL	0.110 + 0.004*SL	0.118 + 0.004*SL
	t_{PLH}	0.211	0.202 + 0.005*SL	0.209 + 0.003*SL	0.232 + 0.002*SL
	t_{PHL}	0.327	0.315 + 0.006*SL	0.323 + 0.004*SL	0.359 + 0.003*SL
CK to QN	t_R	0.044	0.035 + 0.005*SL	0.034 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.045	0.036 + 0.005*SL	0.040 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.168	0.161 + 0.004*SL	0.166 + 0.002*SL	0.173 + 0.002*SL
	t_{PHL}	0.184	0.176 + 0.004*SL	0.182 + 0.003*SL	0.197 + 0.002*SL
RN to QN	t_R	0.041	0.031 + 0.005*SL	0.032 + 0.005*SL	0.022 + 0.005*SL
	t_{PLH}	0.106	0.099 + 0.004*SL	0.103 + 0.002*SL	0.110 + 0.002*SL
SN to QN	t_R	0.040	0.031 + 0.005*SL	0.031 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.020 + 0.004*SL
	t_{PLH}	0.076	0.069 + 0.004*SL	0.073 + 0.002*SL	0.080 + 0.002*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.066 + 0.002*SL	0.073 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd4sq/fd4sqd2

D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive

Logic Symbol



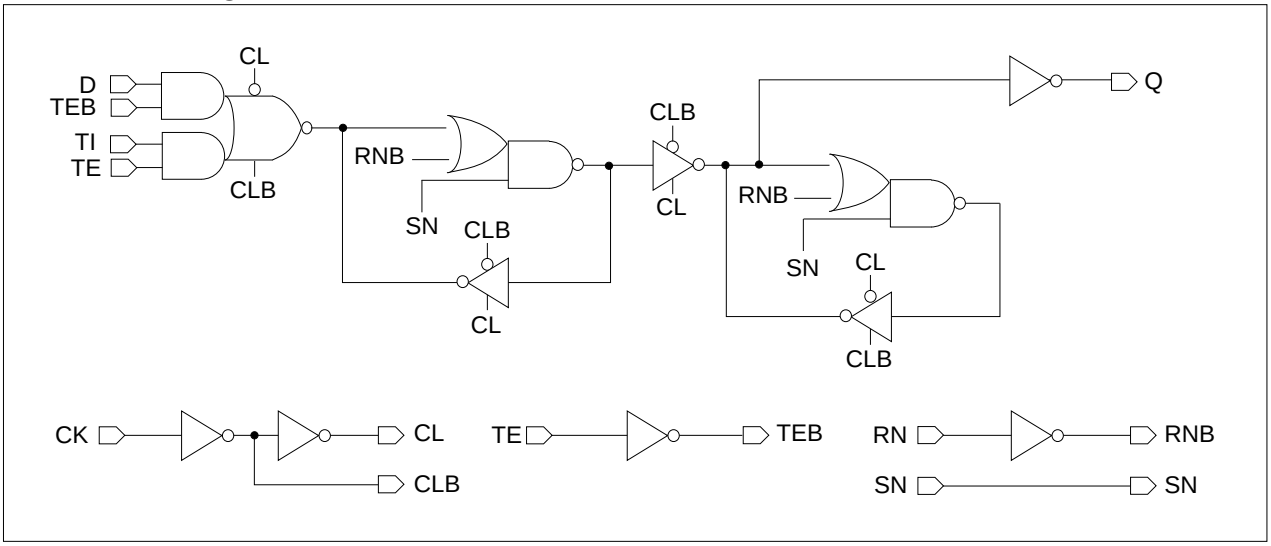
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)
0	x	0	↑	1	1	0
1	x	0	↑	1	1	1
x	0	1	↑	1	1	0
x	1	1	↑	1	1	1
x	x	x	x	1	0	1
x	x	x	x	0	1	0
x	x	x	x	0	0	1
x	x	x	↓	1	1	Q (n)

Cell Data

Input Load (SL)												Gate Count	
fd4sq						*fd4sqd2*						*fd4sq*	*fd4sqd2*
D	CK	RN	SN	TI	TE	D	CK	RN	SN	TI	TE		
0.5	1.0	1.0	1.7	0.6	1.1	0.5	1.0	1.0	1.7	0.6	1.1	10.33	11.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd4sq	fd4sqd2
Input Setup Time (D to CK)	t_{SU}	0.149	0.147
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.183	0.181
Pulse Width High (CK)	t_{PWH}	0.060	0.080
Pulse Width Low (RN)	t_{PWL}	0.126	0.160
Pulse Width Low (SN)	t_{PWL}	0.085	0.105
Recovery Time (RN to CK)	t_{RC}	0.026	0.028
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.064	0.063
Input Setup Time (TI to CK)	t_{SU}	0.175	0.173
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.173	0.172
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010
Removal Time (SN to RN)	t_{RM}	0.010	0.010
Recovery Time (SN to RN)	t_{RC}	0.082	0.081

fd4sq/fd4sqd2

D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.12ns, SL: Standard Load)

fd4sq

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.025 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.045	0.029 + 0.008*SL	0.031 + 0.008*SL	0.028 + 0.008*SL
	t_{PLH}	0.106	0.095 + 0.006*SL	0.099 + 0.005*SL	0.102 + 0.004*SL
	t_{PHL}	0.095	0.082 + 0.006*SL	0.089 + 0.005*SL	0.099 + 0.004*SL
RN to Q	t_F	0.086	0.068 + 0.009*SL	0.072 + 0.008*SL	0.076 + 0.008*SL
	t_{PHL}	0.261	0.243 + 0.009*SL	0.255 + 0.006*SL	0.280 + 0.005*SL
SN to Q	t_R	0.069	0.049 + 0.010*SL	0.051 + 0.009*SL	0.040 + 0.010*SL
	t_F	0.086	0.068 + 0.009*SL	0.073 + 0.008*SL	0.077 + 0.008*SL
	t_{PLH}	0.160	0.146 + 0.007*SL	0.154 + 0.005*SL	0.166 + 0.005*SL
	t_{PHL}	0.231	0.213 + 0.009*SL	0.225 + 0.006*SL	0.250 + 0.005*SL

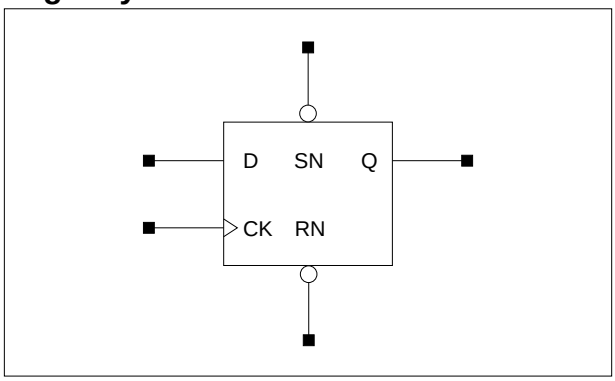
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd4sqd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.039	0.030 + 0.005*SL	0.029 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.045	0.036 + 0.005*SL	0.039 + 0.004*SL	0.036 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.003*SL	0.105 + 0.002*SL	0.112 + 0.002*SL
	t_{PHL}	0.102	0.094 + 0.004*SL	0.100 + 0.003*SL	0.116 + 0.002*SL
RN to Q	t_F	0.108	0.101 + 0.004*SL	0.100 + 0.004*SL	0.108 + 0.004*SL
	t_{PHL}	0.302	0.291 + 0.005*SL	0.299 + 0.003*SL	0.332 + 0.002*SL
SN to Q	t_R	0.071	0.063 + 0.004*SL	0.061 + 0.005*SL	0.057 + 0.005*SL
	t_F	0.109	0.100 + 0.004*SL	0.101 + 0.004*SL	0.108 + 0.004*SL
	t_{PLH}	0.179	0.170 + 0.005*SL	0.176 + 0.003*SL	0.197 + 0.002*SL
	t_{PHL}	0.272	0.261 + 0.005*SL	0.269 + 0.003*SL	0.302 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



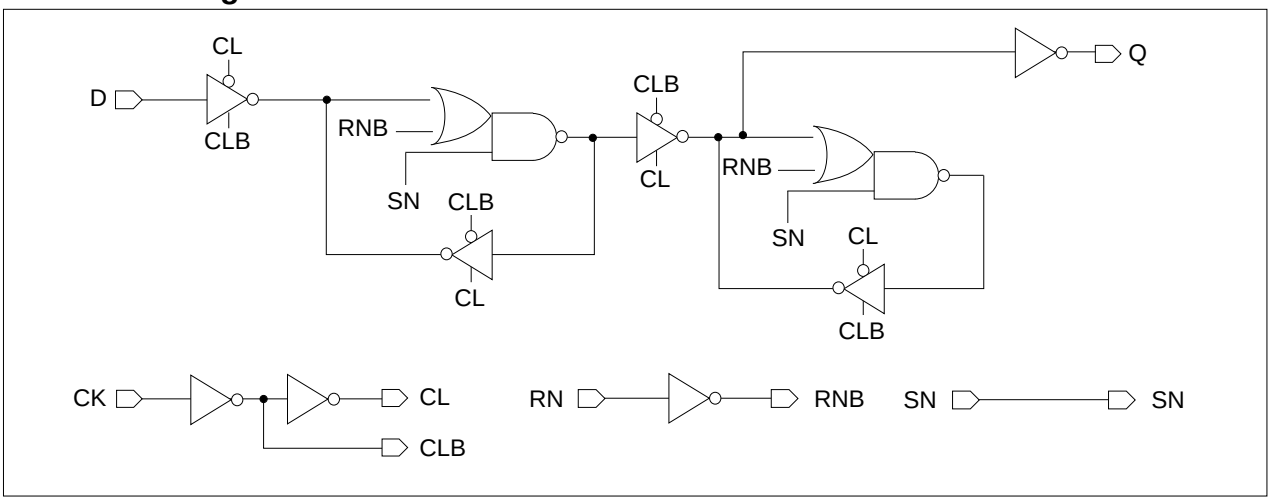
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	1
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
fd4q				*fd4qd2*				*fd4q*	*fd4qd2*
D	CK	RN	SN	D	CK	RN	SN		
0.7	1.0	1.0	1.7	0.7	1.0	1.0	1.7	8.00	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd4q	fd4qd2
Input Setup Time (D to CK)	t_{SU}	0.054	0.053
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.103	0.103
Pulse Width High (CK)	t_{PWH}	0.060	0.079
Pulse Width Low (RN)	t_{PWL}	0.127	0.160
Pulse Width Low (SN)	t_{PWL}	0.086	0.105
Recovery Time (RN to CK)	t_{RC}	0.028	0.028
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.070	0.067
Recovery Time (SN to RN)	t_{RC}	0.087	0.086
Removal Time (SN to RN)	t_{RM}	0.010	0.010

fd4q/fd4qd2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd4q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.024 + 0.010*SL	0.023 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.044	0.028 + 0.008*SL	0.030 + 0.008*SL	0.028 + 0.008*SL
	t_{PLH}	0.105	0.094 + 0.006*SL	0.098 + 0.005*SL	0.101 + 0.005*SL
	t_{PHL}	0.091	0.079 + 0.006*SL	0.086 + 0.005*SL	0.096 + 0.004*SL
RN to Q	t_F	0.088	0.071 + 0.008*SL	0.073 + 0.008*SL	0.077 + 0.008*SL
	t_{PHL}	0.261	0.244 + 0.009*SL	0.256 + 0.006*SL	0.281 + 0.005*SL
SN to Q	t_R	0.068	0.049 + 0.010*SL	0.050 + 0.009*SL	0.041 + 0.010*SL
	t_F	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.077 + 0.008*SL
	t_{PLH}	0.162	0.147 + 0.007*SL	0.156 + 0.005*SL	0.168 + 0.005*SL
	t_{PHL}	0.233	0.215 + 0.009*SL	0.227 + 0.006*SL	0.252 + 0.005*SL

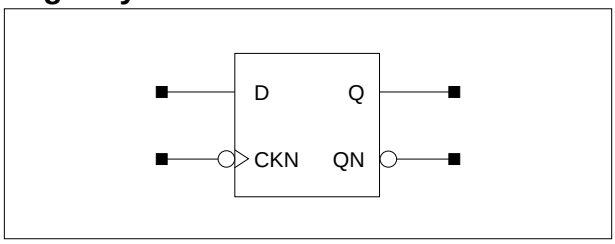
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd4qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.027 + 0.005*SL	0.029 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.045	0.036 + 0.004*SL	0.038 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.003*SL	0.105 + 0.002*SL	0.112 + 0.002*SL
	t_{PHL}	0.098	0.090 + 0.004*SL	0.096 + 0.003*SL	0.113 + 0.002*SL
RN to Q	t_F	0.109	0.101 + 0.004*SL	0.100 + 0.004*SL	0.108 + 0.004*SL
	t_{PHL}	0.301	0.290 + 0.005*SL	0.298 + 0.003*SL	0.332 + 0.002*SL
SN to Q	t_R	0.072	0.063 + 0.005*SL	0.062 + 0.005*SL	0.057 + 0.005*SL
	t_F	0.108	0.101 + 0.004*SL	0.099 + 0.004*SL	0.108 + 0.004*SL
	t_{PLH}	0.179	0.170 + 0.005*SL	0.176 + 0.003*SL	0.197 + 0.002*SL
	t_{PHL}	0.272	0.261 + 0.005*SL	0.269 + 0.003*SL	0.302 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



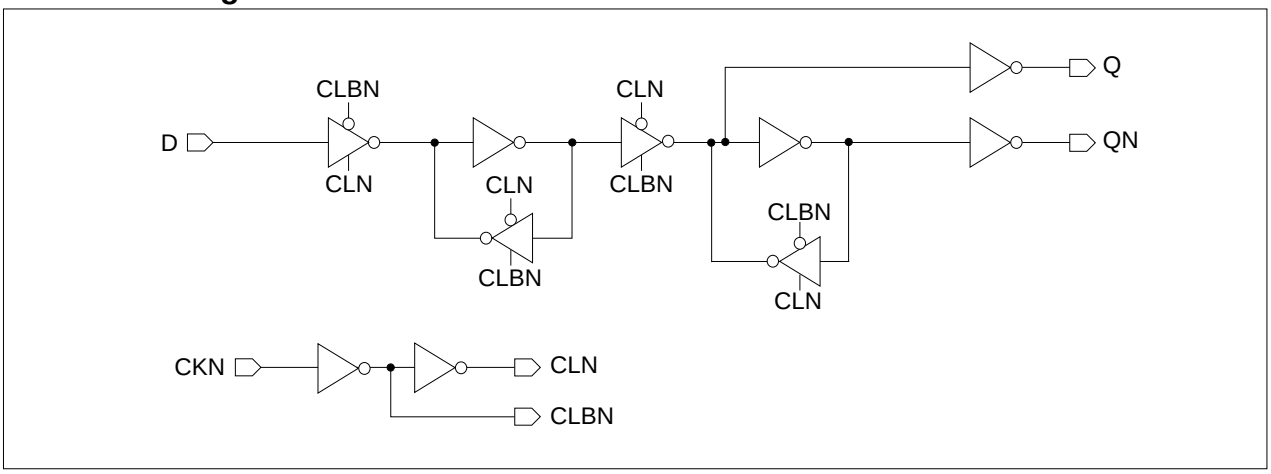
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
fd5		*fd5d2*		*fd5*	*fd5d2*
D	CKN	D	CKN		
0.7	0.7	0.8	0.7	6.33	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd5	fd5d2
Input Setup Time (D to CKN)	t_{SU}	0.062	0.061
Input Hold Time (D to CKN)	t_{HD}	0.023	0.023
Pulse Width Low (CKN)	t_{PWL}	0.089	0.110
Pulse Width High (CKN)	t_{PWH}	0.089	0.110

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.049	0.030 + 0.010*SL	0.030 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.050	0.032 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.113	0.101 + 0.006*SL	0.107 + 0.005*SL	0.111 + 0.004*SL
	t_{PHL}	0.141	0.127 + 0.007*SL	0.135 + 0.005*SL	0.148 + 0.004*SL
CKN to QN	t_R	0.043	0.025 + 0.009*SL	0.022 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.020 + 0.008*SL	0.019 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.166	0.155 + 0.005*SL	0.158 + 0.005*SL	0.159 + 0.004*SL
	t_{PHL}	0.143	0.133 + 0.005*SL	0.137 + 0.004*SL	0.139 + 0.004*SL

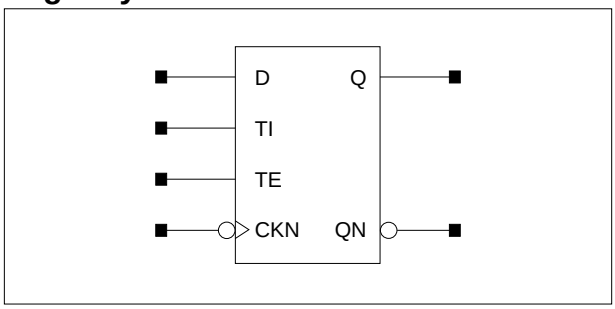
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.045	0.034 + 0.006*SL	0.038 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.049	0.039 + 0.005*SL	0.044 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.121	0.113 + 0.004*SL	0.118 + 0.003*SL	0.128 + 0.002*SL
	t_{PHL}	0.145	0.136 + 0.004*SL	0.143 + 0.003*SL	0.163 + 0.002*SL
CKN to QN	t_R	0.038	0.029 + 0.004*SL	0.028 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.182	0.175 + 0.003*SL	0.179 + 0.002*SL	0.182 + 0.002*SL
	t_{PHL}	0.161	0.155 + 0.003*SL	0.159 + 0.002*SL	0.164 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



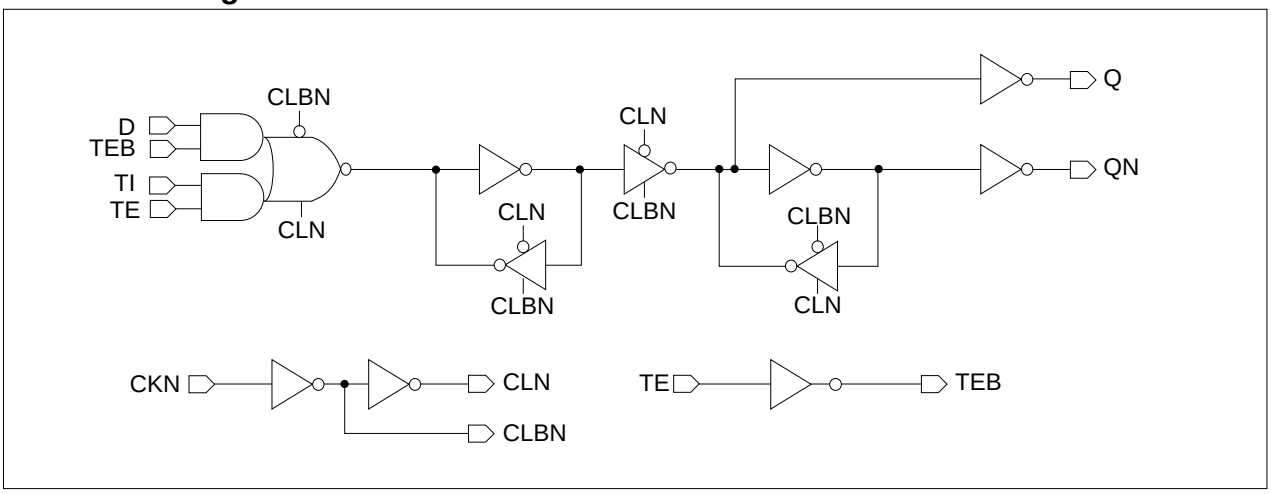
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
fd5s				*fd5sd2*				*fd5s*	*fd5sd2*
D	CKN	TI	TE	D	CKN	TI	TE		
0.5	0.7	0.6	1.1	0.5	0.7	0.6	1.1	8.67	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd5s	fd5sd2
Input Setup Time (D to CKN)	t_{SU}	0.163	0.163
Input Hold Time (D to CKN)	t_{HD}	0.010	0.010
Pulse Width Low (CKN)	t_{PWL}	0.089	0.110
Pulse Width High (CKN)	t_{PWH}	0.089	0.110
Input Setup Time (TI to CKN)	t_{SU}	0.180	0.182
Input Hold Time (TI to CKN)	t_{HD}	0.010	0.010
Input Setup Time (TE to CKN)	t_{SU}	0.181	0.188
Input Hold Time (TE to CKN)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd5s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.048	0.028 + 0.010*SL	0.029 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.050	0.033 + 0.009*SL	0.038 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.109	0.097 + 0.006*SL	0.102 + 0.005*SL	0.108 + 0.004*SL
	t_{PHL}	0.143	0.130 + 0.007*SL	0.138 + 0.005*SL	0.150 + 0.004*SL
CKN to QN	t_R	0.043	0.026 + 0.009*SL	0.021 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.036	0.021 + 0.008*SL	0.020 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.168	0.158 + 0.005*SL	0.161 + 0.005*SL	0.161 + 0.004*SL
	t_{PHL}	0.139	0.129 + 0.005*SL	0.133 + 0.004*SL	0.136 + 0.004*SL

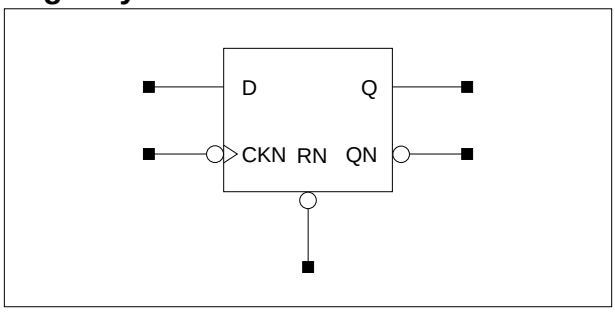
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd5sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.048	0.039 + 0.004*SL	0.041 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.116	0.109 + 0.004*SL	0.114 + 0.003*SL	0.124 + 0.002*SL
	t_{PHL}	0.148	0.139 + 0.004*SL	0.146 + 0.003*SL	0.166 + 0.002*SL
CKN to QN	t_R	0.039	0.030 + 0.004*SL	0.028 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.026 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.189	0.182 + 0.003*SL	0.186 + 0.002*SL	0.188 + 0.002*SL
	t_{PHL}	0.161	0.154 + 0.003*SL	0.158 + 0.002*SL	0.164 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



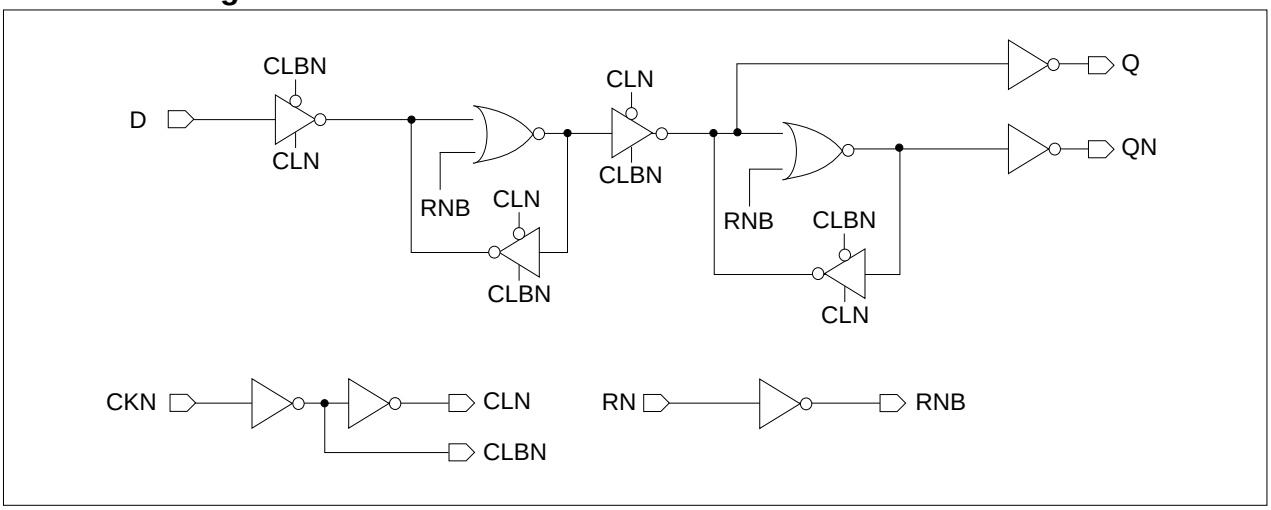
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
fd6			*fd6d2*			*fd6*	*fd6d2*
D	CKN	RN	D	CKN	RN		
0.8	0.7	1.0	0.8	0.7	1.0	7.67	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd6	fd6d2
Input Setup Time (D to CKN)	t_{SU}	0.052	0.052
Input Hold Time (D to CKN)	t_{HD}	0.022	0.023
Pulse Width Low (CKN)	t_{PWL}	0.101	0.119
Pulse Width High (CKN)	t_{PWH}	0.101	0.119
Pulse Width Low (RN)	t_{PWL}	0.091	0.091
Recovery Time (RN to CK)	t_{RC}	0.010	0.010
Removal Time (RN to CK)	t_{RM}	0.033	0.035

fd6/fd6d2

D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.051	0.032 + 0.010*SL	0.031 + 0.010*SL	0.024 + 0.010*SL
	t_F	0.051	0.034 + 0.008*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.117	0.105 + 0.006*SL	0.111 + 0.005*SL	0.116 + 0.004*SL
	t_{PHL}	0.144	0.130 + 0.007*SL	0.139 + 0.005*SL	0.151 + 0.004*SL
RN to Q	t_F	0.094	0.075 + 0.009*SL	0.081 + 0.008*SL	0.088 + 0.008*SL
	t_{PHL}	0.292	0.274 + 0.009*SL	0.287 + 0.006*SL	0.314 + 0.005*SL
CKN to QN	t_R	0.043	0.026 + 0.009*SL	0.021 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.043	0.027 + 0.008*SL	0.029 + 0.008*SL	0.023 + 0.008*SL
	t_{PLH}	0.170	0.160 + 0.005*SL	0.163 + 0.005*SL	0.163 + 0.004*SL
	t_{PHL}	0.163	0.151 + 0.006*SL	0.157 + 0.004*SL	0.162 + 0.004*SL
RN to QN	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.014 + 0.010*SL
	t_{PLH}	0.091	0.081 + 0.005*SL	0.082 + 0.005*SL	0.083 + 0.004*SL

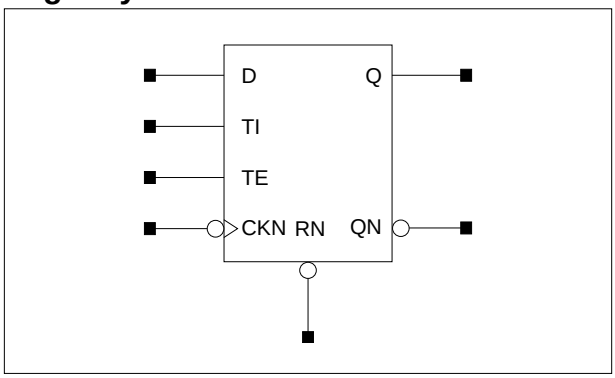
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd6d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.045	0.036 + 0.005*SL	0.035 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.050	0.042 + 0.004*SL	0.043 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.122	0.114 + 0.004*SL	0.119 + 0.003*SL	0.129 + 0.002*SL
	t_{PHL}	0.151	0.141 + 0.005*SL	0.150 + 0.003*SL	0.170 + 0.002*SL
RN to Q	t_F	0.118	0.110 + 0.004*SL	0.109 + 0.004*SL	0.119 + 0.004*SL
	t_{PHL}	0.342	0.330 + 0.006*SL	0.338 + 0.004*SL	0.375 + 0.003*SL
CKN to QN	t_R	0.038	0.029 + 0.005*SL	0.028 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.040	0.032 + 0.004*SL	0.034 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.193	0.186 + 0.004*SL	0.191 + 0.002*SL	0.194 + 0.002*SL
	t_{PHL}	0.184	0.177 + 0.004*SL	0.181 + 0.002*SL	0.194 + 0.002*SL
RN to QN	t_R	0.033	0.025 + 0.004*SL	0.022 + 0.005*SL	0.015 + 0.005*SL
	t_{PLH}	0.091	0.085 + 0.003*SL	0.088 + 0.002*SL	0.090 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



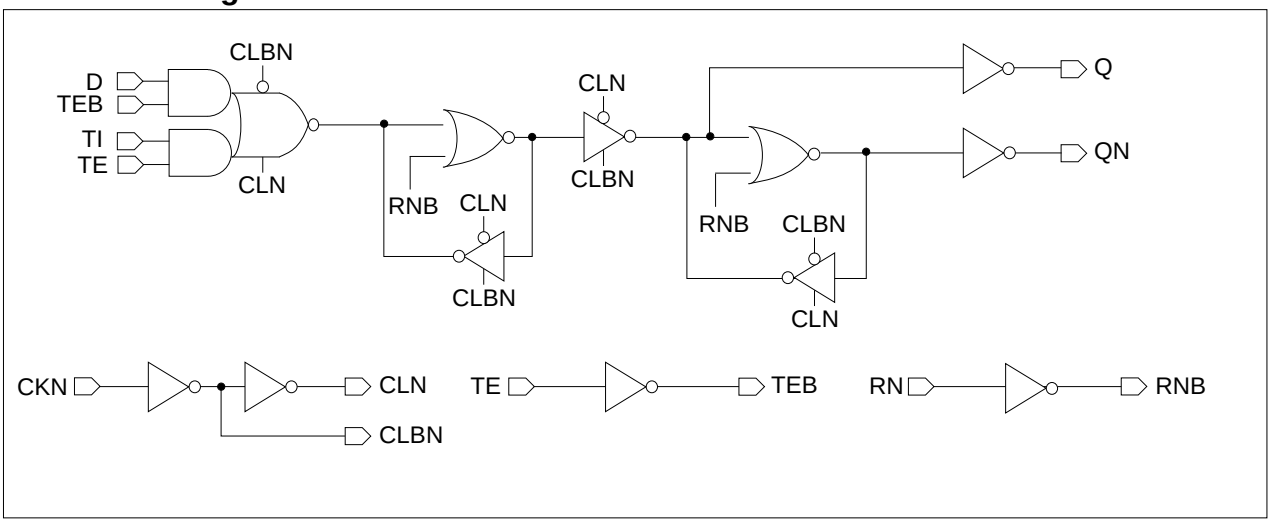
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
fd6s					*fd6sd2*					*fd6s*	*fd6sd2*
D	CKN	RN	TI	TE	D	CKN	RN	TI	TE		
0.5	0.8	1.0	0.6	1.1	0.5	0.7	1.0	0.6	1.1	10.00	10.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd6s	fd6sd2
Input Setup Time (D to CKN)	t_{SU}	0.162	0.160
Input Hold Time (D to CKN)	t_{HD}	0.010	0.010
Pulse Width Low (CKN)	t_{PWL}	0.101	0.119
Pulse Width High (CKN)	t_{PWH}	0.101	0.119
Pulse Width Low (RN)	t_{PWL}	0.090	0.087
Recovery Time (RN to CKN)	t_{RC}	0.010	0.010
Removal Time (RN to CKN)	t_{RM}	0.029	0.032
Input Setup Time (TI to CKN)	t_{SU}	0.180	0.178
Input Hold Time (TI to CKN)	t_{HD}	0.010	0.010
Input Setup Time (TE to CKN)	t_{SU}	0.180	0.184
Input Hold Time (TE to CKN)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd6s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.051	0.034 + 0.009*SL	0.029 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.052	0.035 + 0.008*SL	0.039 + 0.008*SL	0.034 + 0.008*SL
	t_{PLH}	0.119	0.105 + 0.007*SL	0.113 + 0.005*SL	0.116 + 0.004*SL
	t_{PHL}	0.148	0.134 + 0.007*SL	0.144 + 0.005*SL	0.155 + 0.004*SL
RN to Q	t_F	0.095	0.075 + 0.010*SL	0.083 + 0.008*SL	0.090 + 0.008*SL
	t_{PHL}	0.289	0.270 + 0.009*SL	0.283 + 0.006*SL	0.311 + 0.005*SL
CKN to QN	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.043	0.027 + 0.008*SL	0.028 + 0.008*SL	0.021 + 0.008*SL
	t_{PLH}	0.174	0.164 + 0.005*SL	0.167 + 0.004*SL	0.167 + 0.004*SL
	t_{PHL}	0.163	0.150 + 0.006*SL	0.159 + 0.004*SL	0.162 + 0.004*SL
RN to QN	t_R	0.040	0.022 + 0.009*SL	0.017 + 0.010*SL	0.013 + 0.010*SL
	t_{PLH}	0.090	0.080 + 0.005*SL	0.082 + 0.005*SL	0.083 + 0.004*SL

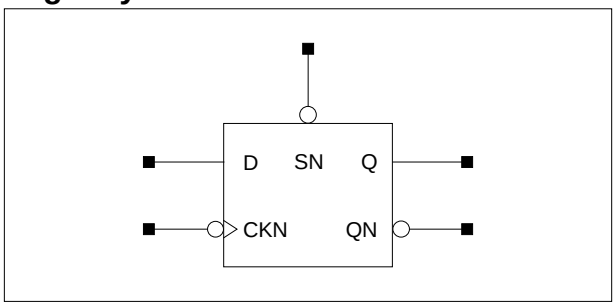
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd6sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.044	0.034 + 0.005*SL	0.035 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.051	0.043 + 0.004*SL	0.044 + 0.004*SL	0.044 + 0.004*SL
	t_{PLH}	0.122	0.114 + 0.004*SL	0.119 + 0.003*SL	0.128 + 0.002*SL
	t_{PHL}	0.151	0.142 + 0.004*SL	0.149 + 0.003*SL	0.170 + 0.002*SL
RN to Q	t_F	0.118	0.109 + 0.004*SL	0.110 + 0.004*SL	0.119 + 0.004*SL
	t_{PHL}	0.336	0.324 + 0.006*SL	0.332 + 0.004*SL	0.369 + 0.003*SL
CKN to QN	t_R	0.039	0.030 + 0.005*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.040	0.031 + 0.005*SL	0.035 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.194	0.187 + 0.003*SL	0.191 + 0.002*SL	0.194 + 0.002*SL
	t_{PHL}	0.184	0.176 + 0.004*SL	0.181 + 0.002*SL	0.194 + 0.002*SL
RN to QN	t_R	0.032	0.022 + 0.005*SL	0.023 + 0.005*SL	0.014 + 0.005*SL
	t_{PLH}	0.090	0.084 + 0.003*SL	0.087 + 0.002*SL	0.089 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



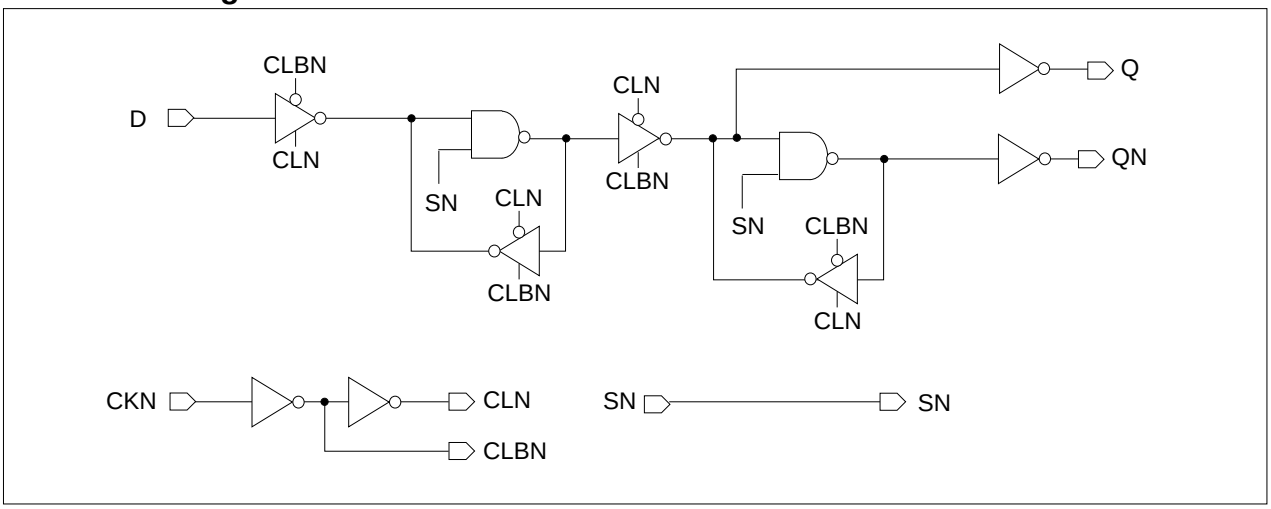
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
fd7			*fd7d2*			*fd7*	*fd7d2*
D	CKN	SN	D	CKN	SN		
0.8	0.7	2.2	0.8	0.7	2.2	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd7	fd7d2
Input Setup Time (D to CKN)	t_{SU}	0.060	0.059
Input Hold Time (D to CKN)	t_{HD}	0.025	0.025
Pulse Width Low (CKN)	t_{PWL}	0.097	0.114
Pulse Width High (CKN)	t_{PWH}	0.097	0.114
Pulse Width Low (SN)	t_{PWL}	0.068	0.068
Recovery Time (SN to CKN)	t_{RC}	0.010	0.010
Removal Time (SN to CKN)	t_{RM}	0.066	0.067

fd7/fd7d2

D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.051	0.031 + 0.010*SL	0.031 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.050	0.033 + 0.009*SL	0.037 + 0.008*SL	0.034 + 0.008*SL
	t_{PLH}	0.119	0.106 + 0.006*SL	0.112 + 0.005*SL	0.118 + 0.004*SL
	t_{PHL}	0.144	0.130 + 0.007*SL	0.139 + 0.005*SL	0.154 + 0.004*SL
SN to Q	t_R	0.072	0.053 + 0.010*SL	0.054 + 0.009*SL	0.046 + 0.010*SL
	t_{PLH}	0.182	0.166 + 0.008*SL	0.176 + 0.005*SL	0.190 + 0.005*SL
CKN to QN	t_R	0.045	0.026 + 0.009*SL	0.024 + 0.010*SL	0.017 + 0.010*SL
	t_F	0.036	0.021 + 0.007*SL	0.020 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.175	0.164 + 0.005*SL	0.167 + 0.005*SL	0.170 + 0.004*SL
	t_{PHL}	0.149	0.139 + 0.005*SL	0.142 + 0.004*SL	0.144 + 0.004*SL
SN to QN	t_F	0.037	0.021 + 0.008*SL	0.022 + 0.008*SL	0.016 + 0.008*SL
	t_{PHL}	0.063	0.052 + 0.005*SL	0.056 + 0.004*SL	0.059 + 0.004*SL

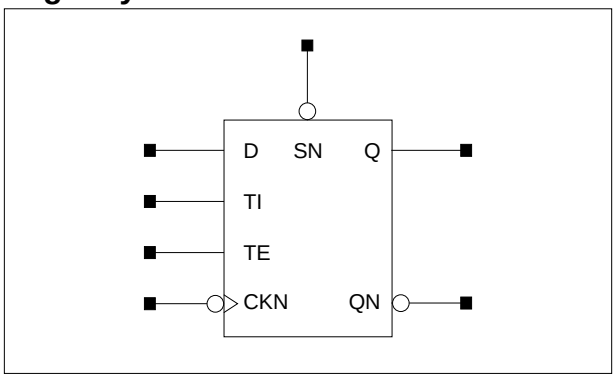
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd7d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.045	0.035 + 0.005*SL	0.036 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.049	0.043 + 0.003*SL	0.040 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.122	0.115 + 0.004*SL	0.120 + 0.003*SL	0.129 + 0.002*SL
	t_{PHL}	0.151	0.142 + 0.004*SL	0.148 + 0.003*SL	0.169 + 0.002*SL
SN to Q	t_R	0.075	0.065 + 0.005*SL	0.066 + 0.005*SL	0.064 + 0.005*SL
	t_{PLH}	0.207	0.198 + 0.005*SL	0.205 + 0.003*SL	0.228 + 0.002*SL
CKN to QN	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.195	0.188 + 0.003*SL	0.192 + 0.002*SL	0.197 + 0.002*SL
	t_{PHL}	0.164	0.157 + 0.003*SL	0.161 + 0.002*SL	0.167 + 0.002*SL
SN to QN	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.018 + 0.004*SL
	t_{PHL}	0.063	0.057 + 0.003*SL	0.061 + 0.002*SL	0.067 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



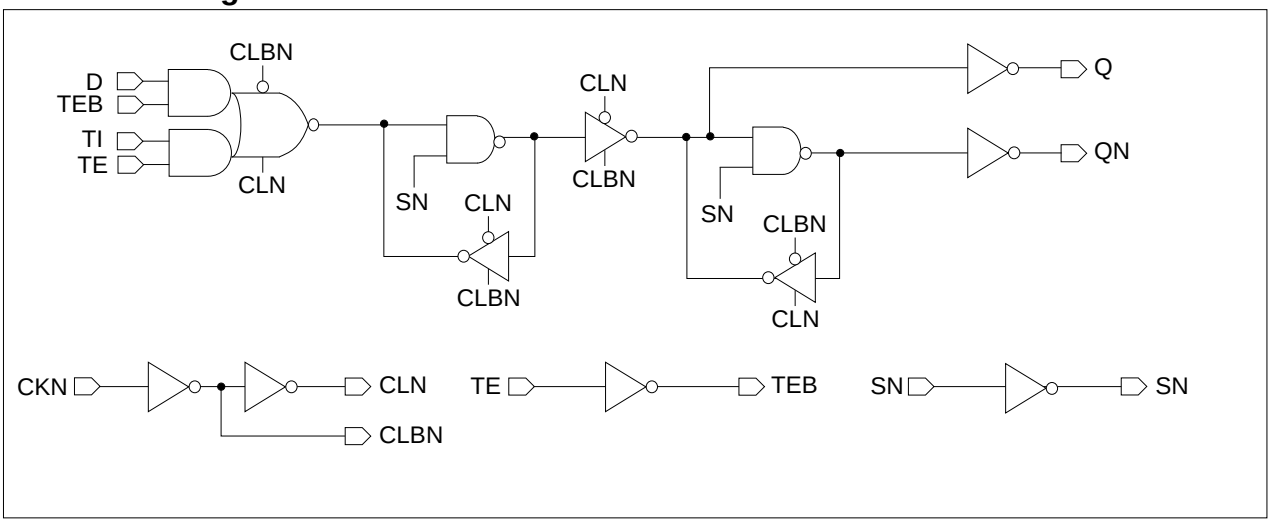
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
fd7s					*fd7sd2*					*fd7s*	*fd7sd2*
D	CKN	SN	TI	TE	D	CKN	SN	TI	TE		
0.5	0.7	2.2	0.6	1.1	0.5	0.7	2.2	0.6	1.1	9.00	9.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd7s	fd7sd2
Input Setup Time (D to CKN)	t_{SU}	0.171	0.170
Input Hold Time (D to CKN)	t_{HD}	0.010	0.010
Pulse Width Low (CKN)	t_{PWL}	0.097	0.114
Pulse Width High (CKN)	t_{PWH}	0.097	0.114
Pulse Width Low (SN)	t_{PWL}	0.068	0.067
Recovery Time (SN to CKN)	t_{RC}	0.010	0.010
Removal Time (SN to CKN)	t_{RM}	0.067	0.066
Input Setup Time (TI to CKN)	t_{SU}	0.190	0.190
Input Hold Time (TI to CKN)	t_{HD}	0.010	0.010
Input Setup Time (TE to CKN)	t_{SU}	0.190	0.187
Input Hold Time (TE to CKN)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd7s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.051	0.032 + 0.010*SL	0.033 + 0.010*SL	0.024 + 0.010*SL
	t_F	0.051	0.034 + 0.008*SL	0.037 + 0.008*SL	0.035 + 0.008*SL
	t_{PLH}	0.119	0.107 + 0.006*SL	0.112 + 0.005*SL	0.118 + 0.004*SL
	t_{PHL}	0.147	0.133 + 0.007*SL	0.142 + 0.005*SL	0.156 + 0.004*SL
SN to Q	t_R	0.073	0.053 + 0.010*SL	0.056 + 0.009*SL	0.045 + 0.010*SL
	t_{PLH}	0.183	0.168 + 0.008*SL	0.178 + 0.005*SL	0.192 + 0.005*SL
CKN to QN	t_R	0.046	0.029 + 0.009*SL	0.024 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.178	0.167 + 0.005*SL	0.170 + 0.005*SL	0.173 + 0.004*SL
	t_{PHL}	0.149	0.138 + 0.005*SL	0.142 + 0.004*SL	0.144 + 0.004*SL
SN to QN	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.015 + 0.008*SL
	t_{PHL}	0.062	0.052 + 0.005*SL	0.055 + 0.004*SL	0.058 + 0.004*SL

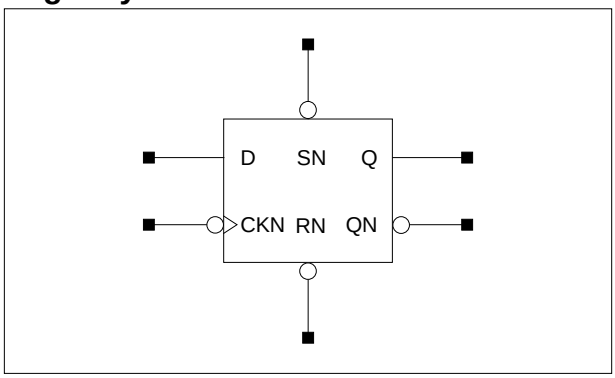
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fd7sd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.046	0.036 + 0.005*SL	0.037 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.049	0.041 + 0.004*SL	0.042 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.121	0.114 + 0.004*SL	0.118 + 0.003*SL	0.129 + 0.002*SL
	t_{PHL}	0.151	0.142 + 0.004*SL	0.149 + 0.003*SL	0.169 + 0.002*SL
SN to Q	t_R	0.076	0.066 + 0.005*SL	0.067 + 0.005*SL	0.063 + 0.005*SL
	t_{PLH}	0.208	0.199 + 0.005*SL	0.206 + 0.003*SL	0.229 + 0.002*SL
CKN to QN	t_R	0.041	0.033 + 0.004*SL	0.031 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.024 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.195	0.188 + 0.003*SL	0.192 + 0.002*SL	0.197 + 0.002*SL
	t_{PHL}	0.162	0.156 + 0.003*SL	0.159 + 0.002*SL	0.166 + 0.002*SL
SN to QN	t_F	0.029	0.022 + 0.004*SL	0.021 + 0.004*SL	0.018 + 0.004*SL
	t_{PHL}	0.062	0.056 + 0.003*SL	0.060 + 0.002*SL	0.065 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



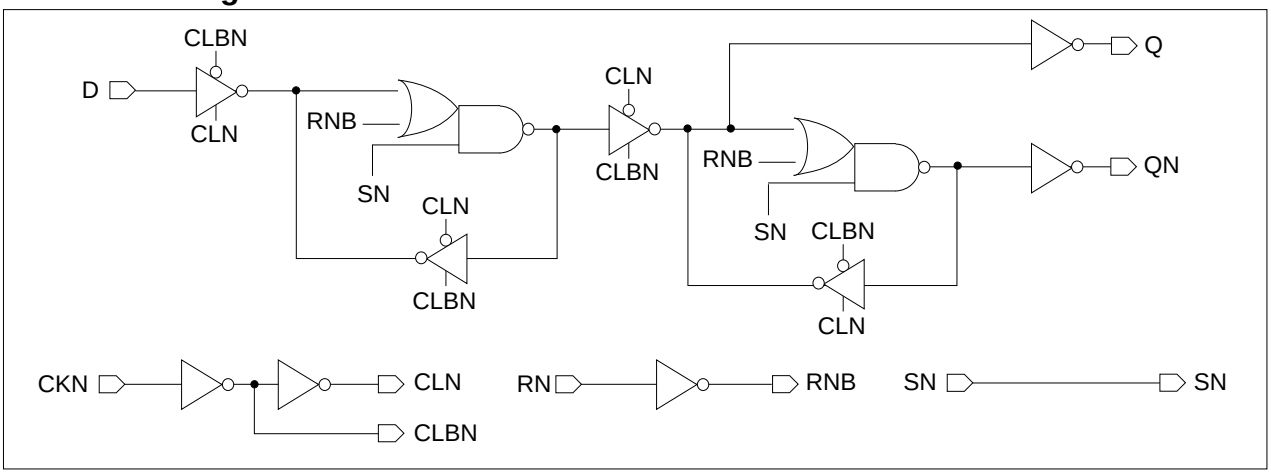
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
fd8				*fd8d2*				*fd8*	*fd8d2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.8	0.7	1.0	2.1	0.8	0.7	1.0	2.1	9.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd8	fd8d2
Input Setup Time (D to CKN)	t_{SU}	0.059	0.060
Input Hold Time (D to CKN)	t_{HD}	0.021	0.021
Pulse Width Low (CKN)	t_{PWL}	0.104	0.123
Pulse Width High (CKN)	t_{PWH}	0.104	0.123
Pulse Width Low (RN)	t_{PWL}	0.110	0.111
Pulse Width Low (SN)	t_{PWL}	0.072	0.073
Recovery Time (RN to CKN)	t_{RC}	0.010	0.010
Removal Time (RN to CKN)	t_{RM}	0.033	0.035
Recovery Time (SN to CKN)	t_{RC}	0.010	0.010
Removal Time (SN to CKN)	t_{RM}	0.066	0.067
Recovery Time (SN to RN)	t_{RC}	0.084	0.084
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.051	0.032 + 0.010*SL	0.032 + 0.010*SL	0.024 + 0.010*SL
	t_F	0.050	0.032 + 0.009*SL	0.036 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.117	0.105 + 0.006*SL	0.111 + 0.005*SL	0.115 + 0.005*SL
	t_{PHL}	0.143	0.130 + 0.007*SL	0.138 + 0.005*SL	0.150 + 0.004*SL
RN to Q	t_F	0.096	0.079 + 0.008*SL	0.081 + 0.008*SL	0.089 + 0.008*SL
	t_{PHL}	0.304	0.285 + 0.009*SL	0.298 + 0.006*SL	0.326 + 0.005*SL
SN to Q	t_R	0.074	0.054 + 0.010*SL	0.056 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.096	0.079 + 0.009*SL	0.082 + 0.008*SL	0.090 + 0.008*SL
	t_{PLH}	0.184	0.169 + 0.008*SL	0.178 + 0.005*SL	0.193 + 0.005*SL
	t_{PHL}	0.276	0.258 + 0.009*SL	0.270 + 0.006*SL	0.298 + 0.005*SL
CKN to QN	t_R	0.048	0.030 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.046	0.031 + 0.008*SL	0.032 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.185	0.174 + 0.006*SL	0.178 + 0.005*SL	0.180 + 0.004*SL
	t_{PHL}	0.173	0.161 + 0.006*SL	0.168 + 0.005*SL	0.176 + 0.004*SL
RN to QN	t_R	0.048	0.029 + 0.009*SL	0.027 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.104	0.092 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.005*SL
SN to QN	t_R	0.047	0.028 + 0.009*SL	0.027 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.021 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.075	0.063 + 0.006*SL	0.067 + 0.005*SL	0.070 + 0.005*SL
	t_{PHL}	0.067	0.057 + 0.005*SL	0.061 + 0.004*SL	0.064 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd8d2

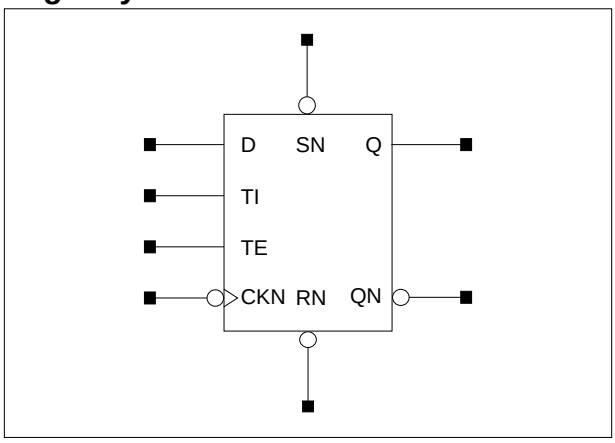
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.046	0.038 + 0.004*SL	0.033 + 0.005*SL	0.028 + 0.005*SL
	t_F	0.046	0.037 + 0.005*SL	0.040 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.122	0.114 + 0.004*SL	0.120 + 0.003*SL	0.128 + 0.002*SL
	t_{PHL}	0.149	0.140 + 0.004*SL	0.146 + 0.003*SL	0.165 + 0.002*SL
RN to Q	t_F	0.118	0.110 + 0.004*SL	0.109 + 0.004*SL	0.118 + 0.004*SL
	t_{PHL}	0.356	0.345 + 0.006*SL	0.353 + 0.004*SL	0.389 + 0.003*SL
SN to Q	t_R	0.078	0.070 + 0.004*SL	0.066 + 0.005*SL	0.066 + 0.005*SL
	t_F	0.117	0.109 + 0.004*SL	0.109 + 0.004*SL	0.119 + 0.004*SL
	t_{PLH}	0.213	0.203 + 0.005*SL	0.210 + 0.003*SL	0.233 + 0.002*SL
	t_{PHL}	0.329	0.317 + 0.006*SL	0.325 + 0.004*SL	0.361 + 0.003*SL
CKN to QN	t_R	0.044	0.035 + 0.005*SL	0.034 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.044	0.035 + 0.005*SL	0.039 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.208	0.201 + 0.004*SL	0.206 + 0.002*SL	0.213 + 0.002*SL
	t_{PHL}	0.197	0.188 + 0.004*SL	0.195 + 0.003*SL	0.210 + 0.002*SL
RN to QN	t_R	0.041	0.031 + 0.005*SL	0.032 + 0.005*SL	0.022 + 0.005*SL
	t_{PLH}	0.106	0.099 + 0.004*SL	0.103 + 0.002*SL	0.110 + 0.002*SL
SN to QN	t_R	0.040	0.031 + 0.005*SL	0.029 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.032	0.023 + 0.004*SL	0.025 + 0.004*SL	0.020 + 0.004*SL
	t_{PLH}	0.077	0.070 + 0.004*SL	0.074 + 0.002*SL	0.081 + 0.002*SL
	t_{PHL}	0.069	0.062 + 0.003*SL	0.066 + 0.002*SL	0.073 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fd8s/fd8sd2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Logic Symbol



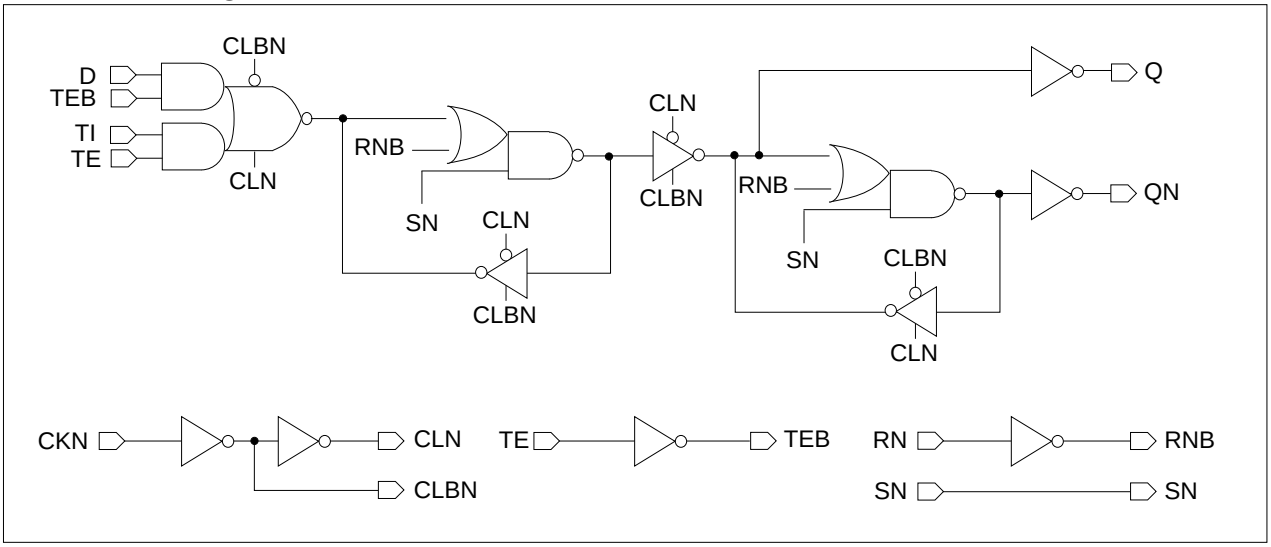
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	1	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
fd8s						*fd8sd2*						*fd8s*	*fd8sd2*
D	CKN	RN	SN	TI	TE	D	CKN	RN	SN	TI	TE		
0.5	0.7	1.0	2.1	0.6	1.1	0.5	0.7	1.0	2.1	0.6	1.1	11.33	11.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fd8s	fd8sd2
Input Setup Time (D to CKN)	t_{SU}	0.171	0.172
Input Hold Time (D to CKN)	t_{HD}	0.010	0.010
Pulse Width Low (CKN)	t_{PWL}	0.101	0.120
Pulse Width High (CKN)	t_{PWH}	0.101	0.120
Pulse Width Low (RN)	t_{PWL}	0.107	0.107
Pulse Width Low (SN)	t_{PWL}	0.068	0.068
Recovery Time (RN to CKN)	t_{RC}	0.010	0.010
Removal Time (RN to CKN)	t_{RM}	0.037	0.037
Recovery Time (SN to CKN)	t_{RC}	0.010	0.010
Removal Time (SN to CKN)	t_{RM}	0.053	0.053
Input Setup Time (TI to CKN)	t_{SU}	0.192	0.192
Input Hold Time (TI to CKN)	t_{HD}	0.010	0.010
Input Setup Time (TE to CKN)	t_{SU}	0.188	0.189
Input Hold Time (TE to CKN)	t_{HD}	0.010	0.010
Recovery Time (SN to RN)	t_{RC}	0.081	0.081
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd8s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.052	0.033 + 0.009*SL	0.032 + 0.010*SL	0.024 + 0.010*SL
	t_F	0.051	0.034 + 0.008*SL	0.037 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.116	0.104 + 0.006*SL	0.110 + 0.005*SL	0.111 + 0.005*SL
	t_{PHL}	0.148	0.134 + 0.007*SL	0.143 + 0.005*SL	0.155 + 0.004*SL
RN to Q	t_F	0.096	0.079 + 0.008*SL	0.080 + 0.008*SL	0.088 + 0.008*SL
	t_{PHL}	0.302	0.284 + 0.009*SL	0.296 + 0.006*SL	0.324 + 0.005*SL
SN to Q	t_R	0.073	0.053 + 0.010*SL	0.054 + 0.010*SL	0.047 + 0.010*SL
	t_F	0.096	0.078 + 0.009*SL	0.082 + 0.008*SL	0.089 + 0.008*SL
	t_{PLH}	0.183	0.168 + 0.008*SL	0.177 + 0.005*SL	0.192 + 0.005*SL
	t_{PHL}	0.274	0.256 + 0.009*SL	0.268 + 0.006*SL	0.296 + 0.005*SL
CKN to QN	t_R	0.048	0.030 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.046	0.030 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.190	0.178 + 0.006*SL	0.183 + 0.005*SL	0.185 + 0.004*SL
	t_{PHL}	0.172	0.159 + 0.006*SL	0.167 + 0.004*SL	0.173 + 0.004*SL
RN to QN	t_R	0.048	0.029 + 0.009*SL	0.027 + 0.010*SL	0.019 + 0.010*SL
	t_{PLH}	0.104	0.092 + 0.006*SL	0.096 + 0.005*SL	0.099 + 0.005*SL
SN to QN	t_R	0.047	0.029 + 0.009*SL	0.026 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.074	0.063 + 0.006*SL	0.067 + 0.005*SL	0.069 + 0.005*SL
	t_{PHL}	0.067	0.056 + 0.005*SL	0.060 + 0.004*SL	0.063 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fd8sd2

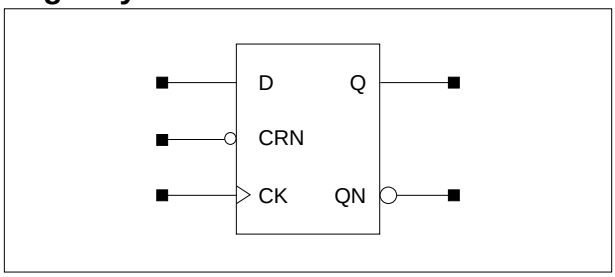
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.046	0.040 + 0.003*SL	0.033 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.041 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.118	0.110 + 0.004*SL	0.117 + 0.002*SL	0.122 + 0.002*SL
	t_{PHL}	0.152	0.144 + 0.004*SL	0.151 + 0.003*SL	0.168 + 0.002*SL
RN to Q	t_F	0.116	0.108 + 0.004*SL	0.108 + 0.004*SL	0.117 + 0.004*SL
	t_{PHL}	0.352	0.341 + 0.006*SL	0.349 + 0.004*SL	0.385 + 0.003*SL
SN to Q	t_R	0.077	0.069 + 0.004*SL	0.066 + 0.005*SL	0.064 + 0.005*SL
	t_F	0.116	0.108 + 0.004*SL	0.107 + 0.004*SL	0.117 + 0.004*SL
	t_{PLH}	0.210	0.201 + 0.005*SL	0.208 + 0.003*SL	0.231 + 0.002*SL
	t_{PHL}	0.324	0.313 + 0.006*SL	0.321 + 0.004*SL	0.356 + 0.003*SL
CKN to QN	t_R	0.044	0.035 + 0.005*SL	0.035 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.045	0.035 + 0.005*SL	0.040 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.212	0.204 + 0.004*SL	0.210 + 0.002*SL	0.216 + 0.002*SL
	t_{PHL}	0.192	0.183 + 0.004*SL	0.191 + 0.002*SL	0.203 + 0.002*SL
RN to QN	t_R	0.041	0.032 + 0.004*SL	0.030 + 0.005*SL	0.022 + 0.005*SL
	t_{PLH}	0.106	0.099 + 0.004*SL	0.103 + 0.002*SL	0.110 + 0.002*SL
SN to QN	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.032	0.023 + 0.004*SL	0.025 + 0.004*SL	0.020 + 0.004*SL
	t_{PLH}	0.076	0.069 + 0.004*SL	0.074 + 0.002*SL	0.080 + 0.002*SL
	t_{PHL}	0.068	0.062 + 0.003*SL	0.066 + 0.002*SL	0.073 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fds2/fds2d2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Logic Symbol



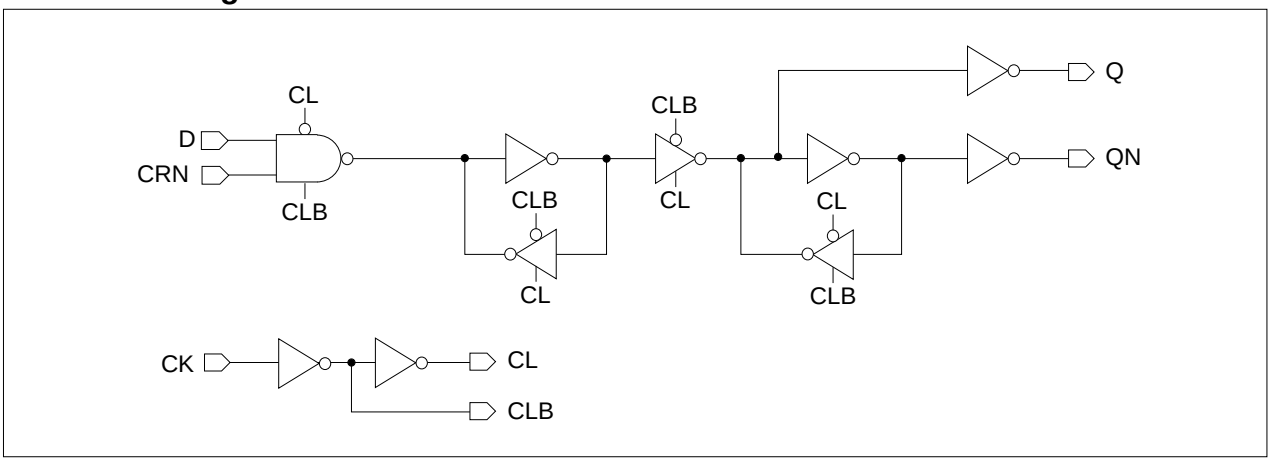
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
fds2			*fds2d2*			*fds2*	*fds2d2*
D	CRN	CK	D	CRN	CK		
0.6	0.6	1.0	0.6	0.6	1.0	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fds2	fds2d2
Input Setup Time (D to CK)	t_{SU}	0.089	0.091
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.117	0.119
Pulse Width High (CK)	t_{PWH}	0.066	0.090
Input Setup Time (CRN to CK)	t_{SU}	0.088	0.090
Input Hold Time (CRN to CK)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fds2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.027 + 0.010*SL	0.027 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.049	0.031 + 0.009*SL	0.037 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.108 + 0.004*SL
	t_{PHL}	0.098	0.084 + 0.007*SL	0.093 + 0.005*SL	0.105 + 0.004*SL
CK to QN	t_R	0.044	0.026 + 0.009*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.121	0.111 + 0.005*SL	0.113 + 0.005*SL	0.114 + 0.004*SL
	t_{PHL}	0.138	0.128 + 0.005*SL	0.131 + 0.004*SL	0.134 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fds2d2

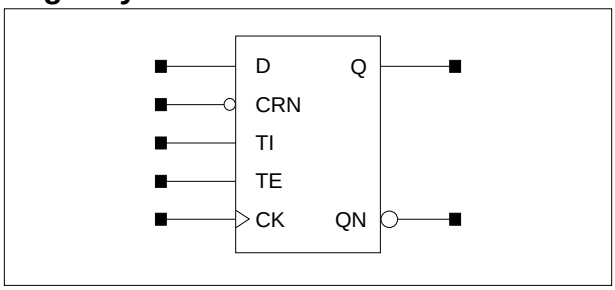
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.040	0.030 + 0.005*SL	0.030 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.048	0.038 + 0.005*SL	0.041 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.111	0.103 + 0.004*SL	0.108 + 0.003*SL	0.116 + 0.002*SL
	t_{PHL}	0.104	0.096 + 0.004*SL	0.103 + 0.003*SL	0.122 + 0.002*SL
CK to QN	t_R	0.038	0.031 + 0.004*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.140	0.133 + 0.003*SL	0.137 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.148	0.141 + 0.003*SL	0.145 + 0.002*SL	0.151 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fds2s/fds2sd2

D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

Logic Symbol



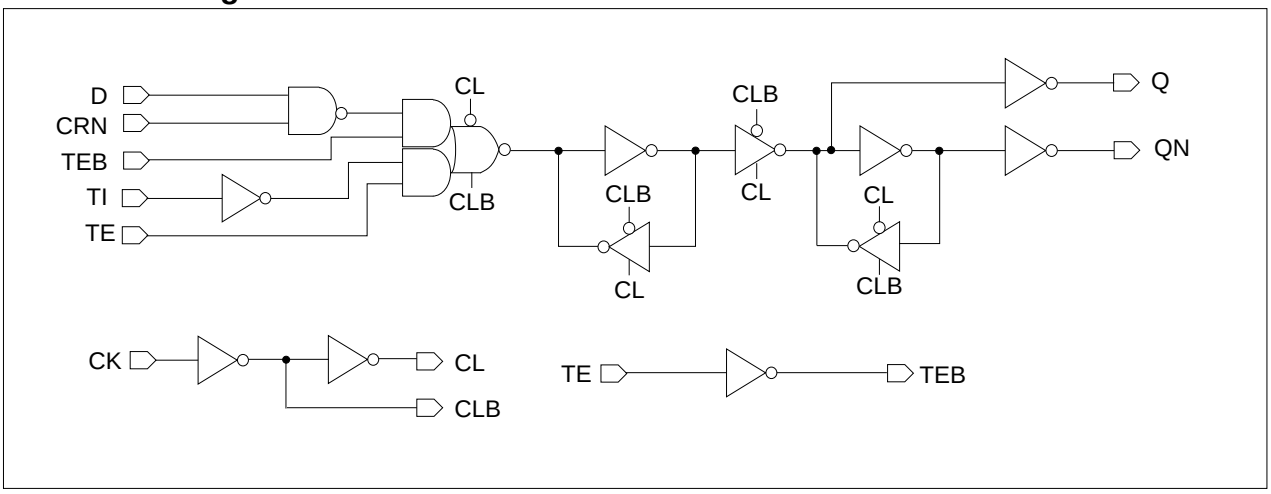
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
fds2s					*fds2sd2*					*fds2s*	*fds2sd2*
D	CRN	CK	TI	TE	D	CRN	CK	TI	TE		
0.6	0.6	1.1	0.6	1.2	0.6	0.6	1.0	0.6	1.2	10.33	11.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fds2s	fds2sd2
Input Setup Time (D to CK)	t_{SU}	0.183	0.183
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Input Setup Time (CRN to CK)	t_{SU}	0.182	0.181
Input Hold Time (CRN to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.169	0.169
Pulse Width High (CK)	t_{PWH}	0.069	0.094
Input Setup Time (TI to CK)	t_{SU}	0.186	0.184
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.170	0.170
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fds2s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.043	0.026 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.020 + 0.008*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.124	0.114 + 0.005*SL	0.117 + 0.005*SL	0.117 + 0.004*SL
	t_{PHL}	0.136	0.126 + 0.005*SL	0.130 + 0.004*SL	0.132 + 0.004*SL
CK to QN	t_R	0.045	0.024 + 0.010*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.049	0.031 + 0.009*SL	0.038 + 0.008*SL	0.032 + 0.008*SL
	t_{PLH}	0.108	0.096 + 0.006*SL	0.100 + 0.005*SL	0.104 + 0.004*SL
	t_{PHL}	0.099	0.086 + 0.007*SL	0.094 + 0.005*SL	0.107 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fds2sd2

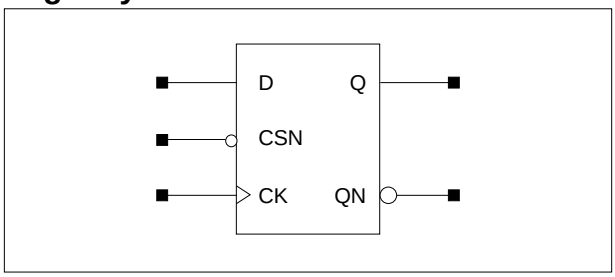
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.038	0.030 + 0.004*SL	0.026 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.026 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.149	0.143 + 0.003*SL	0.147 + 0.002*SL	0.150 + 0.002*SL
	t_{PHL}	0.155	0.149 + 0.003*SL	0.153 + 0.002*SL	0.160 + 0.002*SL
CK to QN	t_R	0.039	0.028 + 0.005*SL	0.029 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.046	0.038 + 0.004*SL	0.039 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.110	0.103 + 0.004*SL	0.108 + 0.002*SL	0.116 + 0.002*SL
	t_{PHL}	0.106	0.097 + 0.004*SL	0.104 + 0.003*SL	0.124 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fds3/fds3d2

D Flip-Flop with Synchronous Set, 1X/2X Drive

Logic Symbol



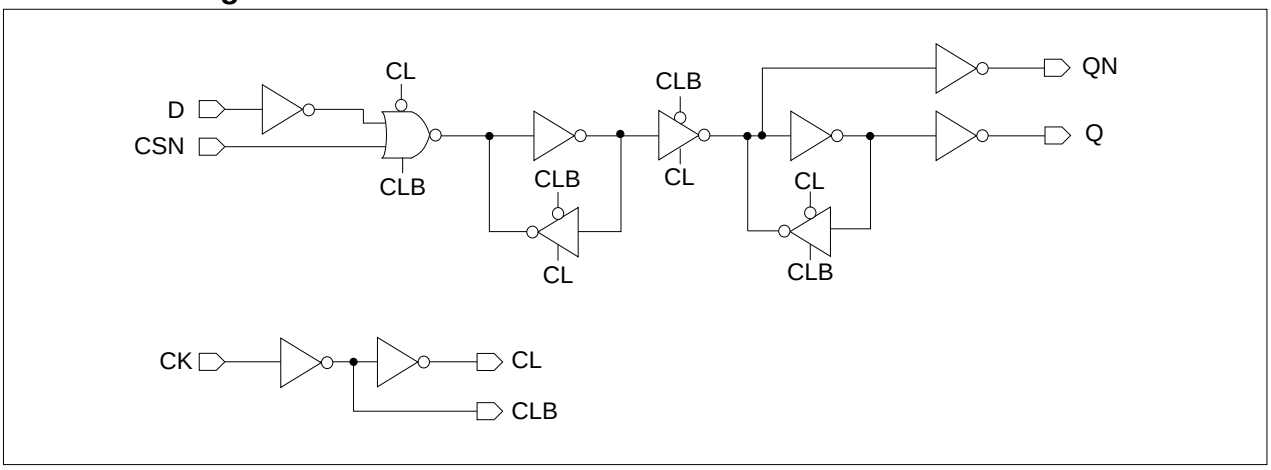
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
fds3			*fds3d2*			*fds3*	*fds3d2*
D	CSN	CK	D	CSN	CK		
0.6	0.6	1.0	0.6	0.6	1.0	7.67	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fds3	fds3d2
Input Setup Time (D to CK)	t_{SU}	0.123	0.124
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Input Setup Time (CSN to CK)	t_{SU}	0.087	0.089
Input Hold Time (CSN to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.117	0.118
Pulse Width High (CK)	t_{PWH}	0.066	0.090

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fds3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.044	0.027 + 0.009*SL	0.021 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.036	0.020 + 0.008*SL	0.021 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.120	0.110 + 0.005*SL	0.113 + 0.005*SL	0.113 + 0.004*SL
	t_{PHL}	0.139	0.129 + 0.005*SL	0.133 + 0.004*SL	0.135 + 0.004*SL
CK to QN	t_R	0.047	0.027 + 0.010*SL	0.027 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.049	0.030 + 0.009*SL	0.038 + 0.007*SL	0.031 + 0.008*SL
	t_{PLH}	0.112	0.100 + 0.006*SL	0.105 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.097	0.083 + 0.007*SL	0.092 + 0.005*SL	0.104 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fds3d2

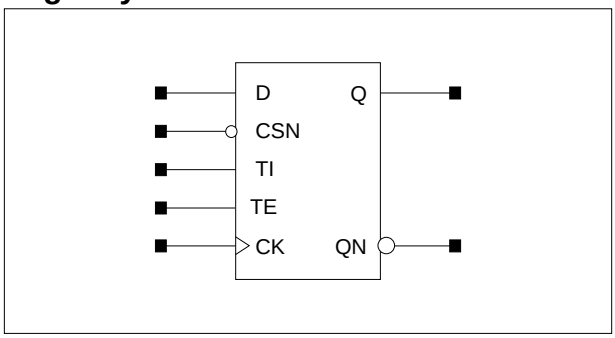
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.031	0.024 + 0.004*SL	0.023 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.139	0.133 + 0.003*SL	0.137 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.152	0.146 + 0.003*SL	0.150 + 0.002*SL	0.155 + 0.002*SL
CK to QN	t_R	0.041	0.030 + 0.005*SL	0.032 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.041 + 0.004*SL	0.042 + 0.004*SL
	t_{PLH}	0.114	0.107 + 0.004*SL	0.112 + 0.003*SL	0.120 + 0.002*SL
	t_{PHL}	0.104	0.095 + 0.004*SL	0.101 + 0.003*SL	0.121 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fds3s/fds3sd2

D Flip-Flop with Synchronous Set, Scan, 1X/2X Drive

Logic Symbol



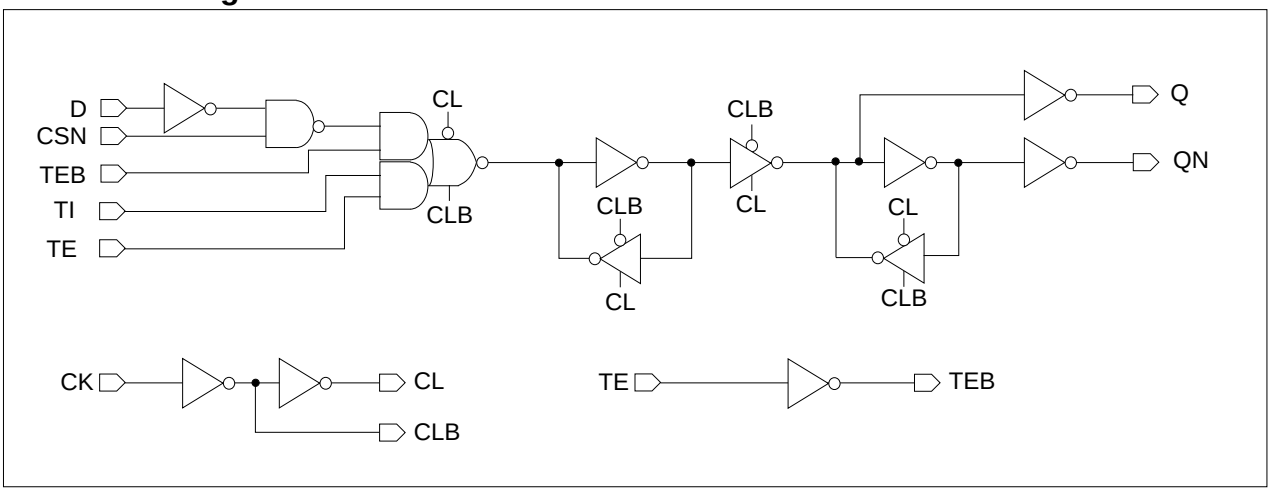
Truth Table

D	CSN	TI	TE	CK	Q(n+1)	QN(n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	0	x	0	↑	1	0
x	x	x	x	↓	Q(n)	QN(n+1)

Cell Data

Input Load (SL)										Gate Count	
fds3s					*fds3sd2*					*fds3s*	*fds3sd2*
D	CSN	CK	TI	TE	D	CSN	CK	TI	TE		
0.6	0.6	1.0	0.6	1.2	0.6	0.6	1.0	0.5	1.2	10.33	11.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fds3s	fds3sd2
Input Setup Time (D to CK)	t_{SU}	0.224	0.224
Input Hold Time (D to CK)	t_{HD}	0.010	0.010
Input Setup Time (CSN to CK)	t_{SU}	0.188	0.189
Input Hold Time (CSN to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.171	0.172
Pulse Width High (CK)	t_{PWH}	0.069	0.092
Input Setup Time (TI to CK)	t_{SU}	0.164	0.167
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.162	0.162
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fds3s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.026 + 0.010*SL	0.026 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.048	0.029 + 0.009*SL	0.037 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.108 + 0.004*SL
	t_{PHL}	0.099	0.086 + 0.007*SL	0.094 + 0.005*SL	0.106 + 0.004*SL
CK to QN	t_R	0.043	0.026 + 0.009*SL	0.021 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.036	0.021 + 0.008*SL	0.020 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.124	0.114 + 0.005*SL	0.117 + 0.005*SL	0.117 + 0.004*SL
	t_{PHL}	0.140	0.130 + 0.005*SL	0.133 + 0.004*SL	0.136 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fds3sd2

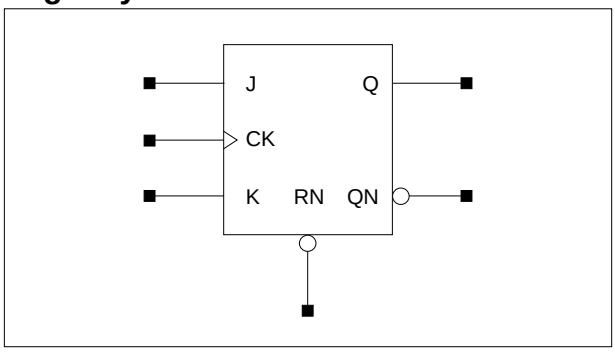
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.039	0.029 + 0.005*SL	0.029 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.047	0.040 + 0.004*SL	0.039 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.112	0.104 + 0.004*SL	0.109 + 0.003*SL	0.117 + 0.002*SL
	t_{PHL}	0.104	0.095 + 0.004*SL	0.102 + 0.003*SL	0.122 + 0.002*SL
CK to QN	t_R	0.039	0.030 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.145	0.138 + 0.003*SL	0.142 + 0.002*SL	0.144 + 0.002*SL
	t_{PHL}	0.154	0.148 + 0.003*SL	0.152 + 0.002*SL	0.158 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fj2/fj2d2

JK Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



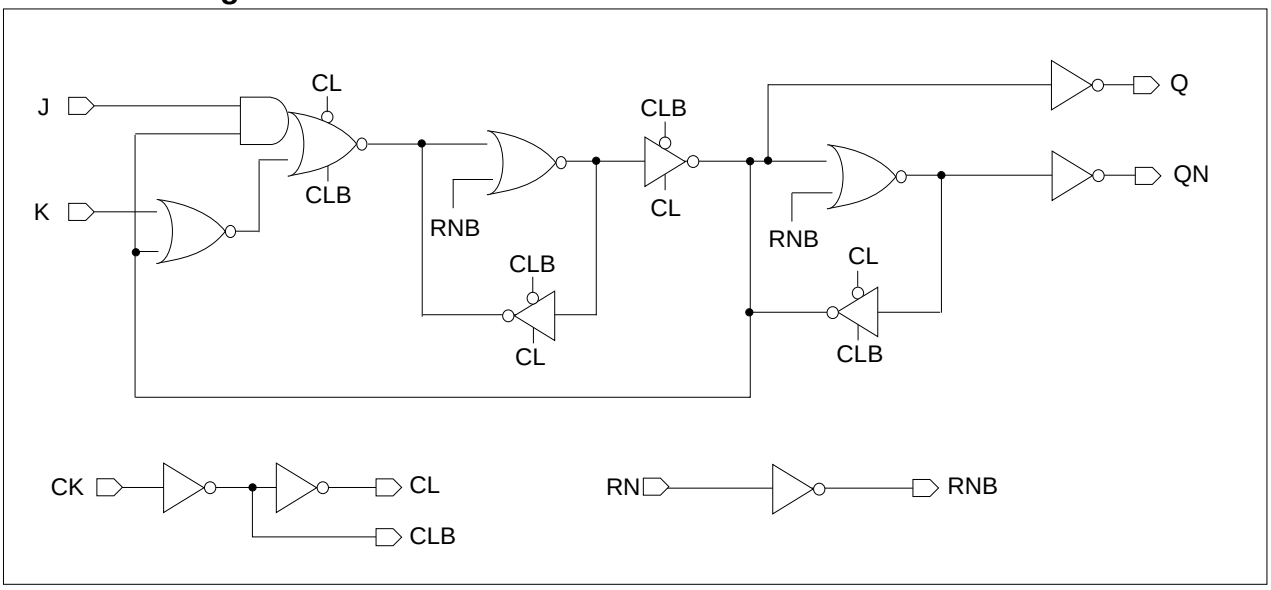
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	0	1	1	0
0	↑	0	1	Q (n)	QN (n)
1	↑	1	1	QN (n)	Q (n)
x	↓	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
fj2				*fj2d2*				*fj2*	*fj2d2*
J	K	CK	RN	J	K	CK	RN		
0.9	0.5	1.1	1.0	0.9	0.5	1.1	1.0	10.33	11.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fj2	fj2d2
Input Setup Time (J to CK)	t_{SU}	0.099	0.101
Input Hold Time (J to CK)	t_{HD}	0.010	0.010
Input Setup Time (K to CK)	t_{SU}	0.099	0.101
Input Hold Time (K to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.096	0.095
Pulse Width High (CK)	t_{PWH}	0.095	0.120
Pulse Width Low (RN)	t_{PWL}	0.240	0.278
Recovery Time (RN to CK)	t_{RC}	0.021	0.019
Removal Time (RN to CK)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.055	0.035 + 0.010*SL	0.036 + 0.010*SL	0.031 + 0.010*SL
	t_F	0.060	0.040 + 0.010*SL	0.049 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.144	0.130 + 0.007*SL	0.138 + 0.005*SL	0.147 + 0.005*SL
	t_{PHL}	0.123	0.107 + 0.008*SL	0.118 + 0.005*SL	0.138 + 0.004*SL
RN to Q	t_F	0.123	0.105 + 0.009*SL	0.108 + 0.008*SL	0.122 + 0.008*SL
	t_{PHL}	0.379	0.357 + 0.011*SL	0.374 + 0.007*SL	0.407 + 0.005*SL
CK to QN	t_R	0.047	0.031 + 0.008*SL	0.025 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.045	0.031 + 0.007*SL	0.029 + 0.008*SL	0.024 + 0.008*SL
	t_{PLH}	0.151	0.141 + 0.005*SL	0.144 + 0.005*SL	0.145 + 0.004*SL
	t_{PHL}	0.193	0.181 + 0.006*SL	0.187 + 0.004*SL	0.194 + 0.004*SL
RN to QN	t_R	0.042	0.024 + 0.009*SL	0.019 + 0.010*SL	0.015 + 0.010*SL
	t_{PLH}	0.091	0.081 + 0.005*SL	0.083 + 0.005*SL	0.083 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fj2d2

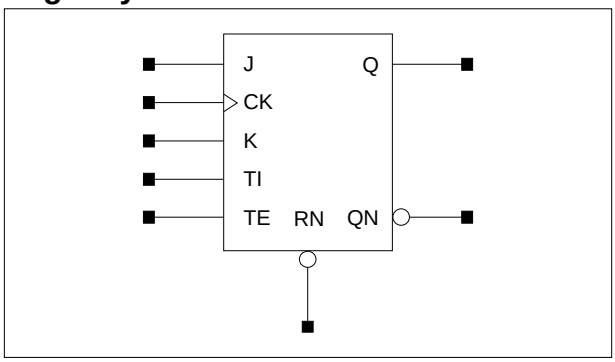
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.050	0.040 + 0.005*SL	0.040 + 0.005*SL	0.035 + 0.005*SL
	t_F	0.058	0.048 + 0.005*SL	0.052 + 0.004*SL	0.059 + 0.004*SL
	t_{PLH}	0.144	0.136 + 0.004*SL	0.142 + 0.003*SL	0.155 + 0.002*SL
	t_{PHL}	0.127	0.117 + 0.005*SL	0.125 + 0.003*SL	0.153 + 0.002*SL
RN to Q	t_F	0.145	0.137 + 0.004*SL	0.135 + 0.004*SL	0.149 + 0.004*SL
	t_{PHL}	0.426	0.413 + 0.007*SL	0.423 + 0.004*SL	0.463 + 0.003*SL
CK to QN	t_R	0.042	0.033 + 0.004*SL	0.032 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.042	0.034 + 0.004*SL	0.034 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.170	0.163 + 0.003*SL	0.168 + 0.002*SL	0.171 + 0.002*SL
	t_{PHL}	0.208	0.200 + 0.004*SL	0.206 + 0.002*SL	0.218 + 0.002*SL
RN to QN	t_R	0.032	0.022 + 0.005*SL	0.023 + 0.005*SL	0.013 + 0.005*SL
	t_{PLH}	0.089	0.083 + 0.003*SL	0.086 + 0.002*SL	0.088 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fj2s/fj2sd2

JK Flip-Flop with Reset, Scan, 1X/2X Drive

Logic Symbol



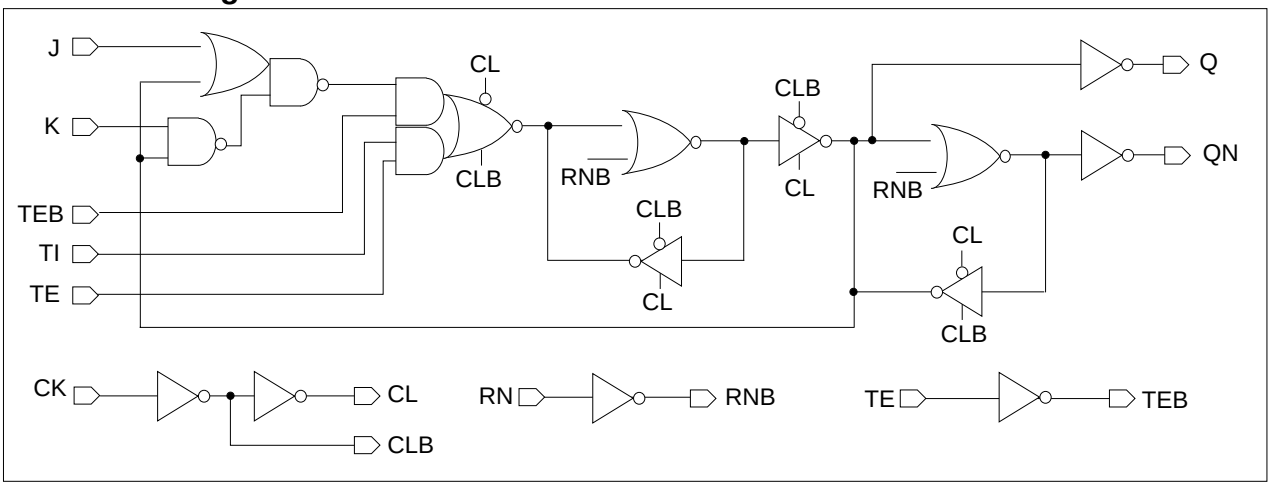
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	x	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
fj2s						*fj2sd2*						*fj2s*	*fj2sd2*
J	K	CK	RN	TI	TE	J	K	CK	RN	TI	TE		
0.7	0.6	1.0	1.0	0.9	1.6	0.7	0.6	1.0	1.0	0.9	1.6	12.67	13.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fj2s	fj2sd2
Input Setup Time (J to CK)	t_{SU}	0.160	0.161
Input Hold Time (J to CK)	t_{HD}	0.010	0.010
Input Setup Time (K to CK)	t_{SU}	0.160	0.161
Input Hold Time (K to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.110	0.112
Pulse Width High (CK)	t_{PWH}	0.096	0.119
Pulse Width Low (RN)	t_{PWL}	0.239	0.276
Recovery Time (RN to CK)	t_{RC}	0.020	0.020
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Input Setup Time (TI to CK)	t_{SU}	0.096	0.097
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	0.122	0.123
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj2s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.053	0.033 + 0.010*SL	0.035 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.060	0.041 + 0.010*SL	0.049 + 0.007*SL	0.045 + 0.008*SL
	t_{PLH}	0.134	0.120 + 0.007*SL	0.128 + 0.005*SL	0.135 + 0.005*SL
	t_{PHL}	0.127	0.111 + 0.008*SL	0.122 + 0.005*SL	0.140 + 0.004*SL
RN to Q	t_F	0.132	0.112 + 0.010*SL	0.118 + 0.008*SL	0.131 + 0.008*SL
	t_{PHL}	0.384	0.361 + 0.011*SL	0.378 + 0.007*SL	0.415 + 0.005*SL
CK to QN	t_R	0.045	0.029 + 0.008*SL	0.022 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.044	0.027 + 0.008*SL	0.030 + 0.008*SL	0.022 + 0.008*SL
	t_{PLH}	0.153	0.143 + 0.005*SL	0.146 + 0.005*SL	0.147 + 0.004*SL
	t_{PHL}	0.180	0.168 + 0.006*SL	0.174 + 0.004*SL	0.180 + 0.004*SL
RN to QN	t_R	0.040	0.021 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_{PLH}	0.091	0.081 + 0.005*SL	0.083 + 0.005*SL	0.084 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

fj2sd2

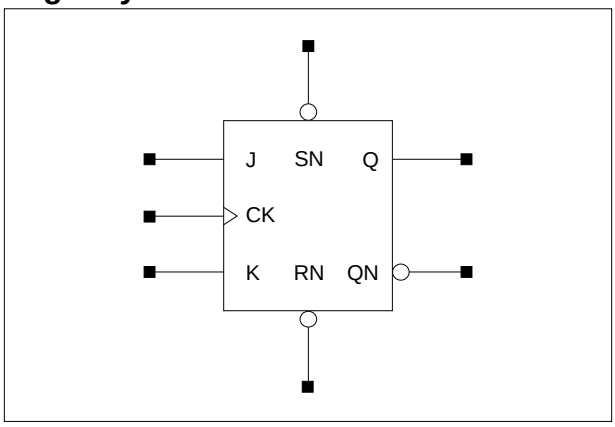
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.048	0.039 + 0.005*SL	0.037 + 0.005*SL	0.032 + 0.005*SL
	t_F	0.057	0.048 + 0.005*SL	0.051 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.134	0.126 + 0.004*SL	0.132 + 0.003*SL	0.143 + 0.002*SL
	t_{PHL}	0.130	0.120 + 0.005*SL	0.128 + 0.003*SL	0.154 + 0.002*SL
RN to Q	t_F	0.154	0.146 + 0.004*SL	0.144 + 0.004*SL	0.159 + 0.004*SL
	t_{PHL}	0.424	0.411 + 0.007*SL	0.421 + 0.004*SL	0.465 + 0.003*SL
CK to QN	t_R	0.040	0.031 + 0.005*SL	0.031 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.041	0.032 + 0.004*SL	0.035 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.174	0.167 + 0.003*SL	0.172 + 0.002*SL	0.175 + 0.002*SL
	t_{PHL}	0.198	0.191 + 0.004*SL	0.195 + 0.002*SL	0.208 + 0.002*SL
RN to QN	t_R	0.032	0.023 + 0.005*SL	0.022 + 0.005*SL	0.013 + 0.005*SL
	t_{PLH}	0.091	0.085 + 0.003*SL	0.088 + 0.002*SL	0.091 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

fj4/fj4d2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol



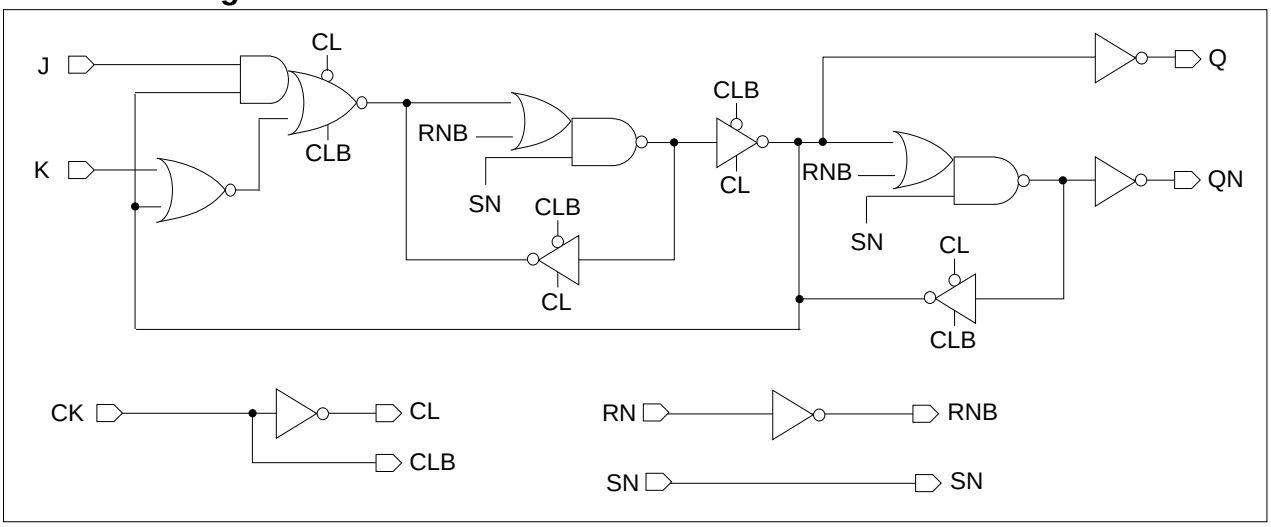
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	1	0

Cell Data

Input Load (SL)										Gate Count	
fj4					*fj4d2*					*fj4*	*fj4d2*
J	K	CK	RN	SN	J	K	CK	RN	SN		
0.9	0.5	1.0	1.0	2.4	0.9	0.5	1.0	1.0	2.3	10.67	11.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fj4	fj4d2
Input Setup Time (J to CK)	t_{SU}	0.100	0.100
Input Hold Time (J to CK)	t_{HD}	0.010	0.010
Input Setup Time (K to CK)	t_{SU}	0.100	0.100
Input Hold Time (K to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.098	0.99
Pulse Width High (CK)	t_{PWH}	0.107	0.132
Pulse Width Low (RN)	t_{PWL}	0.250	0.290
Pulse Width Low (SN)	t_{PWL}	0.149	0.175
Recovery Time (RN to CK)	t_{RC}	0.017	0.017
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.084	0.084
Recovery Time (SN to RN)	t_{RC}	0.092	0.094
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.055	0.035 + 0.010*SL	0.036 + 0.010*SL	0.029 + 0.010*SL
	t_F	0.061	0.042 + 0.010*SL	0.049 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.136	0.123 + 0.007*SL	0.130 + 0.005*SL	0.139 + 0.005*SL
	t_{PHL}	0.131	0.115 + 0.008*SL	0.125 + 0.005*SL	0.145 + 0.004*SL
RN to Q	t_F	0.131	0.112 + 0.010*SL	0.117 + 0.009*SL	0.133 + 0.008*SL
	t_{PHL}	0.399	0.376 + 0.011*SL	0.393 + 0.007*SL	0.429 + 0.005*SL
SN to Q	t_R	0.094	0.072 + 0.011*SL	0.078 + 0.010*SL	0.078 + 0.010*SL
	t_F	0.131	0.111 + 0.010*SL	0.117 + 0.009*SL	0.133 + 0.008*SL
	t_{PLH}	0.248	0.229 + 0.009*SL	0.242 + 0.006*SL	0.267 + 0.005*SL
	t_{PHL}	0.384	0.361 + 0.011*SL	0.378 + 0.007*SL	0.414 + 0.005*SL
CK to QN	t_R	0.050	0.032 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.047	0.031 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.173	0.161 + 0.006*SL	0.166 + 0.005*SL	0.169 + 0.004*SL
	t_{PHL}	0.193	0.180 + 0.006*SL	0.188 + 0.005*SL	0.196 + 0.004*SL
RN to QN	t_R	0.046	0.028 + 0.009*SL	0.023 + 0.010*SL	0.017 + 0.010*SL
	t_{PLH}	0.100	0.089 + 0.006*SL	0.093 + 0.005*SL	0.095 + 0.005*SL
SN to QN	t_R	0.050	0.036 + 0.007*SL	0.023 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.036	0.021 + 0.008*SL	0.020 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.073	0.061 + 0.006*SL	0.065 + 0.005*SL	0.068 + 0.005*SL
	t_{PHL}	0.066	0.055 + 0.005*SL	0.059 + 0.004*SL	0.062 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

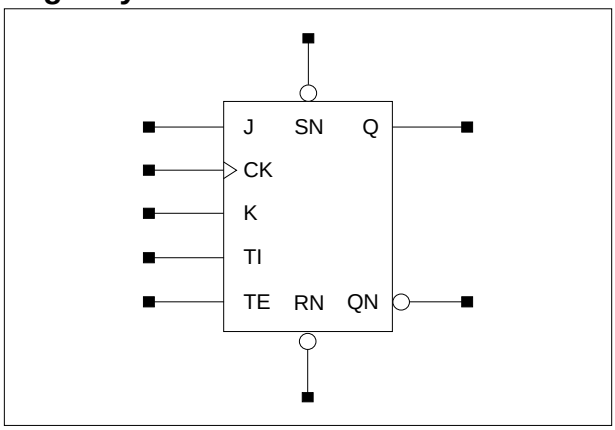
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.048	0.038 + 0.005*SL	0.038 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.058	0.049 + 0.004*SL	0.051 + 0.004*SL	0.057 + 0.004*SL
	t_{PLH}	0.137	0.128 + 0.004*SL	0.134 + 0.003*SL	0.147 + 0.002*SL
	t_{PHL}	0.134	0.124 + 0.005*SL	0.132 + 0.003*SL	0.157 + 0.002*SL
RN to Q	t_F	0.151	0.143 + 0.004*SL	0.142 + 0.004*SL	0.158 + 0.004*SL
	t_{PHL}	0.448	0.435 + 0.007*SL	0.445 + 0.004*SL	0.488 + 0.003*SL
SN to Q	t_R	0.096	0.085 + 0.006*SL	0.087 + 0.005*SL	0.094 + 0.005*SL
	t_F	0.151	0.143 + 0.004*SL	0.141 + 0.004*SL	0.156 + 0.004*SL
	t_{PLH}	0.274	0.263 + 0.006*SL	0.271 + 0.003*SL	0.304 + 0.002*SL
	t_{PHL}	0.433	0.419 + 0.007*SL	0.430 + 0.004*SL	0.472 + 0.003*SL
CK to QN	t_R	0.046	0.038 + 0.004*SL	0.036 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.045	0.036 + 0.005*SL	0.040 + 0.004*SL	0.036 + 0.004*SL
	t_{PLH}	0.196	0.189 + 0.004*SL	0.194 + 0.002*SL	0.201 + 0.002*SL
	t_{PHL}	0.213	0.206 + 0.004*SL	0.211 + 0.003*SL	0.226 + 0.002*SL
RN to QN	t_R	0.040	0.031 + 0.005*SL	0.031 + 0.005*SL	0.021 + 0.005*SL
	t_{PLH}	0.102	0.095 + 0.004*SL	0.100 + 0.002*SL	0.106 + 0.002*SL
SN to QN	t_R	0.043	0.031 + 0.006*SL	0.038 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.074	0.067 + 0.003*SL	0.071 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.066	0.060 + 0.003*SL	0.064 + 0.002*SL	0.070 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



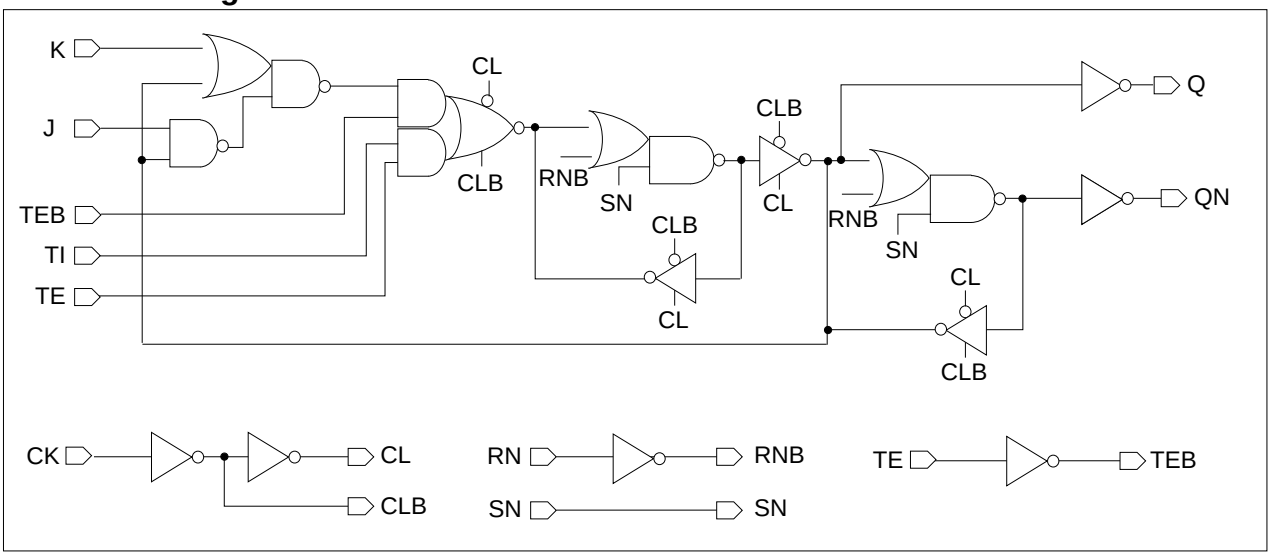
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	x	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	1	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)														Gate Count	
fj4s							*fj4sd2*							*fj4s*	*fj4sd2*
J	K	CK	RN	SN	TI	TE	J	K	CK	RN	SN	TI	TE		
0.7	0.6	1.0	1.0	2.4	0.9	1.6	0.7	0.7	1.0	1.0	2.3	0.9	1.6	13.00	13.67

Schematic Diagram



fj4s/fj4sd2

JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		fj4s	fj4sd2
Input Setup Time (J to CK)	t_{SU}	0.167	0.166
Input Hold Time (J to CK)	t_{HD}	0.010	0.010
Input Setup Time (K to CK)	t_{SU}	0.167	0.166
Input Hold Time (K to CK)	t_{HD}	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.120	0.122
Pulse Width High (CK)	t_{PWH}	0.102	0.127
Pulse Width Low (RN)	t_{PWL}	0.249	0.285
Pulse Width Low (SN)	t_{PWL}	0.142	0.166
Recovery Time (RN to CK)	t_{RC}	0.020	0.017
Removal Time (RN to CK)	t_{RM}	0.010	0.010
Recovery Time (SN to CK)	t_{RC}	0.010	0.010
Removal Time (SN to CK)	t_{RM}	0.095	0.094
Input Setup Time (TI to CK)	t_{SU}	0.101	0.100
Input Hold Time (TI to CK)	t_{HD}	0.010	0.010
Input Setup Time (TE to CK)	t_{SU}	124	0.124
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010
Recovery Time (SN to RN)	t_{RC}	0.098	0.097
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj4s

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.055	0.035 + 0.010*SL	0.035 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.058	0.040 + 0.009*SL	0.046 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.137	0.123 + 0.007*SL	0.130 + 0.005*SL	0.138 + 0.005*SL
	t_{PHL}	0.127	0.112 + 0.008*SL	0.122 + 0.005*SL	0.140 + 0.004*SL
RN to Q	t_F	0.134	0.114 + 0.010*SL	0.121 + 0.008*SL	0.133 + 0.008*SL
	t_{PHL}	0.402	0.379 + 0.011*SL	0.396 + 0.007*SL	0.433 + 0.005*SL
SN to Q	t_R	0.089	0.066 + 0.011*SL	0.073 + 0.010*SL	0.071 + 0.010*SL
	t_F	0.134	0.113 + 0.010*SL	0.121 + 0.008*SL	0.133 + 0.008*SL
	t_{PLH}	0.239	0.222 + 0.009*SL	0.233 + 0.006*SL	0.256 + 0.005*SL
	t_{PHL}	0.386	0.364 + 0.011*SL	0.380 + 0.007*SL	0.418 + 0.005*SL
CK to QN	t_R	0.050	0.033 + 0.009*SL	0.029 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.046	0.029 + 0.008*SL	0.032 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.170	0.158 + 0.006*SL	0.163 + 0.005*SL	0.166 + 0.004*SL
	t_{PHL}	0.194	0.181 + 0.006*SL	0.188 + 0.005*SL	0.196 + 0.004*SL
RN to QN	t_R	0.047	0.028 + 0.009*SL	0.026 + 0.010*SL	0.017 + 0.010*SL
	t_{PLH}	0.101	0.089 + 0.006*SL	0.094 + 0.005*SL	0.096 + 0.005*SL
SN to QN	t_R	0.050	0.035 + 0.007*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.036	0.021 + 0.007*SL	0.019 + 0.008*SL	0.016 + 0.008*SL
	t_{PLH}	0.073	0.062 + 0.006*SL	0.066 + 0.005*SL	0.068 + 0.005*SL
	t_{PHL}	0.066	0.055 + 0.005*SL	0.059 + 0.004*SL	0.062 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fj4sd2

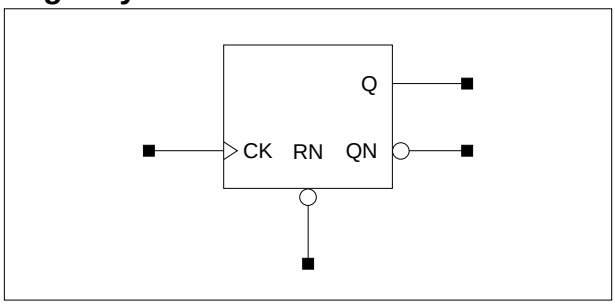
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.047	0.038 + 0.005*SL	0.037 + 0.005*SL	0.032 + 0.005*SL
	t_F	0.055	0.045 + 0.005*SL	0.049 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.137	0.129 + 0.004*SL	0.135 + 0.003*SL	0.147 + 0.002*SL
	t_{PHL}	0.130	0.121 + 0.005*SL	0.128 + 0.003*SL	0.153 + 0.002*SL
RN to Q	t_F	0.155	0.147 + 0.004*SL	0.147 + 0.004*SL	0.161 + 0.004*SL
	t_{PHL}	0.448	0.434 + 0.007*SL	0.445 + 0.004*SL	0.488 + 0.003*SL
SN to Q	t_R	0.092	0.082 + 0.005*SL	0.083 + 0.005*SL	0.088 + 0.005*SL
	t_F	0.155	0.147 + 0.004*SL	0.146 + 0.004*SL	0.160 + 0.004*SL
	t_{PLH}	0.263	0.252 + 0.005*SL	0.260 + 0.003*SL	0.291 + 0.002*SL
	t_{PHL}	0.431	0.418 + 0.007*SL	0.428 + 0.004*SL	0.472 + 0.003*SL
CK to QN	t_R	0.046	0.036 + 0.005*SL	0.037 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.045	0.037 + 0.004*SL	0.039 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.192	0.184 + 0.004*SL	0.190 + 0.002*SL	0.196 + 0.002*SL
	t_{PHL}	0.212	0.204 + 0.004*SL	0.210 + 0.003*SL	0.225 + 0.002*SL
RN to QN	t_R	0.039	0.028 + 0.006*SL	0.031 + 0.005*SL	0.020 + 0.005*SL
	t_{PLH}	0.102	0.095 + 0.004*SL	0.099 + 0.002*SL	0.105 + 0.002*SL
SN to QN	t_R	0.043	0.030 + 0.007*SL	0.038 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.024 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.074	0.067 + 0.004*SL	0.071 + 0.002*SL	0.078 + 0.002*SL
	t_{PHL}	0.066	0.059 + 0.003*SL	0.064 + 0.002*SL	0.070 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ft2/ft2d2

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



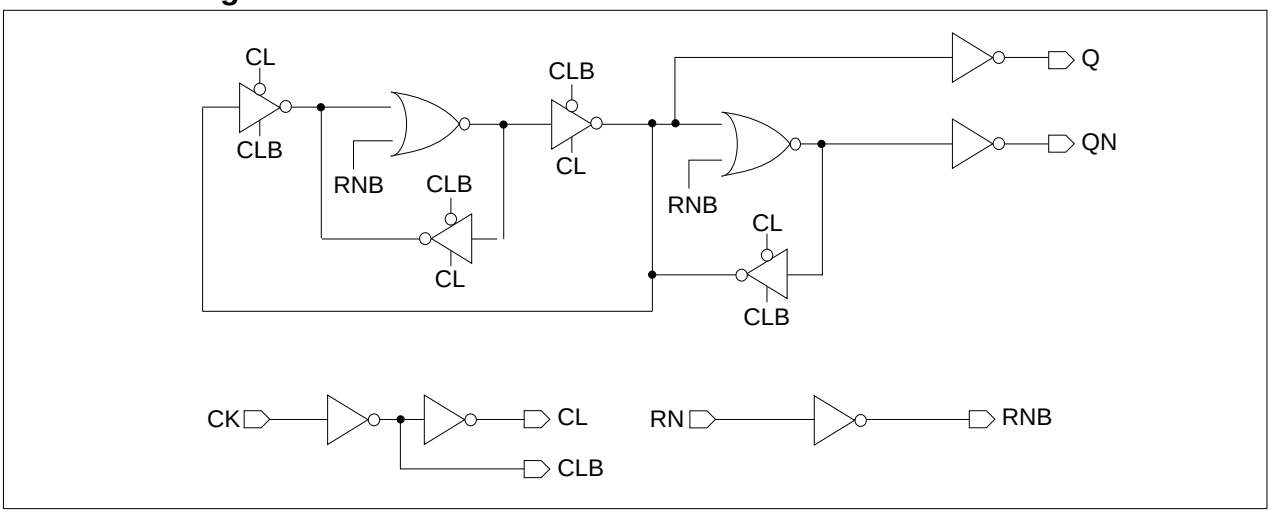
Truth Table

CK	RN	Q (n+1)	QN (n+1)
↑	1	QN (n)	Q (n)
↓	1	Q (n)	QN (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
ft2		*ft2d2*		*ft2*	*ft2d2*
CK	RN	CK	RN		
1.1	1.0	1.1	1.0	8.33	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ft2	ft2d2
Pulse Width Low (CK)	t_{PWL}	0.082	0.079
Pulse Width High (CK)	t_{PWH}	0.075	0.089
Pulse Width Low (RN)	t_{PWL}	0.214	0.244
Recovery Time (RN to CK)	t_{RC}	0.030	0.030
Removal Time (RN to CK)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ft2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.052	0.033 + 0.010*SL	0.032 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.056	0.037 + 0.010*SL	0.046 + 0.007*SL	0.041 + 0.008*SL
	t_{PLH}	0.130	0.117 + 0.006*SL	0.124 + 0.005*SL	0.130 + 0.005*SL
	t_{PHL}	0.113	0.098 + 0.008*SL	0.108 + 0.005*SL	0.125 + 0.004*SL
RN to Q	t_F	0.054	0.036 + 0.009*SL	0.041 + 0.007*SL	0.036 + 0.008*SL
	t_{PHL}	0.176	0.162 + 0.007*SL	0.171 + 0.005*SL	0.184 + 0.004*SL
CK to QN	t_R	0.045	0.028 + 0.009*SL	0.023 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.043	0.027 + 0.008*SL	0.029 + 0.008*SL	0.023 + 0.008*SL
	t_{PLH}	0.141	0.130 + 0.005*SL	0.133 + 0.005*SL	0.134 + 0.004*SL
	t_{PHL}	0.177	0.165 + 0.006*SL	0.171 + 0.004*SL	0.177 + 0.004*SL
RN to QN	t_R	0.040	0.022 + 0.009*SL	0.017 + 0.010*SL	0.014 + 0.010*SL
	t_{PLH}	0.090	0.080 + 0.005*SL	0.082 + 0.005*SL	0.083 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ft2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.046	0.037 + 0.005*SL	0.035 + 0.005*SL	0.029 + 0.005*SL
	t_F	0.054	0.045 + 0.004*SL	0.047 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.130	0.122 + 0.004*SL	0.127 + 0.003*SL	0.137 + 0.002*SL
	t_{PHL}	0.115	0.106 + 0.005*SL	0.113 + 0.003*SL	0.136 + 0.002*SL
RN to Q	t_F	0.052	0.042 + 0.005*SL	0.046 + 0.004*SL	0.044 + 0.004*SL
	t_{PHL}	0.180	0.171 + 0.004*SL	0.178 + 0.003*SL	0.198 + 0.002*SL
CK to QN	t_R	0.039	0.031 + 0.004*SL	0.029 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.040	0.031 + 0.004*SL	0.033 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.157	0.151 + 0.003*SL	0.154 + 0.002*SL	0.157 + 0.002*SL
	t_{PHL}	0.191	0.183 + 0.004*SL	0.189 + 0.002*SL	0.200 + 0.002*SL
RN to QN	t_R	0.031	0.021 + 0.005*SL	0.021 + 0.005*SL	0.013 + 0.005*SL
	t_{PLH}	0.089	0.083 + 0.003*SL	0.086 + 0.002*SL	0.088 + 0.002*SL

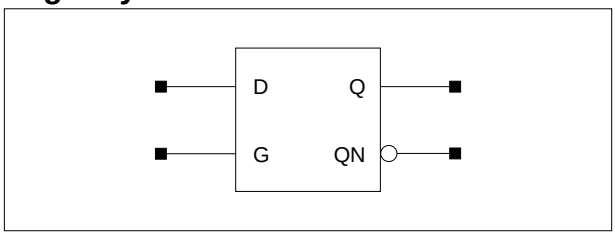
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

LATCHES

Cell List

Cell Name	Function Description
ld1	D Latch with Active High, 1X Drive
ld1d2	D Latch with Active High, 2X Drive
ld1d4	D Latch with Active High, 4X Drive
ld1q	D Latch with Active High, Q Output Only, 1X Drive
ld1qd2	D Latch with Active High, Q Output Only, 2X Drive
ld1qd4	D Latch with Active High, Q Output Only, 4X Drive
ld2	D Latch with Active High, Reset, 1X Drive
ld2d2	D Latch with Active High, Reset, 2X Drive
ld2q	D Latch with Active High, Reset, Q Output Only, 1X Drive
ld2qd2	D Latch with Active High, Reset, Q Output Only, 2X Drive
ld3	D Latch with Active High, Set, 1X Drive
ld3d2	D Latch with Active High, Set, 2X Drive
ld4	D Latch with Active High, Reset, Set, 1X Drive
ld4d2	D Latch with Active High, Reset, Set, 2X Drive
ld5	D Latch with Active Low, 1X Drive
ld5d2	D Latch with Active Low, 2X Drive
ld5q	D Latch with Active Low, Q Output Only, 1X Drive
ld5qd2	D Latch with Active Low, Q Output Only, 2X Drive
ld6	D Latch with Active Low, Reset, 1X Drive
ld6d2	D Latch with Active Low, Reset, 2X Drive
ld6q	D Latch with Active Low, Reset, Q Output Only, 1X Drive
ld6qd2	D Latch with Active Low, Reset, Q Output Only, 2X Drive

Logic Symbol



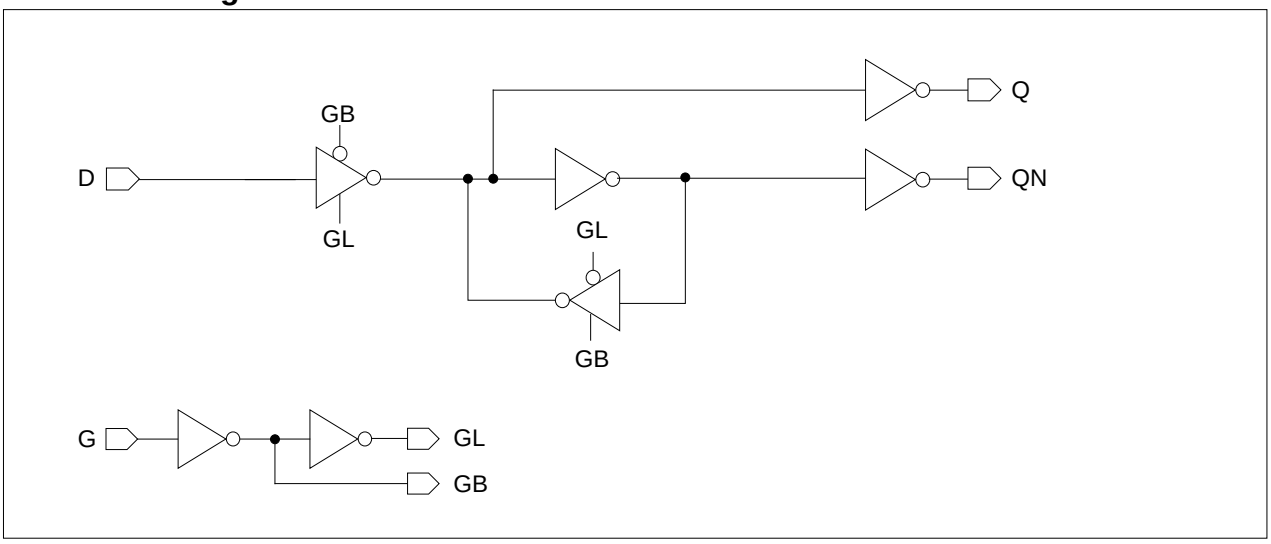
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count		
ld1		*ld1d2*		*ld1d4*		*ld1*	*ld1d2*	*ld1d4*
D	G	D	G	D	G			
1.1	1.1	1.1	1.1	1.1	1.1	4.33	5.33	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		ld1	ld1d2	ld1d4
Input Setup Time (D to G)	t_{SU}	0.053	0.074	0.056
Input Hold Time (D to G)	t_{HD}	0.010	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.055	0.075	0.053

ld1/ld1d2/ld1d4

D Latch with Active High, 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.050	0.029 + 0.010*SL	0.032 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.047	0.029 + 0.009*SL	0.034 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.080	0.068 + 0.006*SL	0.074 + 0.005*SL	0.079 + 0.004*SL
	t_{PHL}	0.087	0.074 + 0.006*SL	0.081 + 0.005*SL	0.091 + 0.004*SL
G to Q	t_R	0.048	0.028 + 0.010*SL	0.029 + 0.010*SL	0.022 + 0.010*SL
	t_F	0.045	0.026 + 0.009*SL	0.033 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.102	0.090 + 0.006*SL	0.095 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.085	0.072 + 0.006*SL	0.080 + 0.005*SL	0.090 + 0.004*SL
D to QN	t_R	0.042	0.023 + 0.009*SL	0.020 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.036	0.021 + 0.007*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.110	0.099 + 0.005*SL	0.102 + 0.005*SL	0.102 + 0.004*SL
	t_{PHL}	0.110	0.100 + 0.005*SL	0.103 + 0.004*SL	0.106 + 0.004*SL
G to QN	t_R	0.042	0.024 + 0.009*SL	0.020 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.036	0.019 + 0.008*SL	0.022 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.108	0.098 + 0.005*SL	0.100 + 0.005*SL	0.101 + 0.004*SL
	t_{PHL}	0.131	0.120 + 0.005*SL	0.124 + 0.004*SL	0.126 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld1d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.043	0.032 + 0.005*SL	0.035 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.042	0.034 + 0.004*SL	0.034 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.083	0.076 + 0.004*SL	0.081 + 0.003*SL	0.091 + 0.002*SL
	t_{PHL}	0.090	0.082 + 0.004*SL	0.088 + 0.003*SL	0.104 + 0.002*SL
G to Q	t_R	0.043	0.033 + 0.005*SL	0.033 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.041	0.032 + 0.005*SL	0.035 + 0.004*SL	0.033 + 0.004*SL
	t_{PLH}	0.104	0.096 + 0.004*SL	0.101 + 0.003*SL	0.111 + 0.002*SL
	t_{PHL}	0.088	0.080 + 0.004*SL	0.086 + 0.003*SL	0.103 + 0.002*SL
D to QN	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.025 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.126 + 0.002*SL
	t_{PHL}	0.126	0.120 + 0.003*SL	0.124 + 0.002*SL	0.130 + 0.002*SL
G to QN	t_R	0.036	0.028 + 0.004*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.026 + 0.004*SL	0.017 + 0.004*SL
	t_{PLH}	0.125	0.119 + 0.003*SL	0.123 + 0.002*SL	0.125 + 0.002*SL
	t_{PHL}	0.147	0.140 + 0.003*SL	0.145 + 0.002*SL	0.150 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld1d4

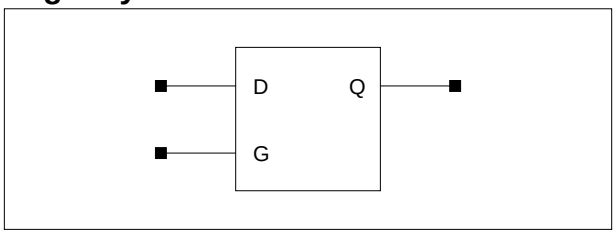
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.031	0.026 + 0.003*SL	0.027 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.141 + 0.001*SL
	t_{PHL}	0.138	0.134 + 0.002*SL	0.137 + 0.001*SL	0.145 + 0.001*SL
G to Q	t_R	0.031	0.027 + 0.002*SL	0.026 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.028	0.024 + 0.002*SL	0.025 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.159	0.156 + 0.002*SL	0.158 + 0.001*SL	0.162 + 0.001*SL
	t_{PHL}	0.137	0.133 + 0.002*SL	0.136 + 0.001*SL	0.144 + 0.001*SL
D to QN	t_R	0.034	0.030 + 0.002*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.030	0.027 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.118	0.114 + 0.002*SL	0.116 + 0.001*SL	0.121 + 0.001*SL
	t_{PHL}	0.111	0.108 + 0.002*SL	0.110 + 0.001*SL	0.119 + 0.001*SL
G to QN	t_R	0.033	0.029 + 0.002*SL	0.028 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.030	0.027 + 0.002*SL	0.026 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.116	0.113 + 0.002*SL	0.115 + 0.001*SL	0.120 + 0.001*SL
	t_{PHL}	0.133	0.129 + 0.002*SL	0.132 + 0.001*SL	0.140 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 61, *Group3 : 61 < SL

ld1q/ld1qd2/ld1qd4

D Latch with Active High, Q Output Only, 1X/2X/4X Drive

Logic Symbol



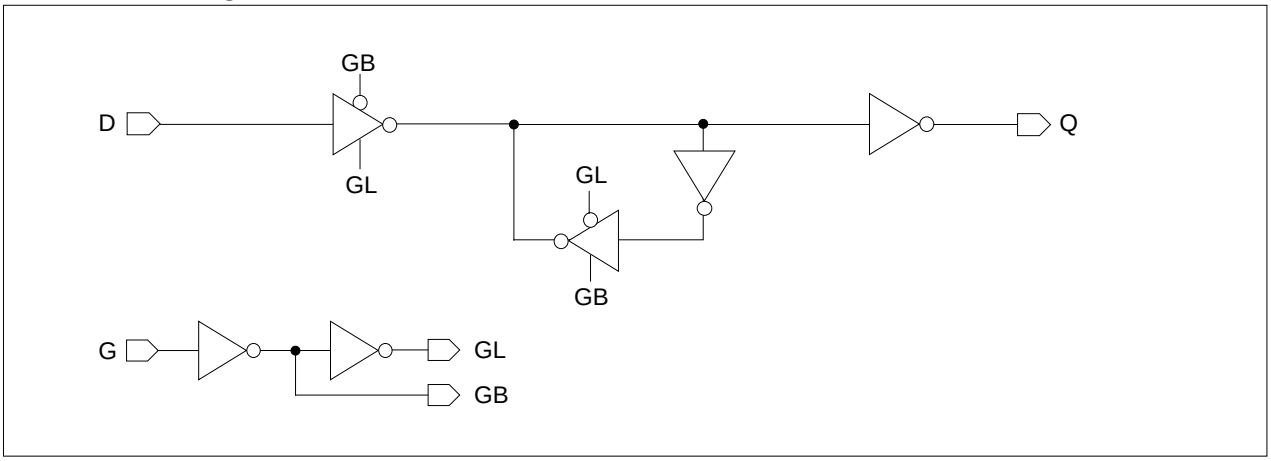
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)						Gate Count		
ld1q		*ld1qd2*		*ld1qd4*		*ld1q*	*ld1qd2*	*ld1qd4*
D	G	D	G	D	G			
1.1	1.1	1.1	1.1	1.1	1.1	4.00	4.33	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		ld1q	ld1qd2	ld1qd4
Input Setup Time (D to G)	t_{SU}	0.051	0.063	0.044
Input Hold Time (D to G)	t_{HD}	0.010	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.045	0.059	0.039

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld1q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.047	0.027 + 0.010*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.044	0.027 + 0.009*SL	0.031 + 0.007*SL	0.023 + 0.008*SL
	t_{PLH}	0.077	0.065 + 0.006*SL	0.070 + 0.005*SL	0.074 + 0.004*SL
	t_{PHL}	0.082	0.069 + 0.006*SL	0.077 + 0.004*SL	0.084 + 0.004*SL
G to Q	t_R	0.046	0.027 + 0.010*SL	0.026 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.043	0.025 + 0.009*SL	0.030 + 0.008*SL	0.023 + 0.008*SL
	t_{PLH}	0.098	0.086 + 0.006*SL	0.091 + 0.005*SL	0.095 + 0.004*SL
	t_{PHL}	0.081	0.068 + 0.006*SL	0.075 + 0.005*SL	0.083 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld1qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.043	0.033 + 0.005*SL	0.033 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.041	0.030 + 0.005*SL	0.037 + 0.004*SL	0.031 + 0.004*SL
	t_{PLH}	0.080	0.073 + 0.004*SL	0.077 + 0.003*SL	0.086 + 0.002*SL
	t_{PHL}	0.086	0.079 + 0.004*SL	0.084 + 0.002*SL	0.098 + 0.002*SL
G to Q	t_R	0.041	0.030 + 0.005*SL	0.032 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.039	0.030 + 0.005*SL	0.034 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.101	0.093 + 0.004*SL	0.098 + 0.003*SL	0.107 + 0.002*SL
	t_{PHL}	0.085	0.077 + 0.004*SL	0.083 + 0.002*SL	0.097 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ld1qd4

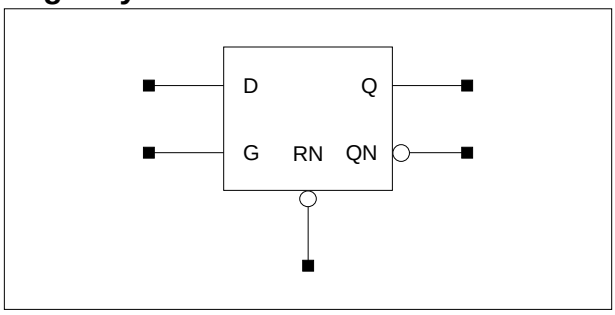
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.032	0.027 + 0.003*SL	0.028 + 0.002*SL	0.017 + 0.003*SL
	t_F	0.029	0.025 + 0.002*SL	0.025 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.124	0.120 + 0.002*SL	0.123 + 0.001*SL	0.127 + 0.001*SL
	t_{PHL}	0.123	0.120 + 0.002*SL	0.122 + 0.001*SL	0.131 + 0.001*SL
G to Q	t_R	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.016 + 0.003*SL
	t_F	0.029	0.024 + 0.002*SL	0.026 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.146	0.142 + 0.002*SL	0.144 + 0.001*SL	0.149 + 0.001*SL
	t_{PHL}	0.122	0.119 + 0.002*SL	0.121 + 0.001*SL	0.130 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

ld2/ld2d2

D Latch with Active High, Reset, 1X/2X Drive

Logic Symbol



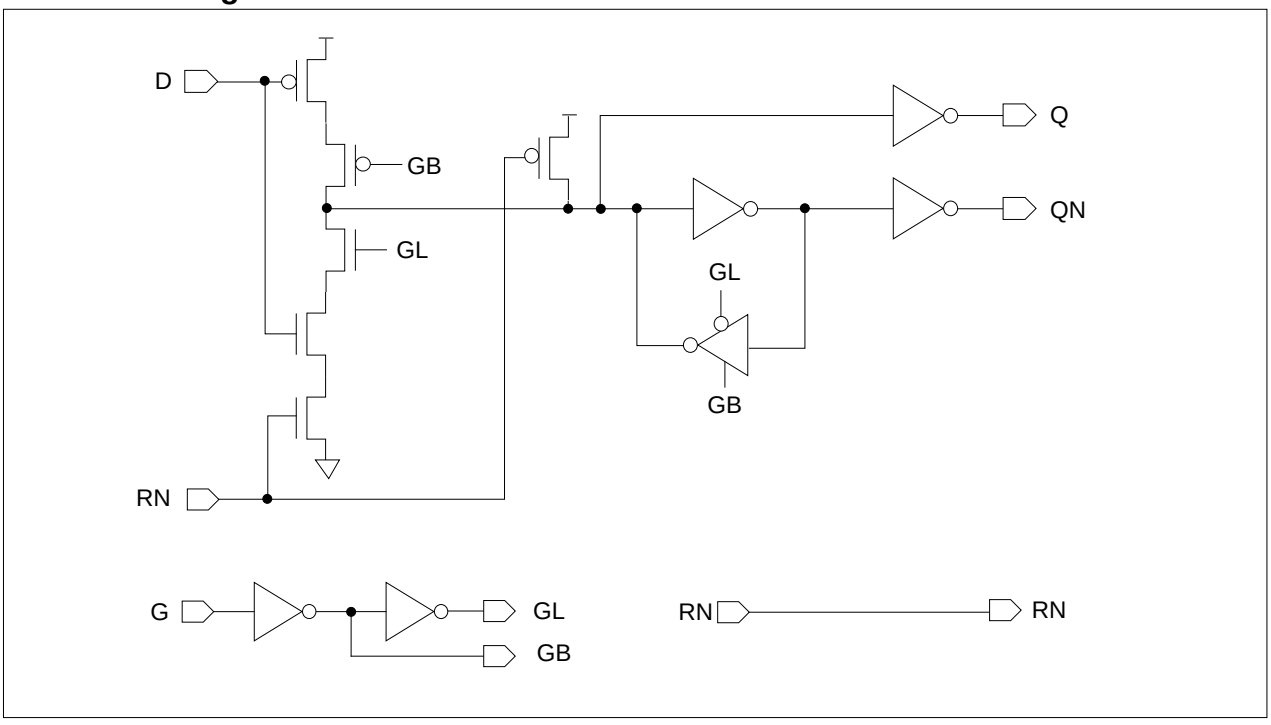
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
ld2			*ld2d2*			*ld2*	*ld2d2*
D	G	RN	D	G	RN		
1.1	1.1	0.8	1.1	1.1	0.8	5.00	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld2	ld2d2
Input Setup Time (D to G)	t_{SU}	0.062	0.081
Input Hold Time (D to G)	t_{HD}	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.066	0.087
Pulse Width Low (RN)	t_{PWL}	0.105	0.140
Recovery Time (RN to G)	t_{RC}	0.033	0.052
Removal Time (RN to G)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.055	0.034 + 0.010*SL	0.038 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.049	0.032 + 0.008*SL	0.036 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.092	0.079 + 0.007*SL	0.086 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.094	0.080 + 0.007*SL	0.088 + 0.005*SL	0.100 + 0.004*SL
G to Q	t_R	0.055	0.033 + 0.011*SL	0.038 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.049	0.030 + 0.009*SL	0.037 + 0.007*SL	0.030 + 0.008*SL
	t_{PLH}	0.114	0.100 + 0.007*SL	0.107 + 0.005*SL	0.116 + 0.004*SL
	t_{PHL}	0.091	0.078 + 0.007*SL	0.086 + 0.005*SL	0.098 + 0.004*SL
RN to Q	t_R	0.055	0.034 + 0.010*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.062	0.043 + 0.010*SL	0.052 + 0.007*SL	0.044 + 0.008*SL
	t_{PLH}	0.091	0.078 + 0.007*SL	0.085 + 0.005*SL	0.093 + 0.004*SL
	t_{PHL}	0.111	0.095 + 0.008*SL	0.107 + 0.005*SL	0.125 + 0.004*SL
D to QN	t_R	0.042	0.024 + 0.009*SL	0.021 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.117	0.107 + 0.005*SL	0.109 + 0.005*SL	0.110 + 0.004*SL
	t_{PHL}	0.123	0.112 + 0.005*SL	0.117 + 0.004*SL	0.119 + 0.004*SL
G to QN	t_R	0.042	0.024 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.022 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.116	0.106 + 0.005*SL	0.108 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.144	0.134 + 0.005*SL	0.138 + 0.004*SL	0.140 + 0.004*SL
RN to QN	t_R	0.045	0.029 + 0.008*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.038	0.022 + 0.008*SL	0.023 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.136	0.125 + 0.005*SL	0.129 + 0.005*SL	0.129 + 0.004*SL
	t_{PHL}	0.122	0.111 + 0.005*SL	0.116 + 0.004*SL	0.118 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld2/ld2d2

D Latch with Active High, Reset, 1X/2X Drive

Switching Characteristics

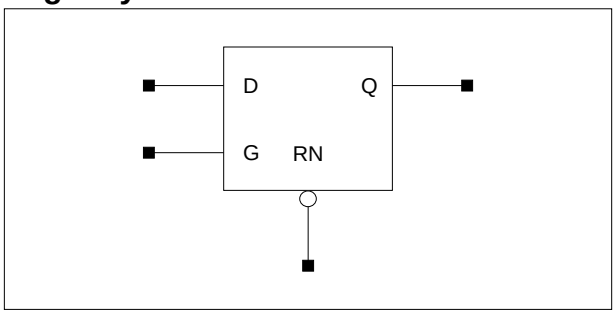
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.047	0.037 + 0.005*SL	0.038 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.038 + 0.004*SL	0.038 + 0.004*SL
	t_{PLH}	0.094	0.086 + 0.004*SL	0.092 + 0.003*SL	0.106 + 0.002*SL
	t_{PHL}	0.096	0.087 + 0.004*SL	0.094 + 0.003*SL	0.112 + 0.002*SL
G to Q	t_R	0.048	0.037 + 0.005*SL	0.040 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.043	0.034 + 0.005*SL	0.037 + 0.004*SL	0.037 + 0.004*SL
	t_{PLH}	0.115	0.107 + 0.004*SL	0.113 + 0.003*SL	0.127 + 0.002*SL
	t_{PHL}	0.093	0.085 + 0.004*SL	0.091 + 0.003*SL	0.110 + 0.002*SL
RN to Q	t_R	0.049	0.038 + 0.006*SL	0.041 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.059	0.050 + 0.004*SL	0.052 + 0.004*SL	0.054 + 0.004*SL
	t_{PLH}	0.093	0.085 + 0.004*SL	0.091 + 0.003*SL	0.105 + 0.002*SL
	t_{PHL}	0.113	0.103 + 0.005*SL	0.111 + 0.003*SL	0.137 + 0.002*SL
D to QN	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.034	0.026 + 0.004*SL	0.028 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.134	0.128 + 0.003*SL	0.132 + 0.002*SL	0.134 + 0.002*SL
	t_{PHL}	0.141	0.134 + 0.003*SL	0.139 + 0.002*SL	0.145 + 0.002*SL
G to QN	t_R	0.038	0.029 + 0.004*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.035	0.027 + 0.004*SL	0.028 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.132	0.126 + 0.003*SL	0.130 + 0.002*SL	0.132 + 0.002*SL
	t_{PHL}	0.162	0.155 + 0.003*SL	0.160 + 0.002*SL	0.166 + 0.002*SL
RN to QN	t_R	0.042	0.034 + 0.004*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.035	0.027 + 0.004*SL	0.029 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.156	0.149 + 0.003*SL	0.153 + 0.002*SL	0.156 + 0.002*SL
	t_{PHL}	0.140	0.133 + 0.003*SL	0.137 + 0.002*SL	0.144 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



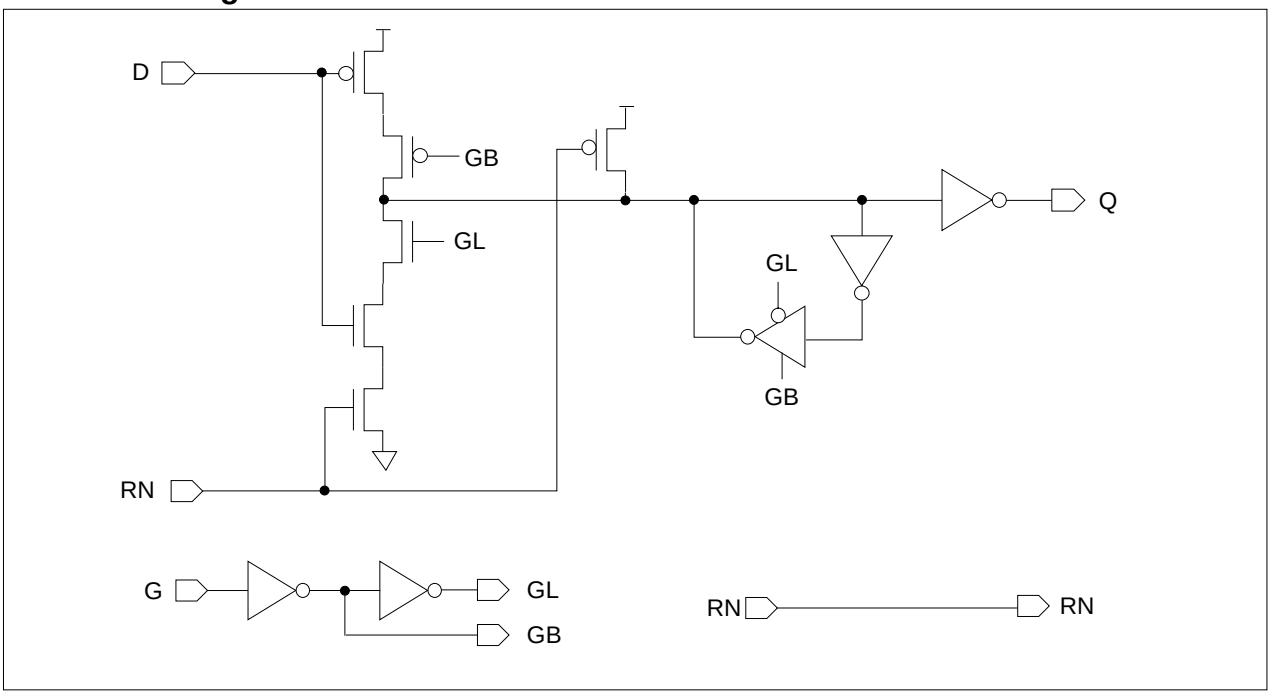
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
ld2q			*ld2qd2*			*ld2q*	*ld2qd2*
D	G	RN	D	G	RN		
1.1	1.1	0.8	1.1	1.1	0.8	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld2q	ld2qd2
Input Setup Time (D to G)	t_{SU}	0.052	0.068
Input Hold Time (D to G)	t_{HD}	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.057	0.072
Pulse Width Low (RN)	t_{PWL}	0.085	0.106
Recovery Time (RN to G)	t_{RC}	0.029	0.044
Removal Time (RN to G)	t_{RM}	0.010	0.010

ld2q/ld2qd2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld2q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.054	0.034 + 0.010*SL	0.034 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.047	0.030 + 0.009*SL	0.035 + 0.007*SL	0.027 + 0.008*SL
	t_{PLH}	0.089	0.076 + 0.006*SL	0.083 + 0.005*SL	0.089 + 0.004*SL
	t_{PHL}	0.090	0.077 + 0.007*SL	0.085 + 0.005*SL	0.094 + 0.004*SL
G to Q	t_R	0.053	0.033 + 0.010*SL	0.035 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.046	0.029 + 0.009*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.111	0.098 + 0.006*SL	0.105 + 0.005*SL	0.111 + 0.004*SL
	t_{PHL}	0.087	0.074 + 0.007*SL	0.082 + 0.005*SL	0.091 + 0.004*SL
RN to Q	t_R	0.055	0.036 + 0.010*SL	0.036 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.060	0.043 + 0.009*SL	0.049 + 0.007*SL	0.040 + 0.008*SL
	t_{PLH}	0.089	0.076 + 0.006*SL	0.082 + 0.005*SL	0.089 + 0.004*SL
	t_{PHL}	0.108	0.092 + 0.008*SL	0.104 + 0.005*SL	0.118 + 0.004*SL

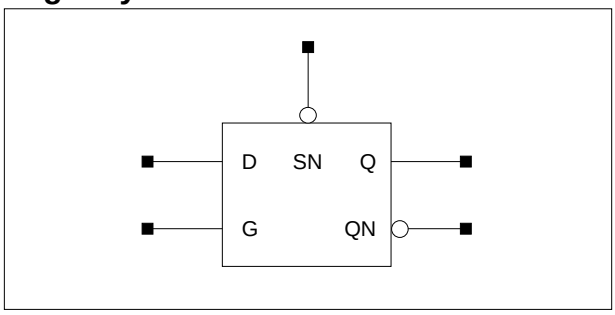
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld2qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.047	0.036 + 0.006*SL	0.040 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.043	0.033 + 0.005*SL	0.037 + 0.004*SL	0.033 + 0.004*SL
	t_{PLH}	0.091	0.083 + 0.004*SL	0.089 + 0.003*SL	0.101 + 0.002*SL
	t_{PHL}	0.093	0.085 + 0.004*SL	0.091 + 0.003*SL	0.106 + 0.002*SL
G to Q	t_R	0.047	0.035 + 0.006*SL	0.039 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.042	0.033 + 0.004*SL	0.036 + 0.004*SL	0.032 + 0.004*SL
	t_{PLH}	0.113	0.105 + 0.004*SL	0.110 + 0.003*SL	0.123 + 0.002*SL
	t_{PHL}	0.089	0.081 + 0.004*SL	0.087 + 0.003*SL	0.103 + 0.002*SL
RN to Q	t_R	0.048	0.035 + 0.007*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.058	0.049 + 0.005*SL	0.053 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.091	0.083 + 0.004*SL	0.088 + 0.003*SL	0.100 + 0.002*SL
	t_{PHL}	0.110	0.100 + 0.005*SL	0.108 + 0.003*SL	0.131 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



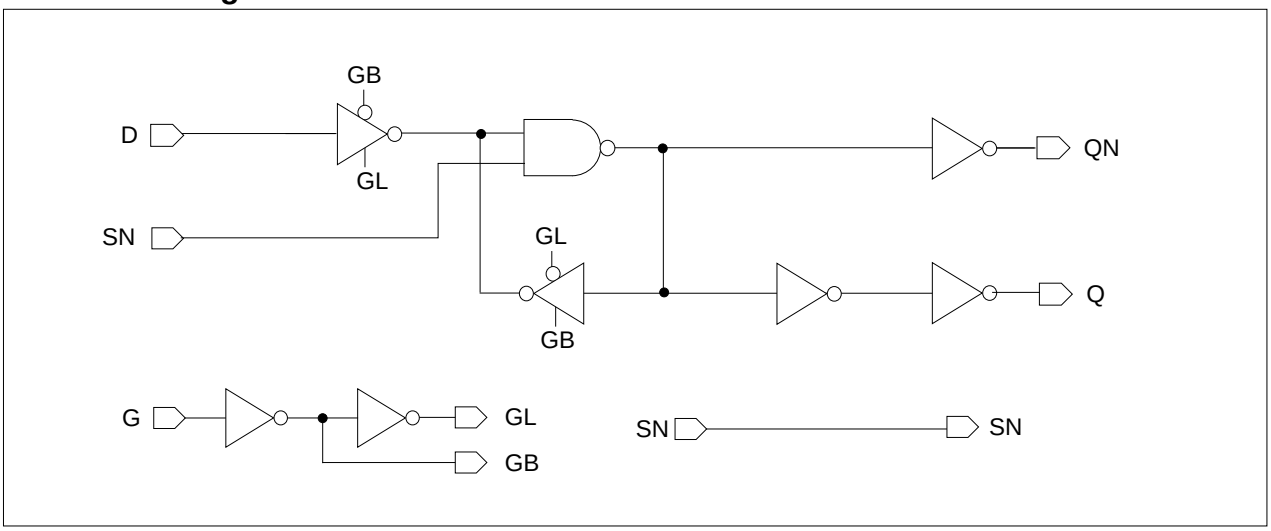
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
ld3			*ld3d2*			*ld3*	*ld3d2*
D	G	SN	D	G	SN		
1.1	1.1	1.0	1.1	1.1	1.1	5.33	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld3	ld3d2
Input Setup Time (D to G)	t_{SU}	0.046	0.051
Input Hold Time (D to G)	t_{HD}	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.043	0.047
Pulse Width Low (SN)	t_{PWL}	0.096	0.100
Recovery Time (SN to G)	t_{RC}	0.010	0.010
Removal Time (SN to G)	t_{RM}	0.051	0.046

ld3/ld3d2

D Latch with Active High, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.035	0.019 + 0.008*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.130	0.120 + 0.005*SL	0.122 + 0.005*SL	0.123 + 0.004*SL
	t_{PHL}	0.129	0.119 + 0.005*SL	0.122 + 0.004*SL	0.124 + 0.004*SL
G to Q	t_R	0.041	0.023 + 0.009*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.035	0.019 + 0.008*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.152	0.142 + 0.005*SL	0.144 + 0.005*SL	0.145 + 0.004*SL
	t_{PHL}	0.128	0.118 + 0.005*SL	0.122 + 0.004*SL	0.123 + 0.004*SL
SN to Q	t_R	0.041	0.023 + 0.009*SL	0.020 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.034	0.017 + 0.008*SL	0.020 + 0.008*SL	0.012 + 0.008*SL
	t_{PLH}	0.096	0.086 + 0.005*SL	0.088 + 0.005*SL	0.089 + 0.004*SL
	t_{PHL}	0.085	0.075 + 0.005*SL	0.078 + 0.004*SL	0.080 + 0.004*SL
D to QN	t_R	0.043	0.024 + 0.010*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.021 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.105	0.094 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.105	0.094 + 0.006*SL	0.099 + 0.004*SL	0.103 + 0.004*SL
G to QN	t_R	0.043	0.024 + 0.010*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.021 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.104	0.093 + 0.006*SL	0.097 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.127	0.116 + 0.006*SL	0.121 + 0.004*SL	0.125 + 0.004*SL
SN to QN	t_R	0.043	0.023 + 0.010*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.038	0.023 + 0.008*SL	0.022 + 0.008*SL	0.017 + 0.008*SL
	t_{PLH}	0.061	0.050 + 0.005*SL	0.053 + 0.005*SL	0.056 + 0.004*SL
	t_{PHL}	0.071	0.060 + 0.006*SL	0.065 + 0.004*SL	0.069 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld3d2

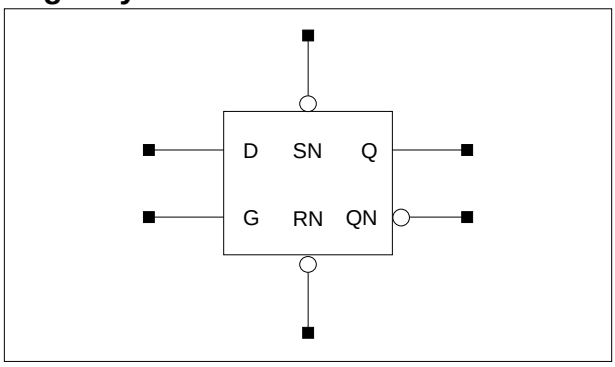
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.034	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.030	0.023 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.140	0.134 + 0.003*SL	0.137 + 0.002*SL	0.139 + 0.002*SL
	t_{PHL}	0.142	0.136 + 0.003*SL	0.139 + 0.002*SL	0.143 + 0.002*SL
G to Q	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.162	0.156 + 0.003*SL	0.159 + 0.002*SL	0.161 + 0.002*SL
	t_{PHL}	0.141	0.135 + 0.003*SL	0.138 + 0.002*SL	0.143 + 0.002*SL
SN to Q	t_R	0.035	0.025 + 0.005*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.103	0.097 + 0.003*SL	0.100 + 0.002*SL	0.102 + 0.002*SL
	t_{PHL}	0.096	0.090 + 0.003*SL	0.093 + 0.002*SL	0.097 + 0.002*SL
D to QN	t_R	0.036	0.027 + 0.005*SL	0.025 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.031	0.023 + 0.004*SL	0.023 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.003*SL	0.105 + 0.002*SL	0.112 + 0.002*SL
	t_{PHL}	0.104	0.097 + 0.003*SL	0.102 + 0.002*SL	0.110 + 0.002*SL
G to QN	t_R	0.036	0.026 + 0.005*SL	0.026 + 0.005*SL	0.019 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.107	0.100 + 0.004*SL	0.105 + 0.002*SL	0.111 + 0.002*SL
	t_{PHL}	0.126	0.119 + 0.003*SL	0.124 + 0.002*SL	0.132 + 0.002*SL
SN to QN	t_R	0.036	0.028 + 0.004*SL	0.025 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.023 + 0.004*SL	0.020 + 0.004*SL
	t_{PLH}	0.062	0.056 + 0.003*SL	0.060 + 0.002*SL	0.065 + 0.002*SL
	t_{PHL}	0.068	0.061 + 0.003*SL	0.066 + 0.002*SL	0.074 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

ld4/ld4d2

D Latch with Active High, Reset, Set, 1X/2X Drive

Logic Symbol



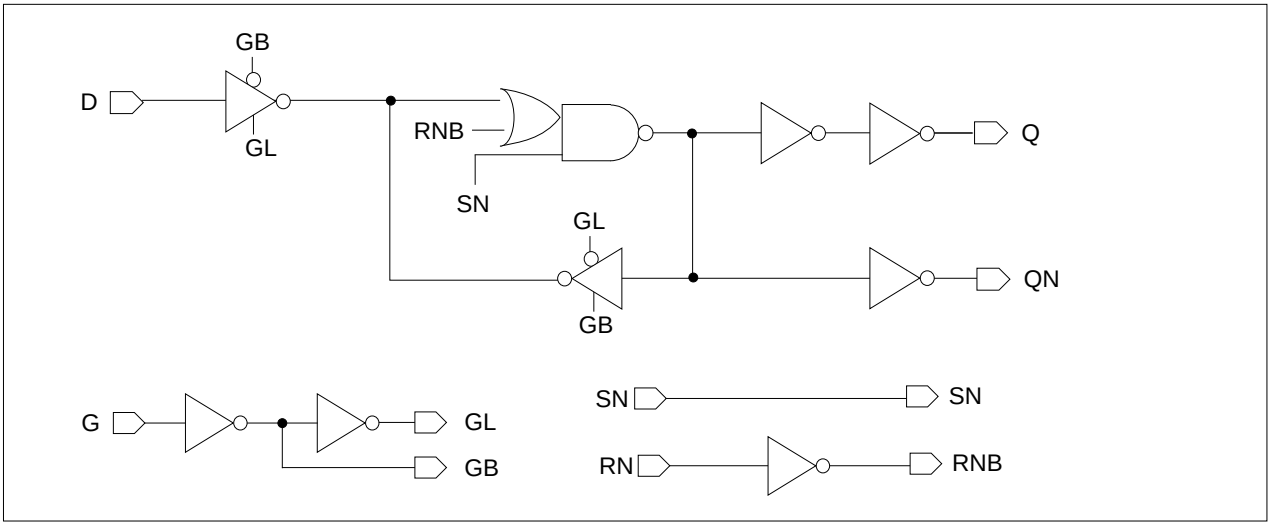
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
ld4				*ld4d2*				*ld4*	*ld4d2*
D	G	SN	RN	D	G	SN	RN		
1.1	1.1	1.1	1.0	1.1	1.1	1.1	1.0	6.33	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld4	ld4d2
Input Setup Time (D to G)	t_{SU}	0.051	0.052
Input Hold Time (D to G)	t_{HD}	0.010	0.010
Pulse Width High (G)	t_{PWH}	0.047	0.050
Pulse Width Low (SN)	t_{PWL}	0.095	0.103
Recovery Time (SN to G)	t_{RC}	0.010	0.010
Removal Time (SN to G)	t_{RM}	0.047	0.042
Pulse Width Low (RN)	t_{PWL}	0.123	0.129
Recovery Time (RN to G)	t_{RC}	0.010	0.010
Removal Time (RN to G)	t_{RM}	0.027	0.023
Recovery Time (SN to RN)	t_{RC}	0.103	0.111
Removal Time (SN to RN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.042	0.024 + 0.009*SL	0.021 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.020 + 0.008*SL	0.021 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.149	0.139 + 0.005*SL	0.142 + 0.004*SL	0.142 + 0.004*SL
	t_{PHL}	0.139	0.129 + 0.005*SL	0.133 + 0.004*SL	0.134 + 0.004*SL
G to Q	t_R	0.042	0.025 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.019 + 0.008*SL	0.021 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.172	0.162 + 0.005*SL	0.165 + 0.005*SL	0.165 + 0.004*SL
	t_{PHL}	0.138	0.128 + 0.005*SL	0.132 + 0.004*SL	0.134 + 0.004*SL
SN to Q	t_R	0.039	0.020 + 0.009*SL	0.018 + 0.010*SL	0.012 + 0.010*SL
	t_F	0.034	0.018 + 0.008*SL	0.020 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.092	0.082 + 0.005*SL	0.084 + 0.005*SL	0.084 + 0.004*SL
	t_{PHL}	0.088	0.078 + 0.005*SL	0.081 + 0.004*SL	0.083 + 0.004*SL
RN to Q	t_R	0.042	0.025 + 0.009*SL	0.019 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.035	0.019 + 0.008*SL	0.021 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.133	0.123 + 0.005*SL	0.125 + 0.005*SL	0.126 + 0.004*SL
	t_{PHL}	0.119	0.109 + 0.005*SL	0.112 + 0.004*SL	0.114 + 0.004*SL
D to QN	t_R	0.044	0.025 + 0.010*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.049	0.031 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.113	0.102 + 0.006*SL	0.106 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.128	0.114 + 0.007*SL	0.122 + 0.005*SL	0.135 + 0.004*SL
G to QN	t_R	0.045	0.025 + 0.010*SL	0.024 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.049	0.032 + 0.009*SL	0.036 + 0.008*SL	0.034 + 0.008*SL
	t_{PLH}	0.112	0.100 + 0.006*SL	0.105 + 0.005*SL	0.109 + 0.004*SL
	t_{PHL}	0.151	0.137 + 0.007*SL	0.146 + 0.005*SL	0.158 + 0.004*SL
SN to QN	t_R	0.043	0.024 + 0.010*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.038	0.023 + 0.008*SL	0.023 + 0.008*SL	0.018 + 0.008*SL
	t_{PLH}	0.063	0.052 + 0.005*SL	0.055 + 0.005*SL	0.057 + 0.004*SL
	t_{PHL}	0.071	0.060 + 0.006*SL	0.066 + 0.004*SL	0.070 + 0.004*SL
RN to QN	t_R	0.045	0.027 + 0.009*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.049	0.031 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.008*SL
	t_{PLH}	0.093	0.081 + 0.006*SL	0.086 + 0.005*SL	0.090 + 0.004*SL
	t_{PHL}	0.112	0.098 + 0.007*SL	0.106 + 0.005*SL	0.119 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

ld4/ld4d2

D Latch with Active High, Reset, Set, 1X/2X Drive

Switching Characteristics

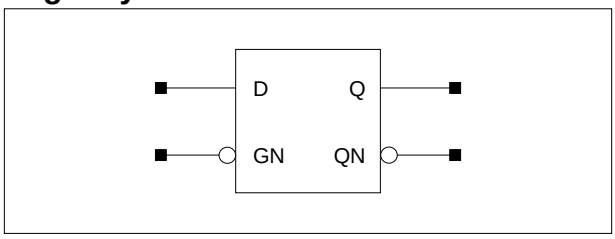
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.036	0.028 + 0.004*SL	0.025 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.165	0.158 + 0.003*SL	0.162 + 0.002*SL	0.164 + 0.002*SL
	t_{PHL}	0.149	0.143 + 0.003*SL	0.146 + 0.002*SL	0.151 + 0.002*SL
G to Q	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.030	0.024 + 0.003*SL	0.022 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.187	0.181 + 0.003*SL	0.184 + 0.002*SL	0.186 + 0.002*SL
	t_{PHL}	0.148	0.141 + 0.003*SL	0.145 + 0.002*SL	0.150 + 0.002*SL
SN to Q	t_R	0.032	0.023 + 0.004*SL	0.021 + 0.005*SL	0.012 + 0.005*SL
	t_F	0.029	0.021 + 0.004*SL	0.021 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.099	0.093 + 0.003*SL	0.096 + 0.002*SL	0.097 + 0.002*SL
	t_{PHL}	0.095	0.089 + 0.003*SL	0.092 + 0.002*SL	0.097 + 0.002*SL
RN to Q	t_R	0.037	0.029 + 0.004*SL	0.026 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.030	0.022 + 0.004*SL	0.023 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.148	0.142 + 0.003*SL	0.145 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.127	0.121 + 0.003*SL	0.125 + 0.002*SL	0.130 + 0.002*SL
D to QN	t_R	0.037	0.027 + 0.005*SL	0.027 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.046	0.036 + 0.005*SL	0.039 + 0.004*SL	0.040 + 0.004*SL
	t_{PLH}	0.113	0.106 + 0.004*SL	0.111 + 0.002*SL	0.118 + 0.002*SL
	t_{PHL}	0.131	0.122 + 0.004*SL	0.129 + 0.003*SL	0.149 + 0.002*SL
G to QN	t_R	0.037	0.028 + 0.005*SL	0.027 + 0.005*SL	0.020 + 0.005*SL
	t_F	0.045	0.036 + 0.005*SL	0.039 + 0.004*SL	0.040 + 0.004*SL
	t_{PLH}	0.112	0.105 + 0.004*SL	0.109 + 0.002*SL	0.117 + 0.002*SL
	t_{PHL}	0.154	0.145 + 0.004*SL	0.152 + 0.003*SL	0.172 + 0.002*SL
SN to QN	t_R	0.032	0.022 + 0.005*SL	0.022 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.032	0.023 + 0.004*SL	0.025 + 0.004*SL	0.021 + 0.004*SL
	t_{PLH}	0.062	0.055 + 0.003*SL	0.059 + 0.002*SL	0.063 + 0.002*SL
	t_{PHL}	0.071	0.064 + 0.004*SL	0.069 + 0.002*SL	0.078 + 0.002*SL
RN to QN	t_R	0.037	0.027 + 0.005*SL	0.028 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.046	0.038 + 0.004*SL	0.039 + 0.004*SL	0.040 + 0.004*SL
	t_{PLH}	0.092	0.085 + 0.004*SL	0.089 + 0.002*SL	0.097 + 0.002*SL
	t_{PHL}	0.114	0.105 + 0.004*SL	0.112 + 0.003*SL	0.132 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Logic Symbol



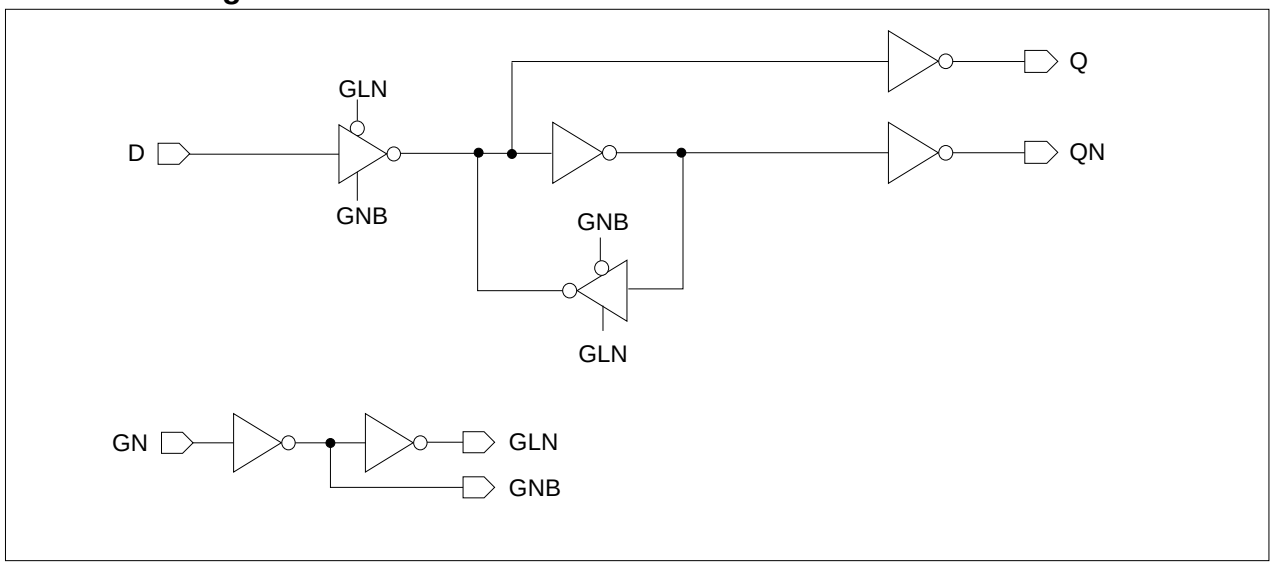
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
ld5		*ld5d2*		*ld5*	*ld5d2*
D	GN	D	GN		
1.0	0.7	1.0	0.7	4.33	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld5	ld5d2
Input Setup Time (D to GN)	t_{SU}	0.058	0.075
Input Hold Time (D to GN)	t_{HD}	0.010	0.010
Pulse Width Low (GN)	t_{PWL}	0.087	0.105

ld5/ld5d2

D Latch with Active Low, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.049	0.030 + 0.010*SL	0.030 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.046	0.029 + 0.009*SL	0.034 + 0.008*SL	0.028 + 0.008*SL
	t_{PLH}	0.080	0.068 + 0.006*SL	0.074 + 0.005*SL	0.079 + 0.004*SL
	t_{PHL}	0.087	0.074 + 0.006*SL	0.081 + 0.005*SL	0.091 + 0.004*SL
GN to Q	t_R	0.049	0.029 + 0.010*SL	0.030 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.045	0.027 + 0.009*SL	0.034 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.109	0.097 + 0.006*SL	0.102 + 0.005*SL	0.108 + 0.004*SL
	t_{PHL}	0.123	0.111 + 0.006*SL	0.116 + 0.005*SL	0.128 + 0.004*SL
D to QN	t_R	0.041	0.023 + 0.009*SL	0.020 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.036	0.021 + 0.007*SL	0.020 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.110	0.100 + 0.005*SL	0.102 + 0.005*SL	0.103 + 0.004*SL
	t_{PHL}	0.110	0.100 + 0.005*SL	0.103 + 0.004*SL	0.106 + 0.004*SL
GN to QN	t_R	0.042	0.025 + 0.008*SL	0.018 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.036	0.022 + 0.007*SL	0.020 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.147	0.136 + 0.005*SL	0.139 + 0.005*SL	0.140 + 0.004*SL
	t_{PHL}	0.138	0.128 + 0.005*SL	0.132 + 0.004*SL	0.134 + 0.004*SL

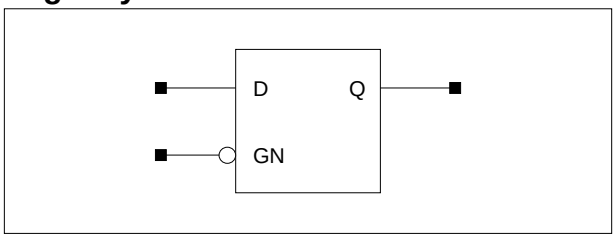
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld5d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.043	0.032 + 0.005*SL	0.035 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.042	0.034 + 0.004*SL	0.034 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.083	0.076 + 0.004*SL	0.081 + 0.003*SL	0.091 + 0.002*SL
	t_{PHL}	0.090	0.082 + 0.004*SL	0.088 + 0.003*SL	0.104 + 0.002*SL
GN to Q	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.027 + 0.005*SL
	t_F	0.042	0.033 + 0.005*SL	0.036 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.112	0.104 + 0.004*SL	0.109 + 0.003*SL	0.120 + 0.002*SL
	t_{PHL}	0.126	0.118 + 0.004*SL	0.125 + 0.003*SL	0.141 + 0.002*SL
D to QN	t_R	0.036	0.027 + 0.004*SL	0.026 + 0.005*SL	0.014 + 0.005*SL
	t_F	0.033	0.025 + 0.004*SL	0.025 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.127	0.121 + 0.003*SL	0.124 + 0.002*SL	0.127 + 0.002*SL
	t_{PHL}	0.127	0.120 + 0.003*SL	0.124 + 0.002*SL	0.130 + 0.002*SL
GN to QN	t_R	0.036	0.027 + 0.005*SL	0.026 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.032	0.024 + 0.004*SL	0.026 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.163	0.157 + 0.003*SL	0.161 + 0.002*SL	0.163 + 0.002*SL
	t_{PHL}	0.155	0.149 + 0.003*SL	0.153 + 0.002*SL	0.159 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



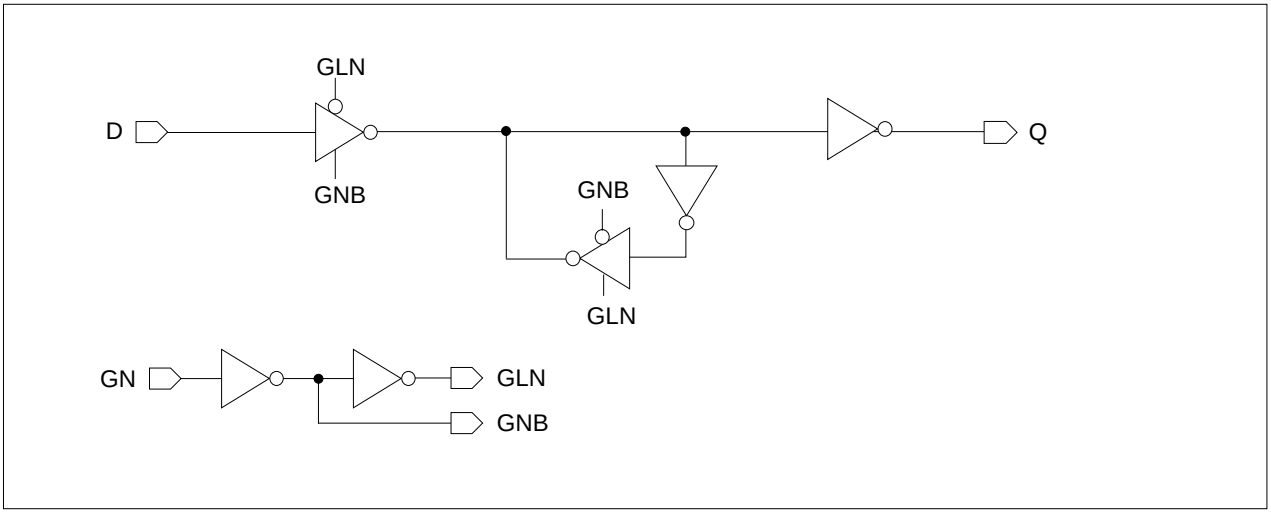
Truth Table

D	GN	Q (n+1)
0	0	0
1	0	1
x	1	Q (n)

Cell Data

Input Load (SL)				Gate Count	
ld5q		*ld5qd2*		*ld5q*	*ld5qd2*
D	GN	D	GN		
1.0	0.7	1.0	0.7	4.00	4.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld5q	ld5qd2
Input Setup Time (D to GN)	t_{SU}	0.053	0.066
Input Hold Time (D to GN)	t_{HD}	0.010	0.010
Pulse Width Low (GN)	t_{PWL}	0.079	0.093

ld5q/ld5qd2

D Latch with Active Low, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld5q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.047	0.026 + 0.010*SL	0.029 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.044	0.025 + 0.009*SL	0.032 + 0.007*SL	0.024 + 0.008*SL
	t_{PLH}	0.077	0.066 + 0.006*SL	0.070 + 0.005*SL	0.074 + 0.004*SL
	t_{PHL}	0.083	0.070 + 0.006*SL	0.077 + 0.005*SL	0.084 + 0.004*SL
GN to Q	t_R	0.049	0.028 + 0.010*SL	0.031 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.044	0.026 + 0.009*SL	0.031 + 0.008*SL	0.024 + 0.008*SL
	t_{PLH}	0.105	0.094 + 0.006*SL	0.097 + 0.005*SL	0.102 + 0.004*SL
	t_{PHL}	0.119	0.107 + 0.006*SL	0.114 + 0.004*SL	0.120 + 0.004*SL

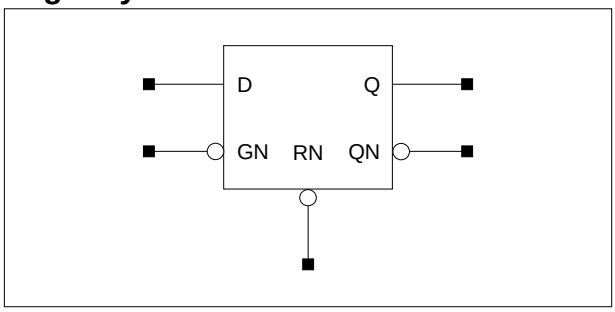
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld5qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.043	0.033 + 0.005*SL	0.034 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.040	0.030 + 0.005*SL	0.036 + 0.004*SL	0.029 + 0.004*SL
	t_{PLH}	0.080	0.072 + 0.004*SL	0.077 + 0.003*SL	0.086 + 0.002*SL
	t_{PHL}	0.086	0.079 + 0.004*SL	0.084 + 0.002*SL	0.098 + 0.002*SL
GN to Q	t_R	0.043	0.032 + 0.005*SL	0.035 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.040	0.030 + 0.005*SL	0.035 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.108	0.101 + 0.004*SL	0.106 + 0.003*SL	0.115 + 0.002*SL
	t_{PHL}	0.123	0.115 + 0.004*SL	0.121 + 0.002*SL	0.134 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Logic Symbol



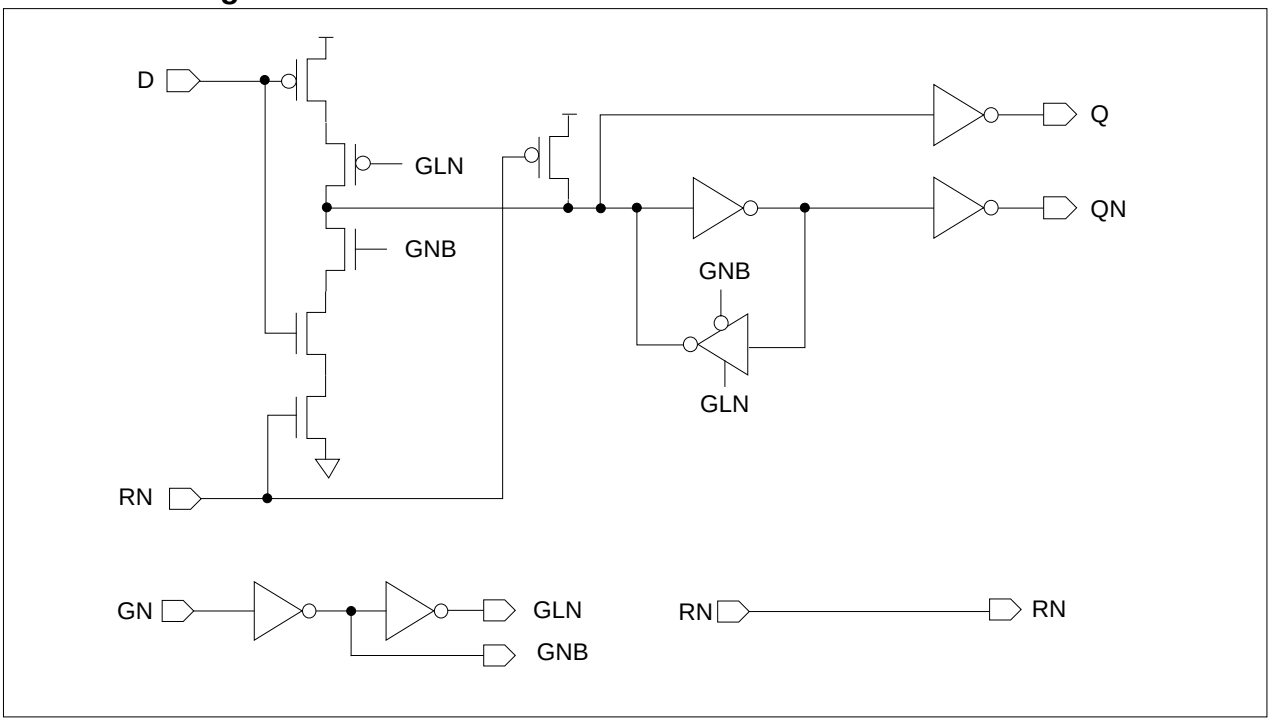
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
ld6			*ld6d2*			*ld6*	*ld6d2*
D	GN	RN	D	GN	RN		
1.0	0.7	0.7	1.0	0.7	0.8	5.00	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld6	ld6d2
Input Setup Time (D to GN)	t_{SU}	0.068	0.089
Input Hold Time (D to GN)	t_{HD}	0.010	0.010
Pulse Width Low (GN)	t_{PWL}	0.098	0.118
Pulse Width Low (RN)	t_{PWL}	0.104	0.140
Recovery Time (RN to GN)	t_{RC}	0.069	0.088
Removal Time (RN to GN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.055	0.034 + 0.010*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.049	0.032 + 0.008*SL	0.035 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.092	0.079 + 0.007*SL	0.085 + 0.005*SL	0.094 + 0.004*SL
	t_{PHL}	0.093	0.080 + 0.007*SL	0.088 + 0.005*SL	0.099 + 0.004*SL
GN to Q	t_R	0.054	0.033 + 0.011*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.048	0.030 + 0.009*SL	0.036 + 0.007*SL	0.029 + 0.008*SL
	t_{PLH}	0.119	0.106 + 0.007*SL	0.113 + 0.005*SL	0.121 + 0.004*SL
	t_{PHL}	0.130	0.116 + 0.007*SL	0.124 + 0.005*SL	0.136 + 0.004*SL
RN to Q	t_R	0.055	0.034 + 0.010*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_F	0.062	0.042 + 0.010*SL	0.052 + 0.007*SL	0.044 + 0.008*SL
	t_{PLH}	0.091	0.077 + 0.007*SL	0.084 + 0.005*SL	0.093 + 0.004*SL
	t_{PHL}	0.111	0.095 + 0.008*SL	0.106 + 0.005*SL	0.124 + 0.004*SL
D to QN	t_R	0.042	0.024 + 0.009*SL	0.021 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.037	0.023 + 0.007*SL	0.021 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.117	0.107 + 0.005*SL	0.109 + 0.005*SL	0.110 + 0.004*SL
	t_{PHL}	0.123	0.112 + 0.005*SL	0.116 + 0.004*SL	0.119 + 0.004*SL
GN to QN	t_R	0.043	0.025 + 0.009*SL	0.020 + 0.010*SL	0.014 + 0.010*SL
	t_F	0.037	0.021 + 0.008*SL	0.022 + 0.008*SL	0.015 + 0.008*SL
	t_{PLH}	0.153	0.143 + 0.005*SL	0.146 + 0.004*SL	0.146 + 0.004*SL
	t_{PHL}	0.150	0.140 + 0.005*SL	0.144 + 0.004*SL	0.146 + 0.004*SL
RN to QN	t_R	0.046	0.029 + 0.008*SL	0.022 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.038	0.023 + 0.008*SL	0.023 + 0.008*SL	0.014 + 0.008*SL
	t_{PLH}	0.136	0.125 + 0.005*SL	0.128 + 0.005*SL	0.129 + 0.004*SL
	t_{PHL}	0.122	0.111 + 0.005*SL	0.115 + 0.004*SL	0.118 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld6d2

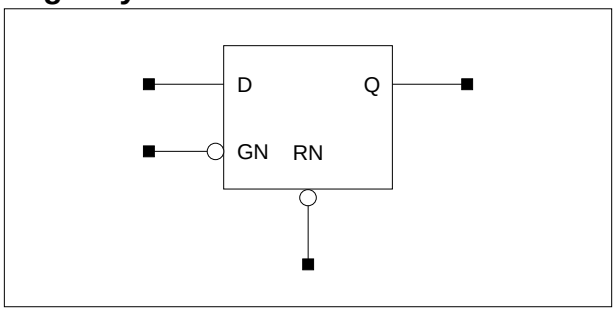
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.048	0.039 + 0.005*SL	0.038 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.039 + 0.004*SL	0.038 + 0.004*SL
	t_{PLH}	0.094	0.086 + 0.004*SL	0.092 + 0.003*SL	0.106 + 0.002*SL
	t_{PHL}	0.096	0.088 + 0.004*SL	0.094 + 0.003*SL	0.113 + 0.002*SL
GN to Q	t_R	0.049	0.038 + 0.005*SL	0.040 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.044	0.035 + 0.004*SL	0.037 + 0.004*SL	0.038 + 0.004*SL
	t_{PLH}	0.122	0.113 + 0.004*SL	0.119 + 0.003*SL	0.133 + 0.002*SL
	t_{PHL}	0.132	0.124 + 0.004*SL	0.130 + 0.003*SL	0.149 + 0.002*SL
RN to Q	t_R	0.049	0.038 + 0.006*SL	0.041 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.059	0.050 + 0.004*SL	0.052 + 0.004*SL	0.054 + 0.004*SL
	t_{PLH}	0.093	0.085 + 0.004*SL	0.091 + 0.003*SL	0.105 + 0.002*SL
	t_{PHL}	0.113	0.103 + 0.005*SL	0.112 + 0.003*SL	0.138 + 0.002*SL
D to QN	t_R	0.037	0.027 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.034	0.027 + 0.003*SL	0.026 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.135	0.129 + 0.003*SL	0.132 + 0.002*SL	0.135 + 0.002*SL
	t_{PHL}	0.142	0.135 + 0.003*SL	0.139 + 0.002*SL	0.146 + 0.002*SL
GN to QN	t_R	0.037	0.027 + 0.005*SL	0.028 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.034	0.026 + 0.004*SL	0.027 + 0.004*SL	0.019 + 0.004*SL
	t_{PLH}	0.171	0.165 + 0.003*SL	0.168 + 0.002*SL	0.171 + 0.002*SL
	t_{PHL}	0.169	0.162 + 0.003*SL	0.167 + 0.002*SL	0.173 + 0.002*SL
RN to QN	t_R	0.043	0.035 + 0.004*SL	0.032 + 0.005*SL	0.018 + 0.005*SL
	t_F	0.035	0.027 + 0.004*SL	0.029 + 0.004*SL	0.018 + 0.004*SL
	t_{PLH}	0.156	0.150 + 0.003*SL	0.154 + 0.002*SL	0.157 + 0.002*SL
	t_{PHL}	0.140	0.134 + 0.003*SL	0.138 + 0.002*SL	0.144 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

ld6q/ld6qd2

D Latch with Active Low, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



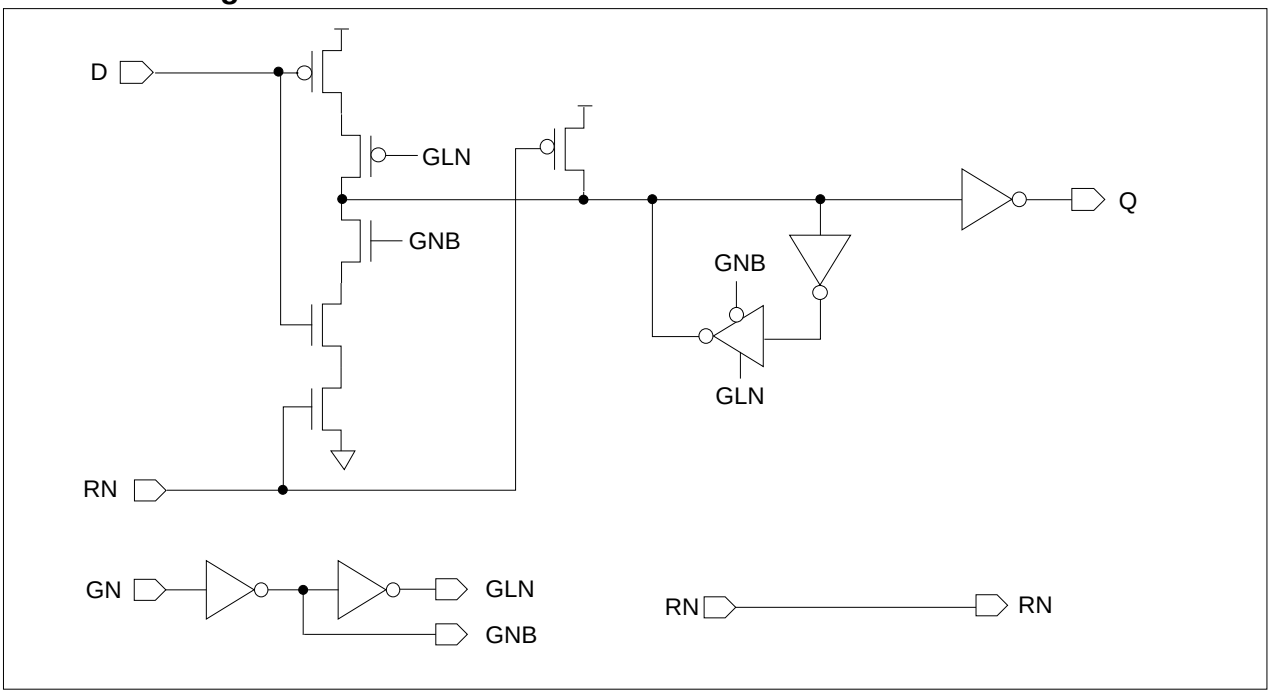
Truth Table

D	GN	RN	Q (n+1)
0	0	1	0
1	0	1	1
x	1	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
ld6q			*ld6qd2*			*ld6q*	*ld6qd2*
D	GN	RN	D	GN	RN		
1.0	0.7	0.7	1.0	0.7	0.8	4.67	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)	
		ld6q	ld6qd2
Input Setup Time (D to GN)	t_{SU}	0.062	0.077
Input Hold Time (D to GN)	t_{HD}	0.010	0.010
Pulse Width Low (GN)	t_{PWL}	0.088	0.104
Pulse Width Low (RN)	t_{PWL}	0.084	0.108
Recovery Time (RN to GN)	t_{RC}	0.063	0.076
Removal Time (RN to GN)	t_{RM}	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ld6q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.054	0.033 + 0.010*SL	0.036 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.047	0.030 + 0.009*SL	0.035 + 0.007*SL	0.026 + 0.008*SL
	t_{PLH}	0.089	0.076 + 0.006*SL	0.082 + 0.005*SL	0.088 + 0.004*SL
	t_{PHL}	0.090	0.077 + 0.006*SL	0.085 + 0.005*SL	0.093 + 0.004*SL
GN to Q	t_R	0.055	0.035 + 0.010*SL	0.036 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.046	0.030 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.117	0.104 + 0.006*SL	0.110 + 0.005*SL	0.116 + 0.004*SL
	t_{PHL}	0.126	0.113 + 0.007*SL	0.122 + 0.004*SL	0.128 + 0.004*SL
RN to Q	t_R	0.055	0.036 + 0.010*SL	0.035 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.060	0.043 + 0.009*SL	0.048 + 0.007*SL	0.040 + 0.008*SL
	t_{PLH}	0.088	0.075 + 0.006*SL	0.081 + 0.005*SL	0.087 + 0.004*SL
	t_{PHL}	0.107	0.091 + 0.008*SL	0.103 + 0.005*SL	0.117 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

ld6qd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.047	0.036 + 0.006*SL	0.040 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.042	0.033 + 0.005*SL	0.036 + 0.004*SL	0.033 + 0.004*SL
	t_{PLH}	0.092	0.084 + 0.004*SL	0.089 + 0.003*SL	0.101 + 0.002*SL
	t_{PHL}	0.093	0.085 + 0.004*SL	0.091 + 0.003*SL	0.106 + 0.002*SL
GN to Q	t_R	0.047	0.037 + 0.005*SL	0.039 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.042	0.033 + 0.004*SL	0.036 + 0.004*SL	0.032 + 0.004*SL
	t_{PLH}	0.120	0.112 + 0.004*SL	0.118 + 0.003*SL	0.130 + 0.002*SL
	t_{PHL}	0.128	0.119 + 0.004*SL	0.126 + 0.003*SL	0.141 + 0.002*SL
RN to Q	t_R	0.047	0.035 + 0.006*SL	0.041 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.058	0.049 + 0.005*SL	0.052 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.090	0.083 + 0.004*SL	0.088 + 0.003*SL	0.100 + 0.002*SL
	t_{PHL}	0.109	0.100 + 0.005*SL	0.108 + 0.003*SL	0.131 + 0.002*SL

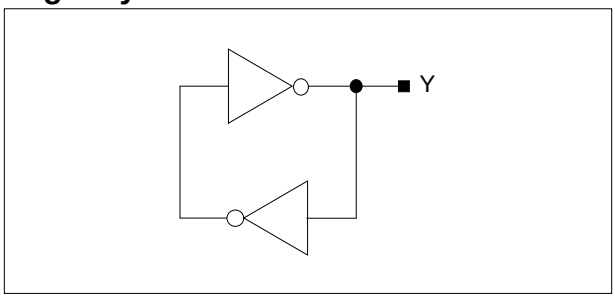
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

BUSHOLDER

Cell List

Cell Name	Function Description
busholder	Bus Holder

Logic Symbol



Cell Data

Input Load (SL)	Gate Count
Y	
5.4	1.67

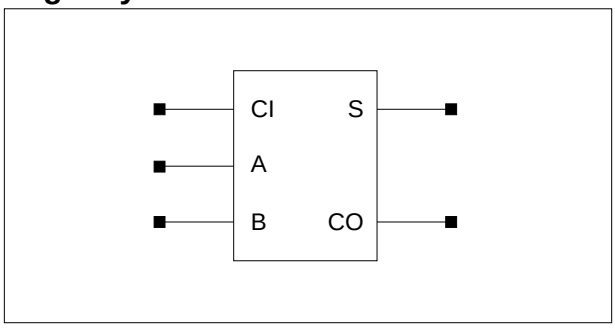
Cell List

Cell Name	Function Description
fa	Full Adder with 1X Drive
fad2	Full Adder with 2X Drive
fad4	Full Adder with 4X Drive
ha	Half Adder with 1x Drive
had2	Half Adder with 2X Drive
had4	Half Adder with 4X Drive

fa/fad2/fad4

Full Adder with 1X/2X/4X Drive

Logic Symbol



Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
fa			*fad2*			*fad4*			*fa*	*fad2*	*fad4*
CI	A	B	CI	A	B	CI	A	B			
1.0	1.1	1.0	1.1	1.1	1.0	1.0	1.0	1.0	8.00	9.00	10.67

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fa

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.053	0.036 + 0.008*SL	0.031 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.049	0.033 + 0.008*SL	0.035 + 0.008*SL	0.029 + 0.008*SL
	t_{PLH}	0.138	0.126 + 0.006*SL	0.131 + 0.005*SL	0.133 + 0.004*SL
	t_{PHL}	0.138	0.126 + 0.006*SL	0.133 + 0.005*SL	0.140 + 0.004*SL
B to S	t_R	0.051	0.033 + 0.009*SL	0.029 + 0.010*SL	0.021 + 0.010*SL
	t_F	0.055	0.040 + 0.008*SL	0.041 + 0.007*SL	0.033 + 0.008*SL
	t_{PLH}	0.160	0.149 + 0.006*SL	0.153 + 0.005*SL	0.156 + 0.004*SL
	t_{PHL}	0.158	0.146 + 0.006*SL	0.153 + 0.005*SL	0.161 + 0.004*SL
CI to S	t_R	0.048	0.030 + 0.009*SL	0.028 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.052	0.037 + 0.008*SL	0.037 + 0.008*SL	0.030 + 0.008*SL
	t_{PLH}	0.105	0.093 + 0.006*SL	0.098 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.108	0.095 + 0.006*SL	0.103 + 0.005*SL	0.111 + 0.004*SL
A to CO	t_R	0.052	0.033 + 0.009*SL	0.032 + 0.010*SL	0.023 + 0.010*SL
	t_F	0.053	0.036 + 0.009*SL	0.041 + 0.007*SL	0.033 + 0.008*SL
	t_{PLH}	0.140	0.129 + 0.006*SL	0.133 + 0.005*SL	0.137 + 0.004*SL
	t_{PHL}	0.145	0.132 + 0.007*SL	0.140 + 0.005*SL	0.150 + 0.004*SL
B to CO	t_R	0.057	0.039 + 0.009*SL	0.036 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.060	0.047 + 0.006*SL	0.044 + 0.007*SL	0.034 + 0.008*SL
	t_{PLH}	0.158	0.147 + 0.006*SL	0.152 + 0.005*SL	0.156 + 0.004*SL
	t_{PHL}	0.167	0.154 + 0.007*SL	0.162 + 0.005*SL	0.172 + 0.004*SL
CI to CO	t_R	0.048	0.029 + 0.010*SL	0.029 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.055	0.038 + 0.009*SL	0.043 + 0.007*SL	0.033 + 0.008*SL
	t_{PLH}	0.086	0.074 + 0.006*SL	0.079 + 0.005*SL	0.082 + 0.004*SL
	t_{PHL}	0.095	0.081 + 0.007*SL	0.089 + 0.005*SL	0.100 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fad2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.048	0.039 + 0.005*SL	0.039 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.052	0.043 + 0.005*SL	0.046 + 0.004*SL	0.041 + 0.004*SL
	t_{PLH}	0.143	0.135 + 0.004*SL	0.140 + 0.002*SL	0.147 + 0.002*SL
	t_{PHL}	0.147	0.139 + 0.004*SL	0.145 + 0.003*SL	0.161 + 0.002*SL
B to S	t_R	0.049	0.040 + 0.004*SL	0.039 + 0.005*SL	0.026 + 0.005*SL
	t_F	0.054	0.044 + 0.005*SL	0.048 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.169	0.162 + 0.004*SL	0.167 + 0.002*SL	0.174 + 0.002*SL
	t_{PHL}	0.173	0.165 + 0.004*SL	0.171 + 0.003*SL	0.188 + 0.002*SL
CI to S	t_R	0.044	0.034 + 0.005*SL	0.035 + 0.005*SL	0.024 + 0.005*SL
	t_F	0.052	0.042 + 0.005*SL	0.046 + 0.004*SL	0.043 + 0.004*SL
	t_{PLH}	0.112	0.104 + 0.004*SL	0.109 + 0.002*SL	0.116 + 0.002*SL
	t_{PHL}	0.115	0.107 + 0.004*SL	0.113 + 0.003*SL	0.131 + 0.002*SL
A to CO	t_R	0.049	0.038 + 0.005*SL	0.040 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.055	0.047 + 0.004*SL	0.048 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.146	0.139 + 0.004*SL	0.144 + 0.003*SL	0.153 + 0.002*SL
	t_{PHL}	0.153	0.144 + 0.004*SL	0.150 + 0.003*SL	0.170 + 0.002*SL
B to CO	t_R	0.051	0.041 + 0.005*SL	0.042 + 0.005*SL	0.031 + 0.005*SL
	t_F	0.057	0.050 + 0.004*SL	0.049 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.167	0.160 + 0.004*SL	0.165 + 0.003*SL	0.175 + 0.002*SL
	t_{PHL}	0.175	0.167 + 0.004*SL	0.173 + 0.003*SL	0.193 + 0.002*SL
CI to CO	t_R	0.044	0.035 + 0.005*SL	0.034 + 0.005*SL	0.025 + 0.005*SL
	t_F	0.054	0.046 + 0.004*SL	0.046 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.090	0.083 + 0.004*SL	0.087 + 0.002*SL	0.095 + 0.002*SL
	t_{PHL}	0.099	0.091 + 0.004*SL	0.097 + 0.003*SL	0.116 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 32, *Group3 : 32 < SL

Switching Characteristics

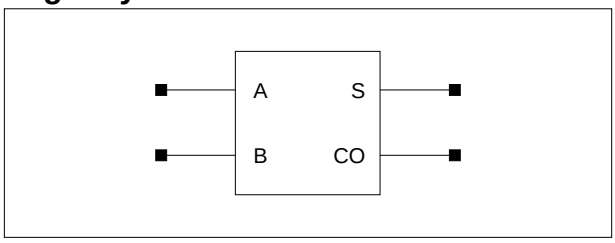
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

fad4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.053	0.047 + 0.003*SL	0.049 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.063	0.061 + 0.001*SL	0.057 + 0.002*SL	0.057 + 0.002*SL
	t_{PLH}	0.158	0.153 + 0.002*SL	0.156 + 0.001*SL	0.170 + 0.001*SL
	t_{PHL}	0.165	0.160 + 0.002*SL	0.164 + 0.001*SL	0.187 + 0.001*SL
B to S	t_R	0.054	0.048 + 0.003*SL	0.051 + 0.002*SL	0.038 + 0.002*SL
	t_F	0.064	0.061 + 0.002*SL	0.060 + 0.002*SL	0.057 + 0.002*SL
	t_{PLH}	0.192	0.188 + 0.002*SL	0.191 + 0.001*SL	0.205 + 0.001*SL
	t_{PHL}	0.200	0.195 + 0.002*SL	0.199 + 0.001*SL	0.222 + 0.001*SL
CI to S	t_R	0.051	0.046 + 0.002*SL	0.046 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.062	0.058 + 0.002*SL	0.059 + 0.002*SL	0.060 + 0.002*SL
	t_{PLH}	0.136	0.132 + 0.002*SL	0.135 + 0.001*SL	0.149 + 0.001*SL
	t_{PHL}	0.138	0.133 + 0.002*SL	0.137 + 0.001*SL	0.162 + 0.001*SL
A to CO	t_R	0.058	0.054 + 0.002*SL	0.054 + 0.002*SL	0.044 + 0.002*SL
	t_F	0.065	0.060 + 0.003*SL	0.063 + 0.002*SL	0.067 + 0.002*SL
	t_{PLH}	0.163	0.159 + 0.002*SL	0.162 + 0.001*SL	0.178 + 0.001*SL
	t_{PHL}	0.168	0.163 + 0.003*SL	0.167 + 0.002*SL	0.194 + 0.001*SL
B to CO	t_R	0.059	0.055 + 0.002*SL	0.053 + 0.002*SL	0.045 + 0.002*SL
	t_F	0.068	0.064 + 0.002*SL	0.063 + 0.002*SL	0.067 + 0.002*SL
	t_{PLH}	0.183	0.179 + 0.002*SL	0.182 + 0.001*SL	0.199 + 0.001*SL
	t_{PHL}	0.192	0.187 + 0.003*SL	0.191 + 0.002*SL	0.218 + 0.001*SL
CI to CO	t_R	0.048	0.043 + 0.002*SL	0.043 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.060	0.057 + 0.002*SL	0.056 + 0.002*SL	0.061 + 0.002*SL
	t_{PLH}	0.101	0.097 + 0.002*SL	0.100 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.112	0.107 + 0.002*SL	0.111 + 0.001*SL	0.136 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



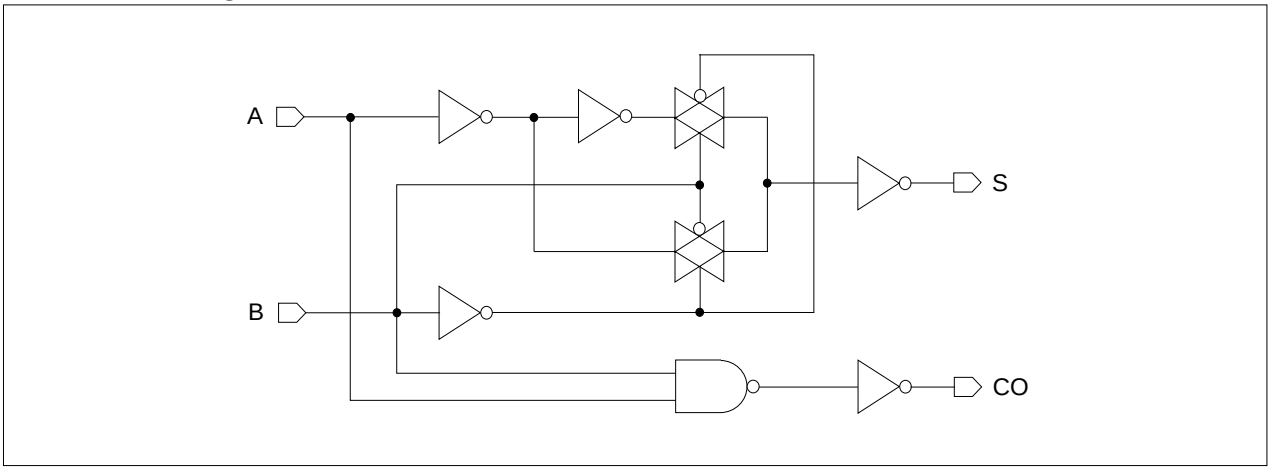
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)						Gate Count		
ha		*had2*		*had4*		*ha*	*had2*	*had4*
A	B	A	B	A	B			
2.0	2.1	2.0	2.2	2.0	2.3	4.67	5.67	7.33

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

ha

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.047	0.029 + 0.009*SL	0.025 + 0.010*SL	0.018 + 0.010*SL
	t_F	0.050	0.035 + 0.008*SL	0.035 + 0.008*SL	0.029 + 0.008*SL
	t_{PLH}	0.093	0.082 + 0.006*SL	0.086 + 0.005*SL	0.088 + 0.004*SL
	t_{PHL}	0.097	0.084 + 0.006*SL	0.091 + 0.005*SL	0.099 + 0.004*SL
B to S	t_R	0.046	0.028 + 0.009*SL	0.025 + 0.010*SL	0.019 + 0.010*SL
	t_F	0.046	0.029 + 0.009*SL	0.033 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.083	0.072 + 0.006*SL	0.075 + 0.005*SL	0.077 + 0.004*SL
	t_{PHL}	0.079	0.067 + 0.006*SL	0.073 + 0.005*SL	0.081 + 0.004*SL
A to CO	t_R	0.042	0.023 + 0.009*SL	0.020 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.034	0.020 + 0.007*SL	0.016 + 0.008*SL	0.013 + 0.008*SL
	t_{PLH}	0.060	0.049 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.004*SL
	t_{PHL}	0.060	0.050 + 0.005*SL	0.053 + 0.004*SL	0.054 + 0.004*SL
B to CO	t_R	0.042	0.022 + 0.010*SL	0.023 + 0.010*SL	0.015 + 0.010*SL
	t_F	0.034	0.019 + 0.007*SL	0.017 + 0.008*SL	0.012 + 0.008*SL
	t_{PLH}	0.060	0.049 + 0.005*SL	0.053 + 0.005*SL	0.053 + 0.004*SL
	t_{PHL}	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.052 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

had2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.042	0.033 + 0.004*SL	0.032 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.048	0.040 + 0.004*SL	0.042 + 0.004*SL	0.036 + 0.004*SL
	t_{PLH}	0.098	0.091 + 0.003*SL	0.095 + 0.002*SL	0.101 + 0.002*SL
	t_{PHL}	0.101	0.093 + 0.004*SL	0.099 + 0.003*SL	0.113 + 0.002*SL
B to S	t_R	0.041	0.032 + 0.005*SL	0.031 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.043	0.032 + 0.005*SL	0.038 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.083	0.076 + 0.003*SL	0.080 + 0.002*SL	0.087 + 0.002*SL
	t_{PHL}	0.080	0.073 + 0.004*SL	0.078 + 0.003*SL	0.093 + 0.002*SL
A to CO	t_R	0.037	0.030 + 0.003*SL	0.024 + 0.005*SL	0.017 + 0.005*SL
	t_F	0.029	0.022 + 0.003*SL	0.020 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.063	0.056 + 0.003*SL	0.060 + 0.002*SL	0.064 + 0.002*SL
	t_{PHL}	0.061	0.055 + 0.003*SL	0.059 + 0.002*SL	0.063 + 0.002*SL
B to CO	t_R	0.035	0.026 + 0.005*SL	0.025 + 0.005*SL	0.016 + 0.005*SL
	t_F	0.028	0.021 + 0.004*SL	0.021 + 0.004*SL	0.016 + 0.004*SL
	t_{PLH}	0.063	0.057 + 0.003*SL	0.060 + 0.002*SL	0.064 + 0.002*SL
	t_{PHL}	0.059	0.053 + 0.003*SL	0.057 + 0.002*SL	0.061 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

had4

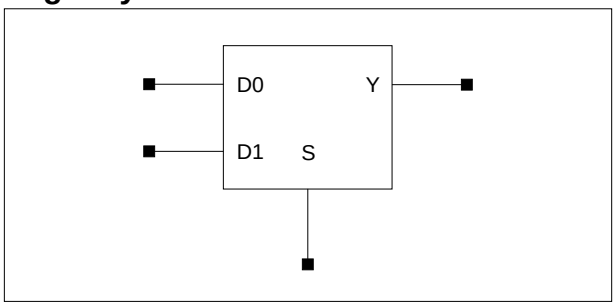
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.050	0.046 + 0.002*SL	0.045 + 0.002*SL	0.035 + 0.003*SL
	t_F	0.062	0.057 + 0.002*SL	0.059 + 0.002*SL	0.061 + 0.002*SL
	t_{PLH}	0.112	0.108 + 0.002*SL	0.111 + 0.001*SL	0.124 + 0.001*SL
	t_{PHL}	0.119	0.114 + 0.002*SL	0.118 + 0.001*SL	0.143 + 0.001*SL
B to S	t_R	0.048	0.043 + 0.003*SL	0.044 + 0.002*SL	0.035 + 0.003*SL
	t_F	0.058	0.053 + 0.003*SL	0.056 + 0.002*SL	0.057 + 0.002*SL
	t_{PLH}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.109 + 0.001*SL
	t_{PHL}	0.100	0.095 + 0.002*SL	0.099 + 0.001*SL	0.123 + 0.001*SL
A to CO	t_R	0.038	0.033 + 0.002*SL	0.033 + 0.002*SL	0.026 + 0.003*SL
	t_F	0.033	0.029 + 0.002*SL	0.029 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.071	0.067 + 0.002*SL	0.070 + 0.001*SL	0.078 + 0.001*SL
	t_{PHL}	0.074	0.070 + 0.002*SL	0.073 + 0.001*SL	0.083 + 0.001*SL
B to CO	t_R	0.037	0.031 + 0.003*SL	0.033 + 0.002*SL	0.024 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.024 + 0.002*SL
	t_{PLH}	0.071	0.067 + 0.002*SL	0.070 + 0.001*SL	0.078 + 0.001*SL
	t_{PHL}	0.072	0.068 + 0.002*SL	0.071 + 0.001*SL	0.081 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 61, *Group3 : 61 < SL

Cell List

Cell Name	Function Description
mx2	2 > 1 Non-Inverting MUX with 1X Drive
mx2d2	2 > 1 Non-Inverting MUX with 2X Drive
mx2d4	2 > 1 Non-Inverting MUX with 4X Drive
mx2d8	2 > 1 Non-Inverting MUX with 8X Drive
mx2i	2 > 1 Inverting MUX with 1X Drive
mx2id2	2 > 1 Inverting MUX with 2X Drive
mx2id4	2 > 1 Inverting MUX with 4X Drive
mx2ia	2 > 1 Inverting MUX with Separate S and SN Inputs, 1X Drive
mx2id2a	2 > 1 Inverting MUX with Separate S and SN Inputs, 2X Drive
mx2id4a	2 > 1 Inverting MUX with Separate S and SN Inputs, 4X Drive
mx4	4 > 1 Non-Inverting MUX with 1X Drive
mx4d2	4 > 1 Non-Inverting MUX with 2X Drive
mx4d4	4 > 1 Non-Inverting MUX with 4X Drive

Logic Symbol



Truth Table

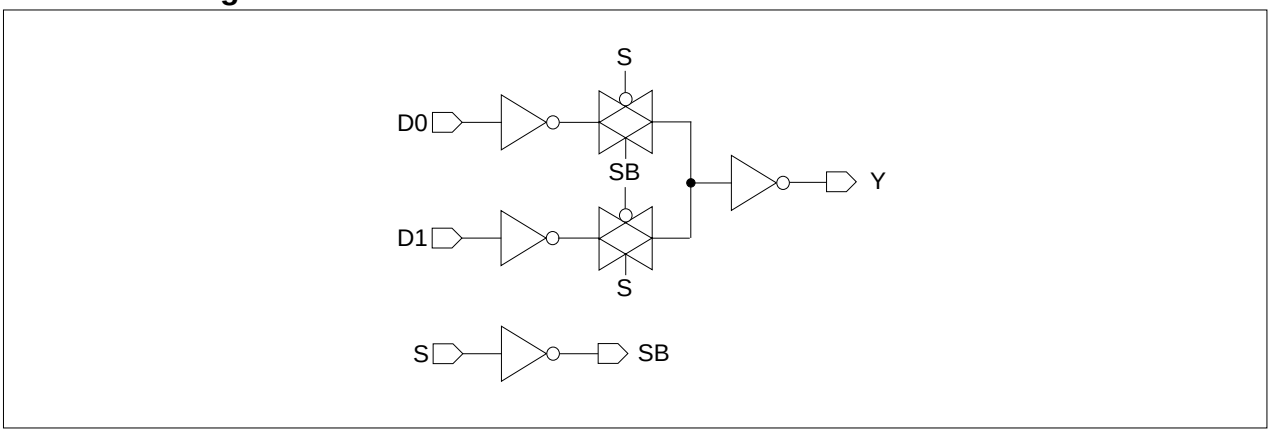
D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)											
mx2			*mx2d2*			*mx2d4*			*mx2d8*		
D0	D1	S	D0	D1	S	D0	D1	S	D0	D1	S
1.0	1.0	1.1	1.0	1.0	1.3	1.0	1.0	1.3	2.0	2.0	1.8

Gate Count			
mx2	*mx2d2*	*mx2d4*	*mx2d8*
3.00	3.33	4.33	7.00

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.049	0.035 + 0.007*SL	0.023 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.048	0.033 + 0.008*SL	0.033 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.069	0.058 + 0.006*SL	0.062 + 0.005*SL	0.064 + 0.004*SL
	t_{PHL}	0.073	0.060 + 0.006*SL	0.067 + 0.005*SL	0.074 + 0.004*SL
D1 to Y	t_R	0.049	0.036 + 0.007*SL	0.023 + 0.010*SL	0.016 + 0.010*SL
	t_F	0.048	0.033 + 0.008*SL	0.033 + 0.008*SL	0.027 + 0.008*SL
	t_{PLH}	0.067	0.056 + 0.005*SL	0.060 + 0.005*SL	0.062 + 0.004*SL
	t_{PHL}	0.073	0.061 + 0.006*SL	0.068 + 0.005*SL	0.075 + 0.004*SL
S to Y	t_R	0.048	0.031 + 0.009*SL	0.026 + 0.010*SL	0.020 + 0.010*SL
	t_F	0.047	0.030 + 0.008*SL	0.033 + 0.008*SL	0.026 + 0.008*SL
	t_{PLH}	0.090	0.079 + 0.006*SL	0.083 + 0.005*SL	0.085 + 0.004*SL
	t_{PHL}	0.085	0.072 + 0.006*SL	0.079 + 0.005*SL	0.086 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

mx2d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.040	0.030 + 0.005*SL	0.031 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.044	0.034 + 0.005*SL	0.039 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.074	0.067 + 0.003*SL	0.071 + 0.002*SL	0.077 + 0.002*SL
	t_{PHL}	0.077	0.069 + 0.004*SL	0.075 + 0.003*SL	0.089 + 0.002*SL
D1 to Y	t_R	0.040	0.030 + 0.005*SL	0.030 + 0.005*SL	0.021 + 0.005*SL
	t_F	0.045	0.035 + 0.005*SL	0.040 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.072	0.065 + 0.003*SL	0.069 + 0.002*SL	0.075 + 0.002*SL
	t_{PHL}	0.077	0.070 + 0.004*SL	0.075 + 0.003*SL	0.089 + 0.002*SL
S to Y	t_R	0.041	0.030 + 0.005*SL	0.033 + 0.005*SL	0.022 + 0.005*SL
	t_F	0.043	0.034 + 0.005*SL	0.038 + 0.004*SL	0.034 + 0.004*SL
	t_{PLH}	0.085	0.078 + 0.003*SL	0.082 + 0.002*SL	0.088 + 0.002*SL
	t_{PHL}	0.081	0.073 + 0.004*SL	0.079 + 0.002*SL	0.093 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.051	0.046 + 0.002*SL	0.046 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.059	0.054 + 0.002*SL	0.056 + 0.002*SL	0.057 + 0.002*SL
	t_{PLH}	0.089	0.085 + 0.002*SL	0.088 + 0.001*SL	0.102 + 0.001*SL
	t_{PHL}	0.095	0.090 + 0.002*SL	0.094 + 0.001*SL	0.118 + 0.001*SL
D1 to Y	t_R	0.050	0.045 + 0.002*SL	0.046 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.059	0.053 + 0.003*SL	0.057 + 0.002*SL	0.056 + 0.002*SL
	t_{PLH}	0.088	0.084 + 0.002*SL	0.087 + 0.001*SL	0.100 + 0.001*SL
	t_{PHL}	0.096	0.091 + 0.002*SL	0.095 + 0.001*SL	0.119 + 0.001*SL
S to Y	t_R	0.051	0.047 + 0.002*SL	0.045 + 0.002*SL	0.036 + 0.003*SL
	t_F	0.059	0.055 + 0.002*SL	0.054 + 0.002*SL	0.057 + 0.002*SL
	t_{PLH}	0.098	0.094 + 0.002*SL	0.097 + 0.001*SL	0.110 + 0.001*SL
	t_{PHL}	0.102	0.097 + 0.002*SL	0.101 + 0.001*SL	0.125 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

mx2d8

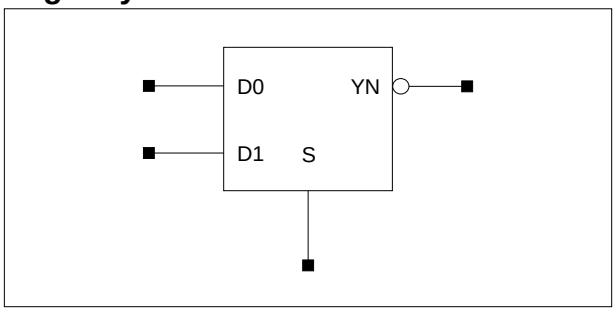
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.056	0.054 + 0.001*SL	0.053 + 0.001*SL	0.043 + 0.001*SL
	t_F	0.065	0.062 + 0.001*SL	0.063 + 0.001*SL	0.064 + 0.001*SL
	t_{PLH}	0.091	0.088 + 0.001*SL	0.090 + 0.001*SL	0.107 + 0.001*SL
	t_{PHL}	0.101	0.098 + 0.001*SL	0.100 + 0.001*SL	0.127 + 0.001*SL
D1 to Y	t_R	0.055	0.053 + 0.001*SL	0.053 + 0.001*SL	0.042 + 0.001*SL
	t_F	0.064	0.061 + 0.002*SL	0.064 + 0.001*SL	0.064 + 0.001*SL
	t_{PLH}	0.089	0.087 + 0.001*SL	0.088 + 0.001*SL	0.105 + 0.001*SL
	t_{PHL}	0.101	0.099 + 0.001*SL	0.101 + 0.001*SL	0.128 + 0.001*SL
S to Y	t_R	0.055	0.053 + 0.001*SL	0.052 + 0.001*SL	0.043 + 0.001*SL
	t_F	0.064	0.062 + 0.001*SL	0.063 + 0.001*SL	0.064 + 0.001*SL
	t_{PLH}	0.097	0.094 + 0.001*SL	0.096 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.102	0.100 + 0.001*SL	0.102 + 0.001*SL	0.128 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 118, *Group3 : 118 < SL

mx2i/mx2id2/mx2id4

2 > 1 Inverting MUX with 1X/2X/4X Drive

Logic Symbol



Truth Table

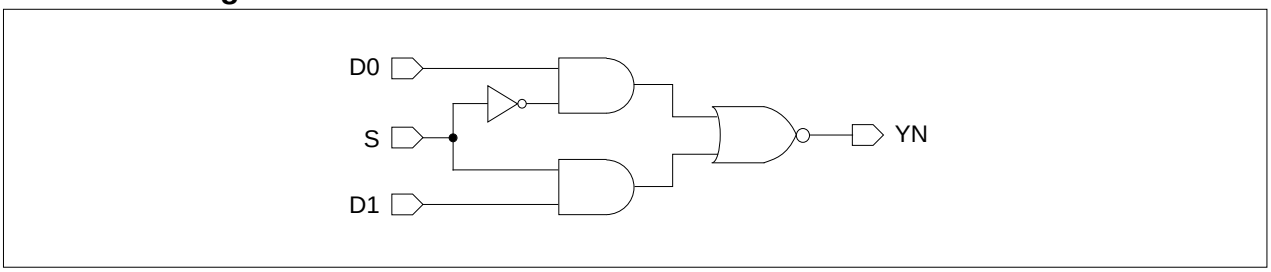
D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)								
mx2i			*mx2id2*			*mx2id4*		
D0	D1	S	D0	D1	S	D0	D1	S
1.0	1.1	1.7	2.0	2.0	2.8	1.1	1.1	1.7

Gate Count		
mx2i	*mx2id2*	*mx2id4*
2.67	4.33	4.67

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2i

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.100	0.063 + 0.018*SL	0.057 + 0.020*SL	0.047 + 0.020*SL
	t_F	0.068	0.047 + 0.011*SL	0.042 + 0.012*SL	0.030 + 0.012*SL
	t_{PLH}	0.057	0.039 + 0.009*SL	0.039 + 0.009*SL	0.039 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.033 + 0.006*SL	0.034 + 0.006*SL
D1 to YN	t_R	0.095	0.055 + 0.020*SL	0.053 + 0.020*SL	0.049 + 0.020*SL
	t_F	0.083	0.061 + 0.011*SL	0.057 + 0.012*SL	0.048 + 0.012*SL
	t_{PLH}	0.073	0.055 + 0.009*SL	0.056 + 0.009*SL	0.056 + 0.009*SL
	t_{PHL}	0.056	0.043 + 0.007*SL	0.044 + 0.006*SL	0.046 + 0.006*SL
S to YN	t_R	0.092	0.054 + 0.019*SL	0.050 + 0.020*SL	0.049 + 0.020*SL
	t_F	0.073	0.050 + 0.011*SL	0.046 + 0.012*SL	0.042 + 0.012*SL
	t_{PLH}	0.069	0.051 + 0.009*SL	0.051 + 0.009*SL	0.051 + 0.009*SL
	t_{PHL}	0.079	0.066 + 0.007*SL	0.068 + 0.006*SL	0.068 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2id2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.078	0.060 + 0.009*SL	0.058 + 0.010*SL	0.046 + 0.010*SL
	t_F	0.058	0.047 + 0.005*SL	0.045 + 0.006*SL	0.032 + 0.006*SL
	t_{PLH}	0.047	0.038 + 0.005*SL	0.039 + 0.004*SL	0.038 + 0.005*SL
	t_{PHL}	0.036	0.027 + 0.004*SL	0.031 + 0.003*SL	0.034 + 0.003*SL
D1 to YN	t_R	0.077	0.058 + 0.009*SL	0.056 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.072	0.062 + 0.005*SL	0.058 + 0.006*SL	0.048 + 0.006*SL
	t_{PLH}	0.063	0.053 + 0.005*SL	0.055 + 0.005*SL	0.055 + 0.005*SL
	t_{PHL}	0.048	0.041 + 0.004*SL	0.042 + 0.003*SL	0.044 + 0.003*SL
S to YN	t_R	0.072	0.052 + 0.010*SL	0.052 + 0.010*SL	0.049 + 0.010*SL
	t_F	0.059	0.048 + 0.005*SL	0.045 + 0.006*SL	0.038 + 0.006*SL
	t_{PLH}	0.073	0.064 + 0.005*SL	0.064 + 0.005*SL	0.064 + 0.005*SL
	t_{PHL}	0.091	0.084 + 0.004*SL	0.086 + 0.003*SL	0.090 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

mx2id4

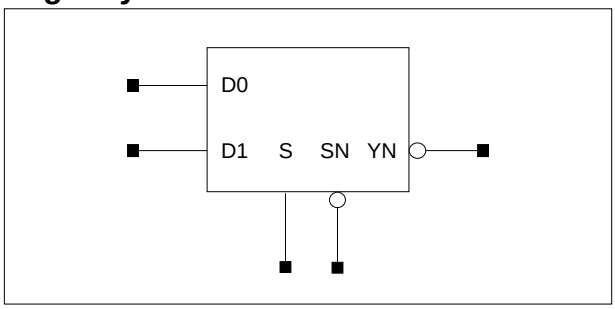
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.034	0.030 + 0.002*SL	0.028 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.103 + 0.001*SL
D1 to YN	t_R	0.034	0.029 + 0.003*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.029 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.127	0.123 + 0.002*SL	0.125 + 0.001*SL	0.130 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.117 + 0.001*SL
S to YN	t_R	0.035	0.030 + 0.003*SL	0.031 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.030	0.026 + 0.002*SL	0.027 + 0.002*SL	0.020 + 0.002*SL
	t_{PLH}	0.124	0.120 + 0.002*SL	0.122 + 0.001*SL	0.127 + 0.001*SL
	t_{PHL}	0.130	0.127 + 0.002*SL	0.129 + 0.001*SL	0.137 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

mx2ia/mx2id2a/mx2id4a

2 > 1 Inverting MUX with Separate S and SN Inputs, 1X/2X/4X Drive

Logic Symbol



Truth Table

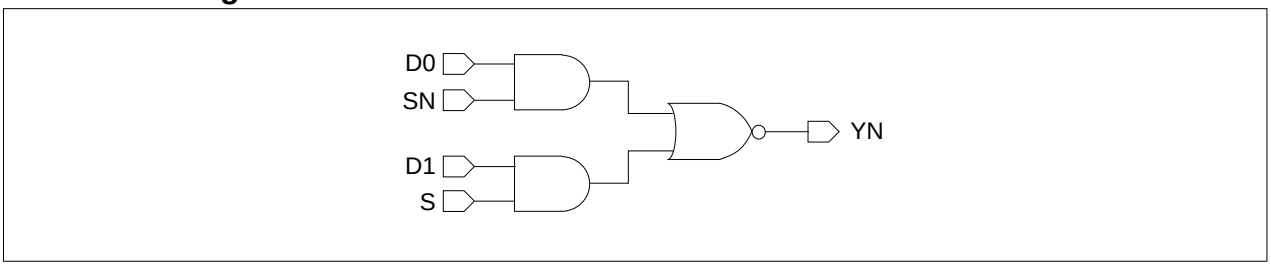
D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)											
mx2ia				*mx2id2a*				*mx2id4a*			
D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN
1.0	1.1	1.1	1.1	2.0	2.0	2.2	2.2	1.1	1.1	1.1	1.1

Gate Count		
mx2ia	*mx2id2a*	*mx2id4a*
2.00	3.67	4.33

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2ia

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.098	0.061 + 0.019*SL	0.056 + 0.020*SL	0.046 + 0.020*SL
	t_F	0.066	0.044 + 0.011*SL	0.040 + 0.012*SL	0.029 + 0.012*SL
	t_{PLH}	0.057	0.039 + 0.009*SL	0.039 + 0.009*SL	0.038 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.032 + 0.006*SL	0.033 + 0.006*SL
D1 to YN	t_R	0.093	0.053 + 0.020*SL	0.052 + 0.020*SL	0.047 + 0.020*SL
	t_F	0.077	0.055 + 0.011*SL	0.052 + 0.012*SL	0.043 + 0.012*SL
	t_{PLH}	0.072	0.053 + 0.009*SL	0.054 + 0.009*SL	0.054 + 0.009*SL
	t_{PHL}	0.055	0.042 + 0.007*SL	0.044 + 0.006*SL	0.045 + 0.006*SL
S to YN	t_R	0.100	0.060 + 0.020*SL	0.058 + 0.020*SL	0.054 + 0.020*SL
	t_F	0.075	0.053 + 0.011*SL	0.049 + 0.012*SL	0.042 + 0.012*SL
	t_{PLH}	0.076	0.058 + 0.009*SL	0.058 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.056	0.042 + 0.007*SL	0.044 + 0.006*SL	0.046 + 0.006*SL
SN to YN	t_R	0.104	0.066 + 0.019*SL	0.061 + 0.020*SL	0.053 + 0.020*SL
	t_F	0.061	0.038 + 0.012*SL	0.037 + 0.012*SL	0.028 + 0.012*SL
	t_{PLH}	0.061	0.043 + 0.009*SL	0.043 + 0.009*SL	0.042 + 0.009*SL
	t_{PHL}	0.043	0.029 + 0.007*SL	0.033 + 0.006*SL	0.034 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

mx2id2a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.078	0.060 + 0.009*SL	0.057 + 0.010*SL	0.046 + 0.010*SL
	t_F	0.056	0.045 + 0.006*SL	0.044 + 0.006*SL	0.030 + 0.006*SL
	t_{PLH}	0.047	0.038 + 0.005*SL	0.039 + 0.004*SL	0.038 + 0.005*SL
	t_{PHL}	0.035	0.027 + 0.004*SL	0.031 + 0.003*SL	0.033 + 0.003*SL
D1 to YN	t_R	0.073	0.054 + 0.010*SL	0.053 + 0.010*SL	0.046 + 0.010*SL
	t_F	0.066	0.055 + 0.006*SL	0.054 + 0.006*SL	0.042 + 0.006*SL
	t_{PLH}	0.061	0.052 + 0.005*SL	0.052 + 0.005*SL	0.053 + 0.005*SL
	t_{PHL}	0.048	0.041 + 0.004*SL	0.042 + 0.003*SL	0.044 + 0.003*SL
S to YN	t_R	0.079	0.060 + 0.010*SL	0.058 + 0.010*SL	0.053 + 0.010*SL
	t_F	0.062	0.050 + 0.006*SL	0.049 + 0.006*SL	0.041 + 0.006*SL
	t_{PLH}	0.066	0.057 + 0.005*SL	0.057 + 0.005*SL	0.057 + 0.005*SL
	t_{PHL}	0.048	0.041 + 0.004*SL	0.043 + 0.003*SL	0.045 + 0.003*SL
SN to YN	t_R	0.085	0.067 + 0.009*SL	0.065 + 0.010*SL	0.053 + 0.010*SL
	t_F	0.051	0.040 + 0.006*SL	0.039 + 0.006*SL	0.029 + 0.006*SL
	t_{PLH}	0.052	0.043 + 0.005*SL	0.043 + 0.004*SL	0.042 + 0.005*SL
	t_{PHL}	0.036	0.028 + 0.004*SL	0.031 + 0.003*SL	0.034 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

2 > 1 Inverting MUX with Separate S and SN Inputs, 1X/2X/4X Drive

Switching Characteristics

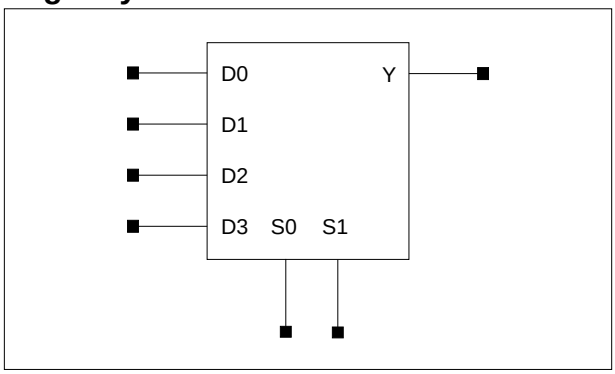
(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx2id4a

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.035	0.031 + 0.002*SL	0.029 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.110	0.107 + 0.002*SL	0.109 + 0.001*SL	0.114 + 0.001*SL
	t_{PHL}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.104 + 0.001*SL
D1 to YN	t_R	0.036	0.031 + 0.002*SL	0.031 + 0.002*SL	0.018 + 0.003*SL
	t_F	0.032	0.027 + 0.002*SL	0.029 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.125	0.122 + 0.002*SL	0.124 + 0.001*SL	0.129 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.118 + 0.001*SL
S to YN	t_R	0.036	0.031 + 0.003*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.032	0.028 + 0.002*SL	0.028 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.130	0.127 + 0.002*SL	0.129 + 0.001*SL	0.134 + 0.001*SL
	t_{PHL}	0.110	0.106 + 0.002*SL	0.109 + 0.001*SL	0.117 + 0.001*SL
SN to YN	t_R	0.037	0.031 + 0.003*SL	0.032 + 0.002*SL	0.019 + 0.003*SL
	t_F	0.031	0.026 + 0.002*SL	0.028 + 0.002*SL	0.021 + 0.002*SL
	t_{PLH}	0.115	0.112 + 0.002*SL	0.114 + 0.001*SL	0.119 + 0.001*SL
	t_{PHL}	0.096	0.092 + 0.002*SL	0.095 + 0.001*SL	0.103 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

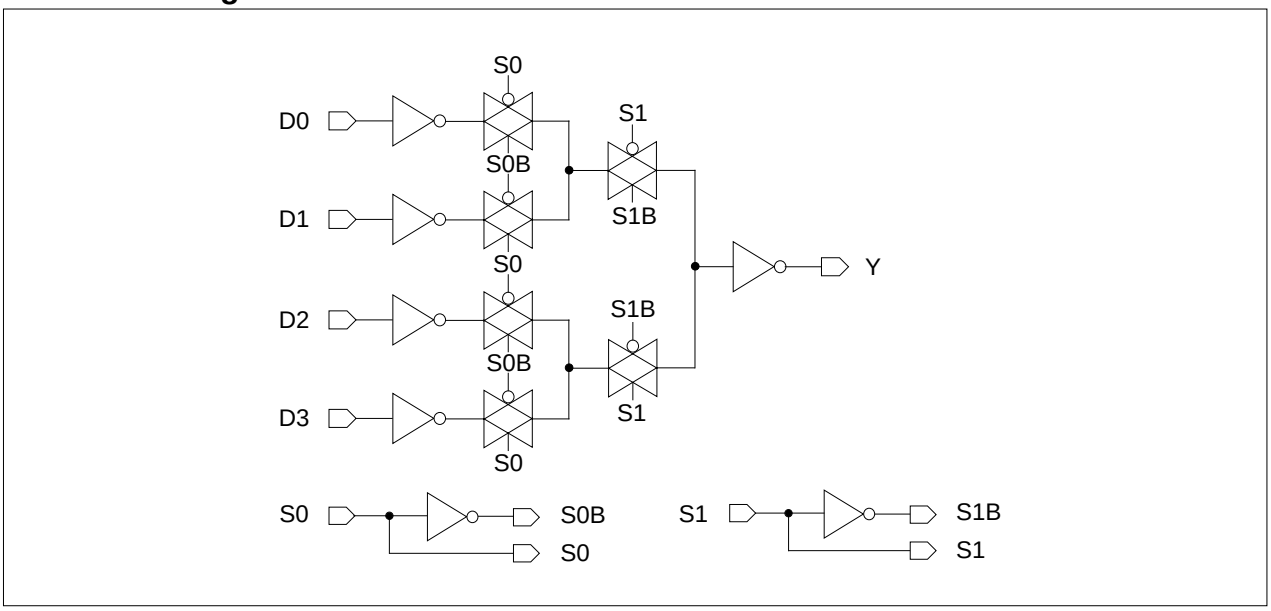
S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)																	
mx4						*mx4d2*						*mx4d4*					
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1
1.0	1.0	1.0	1.0	2.4	1.3	1.0	1.0	1.0	1.0	2.4	1.2	1.0	1.0	1.0	1.0	2.4	1.3

Gate Count		
mx4	*mx4d2*	*mx4d4*
6.33	6.67	7.67

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.055	0.037 + 0.009*SL	0.033 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.063	0.047 + 0.008*SL	0.049 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.100	0.088 + 0.006*SL	0.094 + 0.005*SL	0.100 + 0.004*SL
	t_{PHL}	0.108	0.093 + 0.008*SL	0.103 + 0.005*SL	0.119 + 0.004*SL
D1 to Y	t_R	0.053	0.034 + 0.010*SL	0.033 + 0.010*SL	0.026 + 0.010*SL
	t_F	0.064	0.047 + 0.008*SL	0.049 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.099	0.086 + 0.006*SL	0.093 + 0.005*SL	0.099 + 0.004*SL
	t_{PHL}	0.108	0.093 + 0.008*SL	0.103 + 0.005*SL	0.119 + 0.004*SL
D2 to Y	t_R	0.054	0.034 + 0.010*SL	0.036 + 0.010*SL	0.025 + 0.010*SL
	t_F	0.063	0.046 + 0.008*SL	0.049 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.097	0.084 + 0.006*SL	0.091 + 0.005*SL	0.096 + 0.004*SL
	t_{PHL}	0.106	0.091 + 0.008*SL	0.101 + 0.005*SL	0.117 + 0.004*SL
D3 to Y	t_R	0.054	0.034 + 0.010*SL	0.035 + 0.010*SL	0.025 + 0.010*SL
	t_F	0.063	0.047 + 0.008*SL	0.050 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.096	0.083 + 0.006*SL	0.089 + 0.005*SL	0.095 + 0.004*SL
	t_{PHL}	0.106	0.091 + 0.008*SL	0.101 + 0.005*SL	0.117 + 0.004*SL
S0 to Y	t_R	0.055	0.036 + 0.010*SL	0.035 + 0.010*SL	0.027 + 0.010*SL
	t_F	0.063	0.045 + 0.009*SL	0.051 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.107	0.095 + 0.006*SL	0.101 + 0.005*SL	0.107 + 0.004*SL
	t_{PHL}	0.116	0.101 + 0.008*SL	0.111 + 0.005*SL	0.128 + 0.004*SL
S1 to Y	t_R	0.052	0.033 + 0.010*SL	0.032 + 0.010*SL	0.025 + 0.010*SL
	t_F	0.057	0.038 + 0.009*SL	0.044 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.083	0.070 + 0.006*SL	0.076 + 0.005*SL	0.082 + 0.004*SL
	t_{PHL}	0.093	0.078 + 0.007*SL	0.088 + 0.005*SL	0.103 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx4d2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.052	0.041 + 0.005*SL	0.043 + 0.005*SL	0.035 + 0.005*SL
	t_F	0.067	0.058 + 0.005*SL	0.061 + 0.004*SL	0.064 + 0.004*SL
	t_{PLH}	0.106	0.098 + 0.004*SL	0.103 + 0.003*SL	0.116 + 0.002*SL
	t_{PHL}	0.115	0.106 + 0.005*SL	0.113 + 0.003*SL	0.138 + 0.002*SL
D1 to Y	t_R	0.050	0.039 + 0.006*SL	0.043 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.067	0.058 + 0.005*SL	0.061 + 0.004*SL	0.064 + 0.004*SL
	t_{PLH}	0.105	0.097 + 0.004*SL	0.102 + 0.003*SL	0.115 + 0.002*SL
	t_{PHL}	0.116	0.106 + 0.005*SL	0.113 + 0.003*SL	0.139 + 0.002*SL
D2 to Y	t_R	0.051	0.039 + 0.006*SL	0.044 + 0.005*SL	0.033 + 0.005*SL
	t_F	0.066	0.058 + 0.004*SL	0.059 + 0.004*SL	0.062 + 0.004*SL
	t_{PLH}	0.102	0.094 + 0.004*SL	0.099 + 0.003*SL	0.112 + 0.002*SL
	t_{PHL}	0.114	0.104 + 0.005*SL	0.112 + 0.003*SL	0.136 + 0.002*SL
D3 to Y	t_R	0.052	0.043 + 0.005*SL	0.042 + 0.005*SL	0.034 + 0.005*SL
	t_F	0.067	0.060 + 0.004*SL	0.058 + 0.004*SL	0.062 + 0.004*SL
	t_{PLH}	0.101	0.093 + 0.004*SL	0.098 + 0.003*SL	0.111 + 0.002*SL
	t_{PHL}	0.114	0.105 + 0.005*SL	0.112 + 0.003*SL	0.136 + 0.002*SL
S0 to Y	t_R	0.053	0.043 + 0.005*SL	0.043 + 0.005*SL	0.035 + 0.005*SL
	t_F	0.067	0.057 + 0.005*SL	0.061 + 0.004*SL	0.063 + 0.004*SL
	t_{PLH}	0.112	0.104 + 0.004*SL	0.110 + 0.003*SL	0.123 + 0.002*SL
	t_{PHL}	0.125	0.115 + 0.005*SL	0.122 + 0.003*SL	0.148 + 0.002*SL
S1 to Y	t_R	0.049	0.038 + 0.005*SL	0.041 + 0.005*SL	0.035 + 0.005*SL
	t_F	0.064	0.056 + 0.004*SL	0.056 + 0.004*SL	0.061 + 0.004*SL
	t_{PLH}	0.087	0.079 + 0.004*SL	0.084 + 0.003*SL	0.097 + 0.002*SL
	t_{PHL}	0.101	0.091 + 0.005*SL	0.098 + 0.003*SL	0.123 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

mx4d4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.066	0.062 + 0.002*SL	0.061 + 0.002*SL	0.056 + 0.002*SL
	t_F	0.095	0.090 + 0.002*SL	0.091 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.129	0.124 + 0.002*SL	0.127 + 0.001*SL	0.148 + 0.001*SL
	t_{PHL}	0.146	0.140 + 0.003*SL	0.144 + 0.002*SL	0.178 + 0.001*SL
D1 to Y	t_R	0.066	0.061 + 0.002*SL	0.061 + 0.002*SL	0.056 + 0.002*SL
	t_F	0.094	0.090 + 0.002*SL	0.091 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.128	0.123 + 0.002*SL	0.126 + 0.001*SL	0.147 + 0.001*SL
	t_{PHL}	0.146	0.141 + 0.003*SL	0.145 + 0.002*SL	0.179 + 0.001*SL
D2 to Y	t_R	0.065	0.061 + 0.002*SL	0.060 + 0.002*SL	0.055 + 0.002*SL
	t_F	0.093	0.088 + 0.003*SL	0.090 + 0.002*SL	0.096 + 0.002*SL
	t_{PLH}	0.125	0.121 + 0.002*SL	0.124 + 0.001*SL	0.144 + 0.001*SL
	t_{PHL}	0.144	0.139 + 0.003*SL	0.143 + 0.002*SL	0.176 + 0.001*SL
D3 to Y	t_R	0.065	0.060 + 0.002*SL	0.059 + 0.002*SL	0.054 + 0.002*SL
	t_F	0.092	0.087 + 0.003*SL	0.090 + 0.002*SL	0.096 + 0.002*SL
	t_{PLH}	0.124	0.119 + 0.002*SL	0.123 + 0.001*SL	0.143 + 0.001*SL
	t_{PHL}	0.144	0.139 + 0.003*SL	0.143 + 0.002*SL	0.177 + 0.001*SL
S0 to Y	t_R	0.067	0.062 + 0.003*SL	0.063 + 0.002*SL	0.057 + 0.002*SL
	t_F	0.095	0.091 + 0.002*SL	0.090 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.135	0.130 + 0.002*SL	0.133 + 0.001*SL	0.154 + 0.001*SL
	t_{PHL}	0.155	0.150 + 0.003*SL	0.154 + 0.002*SL	0.188 + 0.001*SL
S1 to Y	t_R	0.066	0.061 + 0.003*SL	0.062 + 0.002*SL	0.056 + 0.002*SL
	t_F	0.093	0.089 + 0.002*SL	0.090 + 0.002*SL	0.096 + 0.002*SL
	t_{PLH}	0.107	0.103 + 0.002*SL	0.106 + 0.002*SL	0.127 + 0.001*SL
	t_{PHL}	0.131	0.126 + 0.003*SL	0.130 + 0.002*SL	0.164 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

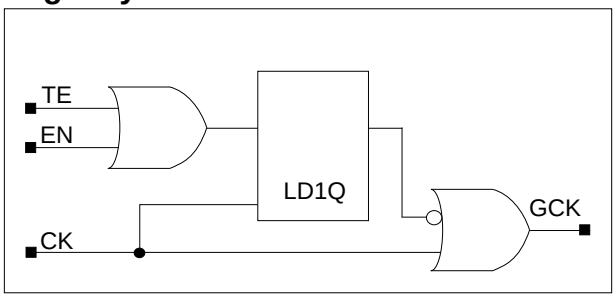
Cell List

Cell Name	Function Description
cgln	Negative Edge Triggered Clock-Gating with 1X Drive
cglnd2	Negative Edge Triggered Clock-Gating with 2X Drive
cglnd4	Negative Edge Triggered Clock-Gating with 4X Drive
cglp	Positive Edge Triggered Clock-Gating with 1X Drive
cglpd2	Positive Edge Triggered Clock-Gating with 2X Drive
cglpd4	Positive Edge Triggered Clock-Gating with 4X Drive

cgln/cglnd2/cglnd4

Negative Edge Triggered Clock-Gating with 1X/2X/4X Drive

Logic Symbol



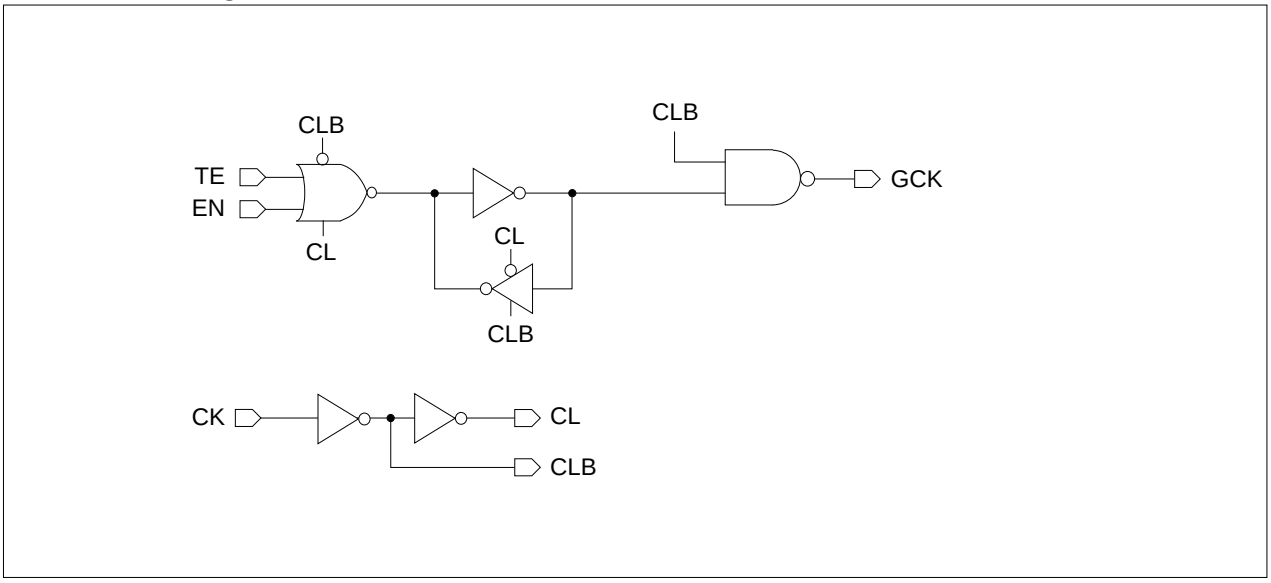
Truth Table

CK	EN	TE	GCK
↓	0	0	1
↓	1	x	0
↓	x	1	0
1	x	x	1

Cell Data

Input Load (SL)								
cgln			*cglnd2*			*cglnd4*		
EN	CK	TE	EN	CK	TE	EN	CK	TE
0.9	1.0	0.9	0.9	1.0	0.9	0.9	1.0	0.9
Gate Count								
cgln			*cglnd2*			*cglnd4*		
5.00			5.67			7.33		

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		cgIn	cgInd2	cgInd4
Input Setup Time (EN to CK)	t_{SU}	0.066	0.066	0.061
Input Hold Time (EN to CK)	t_{HD}	0.010	0.010	0.013
Pulse Width High (CK)	t_{PWH}	0.063	0.069	0.081
Input Setup Time (TE to CK)	t_{SU}	0.074	0.073	0.070
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010

cgIn/cgInd2/cgInd4

Negative Edge Triggered Clock-Gating with 1X/2X/4X Drive

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

cgIn

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.054	0.037 + 0.008*SL	0.029 + 0.010*SL	0.022 + 0.011*SL
	t_F	0.047	0.029 + 0.009*SL	0.027 + 0.010*SL	0.022 + 0.010*SL
	t_{PLH}	0.070	0.059 + 0.006*SL	0.062 + 0.005*SL	0.063 + 0.005*SL
	t_{PHL}	0.069	0.057 + 0.006*SL	0.061 + 0.005*SL	0.063 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

cgInd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.048	0.036 + 0.006*SL	0.040 + 0.005*SL	0.023 + 0.005*SL
	t_F	0.044	0.036 + 0.004*SL	0.033 + 0.005*SL	0.024 + 0.005*SL
	t_{PLH}	0.071	0.065 + 0.003*SL	0.068 + 0.002*SL	0.072 + 0.002*SL
	t_{PHL}	0.070	0.063 + 0.003*SL	0.066 + 0.003*SL	0.072 + 0.002*SL

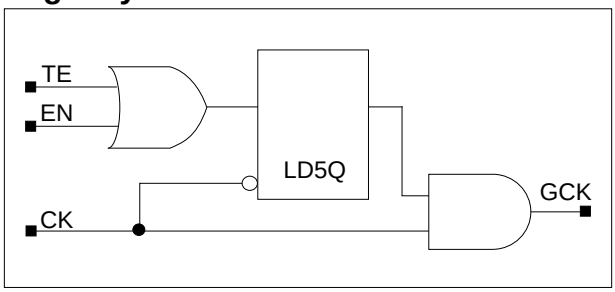
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

cgInd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.047	0.043 + 0.002*SL	0.041 + 0.003*SL	0.032 + 0.003*SL
	t_F	0.043	0.038 + 0.003*SL	0.039 + 0.002*SL	0.034 + 0.002*SL
	t_{PLH}	0.084	0.080 + 0.002*SL	0.083 + 0.001*SL	0.091 + 0.001*SL
	t_{PHL}	0.081	0.077 + 0.002*SL	0.079 + 0.001*SL	0.089 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Logic Symbol



Truth Table

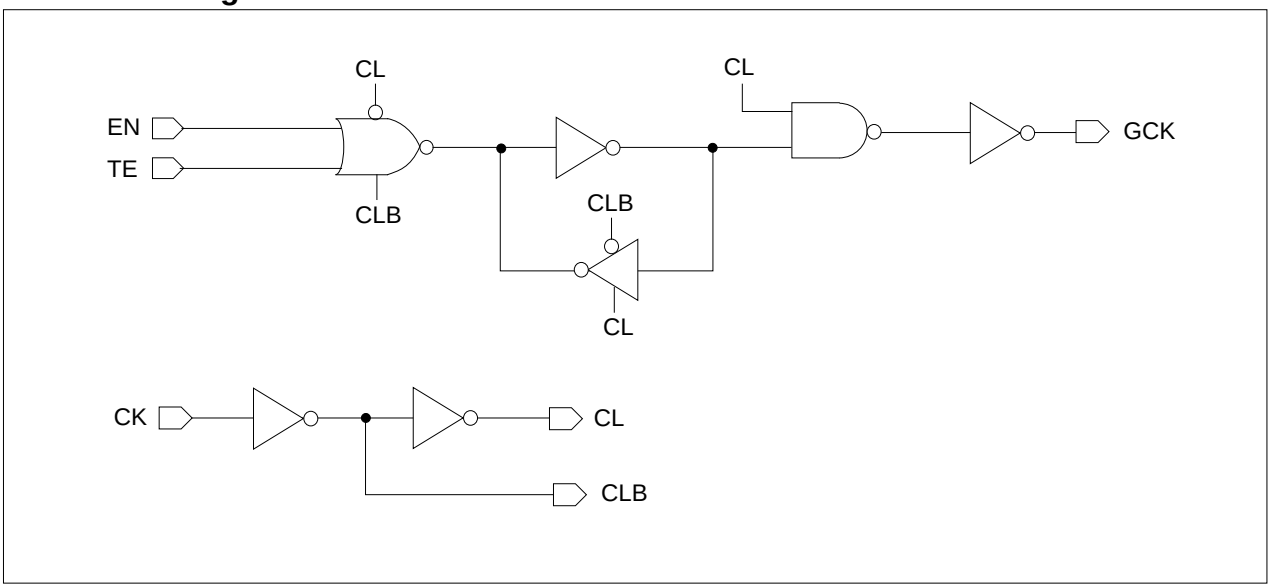
CK	EN	TE	GCK
↑	0	0	0
↑	1	x	1
↑	x	1	1
0	x	x	0

Cell Data

Input Load (SL)								
cglp			*cglpd2*			*cglpd4*		
EN	CK	TE	EN	CK	TE	EN	CK	TE
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9

Gate Count		
cglp	*cglpd2*	*cglpd4*
5.33	6.00	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.2V, Unit = ns)

Parameter	Symbol	Value (ns)		
		cglp	cglpd2	cglpd4
Input Setup Time (EN to CK)	t_{SU}	0.058	0.057	0.059
Input Hold Time (EN to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.067	0.066	0.067
Input Setup Time (TE to CK)	t_{SU}	0.068	0.069	0.069
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 0.08ns, SL: Standard Load)

cglp

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.040	0.021 + 0.009*SL	0.019 + 0.010*SL	0.013 + 0.010*SL
	t_F	0.032	0.016 + 0.008*SL	0.017 + 0.008*SL	0.012 + 0.008*SL
	t_{PLH}	0.103	0.093 + 0.005*SL	0.096 + 0.005*SL	0.096 + 0.004*SL
	t_{PHL}	0.107	0.097 + 0.005*SL	0.100 + 0.004*SL	0.102 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 18, *Group3 : 18 < SL

cglpd2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.033	0.023 + 0.005*SL	0.024 + 0.005*SL	0.015 + 0.005*SL
	t_F	0.027	0.019 + 0.004*SL	0.020 + 0.004*SL	0.015 + 0.004*SL
	t_{PLH}	0.104	0.098 + 0.003*SL	0.101 + 0.002*SL	0.104 + 0.002*SL
	t_{PHL}	0.108	0.102 + 0.003*SL	0.105 + 0.002*SL	0.110 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 32, *Group3 : 32 < SL

cglpd4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.035	0.032 + 0.002*SL	0.029 + 0.002*SL	0.021 + 0.003*SL
	t_F	0.031	0.027 + 0.002*SL	0.026 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.114	0.110 + 0.002*SL	0.113 + 0.001*SL	0.121 + 0.001*SL
	t_{PHL}	0.118	0.114 + 0.002*SL	0.117 + 0.001*SL	0.126 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 61, *Group3 : 61 < SL

Input/Output Cells

4

Contents

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OVERVIEW

This chapter describes the Input/Output cells (2.5V/ 3.3V drive and 5V-tolerant), power/ground and ESD slot cells in the STDH150 library.

The switching characteristics of each cell follow the table of switching characteristics of the cell. The AC characteristics of bi-directional buffers are not included in this data sheet. However, they are the same as the component input and output buffers that make up the bi-directional buffer.

There are many possible combinations of input/output cells, therefore, the naming convention is adopted to help efficiently identify the cell and its characteristics from its name (refer to the naming conventions contained in “Summary Tables” section.)

The “Summary Tables” section shows the list of 2.5V/3.3V drive and 5V-tolerant I/O cells by category (input, output, bi-directional, etc.). Moreover, each section begins with a table containing a brief functional description of each cell in that section.

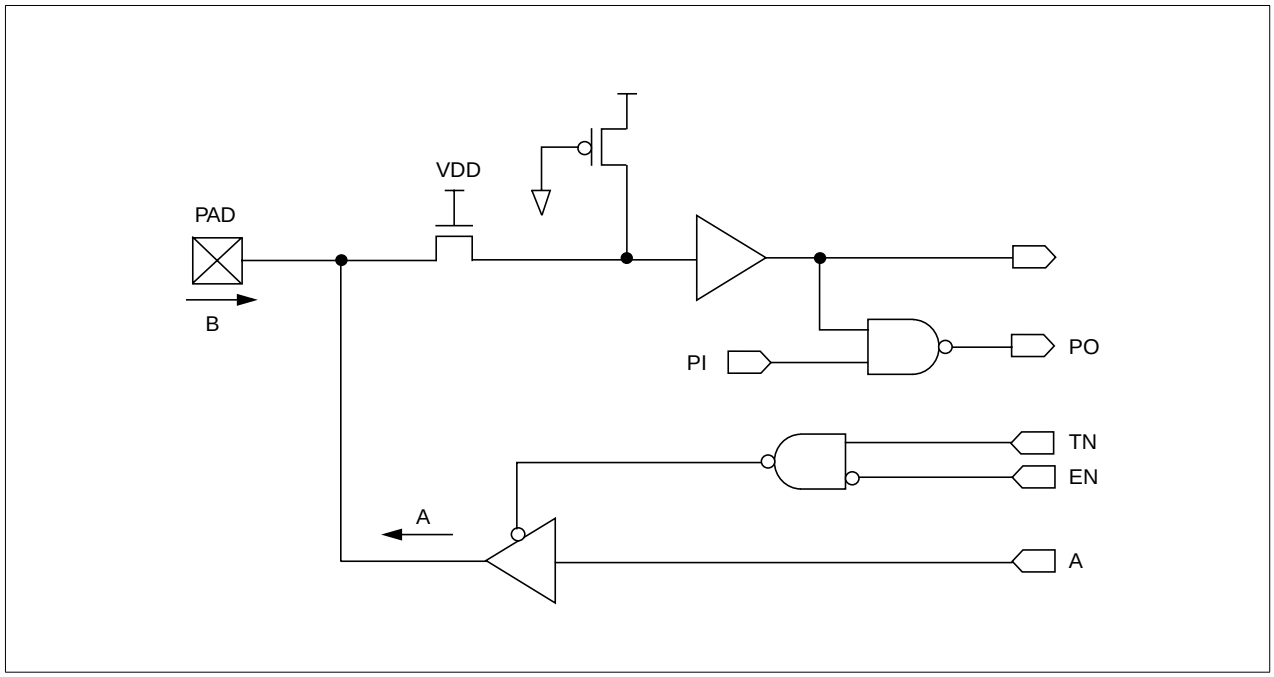


Figure 4-1.

NOTES:

1. It is not allowed to use together the 2.5V / 3.3V interface IO in a chip.
2. As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.
3. When both A and B driving signals do not exist, SEC tolerant IO’s pad voltage goes high state. However, those 3.3V / 5V tolerant input and bi-directional cells with 100kΩ pull-up resistor have NMOS pass transistor like Figure 4.1. Therefore, pad voltage of 3.3V tolerant IO for 2.5V interface could be 1.63V instead of VDD, and pad voltage of 5V tolerant IO for 3.3V interface could be 2.20V instead of VDD.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	Page
CMOS Level	pmic/pmicd/pmicu pmtic/pmticu/pmticd	4-9
	pmnc	
	phic/phicd/phicu phtic/phticd/phticu	
	phnc	
CMOS Schmitt Trigger Level	pmis/pmisd/pmisu	4-14
	phis/phisd/phisu phtis/phtisd/phtisu	

<Naming Convention of Input Buffers>

Pvwlab							
v		**w**		**a**		**b**	
None	1.2V interface	None	Normal	C	CMOS level	None	No resistor
M	2.5V interface	T	Tolerant	S	Schmitt trigger level	D	Pull-down resistor
H	3.3V interface					U	Pull-up resistor

Output Buffers

Cell Type	Cell Name	Current Drive (mA)	Page
Normal	PMOBy	2/4/8/12/16/20/24	4-19
	PMOBySM	4/8/12/16/20/24	
	PMOBySH	12/16/20/24	
	PHOBy	2/4/8/12/16/20/24	
	PHOBySM	4/8/12/16/20/24	
	PHOBySH	12/16/20/24	
Open Drain	PMODy	2/4/8/12/16/20/24	4-30
	PMODySM	4/8/12/16/20/24	
	PMODySH	12/16/20/24	
	PHODy	2/4/8/12/16/20/24	
	PHODySM	4/8/12/16/20/24	
	PHODySH	12/16/20/24	
	PMTODy	2/4/6	
	PMTODySM	4/6	
	PHTODy	2/4/6	
	PHTODySM	4/6	

Cell Type	Cell Name	Current Drive (mA)	Page
Tri-State	PMOTy	2/4/8/12/16/20/24	4-45
	PMOTySM	4/8/12/16/20/24	
	PMOTySH	12/16/20/24	
	PHOTy	2/4/8/12/16/20/24	
	PHOTySM	4/8/12/16/20/24	
	PHOTySH	12/16/20/24	
	PMTOTy	2/4/6	
	PMTOTySM	4/6	
	PHTOTy	2/4/6	
	PHTOTySM	4/6	
DC Output PAD	PMDC		
	PHDC		

<Naming Convention of Output Buffers>

P v O x y z: Normal Output Buffer			
v		**y**	
None	1.2V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
x		8	8mA drive
B	Normal buffer	12	12mA drive
D	Open drain buffer		
T	Tri-state buffer		
z			
None	No slew-rate control		
SM	Medium slew-rate control		
SH	High slew-rate control		
P v T O x y z: Tolerant Output Buffer			
v		**y**	
None	1.2V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
x		6	6mA drive
D	Open drain buffer		
T	Tri-state buffer		
z			
None	No slew-rate control		
SM	Medium slew-rate control		

Bi-Directional Buffers

Cell Type	Cell Name	Page
Open Drain	PMBaDyz/PMBaUDyz PMTBaDyz/PMTBaUDyz	4-71
	PHBaDyz/PHBaUDyz PHTBaDyz/PHTBaUDyz	
Tri-State	PMBaTyz/PMBaDTyz/PMBaUTyz PMTBaTyz/PMTBaDTyz/PMTBaUTyz	4-71
	PHBaTyz/PHBaDTyz/PHBaUTyz PHTBaTyz/PHTBaDTyz/PHTBaUTyz	

<Naming Convention of Bi-Directional Buffers>

P v B a b x y z: Normal Bi-Directional Buffer			
v		**y**	
None	1.2V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
a		8	8mA drive
C	CMOS level	12	12mA driver
S	CMOS Schmitt trigger level		
b			
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		
x		**z**	
B	Normal buffer	None	No slew-rate control
D	Open drain buffer	SM	Medium slew-rate control
T	Tri-state buffer	SH	High slew-rate control
P v T B a b x y z: Tolerant Bi-Directional Buffer			
v		**x**	
None	1.2V interface	D	Open drain buffer
M	2.5V interface	T	Tri-state buffer
H	3.3V interface	**y**	
a		1	1mA drive
C	CMOS level	2	2mA drive
S	CMOS Schmitt trigger level	4	4mA drive
T	TTL level	6	6mA drive
b		**z**	
None	No resistor	None	No slew rate control
D	Pull-down resistor	SM	Midium slew rate control
U	Pull-up resistor		

Oscillators

Cell Type	Cell Name	Page
3.3V Oscillator	phsosck1//m1/m2/m3	4-74
	phsosck17/m16/m26/m36	4-79
2.5V Oscillator	pmsosck1/m1/m2	4-84

PCI Buffers

Cell Type	Cell Name	Page
5V-tolerant PCI-X Input	ptipcix	4-91
5V-tolerant PCI-X Input	ptopcix	4-92

Power Ground Pads

Descriptions		Cell Name	Supply Voltage	Page
Power for	2.5V Interface Digital I/O	vdd12im, vdd12im_core	1.2V	4-93
		vdd25(o/p/op)m	2.5V	
	3.3V Interface Digital I/O	vdd12ih, vdd12ih_core	1.2V	
		vdd33(o/p/op)h	3.3V	
	2.5V Interface Analog I/O	vdd12im_abb	1.2V	4-94
		vdd25(i/op/t)m_abb	2.5V	
	3.3V Interface Analog I/O	vdd12i_abb	1.2V	
		vdd33(i/op/t)h_abb	3.3V	
Ground for	2.5V Interface Digital I/O	vss(i/o/p/ip/op/t)m		4-93
	3.3V Interface Digital I/O	vss(i/o/p/ip/op/t)h		
	2.5V Interface Analog I/O	vss(i/op/t)m_abb		4-94
		vbbm_abb/vssbbm_abb		
	3.3V Interface Analog I/O	vss(i/op/t)h_abb		
		vbbh_abb/vssbbh_abb		

Analog Interface

Cell Type	Cell Name	Page
2.5V Analog Input with Separated Bulk-Bias	pmnc_abb pmia_abb/pmiar10_abb/pmiar50_abb pmic_abb/pmicd_abb/pmicu_abb/ pmicc_abb/pmicen_abb pmis_abb/pmisd_abb/pmisu_abb	4-97
3.3V Analog Input with Separated Bulk-Bias	phnc_abb phia_abb/phiar10_abb/phiar50_abb phic_abb/phicd_abb/phicu_abb/ phicc_abb/phicen_abb phis_abb/phisd_abb/phisu_abb	
2.5V Analog Output with Separated Bulk-Bias	pmoa_abb/pmoar10_abb/pmoar50_abb pmob(1/2/4/8/12)_abb/pmot(1/2/4/8/12)_abb	4-106
3.3V Analog Output with Separated Bulk-Bias	phoa_abb/phoar10_abb/phoar50_abb phob(1/2/4/8/12)_abb/phot(1/2/4/8/12)_abb, phod4sm_abb	
2.5V Analog Bi-Directional with Separated Bulk-Bias	pmbct(1/2/4/8)_abb	
3.3V Analog Bi-Directional with Separated Bulk-Bias	phbct(1/2/4/8)_abb, phbsd4sm_abb	

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

Slot Cells

Descriptions		Cell Name	Page
ESD Slot Cells for	2.5V Interface Digital I/Os	ev12im	4-119
		ev25(o//p/op)m	
	3.3V Interface Digital I/Os	ev12ih	
		ev33(o/p/op)h	
	2.5V Interface Analog I/Os	ev12im_abb	
		ev25(i/op/t)m_abb	
	3.3V Interface Analog I/Os	ev12ih_abb	
		ev33(i/op/t)h_abb	
Common Slot Cells		ec0c0/ec0c0d ec0ca0/ec0ca0d eca0ca0/eca0ca0d eca0ca0_vbb/eca0ca0d_vbb	4-120

IO Filler Cells

Descriptions		Cell Name
Digital Filler Cells	2.5V Interface Filler I/Os	IOFILLERM(1/10/35/_02/_1)
	3.3V Interface Filler I/Os	IOFILLERH(1/10/35/_02/_1)
Analog Filler Cells	2.5V Interface Filler I/Os	IOFILLERM(1/10/35/_02/_1)_ABB
	3.3V Interface Filler I/Os	IOFILLERH(1/10/35/_02/_1)_ABB

Corner Cells

Descriptions		Cell Name
Digital Corner Cells	2.5V Interface Corner I/Os	(L/R) (T/B)CORNERM
	3.3V Interface Corner I/Os	(L/R) (T/B)CORNERH
Analog Cornet Cells	2.5V Interface Corner I/Os	(L/R) (T/B)CORNERM_ABB
	3.3V Interface Corner I/Os	(L/R) (T/B)CORNERH_ABB

INPUT BUFFERS

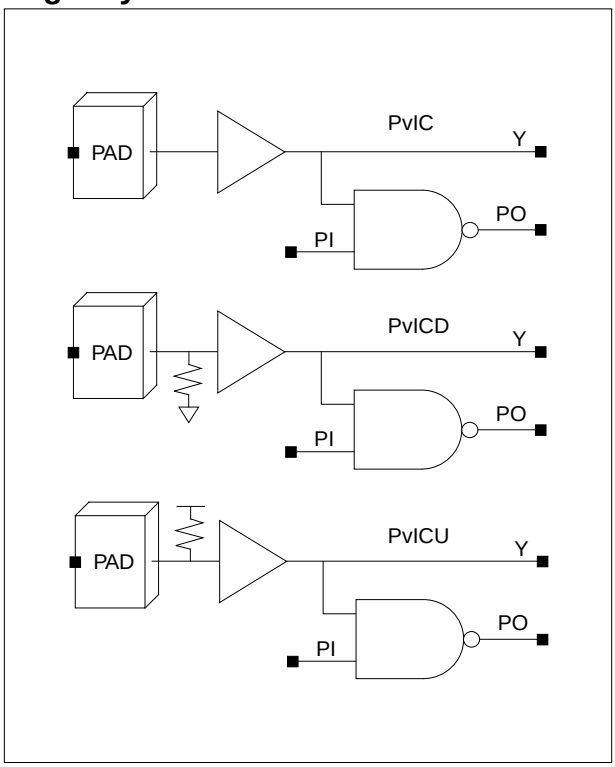
Cell List

Cell Name	Function Description
pmic/pmicd/pmicu	2.5V Interface CMOS Level Input Buffers
phic/phicd/phicu	3.3V Interface CMOS Level Input Buffers
pmtic/pmticd/pmticu	5V-tolerant for 2.5V Interface CMOS Level Input Buffers
phtic/phticd/phticu	5V-tolerant for 3.3V Interface CMOS Level Input Buffers
pmis/pmisd/pmisu	2.5V Interface CMOS Schmitt Trigger Level Input Buffers
phis/phisd/phisu	3.3V Interface CMOS Schmitt Trigger Level Input Buffers
phtis/phtisd/phtisu	5V-tolerant for 3.3V Interface CMOS Schmitt Trigger Level Input Buffers
pmnc	No Connection PAD for 2.5V Interface
phnc	No Connection PAD for 3.3V Interface

Cell Availability

2.5V Interface		3.3V Interface	
2.5V Interface	**5V-Tolerant**	**3.3V Interface**	**5V-Tolerant**
pmic pmicd pmicu	pmtic pmticd pmticu	phic phicd phicu	phtic phticd phticu

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
pmic/pmicd/pmicu	10.52
pmtic/pmticd/pmticu	10.52
phic/phicd/phicu	10.52
phtic/phticd/phticu	10.52

Input Buffers

Switching Characteristics (Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmic

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.135 + 0.013*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.153	0.123 + 0.016*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.705	0.689 + 0.009*SL	0.691 + 0.007*SL	0.705 + 0.006*SL
	t_{PHL}	0.761	0.741 + 0.013*SL	0.742 + 0.009*SL	0.767 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmicd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.136 + 0.012*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.152	0.122 + 0.017*SL	0.123 + 0.014*SL	0.128 + 0.014*SL
	t_{PLH}	0.739	0.724 + 0.009*SL	0.725 + 0.007*SL	0.739 + 0.006*SL
	t_{PHL}	0.772	0.751 + 0.012*SL	0.753 + 0.009*SL	0.778 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmicu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.136 + 0.012*SL	0.136 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.153	0.123 + 0.016*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.714	0.699 + 0.009*SL	0.700 + 0.007*SL	0.714 + 0.006*SL
	t_{PHL}	0.794	0.774 + 0.012*SL	0.775 + 0.009*SL	0.800 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics (Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmtic

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.135 + 0.012*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.152	0.122 + 0.016*SL	0.123 + 0.014*SL	0.128 + 0.014*SL
	t_{PLH}	0.900	0.884 + 0.009*SL	0.885 + 0.007*SL	0.900 + 0.006*SL
	t_{PHL}	0.947	0.926 + 0.012*SL	0.928 + 0.009*SL	0.952 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmticd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.134 + 0.013*SL	0.135 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.152	0.122 + 0.016*SL	0.123 + 0.014*SL	0.128 + 0.014*SL
	t_{PLH}	0.940	0.924 + 0.009*SL	0.925 + 0.007*SL	0.939 + 0.006*SL
	t_{PHL}	0.953	0.932 + 0.012*SL	0.934 + 0.009*SL	0.959 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmticu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.140 + 0.006*SL	0.136 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.150	0.121 + 0.016*SL	0.121 + 0.015*SL	0.128 + 0.014*SL
	t_{PLH}	0.908	0.892 + 0.009*SL	0.893 + 0.007*SL	0.908 + 0.006*SL
	t_{PHL}	1.019	0.998 + 0.012*SL	1.000 + 0.009*SL	1.025 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).11

Input Buffers

Switching Characteristics (Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phic

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.134 + 0.013*SL	0.134 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.151	0.121 + 0.016*SL	0.122 + 0.015*SL	0.128 + 0.014*SL
	t_{PLH}	0.535	0.520 + 0.009*SL	0.521 + 0.007*SL	0.535 + 0.006*SL
	t_{PHL}	0.875	0.855 + 0.012*SL	0.857 + 0.009*SL	0.881 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phicd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.135 + 0.013*SL	0.136 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.151	0.119 + 0.019*SL	0.122 + 0.015*SL	0.128 + 0.014*SL
	t_{PLH}	0.578	0.562 + 0.009*SL	0.563 + 0.007*SL	0.578 + 0.006*SL
	t_{PHL}	0.896	0.876 + 0.012*SL	0.877 + 0.009*SL	0.902 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phicu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.135 + 0.013*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.153	0.122 + 0.017*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.537	0.522 + 0.009*SL	0.523 + 0.007*SL	0.537 + 0.006*SL
	t_{PHL}	0.904	0.883 + 0.012*SL	0.885 + 0.009*SL	0.909 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics (Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phtic

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.136 + 0.010*SL	0.135 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.152	0.122 + 0.017*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.681	0.665 + 0.009*SL	0.667 + 0.007*SL	0.681 + 0.006*SL
	t_{PHL}	0.996	0.975 + 0.012*SL	0.977 + 0.009*SL	1.002 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phticd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.135 + 0.013*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.152	0.120 + 0.018*SL	0.123 + 0.015*SL	0.129 + 0.014*SL
	t_{PLH}	0.727	0.711 + 0.009*SL	0.712 + 0.007*SL	0.727 + 0.006*SL
	t_{PHL}	1.011	0.991 + 0.012*SL	0.992 + 0.009*SL	1.017 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phticu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.136 + 0.013*SL	0.136 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.151	0.121 + 0.016*SL	0.122 + 0.015*SL	0.128 + 0.014*SL
	t_{PLH}	0.680	0.664 + 0.009*SL	0.666 + 0.007*SL	0.680 + 0.006*SL
	t_{PHL}	1.037	1.016 + 0.012*SL	1.018 + 0.009*SL	1.043 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

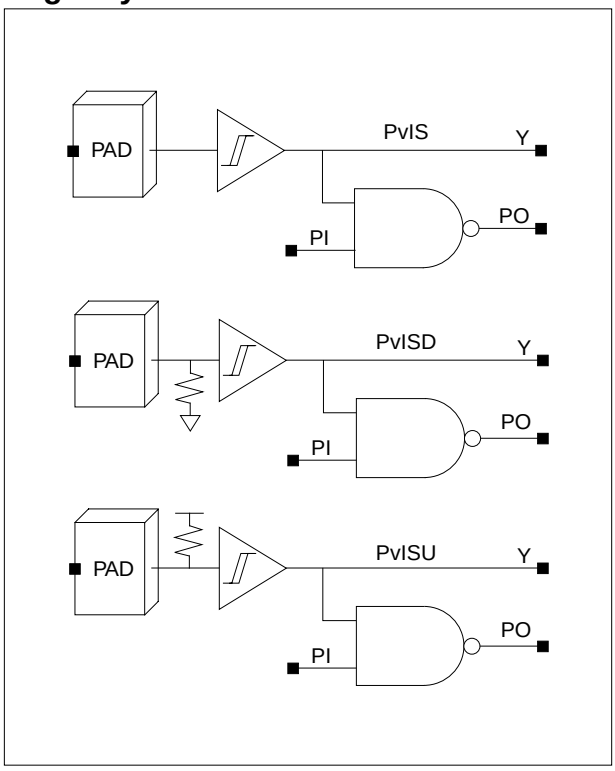
PvIS/PvISD/PvISU

Schmitt Trigger Level Input Buffers

Cell Availability

2.5V Interface	3.3V Interface	
	3.3V Interface	5V-Tolerant
pmis pmisd pmisu	phis phisd phisu	phtis phtisd phtisu

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
pmis/pmisd/pmisu	10.52
phis/phisd/phisu	10.52
phtis/phtisd/phtisu	10.52

Switching Characteristics

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmis

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.136 + 0.011*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.150	0.120 + 0.016*SL	0.121 + 0.015*SL	0.127 + 0.014*SL
	t_{PLH}	1.059	1.044 + 0.009*SL	1.045 + 0.007*SL	1.059 + 0.006*SL
	t_{PHL}	1.219	1.199 + 0.012*SL	1.201 + 0.009*SL	1.225 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmisd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.135 + 0.013*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.151	0.122 + 0.015*SL	0.122 + 0.014*SL	0.128 + 0.014*SL
	t_{PLH}	1.069	1.054 + 0.009*SL	1.055 + 0.007*SL	1.069 + 0.006*SL
	t_{PHL}	1.279	1.259 + 0.012*SL	1.260 + 0.009*SL	1.285 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmisu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.135 + 0.011*SL	0.134 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.152	0.122 + 0.015*SL	0.123 + 0.014*SL	0.128 + 0.014*SL
	t_{PLH}	1.093	1.078 + 0.009*SL	1.079 + 0.007*SL	1.093 + 0.006*SL
	t_{PHL}	1.211	1.190 + 0.012*SL	1.192 + 0.009*SL	1.217 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics (Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phis

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.135 + 0.013*SL	0.136 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.152	0.123 + 0.015*SL	0.123 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.865	0.850 + 0.009*SL	0.851 + 0.007*SL	0.866 + 0.006*SL
	t_{PHL}	1.235	1.214 + 0.012*SL	1.216 + 0.009*SL	1.240 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phisd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.135 + 0.013*SL	0.135 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.150	0.121 + 0.015*SL	0.121 + 0.015*SL	0.128 + 0.014*SL
	t_{PLH}	0.889	0.873 + 0.009*SL	0.875 + 0.007*SL	0.889 + 0.006*SL
	t_{PHL}	1.278	1.257 + 0.012*SL	1.259 + 0.009*SL	1.284 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phisu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.135 + 0.014*SL	0.136 + 0.012*SL	0.127 + 0.013*SL
	t_F	0.152	0.123 + 0.015*SL	0.123 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	0.886	0.871 + 0.009*SL	0.872 + 0.007*SL	0.887 + 0.006*SL
	t_{PHL}	1.237	1.216 + 0.012*SL	1.218 + 0.009*SL	1.242 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics (Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phtis

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.136 + 0.013*SL	0.136 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.152	0.123 + 0.015*SL	0.123 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	1.054	1.038 + 0.009*SL	1.039 + 0.007*SL	1.054 + 0.006*SL
	t_{PHL}	1.376	1.355 + 0.012*SL	1.357 + 0.009*SL	1.381 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phtisd

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.161	0.136 + 0.012*SL	0.136 + 0.013*SL	0.127 + 0.013*SL
	t_F	0.153	0.123 + 0.016*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	1.079	1.064 + 0.009*SL	1.065 + 0.007*SL	1.079 + 0.006*SL
	t_{PHL}	1.404	1.384 + 0.012*SL	1.386 + 0.009*SL	1.410 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phtisu

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.160	0.136 + 0.010*SL	0.134 + 0.013*SL	0.128 + 0.013*SL
	t_F	0.153	0.123 + 0.016*SL	0.124 + 0.014*SL	0.129 + 0.014*SL
	t_{PLH}	1.083	1.068 + 0.009*SL	1.069 + 0.007*SL	1.083 + 0.006*SL
	t_{PHL}	1.370	1.349 + 0.012*SL	1.351 + 0.009*SL	1.376 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

OUTPUT BUFFERS

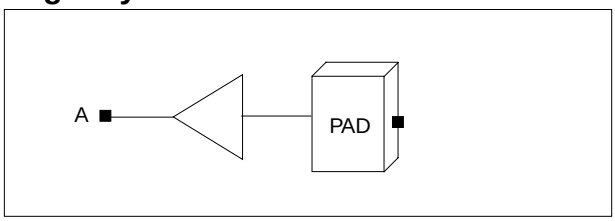
Cell List

Cell Name	Function Description
pmob(2/4/8/12/16/20/24)	2.5V CMOS Normal Output Buffers
pmob(4/8/12/16/20/24)sm	2.5V CMOS Normal Output Buffers with Medium Slew-Rate
pmob(12/16/20/24)sh	2.5V CMOS Normal Output Buffers with High Slew-Rate
phob(2/4/8/12/16/20/24)	3.3V CMOS Normal Output Buffers
phob(4/8/12/16/20/24)sm	3.3V CMOS Normal Output Buffers with Medium Slew-Rate
phob(12/16/20/24)sh	3.3V CMOS Normal Output Buffers with High Slew-Rate
pmod(2/4/8/12/16/20/24)	2.5V CMOS Open Drain Output Buffers
pmod(4/8/12/16/20/24)sm	2.5V CMOS Open Drain Output Buffers with Medium Slew-Rate
pmod(12/16/20/24)sh	2.5V CMOS Open Drain Output Buffers with High Slew-Rate
phod(2/4/8/12/16/20/24)	3.3V CMOS Open Drain Output Buffers
phod(4/8/12/16/20/24)sm	3.3V CMOS Open Drain Output Buffers with Medium Slew-Rate
phod(12/16/20/24)sh	3.3V CMOS Open Drain Output Buffers with High Slew-Rate
pmot(2/4/8/12/16/20/24)	2.5V CMOS Tri-State Output Buffers
pmot(4/8/12/16/20/24)sm	2.5V CMOS Tri-State Output Buffers with Medium Slew-Rate
pmot(12/16/20/24)sh	2.5V CMOS Tri-State Output Buffers with High Slew-Rate
phot(2/4/8/12/16/20/24)	3.3V CMOS Tri-State Output Buffers
phot(4/8/12/16/20/24)sm	3.3V CMOS Tri-State Output Buffers with Medium Slew-Rate
phot(12/16/20/24)sh	3.3V CMOS Tri-State Output Buffers with High Slew-Rate
pmtod(2/4/6)	5V-Tolerant for 2.5V CMOS Open Drain Output Buffers
pmtod(4/6)sm	5V-Tolerant for 2.5V CMOS Open Drain Output Buffers with Medium Slew-Rate
phtod(2/4/6)	5V-Tolerant for 3.3V CMOS Open Drain Output Buffers
phtod(4/6)sm	5V-Tolerant for 3.3V CMOS Open Drain Output Buffers with Medium Slew-Rate
pmtot(2/4/6)	5V-Tolerant for 2.5V CMOS Tri-State Output Buffers
pmtot(4/6)sm	5V-Tolerant for 2.5V CMOS Tri-State Output Buffers with Medium Slew-Rate
phtot(2/4/6)	5V-Tolerant for 3.3V CMOS Tri-State Output Buffers
phtot(4/6)sm	5V-Tolerant for 3.3V CMOS Tri-State Output Buffers with Medium Slew-Rate

Cell Availability

2.5V Interface	3.3V Interface
pmob(2/4/8/12/16/20/24) pmob(4/8/12/16/20/24)sm pmob(12/16/20/24)sh	phob(2/4/8/12/16/20/24) phob(4/8/12/16/20/24)sm phob(12/16/20/24)sh

Logic Symbol



Truth Table

A	PAD
0	0
1	1

Standard Load (SL)

Cell Name	A
pmob(2/4/8/12/16/20/24)	8.95
pmob(4/8/12/16/20/24)sm	8.95
pmob(12/16/20/24)sh	8.95
phob(2/4/8/12/16/20/24)	8.95
phob(4/8/12/16/20/24)sm	8.95
phob(12/16/20/24)sh	8.95

PvOByz

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmob2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	11.872	0.388 + 0.229*CL	0.317 + 0.231*CL	0.296 + 0.232*CL
	t_F	10.870	0.353 + 0.209*CL	0.290 + 0.212*CL	0.266 + 0.212*CL
	t_{PLH}	6.293	1.294 + 0.100*CL	1.300 + 0.100*CL	1.301 + 0.100*CL
	t_{PHL}	6.653	1.288 + 0.107*CL	1.296 + 0.107*CL	1.297 + 0.107*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.925	0.138 + 0.116*CL	0.133 + 0.116*CL	0.133 + 0.116*CL
	t_F	6.616	0.130 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PLH}	3.372	0.876 + 0.050*CL	0.876 + 0.050*CL	0.876 + 0.050*CL
	t_{PHL}	4.266	0.829 + 0.069*CL	0.826 + 0.069*CL	0.825 + 0.069*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.982	0.132 + 0.057*CL	0.102 + 0.058*CL	0.090 + 0.058*CL
	t_F	3.313	0.092 + 0.064*CL	0.072 + 0.065*CL	0.070 + 0.065*CL
	t_{PLH}	2.194	0.944 + 0.025*CL	0.946 + 0.025*CL	0.946 + 0.025*CL
	t_{PHL}	2.540	0.840 + 0.034*CL	0.827 + 0.034*CL	0.823 + 0.034*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.022	0.170 + 0.037*CL	0.135 + 0.038*CL	0.111 + 0.038*CL
	t_F	2.217	0.129 + 0.041*CL	0.079 + 0.043*CL	0.058 + 0.043*CL
	t_{PLH}	1.858	1.004 + 0.017*CL	1.024 + 0.017*CL	1.025 + 0.017*CL
	t_{PHL}	1.988	0.889 + 0.022*CL	0.863 + 0.023*CL	0.852 + 0.023*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmob16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.567	0.208 + 0.027*CL	0.183 + 0.028*CL	0.157 + 0.028*CL
	t_F	1.684	0.187 + 0.029*CL	0.123 + 0.031*CL	0.088 + 0.032*CL
	t_{PLH}	1.730	1.046 + 0.014*CL	1.092 + 0.013*CL	1.104 + 0.013*CL
	t_{PHL}	1.737	0.946 + 0.015*CL	0.916 + 0.016*CL	0.896 + 0.017*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.262	0.179 + 0.021*CL	0.158 + 0.022*CL	0.136 + 0.023*CL
	t_F	1.445	0.404 + 0.019*CL	0.289 + 0.023*CL	0.228 + 0.024*CL
	t_{PLH}	1.516	0.963 + 0.012*CL	1.004 + 0.010*CL	1.014 + 0.010*CL
	t_{PHL}	1.642	1.032 + 0.012*CL	1.051 + 0.012*CL	1.014 + 0.013*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.095	0.198 + 0.018*CL	0.191 + 0.018*CL	0.171 + 0.018*CL
	t_F	1.294	0.508 + 0.014*CL	0.399 + 0.018*CL	0.318 + 0.020*CL
	t_{PLH}	1.484	0.986 + 0.011*CL	1.040 + 0.009*CL	1.060 + 0.008*CL
	t_{PHL}	1.602	1.072 + 0.011*CL	1.108 + 0.010*CL	1.105 + 0.010*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOByz

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmob4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.978	0.306 + 0.113*CL	0.253 + 0.115*CL	0.215 + 0.115*CL
	t_F	6.654	0.220 + 0.128*CL	0.183 + 0.129*CL	0.170 + 0.130*CL
	t_{PLH}	3.733	1.206 + 0.051*CL	1.235 + 0.050*CL	1.236 + 0.050*CL
	t_{PHL}	4.517	1.070 + 0.069*CL	1.074 + 0.069*CL	1.075 + 0.069*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.384	0.592 + 0.056*CL	0.638 + 0.055*CL	0.612 + 0.055*CL
	t_F	3.454	0.301 + 0.063*CL	0.298 + 0.063*CL	0.267 + 0.064*CL
	t_{PLH}	3.275	1.677 + 0.034*CL	1.866 + 0.028*CL	1.962 + 0.026*CL
	t_{PHL}	2.995	1.159 + 0.038*CL	1.241 + 0.035*CL	1.267 + 0.035*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.714	0.699 + 0.042*CL	0.834 + 0.038*CL	0.881 + 0.037*CL
	t_F	2.679	0.446 + 0.046*CL	0.578 + 0.042*CL	0.613 + 0.041*CL
	t_{PLH}	3.243	1.830 + 0.032*CL	2.073 + 0.023*CL	2.226 + 0.020*CL
	t_{PHL}	2.811	1.266 + 0.033*CL	1.444 + 0.027*CL	1.560 + 0.025*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmob16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.191	0.619 + 0.033*CL	0.748 + 0.029*CL	0.805 + 0.028*CL
	t_F	2.066	0.360 + 0.035*CL	0.460 + 0.032*CL	0.497 + 0.031*CL
	t_{PLH}	2.842	1.676 + 0.026*CL	1.890 + 0.019*CL	2.028 + 0.016*CL
	t_{PHL}	2.466	1.287 + 0.025*CL	1.417 + 0.021*CL	1.504 + 0.019*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.887	0.596 + 0.028*CL	0.726 + 0.023*CL	0.787 + 0.022*CL
	t_F	1.612	0.291 + 0.027*CL	0.350 + 0.025*CL	0.368 + 0.025*CL
	t_{PLH}	2.682	1.647 + 0.023*CL	1.856 + 0.017*CL	1.993 + 0.014*CL
	t_{PHL}	2.132	1.245 + 0.019*CL	1.331 + 0.016*CL	1.390 + 0.015*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.829	0.642 + 0.026*CL	0.790 + 0.021*CL	0.875 + 0.019*CL
	t_F	1.440	0.309 + 0.023*CL	0.371 + 0.021*CL	0.401 + 0.021*CL
	t_{PLH}	2.757	1.719 + 0.024*CL	1.943 + 0.016*CL	2.094 + 0.013*CL
	t_{PHL}	2.103	1.315 + 0.017*CL	1.394 + 0.014*CL	1.457 + 0.013*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOByz

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmob12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.351	0.853 + 0.054*CL	1.137 + 0.044*CL	1.330 + 0.040*CL
	t_F	2.850	0.560 + 0.048*CL	0.708 + 0.043*CL	0.768 + 0.042*CL
	t_{PLH}	3.655	1.827 + 0.041*CL	2.122 + 0.031*CL	2.356 + 0.026*CL
	t_{PHL}	3.200	1.528 + 0.036*CL	1.743 + 0.029*CL	1.886 + 0.026*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.013	0.887 + 0.047*CL	1.188 + 0.037*CL	1.399 + 0.032*CL
	t_F	2.401	0.541 + 0.040*CL	0.721 + 0.034*CL	0.813 + 0.032*CL
	t_{PLH}	3.535	1.830 + 0.038*CL	2.137 + 0.028*CL	2.380 + 0.023*CL
	t_{PHL}	2.983	1.556 + 0.031*CL	1.759 + 0.024*CL	1.907 + 0.022*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.505	0.866 + 0.036*CL	1.080 + 0.029*CL	1.222 + 0.026*CL
	t_F	2.140	0.567 + 0.034*CL	0.736 + 0.028*CL	0.832 + 0.026*CL
	t_{PLH}	3.457	2.039 + 0.032*CL	2.330 + 0.023*CL	2.531 + 0.019*CL
	t_{PHL}	2.950	1.649 + 0.029*CL	1.860 + 0.022*CL	2.011 + 0.019*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.325	0.856 + 0.032*CL	1.065 + 0.025*CL	1.208 + 0.022*CL
	t_F	1.989	0.521 + 0.032*CL	0.706 + 0.026*CL	0.830 + 0.023*CL
	t_{PLH}	3.347	2.013 + 0.030*CL	2.297 + 0.021*CL	2.494 + 0.017*CL
	t_{PHL}	2.818	1.643 + 0.026*CL	1.816 + 0.020*CL	1.957 + 0.017*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phob2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.755	0.592 + 0.262*CL	0.466 + 0.266*CL	0.401 + 0.267*CL
	t_F	12.919	0.661 + 0.243*CL	0.534 + 0.248*CL	0.447 + 0.249*CL
	t_{PLH}	7.767	1.815 + 0.119*CL	1.847 + 0.118*CL	1.850 + 0.118*CL
	t_{PHL}	8.099	1.928 + 0.124*CL	1.998 + 0.122*CL	2.006 + 0.122*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.843	0.162 + 0.133*CL	0.151 + 0.134*CL	0.149 + 0.134*CL
	t_F	6.407	0.172 + 0.124*CL	0.148 + 0.125*CL	0.143 + 0.125*CL
	t_{PLH}	3.838	0.878 + 0.059*CL	0.879 + 0.059*CL	0.879 + 0.059*CL
	t_{PHL}	4.035	0.989 + 0.061*CL	0.989 + 0.061*CL	0.989 + 0.061*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.462	0.195 + 0.065*CL	0.153 + 0.066*CL	0.130 + 0.067*CL
	t_F	3.270	0.224 + 0.061*CL	0.197 + 0.061*CL	0.168 + 0.062*CL
	t_{PLH}	2.499	1.004 + 0.030*CL	1.018 + 0.030*CL	1.020 + 0.030*CL
	t_{PHL}	2.695	1.135 + 0.032*CL	1.168 + 0.031*CL	1.172 + 0.030*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.387	0.263 + 0.042*CL	0.235 + 0.043*CL	0.201 + 0.044*CL
	t_F	2.299	0.289 + 0.040*CL	0.286 + 0.040*CL	0.269 + 0.041*CL
	t_{PLH}	2.161	1.102 + 0.022*CL	1.159 + 0.020*CL	1.172 + 0.020*CL
	t_{PHL}	2.381	1.257 + 0.023*CL	1.325 + 0.021*CL	1.355 + 0.021*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOByz

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phob16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.901	0.312 + 0.032*CL	0.322 + 0.032*CL	0.295 + 0.032*CL
	t_F	1.867	0.351 + 0.031*CL	0.368 + 0.030*CL	0.362 + 0.030*CL
	t_{PLH}	2.064	1.176 + 0.019*CL	1.269 + 0.016*CL	1.308 + 0.015*CL
	t_{PHL}	2.305	1.383 + 0.019*CL	1.451 + 0.017*CL	1.503 + 0.016*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.474	0.210 + 0.025*CL	0.193 + 0.026*CL	0.171 + 0.026*CL
	t_F	1.494	0.483 + 0.019*CL	0.385 + 0.022*CL	0.331 + 0.023*CL
	t_{PLH}	1.687	1.054 + 0.013*CL	1.084 + 0.012*CL	1.095 + 0.012*CL
	t_{PHL}	1.940	1.307 + 0.013*CL	1.351 + 0.012*CL	1.354 + 0.012*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.227	0.174 + 0.021*CL	0.159 + 0.021*CL	0.141 + 0.022*CL
	t_F	1.239	0.391 + 0.016*CL	0.312 + 0.019*CL	0.268 + 0.019*CL
	t_{PLH}	1.539	1.014 + 0.011*CL	1.038 + 0.010*CL	1.046 + 0.010*CL
	t_{PHL}	1.740	1.215 + 0.011*CL	1.250 + 0.010*CL	1.251 + 0.010*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phob4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.231	0.741 + 0.130*CL	0.747 + 0.130*CL	0.688 + 0.131*CL
	t_F	6.712	0.689 + 0.120*CL	0.661 + 0.121*CL	0.582 + 0.123*CL
	t_{PLH}	5.171	1.869 + 0.069*CL	2.083 + 0.062*CL	2.173 + 0.060*CL
	t_{PHL}	5.232	1.908 + 0.069*CL	2.107 + 0.063*CL	2.167 + 0.061*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.922	0.683 + 0.066*CL	0.743 + 0.064*CL	0.719 + 0.064*CL
	t_F	3.900	0.736 + 0.065*CL	0.877 + 0.060*CL	0.907 + 0.060*CL
	t_{PLH}	3.705	1.807 + 0.041*CL	2.031 + 0.033*CL	2.147 + 0.031*CL
	t_{PHL}	4.146	1.977 + 0.047*CL	2.278 + 0.037*CL	2.457 + 0.034*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.161	0.824 + 0.049*CL	0.980 + 0.044*CL	1.039 + 0.042*CL
	t_F	3.320	0.857 + 0.052*CL	1.098 + 0.044*CL	1.234 + 0.042*CL
	t_{PLH}	3.704	2.019 + 0.038*CL	2.312 + 0.028*CL	2.495 + 0.024*CL
	t_{PHL}	4.212	2.185 + 0.045*CL	2.550 + 0.033*CL	2.798 + 0.028*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOByz

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phob16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.661	0.792 + 0.040*CL	0.958 + 0.034*CL	1.042 + 0.032*CL
	t_F	2.905	0.840 + 0.045*CL	1.094 + 0.036*CL	1.249 + 0.033*CL
	t_{PLH}	3.411	1.941 + 0.033*CL	2.223 + 0.024*CL	2.405 + 0.020*CL
	t_{PHL}	4.049	2.217 + 0.041*CL	2.572 + 0.030*CL	2.820 + 0.025*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.079	0.632 + 0.031*CL	0.761 + 0.026*CL	0.815 + 0.025*CL
	t_F	2.093	0.509 + 0.034*CL	0.708 + 0.028*CL	0.823 + 0.025*CL
	t_{PLH}	2.819	1.673 + 0.026*CL	1.898 + 0.018*CL	2.042 + 0.016*CL
	t_{PHL}	3.078	1.838 + 0.027*CL	2.040 + 0.021*CL	2.197 + 0.018*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.606	0.415 + 0.025*CL	0.520 + 0.022*CL	0.554 + 0.021*CL
	t_F	1.593	0.498 + 0.022*CL	0.527 + 0.021*CL	0.564 + 0.021*CL
	t_{PLH}	2.241	1.391 + 0.019*CL	1.539 + 0.014*CL	1.635 + 0.012*CL
	t_{PHL}	2.482	1.707 + 0.016*CL	1.774 + 0.014*CL	1.838 + 0.013*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phob12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.022	1.233 + 0.060*CL	1.547 + 0.050*CL	1.739 + 0.046*CL
	t_F	4.453	1.170 + 0.072*CL	1.614 + 0.057*CL	1.932 + 0.050*CL
	t_{PLH}	4.907	2.629 + 0.051*CL	3.071 + 0.037*CL	3.374 + 0.031*CL
	t_{PHL}	5.229	2.454 + 0.062*CL	2.940 + 0.046*CL	3.298 + 0.039*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.558	1.144 + 0.053*CL	1.486 + 0.041*CL	1.716 + 0.037*CL
	t_F	3.677	1.243 + 0.054*CL	1.607 + 0.041*CL	1.846 + 0.037*CL
	t_{PLH}	4.331	2.263 + 0.047*CL	2.669 + 0.033*CL	2.968 + 0.027*CL
	t_{PHL}	5.431	3.009 + 0.055*CL	3.522 + 0.038*CL	3.884 + 0.031*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.806	1.009 + 0.039*CL	1.233 + 0.031*CL	1.374 + 0.029*CL
	t_F	3.635	1.341 + 0.051*CL	1.717 + 0.038*CL	1.975 + 0.033*CL
	t_{PLH}	3.906	2.283 + 0.037*CL	2.631 + 0.026*CL	2.864 + 0.021*CL
	t_{PHL}	5.625	3.189 + 0.056*CL	3.728 + 0.038*CL	4.108 + 0.030*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.563	1.010 + 0.034*CL	1.230 + 0.027*CL	1.369 + 0.024*CL
	t_F	2.985	0.963 + 0.046*CL	1.355 + 0.033*CL	1.594 + 0.028*CL
	t_{PLH}	3.838	2.320 + 0.035*CL	2.663 + 0.024*CL	2.898 + 0.019*CL
	t_{PHL}	4.711	2.777 + 0.044*CL	3.168 + 0.031*CL	3.466 + 0.025*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

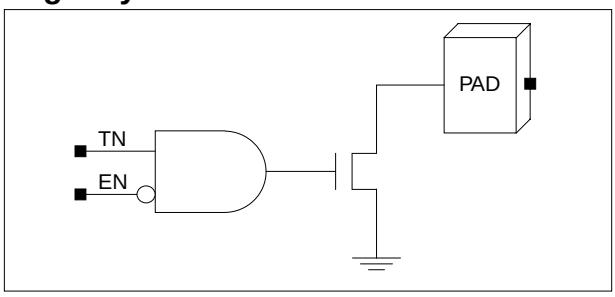
PvODyz

Open Drain Output Buffers

Cell Availability

2.5V Interface	**2.5V Interface**	pmod(2/4/8/12/16/20/24)
		pmod(4/8/12/16/20/24)sm
		pmod(12/16/20/24)sh
3.3V Interface	**3.3V Interface**	phod(2/4/8/12/16/20/24)
		phod(4/8/12/16/20/24)sm
		phod(12/16/20/24)sh
	5V-Tolerant	pmtod(2/4/6)
		pmtod(4/6)sm
		phtod(2/4/6)
		phtod(4/6)sm

Logic Symbol



Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Standard Load (SL)

Cell Name	TN	EN
pmod(2/4/8/12/16/20/24)	10.62	8.99
pmod(4/8/12/16/20/24)sm	10.62	8.99
pmod(12/16/20/24)sh	10.62	8.99
phod(2/4/8/12/16/20/24)	10.62	8.99
phod(4/8/12/16/20/24)sm	10.62	8.99
phod(12/16/20/24)sh	10.62	8.99
pmtod(2/4/6)	10.62	8.99
pmtod(4/6)sm	10.62	8.99
phtod(2/4/6)	10.62	8.99
phtod(4/6)sm	10.62	8.99

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmod2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	10.870	0.359 + 0.209*CL	0.292 + 0.212*CL	0.266 + 0.212*CL
	t_{PHL}	6.777	1.413 + 0.107*CL	1.421 + 0.107*CL	1.421 + 0.107*CL
	t_{PLZ}	0.893	0.893 + 0.000*CL	0.893 + 0.000*CL	0.893 + 0.000*CL
EN to PAD	t_F	10.870	0.359 + 0.209*CL	0.292 + 0.212*CL	0.266 + 0.212*CL
	t_{PHL}	6.865	1.500 + 0.107*CL	1.508 + 0.107*CL	1.509 + 0.107*CL
	t_{PLZ}	0.979	0.980 + 0.000*CL	0.979 + 0.000*CL	0.979 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.616	0.130 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PHL}	4.383	0.942 + 0.069*CL	0.942 + 0.069*CL	0.942 + 0.069*CL
	t_{PLZ}	0.831	0.831 + 0.000*CL	0.831 + 0.000*CL	0.831 + 0.000*CL
EN to PAD	t_F	6.616	0.130 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PHL}	4.471	1.030 + 0.069*CL	1.030 + 0.069*CL	1.030 + 0.069*CL
	t_{PLZ}	0.917	0.917 + 0.000*CL	0.917 + 0.000*CL	0.917 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.313	0.076 + 0.065*CL	0.071 + 0.065*CL	0.070 + 0.065*CL
	t_{PHL}	2.652	0.931 + 0.034*CL	0.931 + 0.034*CL	0.931 + 0.034*CL
	t_{PLZ}	0.857	0.857 + 0.000*CL	0.857 + 0.000*CL	0.857 + 0.000*CL
EN to PAD	t_F	3.313	0.076 + 0.065*CL	0.071 + 0.065*CL	0.070 + 0.065*CL
	t_{PHL}	2.739	1.019 + 0.034*CL	1.019 + 0.034*CL	1.019 + 0.034*CL
	t_{PLZ}	0.943	0.943 + 0.000*CL	0.943 + 0.000*CL	0.943 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.215	0.069 + 0.043*CL	0.057 + 0.043*CL	0.053 + 0.043*CL
	t_{PHL}	2.089	0.941 + 0.023*CL	0.942 + 0.023*CL	0.942 + 0.023*CL
	t_{PLZ}	0.880	0.879 + 0.000*CL	0.880 + 0.000*CL	0.880 + 0.000*CL
EN to PAD	t_F	2.215	0.069 + 0.043*CL	0.057 + 0.043*CL	0.053 + 0.043*CL
	t_{PHL}	2.176	1.029 + 0.023*CL	1.029 + 0.023*CL	1.029 + 0.023*CL
	t_{PLZ}	0.966	0.966 + 0.000*CL	0.966 + 0.000*CL	0.966 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmod16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.669	0.074 + 0.032*CL	0.058 + 0.032*CL	0.050 + 0.032*CL
	t_{PHL}	1.818	0.954 + 0.017*CL	0.957 + 0.017*CL	0.957 + 0.017*CL
	t_{PLZ}	0.902	0.902 + 0.000*CL	0.902 + 0.000*CL	0.902 + 0.000*CL
EN to PAD	t_F	1.669	0.074 + 0.032*CL	0.058 + 0.032*CL	0.050 + 0.032*CL
	t_{PHL}	1.905	1.042 + 0.017*CL	1.045 + 0.017*CL	1.045 + 0.017*CL
	t_{PLZ}	0.988	0.988 + 0.000*CL	0.988 + 0.000*CL	0.988 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.339	0.069 + 0.025*CL	0.054 + 0.026*CL	0.045 + 0.026*CL
	t_{PHL}	1.632	0.939 + 0.014*CL	0.944 + 0.014*CL	0.944 + 0.014*CL
	t_{PLZ}	0.996	0.996 + 0.000*CL	0.996 + 0.000*CL	0.996 + 0.000*CL
EN to PAD	t_F	1.338	0.069 + 0.025*CL	0.054 + 0.026*CL	0.045 + 0.026*CL
	t_{PHL}	1.720	1.027 + 0.014*CL	1.031 + 0.014*CL	1.031 + 0.014*CL
	t_{PLZ}	1.082	1.080 + 0.000*CL	1.082 + 0.000*CL	1.082 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.124	0.075 + 0.021*CL	0.060 + 0.021*CL	0.051 + 0.021*CL
	t_{PHL}	1.531	0.948 + 0.012*CL	0.957 + 0.011*CL	0.958 + 0.011*CL
	t_{PLZ}	1.025	1.025 + 0.000*CL	1.025 + 0.000*CL	1.025 + 0.000*CL
EN to PAD	t_F	1.124	0.075 + 0.021*CL	0.060 + 0.021*CL	0.051 + 0.021*CL
	t_{PHL}	1.619	1.035 + 0.012*CL	1.044 + 0.011*CL	1.045 + 0.011*CL
	t_{PLZ}	1.110	1.110 + 0.000*CL	1.110 + 0.000*CL	1.110 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmod4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.654	0.227 + 0.128*CL	0.185 + 0.129*CL	0.170 + 0.130*CL
	t_{PHL}	4.640	1.194 + 0.069*CL	1.198 + 0.069*CL	1.198 + 0.069*CL
	t_{PLZ}	0.809	0.809 + 0.000*CL	0.809 + 0.000*CL	0.809 + 0.000*CL
EN to PAD	t_F	6.654	0.227 + 0.128*CL	0.185 + 0.129*CL	0.170 + 0.130*CL
	t_{PHL}	4.727	1.281 + 0.069*CL	1.285 + 0.069*CL	1.286 + 0.069*CL
	t_{PLZ}	0.895	0.895 + 0.000*CL	0.895 + 0.000*CL	0.895 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.458	0.320 + 0.063*CL	0.309 + 0.063*CL	0.274 + 0.064*CL
	t_{PHL}	3.116	1.277 + 0.038*CL	1.361 + 0.035*CL	1.388 + 0.035*CL
	t_{PLZ}	0.827	0.827 + 0.000*CL	0.827 + 0.000*CL	0.827 + 0.000*CL
EN to PAD	t_F	3.458	0.320 + 0.063*CL	0.309 + 0.063*CL	0.274 + 0.064*CL
	t_{PHL}	3.204	1.365 + 0.038*CL	1.448 + 0.035*CL	1.476 + 0.035*CL
	t_{PLZ}	0.913	0.913 + 0.000*CL	0.913 + 0.000*CL	0.913 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.692	0.486 + 0.046*CL	0.605 + 0.042*CL	0.634 + 0.041*CL
	t_{PHL}	2.931	1.368 + 0.034*CL	1.557 + 0.027*CL	1.678 + 0.025*CL
	t_{PLZ}	0.890	0.891 + 0.000*CL	0.890 + 0.000*CL	0.890 + 0.000*CL
EN to PAD	t_F	2.692	0.486 + 0.046*CL	0.605 + 0.042*CL	0.634 + 0.041*CL
	t_{PHL}	3.018	1.455 + 0.034*CL	1.645 + 0.027*CL	1.765 + 0.025*CL
	t_{PLZ}	0.976	0.976 + 0.000*CL	0.976 + 0.000*CL	0.976 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmod16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.079	0.407 + 0.035*CL	0.489 + 0.032*CL	0.518 + 0.031*CL
	t_{PHL}	2.585	1.387 + 0.026*CL	1.530 + 0.021*CL	1.621 + 0.019*CL
	t_{PLZ}	0.890	0.890 + 0.000*CL	0.890 + 0.000*CL	0.890 + 0.000*CL
EN to PAD	t_F	2.079	0.407 + 0.035*CL	0.489 + 0.032*CL	0.518 + 0.031*CL
	t_{PHL}	2.673	1.475 + 0.026*CL	1.617 + 0.021*CL	1.708 + 0.019*CL
	t_{PLZ}	0.975	0.975 + 0.000*CL	0.975 + 0.000*CL	0.974 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.629	0.338 + 0.027*CL	0.391 + 0.025*CL	0.397 + 0.025*CL
	t_{PHL}	2.246	1.312 + 0.020*CL	1.429 + 0.016*CL	1.498 + 0.015*CL
	t_{PLZ}	0.940	0.940 + 0.000*CL	0.940 + 0.000*CL	0.940 + 0.000*CL
EN to PAD	t_F	1.629	0.338 + 0.027*CL	0.391 + 0.025*CL	0.397 + 0.025*CL
	t_{PHL}	2.334	1.400 + 0.020*CL	1.517 + 0.016*CL	1.585 + 0.015*CL
	t_{PLZ}	1.026	1.026 + 0.000*CL	1.026 + 0.000*CL	1.026 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.466	0.356 + 0.023*CL	0.423 + 0.021*CL	0.444 + 0.020*CL
	t_{PHL}	2.211	1.350 + 0.019*CL	1.476 + 0.015*CL	1.554 + 0.013*CL
	t_{PLZ}	0.940	0.940 + 0.000*CL	0.940 + 0.000*CL	0.940 + 0.000*CL
EN to PAD	t_F	1.466	0.356 + 0.023*CL	0.423 + 0.021*CL	0.444 + 0.020*CL
	t_{PHL}	2.298	1.438 + 0.019*CL	1.563 + 0.015*CL	1.642 + 0.013*CL
	t_{PLZ}	1.026	1.026 + 0.000*CL	1.026 + 0.000*CL	1.026 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmod12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.864	0.598 + 0.047*CL	0.734 + 0.043*CL	0.790 + 0.041*CL
	t_{PHL}	3.321	1.642 + 0.036*CL	1.861 + 0.029*CL	2.005 + 0.026*CL
	t_{PLZ}	0.900	0.900 + 0.000*CL	0.900 + 0.000*CL	0.900 + 0.000*CL
EN to PAD	t_F	2.864	0.598 + 0.047*CL	0.734 + 0.043*CL	0.790 + 0.041*CL
	t_{PHL}	3.408	1.729 + 0.036*CL	1.948 + 0.029*CL	2.093 + 0.026*CL
	t_{PLZ}	0.986	0.986 + 0.000*CL	0.986 + 0.000*CL	0.986 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.422	0.611 + 0.038*CL	0.764 + 0.033*CL	0.845 + 0.032*CL
	t_{PHL}	3.101	1.645 + 0.032*CL	1.868 + 0.025*CL	2.021 + 0.022*CL
	t_{PLZ}	0.954	0.954 + 0.000*CL	0.954 + 0.000*CL	0.954 + 0.000*CL
EN to PAD	t_F	2.422	0.611 + 0.038*CL	0.764 + 0.033*CL	0.845 + 0.032*CL
	t_{PHL}	3.188	1.732 + 0.032*CL	1.955 + 0.025*CL	2.108 + 0.022*CL
	t_{PLZ}	1.040	1.040 + 0.000*CL	1.040 + 0.000*CL	1.040 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.162	0.622 + 0.033*CL	0.774 + 0.028*CL	0.863 + 0.026*CL
	t_{PHL}	3.070	1.757 + 0.029*CL	1.977 + 0.022*CL	2.129 + 0.019*CL
	t_{PLZ}	0.956	0.956 + 0.000*CL	0.956 + 0.000*CL	0.956 + 0.000*CL
EN to PAD	t_F	2.162	0.622 + 0.033*CL	0.774 + 0.028*CL	0.863 + 0.026*CL
	t_{PHL}	3.158	1.845 + 0.029*CL	2.064 + 0.022*CL	2.216 + 0.019*CL
	t_{PLZ}	1.042	1.042 + 0.000*CL	1.042 + 0.000*CL	1.042 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmod24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.024	0.618 + 0.030*CL	0.777 + 0.025*CL	0.882 + 0.023*CL
	t_{PHL}	2.930	1.692 + 0.028*CL	1.908 + 0.020*CL	2.060 + 0.017*CL
	t_{PLZ}	1.010	1.010 + 0.000*CL	1.010 + 0.000*CL	1.010 + 0.000*CL
EN to PAD	t_F	2.024	0.618 + 0.030*CL	0.777 + 0.025*CL	0.882 + 0.023*CL
	t_{PHL}	3.017	1.779 + 0.028*CL	1.995 + 0.020*CL	2.147 + 0.017*CL
	t_{PLZ}	1.096	1.096 + 0.000*CL	1.096 + 0.000*CL	1.096 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phod2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.920	0.673 + 0.243*CL	0.538 + 0.248*CL	0.448 + 0.249*CL
	t_{PHL}	8.232	2.059 + 0.124*CL	2.130 + 0.122*CL	2.137 + 0.122*CL
	t_{PLZ}	0.907	0.908 + 0.000*CL	0.907 + 0.000*CL	0.907 + 0.000*CL
EN to PAD	t_F	12.920	0.673 + 0.243*CL	0.538 + 0.248*CL	0.448 + 0.249*CL
	t_{PHL}	8.319	2.147 + 0.124*CL	2.218 + 0.122*CL	2.225 + 0.122*CL
	t_{PLZ}	0.993	0.993 + 0.000*CL	0.993 + 0.000*CL	0.993 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.407	0.176 + 0.124*CL	0.149 + 0.125*CL	0.143 + 0.125*CL
	t_{PHL}	4.163	1.115 + 0.061*CL	1.116 + 0.061*CL	1.117 + 0.061*CL
	t_{PLZ}	0.934	0.935 + 0.000*CL	0.934 + 0.000*CL	0.934 + 0.000*CL
EN to PAD	t_F	6.407	0.176 + 0.124*CL	0.149 + 0.125*CL	0.143 + 0.125*CL
	t_{PHL}	4.250	1.202 + 0.061*CL	1.204 + 0.061*CL	1.204 + 0.061*CL
	t_{PLZ}	1.020	1.020 + 0.000*CL	1.020 + 0.000*CL	1.020 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.273	0.244 + 0.060*CL	0.206 + 0.061*CL	0.173 + 0.062*CL
	t_{PHL}	2.820	1.246 + 0.032*CL	1.289 + 0.031*CL	1.295 + 0.030*CL
	t_{PLZ}	1.048	1.048 + 0.000*CL	1.048 + 0.000*CL	1.048 + 0.000*CL
EN to PAD	t_F	3.273	0.244 + 0.060*CL	0.206 + 0.061*CL	0.173 + 0.062*CL
	t_{PHL}	2.907	1.333 + 0.032*CL	1.376 + 0.031*CL	1.383 + 0.030*CL
	t_{PLZ}	1.133	1.133 + 0.000*CL	1.133 + 0.000*CL	1.133 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.308	0.308 + 0.040*CL	0.313 + 0.040*CL	0.286 + 0.040*CL
	t_{PHL}	2.500	1.328 + 0.025*CL	1.428 + 0.021*CL	1.468 + 0.021*CL
	t_{PLZ}	1.158	1.159 + 0.000*CL	1.158 + 0.000*CL	1.158 + 0.000*CL
EN to PAD	t_F	2.308	0.308 + 0.040*CL	0.313 + 0.040*CL	0.286 + 0.040*CL
	t_{PHL}	2.587	1.415 + 0.025*CL	1.516 + 0.021*CL	1.555 + 0.021*CL
	t_{PLZ}	1.244	1.245 + 0.000*CL	1.244 + 0.000*CL	1.244 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phod16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.887	0.351 + 0.031*CL	0.397 + 0.030*CL	0.395 + 0.030*CL
	t_{PHL}	2.411	1.389 + 0.022*CL	1.522 + 0.018*CL	1.595 + 0.016*CL
	t_{PLZ}	1.268	1.269 + 0.000*CL	1.268 + 0.000*CL	1.268 + 0.000*CL
EN to PAD	t_F	1.887	0.351 + 0.031*CL	0.397 + 0.030*CL	0.395 + 0.030*CL
	t_{PHL}	2.498	1.476 + 0.022*CL	1.609 + 0.018*CL	1.682 + 0.016*CL
	t_{PLZ}	1.354	1.355 + 0.000*CL	1.354 + 0.000*CL	1.353 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.887	0.351 + 0.031*CL	0.397 + 0.030*CL	0.395 + 0.030*CL
	t_{PHL}	2.411	1.389 + 0.022*CL	1.522 + 0.018*CL	1.595 + 0.016*CL
	t_{PLZ}	1.268	1.269 + 0.000*CL	1.268 + 0.000*CL	1.268 + 0.000*CL
EN to PAD	t_F	1.887	0.351 + 0.031*CL	0.397 + 0.030*CL	0.395 + 0.030*CL
	t_{PHL}	2.498	1.476 + 0.022*CL	1.609 + 0.018*CL	1.682 + 0.016*CL
	t_{PLZ}	1.354	1.355 + 0.000*CL	1.354 + 0.000*CL	1.353 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.206	0.197 + 0.020*CL	0.213 + 0.020*CL	0.205 + 0.020*CL
	t_{PHL}	1.790	1.159 + 0.014*CL	1.228 + 0.011*CL	1.262 + 0.011*CL
	t_{PLZ}	1.340	1.341 + 0.000*CL	1.340 + 0.000*CL	1.340 + 0.000*CL
EN to PAD	t_F	1.206	0.196 + 0.020*CL	0.214 + 0.020*CL	0.205 + 0.020*CL
	t_{PHL}	1.878	1.246 + 0.014*CL	1.316 + 0.011*CL	1.350 + 0.011*CL
	t_{PLZ}	1.426	1.427 + 0.000*CL	1.426 + 0.000*CL	1.426 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phod4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.716	0.710 + 0.120*CL	0.673 + 0.121*CL	0.590 + 0.123*CL
	t_{PHL}	5.365	2.038 + 0.069*CL	2.239 + 0.063*CL	2.300 + 0.061*CL
	t_{PLZ}	1.014	1.014 + 0.000*CL	1.014 + 0.000*CL	1.013 + 0.000*CL
EN to PAD	t_F	6.716	0.710 + 0.120*CL	0.673 + 0.121*CL	0.590 + 0.123*CL
	t_{PHL}	5.453	2.125 + 0.069*CL	2.327 + 0.063*CL	2.388 + 0.061*CL
	t_{PLZ}	1.100	1.100 + 0.000*CL	1.100 + 0.000*CL	1.099 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.912	0.767 + 0.065*CL	0.900 + 0.060*CL	0.925 + 0.060*CL
	t_{PHL}	4.275	2.102 + 0.048*CL	2.405 + 0.037*CL	2.585 + 0.034*CL
	t_{PLZ}	1.042	1.042 + 0.000*CL	1.042 + 0.000*CL	1.042 + 0.000*CL
EN to PAD	t_F	3.912	0.767 + 0.065*CL	0.900 + 0.060*CL	0.925 + 0.060*CL
	t_{PHL}	4.363	2.189 + 0.048*CL	2.493 + 0.037*CL	2.673 + 0.034*CL
	t_{PLZ}	1.128	1.129 + 0.000*CL	1.128 + 0.000*CL	1.128 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.340	0.899 + 0.052*CL	1.131 + 0.044*CL	1.262 + 0.042*CL
	t_{PHL}	4.340	2.307 + 0.046*CL	2.674 + 0.033*CL	2.923 + 0.028*CL
	t_{PLZ}	1.264	1.266 + 0.000*CL	1.264 + 0.000*CL	1.264 + 0.000*CL
EN to PAD	t_F	3.339	0.898 + 0.052*CL	1.131 + 0.044*CL	1.261 + 0.042*CL
	t_{PHL}	4.427	2.394 + 0.046*CL	2.761 + 0.033*CL	3.011 + 0.028*CL
	t_{PLZ}	1.350	1.351 + 0.000*CL	1.350 + 0.000*CL	1.350 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phod16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.929	0.897 + 0.044*CL	1.135 + 0.036*CL	1.283 + 0.033*CL
	t_{PHL}	4.176	2.332 + 0.042*CL	2.694 + 0.030*CL	2.944 + 0.025*CL
	t_{PLZ}	1.260	1.261 + 0.000*CL	1.260 + 0.000*CL	1.260 + 0.000*CL
EN to PAD	t_F	2.929	0.897 + 0.044*CL	1.135 + 0.036*CL	1.283 + 0.033*CL
	t_{PHL}	4.263	2.419 + 0.042*CL	2.782 + 0.030*CL	3.031 + 0.025*CL
	t_{PLZ}	1.347	1.347 + 0.000*CL	1.347 + 0.000*CL	1.346 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.127	0.629 + 0.032*CL	0.788 + 0.027*CL	0.878 + 0.025*CL
	t_{PHL}	3.194	1.875 + 0.030*CL	2.130 + 0.021*CL	2.303 + 0.018*CL
	t_{PLZ}	1.473	1.474 + 0.000*CL	1.473 + 0.000*CL	1.473 + 0.000*CL
EN to PAD	t_F	2.127	0.629 + 0.032*CL	0.788 + 0.027*CL	0.878 + 0.025*CL
	t_{PHL}	3.282	1.962 + 0.030*CL	2.217 + 0.021*CL	2.391 + 0.018*CL
	t_{PLZ}	1.559	1.560 + 0.000*CL	1.559 + 0.000*CL	1.559 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.637	0.449 + 0.025*CL	0.558 + 0.022*CL	0.616 + 0.020*CL
	t_{PHL}	2.545	1.554 + 0.022*CL	1.735 + 0.016*CL	1.856 + 0.014*CL
	t_{PLZ}	1.486	1.487 + 0.000*CL	1.486 + 0.000*CL	1.486 + 0.000*CL
EN to PAD	t_F	1.637	0.448 + 0.025*CL	0.558 + 0.022*CL	0.615 + 0.020*CL
	t_{PHL}	2.632	1.641 + 0.022*CL	1.823 + 0.016*CL	1.944 + 0.014*CL
	t_{PLZ}	1.572	1.573 + 0.000*CL	1.572 + 0.000*CL	1.572 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phod12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.481	1.228 + 0.071*CL	1.658 + 0.056*CL	1.969 + 0.050*CL
	t_{PHL}	5.352	2.565 + 0.062*CL	3.056 + 0.046*CL	3.417 + 0.039*CL
	t_{PLZ}	1.283	1.284 + 0.000*CL	1.283 + 0.000*CL	1.283 + 0.000*CL
EN to PAD	t_F	4.481	1.228 + 0.071*CL	1.659 + 0.056*CL	1.969 + 0.050*CL
	t_{PHL}	5.440	2.652 + 0.062*CL	3.143 + 0.046*CL	3.505 + 0.039*CL
	t_{PLZ}	1.369	1.370 + 0.000*CL	1.369 + 0.000*CL	1.369 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.707	1.301 + 0.053*CL	1.650 + 0.041*CL	1.885 + 0.036*CL
	t_{PHL}	5.557	3.127 + 0.055*CL	3.645 + 0.038*CL	4.008 + 0.031*CL
	t_{PLZ}	1.504	1.504 + 0.000*CL	1.504 + 0.000*CL	1.503 + 0.000*CL
EN to PAD	t_F	3.707	1.301 + 0.053*CL	1.650 + 0.041*CL	1.885 + 0.036*CL
	t_{PHL}	5.644	3.215 + 0.055*CL	3.732 + 0.038*CL	4.095 + 0.031*CL
	t_{PLZ}	1.590	1.590 + 0.000*CL	1.590 + 0.000*CL	1.589 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.672	1.400 + 0.050*CL	1.766 + 0.038*CL	2.021 + 0.033*CL
	t_{PHL}	5.749	3.309 + 0.056*CL	3.850 + 0.038*CL	4.230 + 0.030*CL
	t_{PLZ}	1.498	1.499 + 0.000*CL	1.498 + 0.000*CL	1.498 + 0.000*CL
EN to PAD	t_F	3.672	1.400 + 0.050*CL	1.766 + 0.038*CL	2.021 + 0.033*CL
	t_{PHL}	5.837	3.397 + 0.056*CL	3.938 + 0.038*CL	4.317 + 0.030*CL
	t_{PLZ}	1.584	1.585 + 0.000*CL	1.584 + 0.000*CL	1.584 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phod24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.033	1.148 + 0.042*CL	1.451 + 0.032*CL	1.662 + 0.027*CL
	t_{PHL}	4.828	2.818 + 0.046*CL	3.262 + 0.031*CL	3.574 + 0.025*CL
	t_{PLZ}	1.704	1.704 + 0.000*CL	1.704 + 0.000*CL	1.704 + 0.000*CL
EN to PAD	t_F	3.033	1.148 + 0.042*CL	1.452 + 0.032*CL	1.662 + 0.027*CL
	t_{PHL}	4.915	2.906 + 0.046*CL	3.350 + 0.031*CL	3.662 + 0.025*CL
	t_{PLZ}	1.790	1.791 + 0.000*CL	1.790 + 0.000*CL	1.790 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmtod2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.869	1.302 + 0.237*CL	1.701 + 0.223*CL	1.957 + 0.218*CL
	t_{PHL}	7.475	1.604 + 0.120*CL	1.804 + 0.113*CL	1.925 + 0.111*CL
	t_{PLZ}	0.838	0.838 + 0.000*CL	0.838 + 0.000*CL	0.838 + 0.000*CL
EN to PAD	t_F	12.869	1.302 + 0.237*CL	1.701 + 0.223*CL	1.957 + 0.218*CL
	t_{PHL}	7.562	1.691 + 0.120*CL	1.892 + 0.113*CL	2.011 + 0.111*CL
	t_{PLZ}	0.923	0.924 + 0.000*CL	0.923 + 0.000*CL	0.923 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmtod4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.951	0.677 + 0.130*CL	1.019 + 0.119*CL	1.269 + 0.114*CL
	t_{PHL}	4.060	0.994 + 0.062*CL	1.076 + 0.060*CL	1.186 + 0.057*CL
	t_{PLZ}	0.878	0.878 + 0.000*CL	0.878 + 0.000*CL	0.878 + 0.000*CL
EN to PAD	t_F	6.951	0.677 + 0.130*CL	1.019 + 0.119*CL	1.269 + 0.114*CL
	t_{PHL}	4.148	1.081 + 0.062*CL	1.164 + 0.060*CL	1.273 + 0.057*CL
	t_{PLZ}	0.965	0.964 + 0.000*CL	0.965 + 0.000*CL	0.964 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmtod6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.907	0.489 + 0.092*CL	0.767 + 0.083*CL	0.987 + 0.078*CL
	t_{PHL}	3.123	1.000 + 0.043*CL	1.065 + 0.041*CL	1.132 + 0.040*CL
	t_{PLZ}	0.910	0.910 + 0.000*CL	0.910 + 0.000*CL	0.910 + 0.000*CL
EN to PAD	t_F	4.907	0.489 + 0.092*CL	0.767 + 0.083*CL	0.987 + 0.078*CL
	t_{PHL}	3.210	1.087 + 0.043*CL	1.153 + 0.041*CL	1.219 + 0.040*CL
	t_{PLZ}	0.996	0.995 + 0.000*CL	0.996 + 0.000*CL	0.994 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmtod4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	7.065	0.946 + 0.126*CL	1.240 + 0.117*CL	1.444 + 0.112*CL
	t_{PHL}	4.892	1.675 + 0.067*CL	1.852 + 0.061*CL	1.994 + 0.058*CL
	t_{PLZ}	0.881	0.881 + 0.000*CL	0.881 + 0.000*CL	0.881 + 0.000*CL
EN to PAD	t_F	7.065	0.946 + 0.126*CL	1.240 + 0.117*CL	1.444 + 0.112*CL
	t_{PHL}	4.979	1.762 + 0.067*CL	1.940 + 0.061*CL	2.081 + 0.058*CL
	t_{PLZ}	0.967	0.968 + 0.000*CL	0.967 + 0.000*CL	0.967 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmtod6sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.347	1.066 + 0.090*CL	1.373 + 0.079*CL	1.566 + 0.076*CL
	t_{PHL}	4.478	1.884 + 0.056*CL	2.179 + 0.046*CL	2.365 + 0.042*CL
	t_{PLZ}	0.881	0.881 + 0.000*CL	0.881 + 0.000*CL	0.881 + 0.000*CL
EN to PAD	t_F	5.347	1.066 + 0.090*CL	1.373 + 0.079*CL	1.566 + 0.076*CL
	t_{PHL}	4.566	1.972 + 0.056*CL	2.267 + 0.046*CL	2.452 + 0.042*CL
	t_{PLZ}	0.968	0.968 + 0.000*CL	0.968 + 0.000*CL	0.968 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phtod2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	13.839	1.131 + 0.261*CL	1.655 + 0.244*CL	2.031 + 0.236*CL
	t_{PHL}	7.071	1.198 + 0.120*CL	1.392 + 0.114*CL	1.519 + 0.111*CL
	t_{PLZ}	0.954	0.954 + 0.000*CL	0.954 + 0.000*CL	0.954 + 0.000*CL
EN to PAD	t_F	13.839	1.131 + 0.261*CL	1.655 + 0.244*CL	2.031 + 0.236*CL
	t_{PHL}	7.159	1.286 + 0.120*CL	1.479 + 0.114*CL	1.606 + 0.111*CL
	t_{PLZ}	1.040	1.040 + 0.000*CL	1.040 + 0.000*CL	1.040 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phtod4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	7.411	0.638 + 0.140*CL	0.971 + 0.129*CL	1.252 + 0.123*CL
	t_{PHL}	4.431	1.267 + 0.065*CL	1.377 + 0.061*CL	1.507 + 0.058*CL
	t_{PLZ}	1.067	1.067 + 0.000*CL	1.067 + 0.000*CL	1.067 + 0.000*CL
EN to PAD	t_F	7.411	0.638 + 0.140*CL	0.971 + 0.129*CL	1.254 + 0.123*CL
	t_{PHL}	4.518	1.355 + 0.065*CL	1.464 + 0.061*CL	1.594 + 0.058*CL
	t_{PLZ}	1.153	1.153 + 0.000*CL	1.153 + 0.000*CL	1.153 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phtod6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.236	0.512 + 0.098*CL	0.767 + 0.089*CL	0.998 + 0.085*CL
	t_{PHL}	3.654	1.348 + 0.048*CL	1.485 + 0.043*CL	1.589 + 0.041*CL
	t_{PLZ}	1.177	1.178 + 0.000*CL	1.177 + 0.000*CL	1.177 + 0.000*CL
EN to PAD	t_F	5.236	0.512 + 0.098*CL	0.767 + 0.089*CL	0.998 + 0.085*CL
	t_{PHL}	3.742	1.435 + 0.048*CL	1.573 + 0.043*CL	1.676 + 0.041*CL
	t_{PLZ}	1.263	1.263 + 0.000*CL	1.263 + 0.000*CL	1.263 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phtod4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	7.914	1.321 + 0.136*CL	1.665 + 0.125*CL	1.909 + 0.120*CL
	t_{PHL}	6.364	2.668 + 0.079*CL	3.038 + 0.067*CL	3.303 + 0.061*CL
	t_{PLZ}	1.101	1.102 + 0.000*CL	1.101 + 0.000*CL	1.101 + 0.000*CL
EN to PAD	t_F	7.914	1.321 + 0.136*CL	1.665 + 0.125*CL	1.909 + 0.120*CL
	t_{PHL}	6.452	2.755 + 0.079*CL	3.125 + 0.067*CL	3.390 + 0.061*CL
	t_{PLZ}	1.188	1.188 + 0.000*CL	1.188 + 0.000*CL	1.187 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phtod6sm

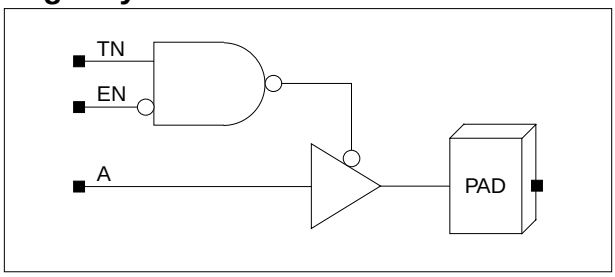
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.986	1.309 + 0.098*CL	1.641 + 0.087*CL	1.870 + 0.082*CL
	t_{PHL}	6.086	3.066 + 0.066*CL	3.494 + 0.052*CL	3.770 + 0.046*CL
	t_{PLZ}	1.101	1.101 + 0.000*CL	1.101 + 0.000*CL	1.100 + 0.000*CL
EN to PAD	t_F	5.986	1.309 + 0.098*CL	1.641 + 0.087*CL	1.870 + 0.082*CL
	t_{PHL}	6.174	3.154 + 0.066*CL	3.581 + 0.052*CL	3.857 + 0.046*CL
	t_{PLZ}	1.187	1.187 + 0.000*CL	1.187 + 0.000*CL	1.187 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Cell Availability

2.5V Interface	**2.5V Interface**	pmot(2/4/8/12/16/20/24)
		pmot(4/8/12/16/20/24)sm
		pmot(12/16/20/24)sh
3.3V Interface	**3.3V Interface**	phot(2/4/8/12/16/20/24)
		phot(4/8/12/16/20/24)sm
		phot(12/16/20/24)sh
	5V-Tolerant	pmtot(2/4/6)
		pmtot(4/6)sm
		phtot(2/4/6)
		phtot(4/6)sm

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

Standard Load (SL)

Cell Name	TN	EN	A
pmot(2/4/8/12/16/20/24)	10.62	8.99	11.92
pmot(4/8/12/16/20/24)sm	10.62	8.99	11.92
pmot(12/16/20/24)sh	10.62	8.99	11.92
phot(2/4/8/12/16/20/24)	10.62	8.99	11.92
phot(4/8/12/16/20/24)sm	10.62	8.99	11.92
phot(12/16/20/24)sh	10.62	8.99	11.92
pmtot(2/4/6)	10.62	8.99	11.92
pmtot(4/6)sm	10.62	8.99	11.92
phtot(2/4/6)	10.62	8.99	11.92
phtot(4/6)sm	10.62	8.99	11.92

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	11.872	0.388 + 0.229*CL	0.317 + 0.231*CL	0.296 + 0.232*CL
	t_F	10.870	0.353 + 0.209*CL	0.290 + 0.212*CL	0.266 + 0.212*CL
	t_{PLH}	6.293	1.294 + 0.100*CL	1.300 + 0.100*CL	1.301 + 0.100*CL
	t_{PHL}	6.653	1.288 + 0.107*CL	1.296 + 0.107*CL	1.297 + 0.107*CL
TN to PAD	t_R	11.872	0.388 + 0.229*CL	0.317 + 0.231*CL	0.296 + 0.232*CL
	t_F	10.870	0.353 + 0.209*CL	0.290 + 0.212*CL	0.266 + 0.212*CL
	t_{PLH}	6.468	1.466 + 0.100*CL	1.473 + 0.100*CL	1.474 + 0.100*CL
	t_{PHL}	6.780	1.412 + 0.107*CL	1.422 + 0.107*CL	1.423 + 0.107*CL
	t_{PLZ}	0.892	0.892 + 0.000*CL	0.892 + 0.000*CL	0.892 + 0.000*CL
	t_{PHZ}	0.984	0.984 + 0.000*CL	0.984 + 0.000*CL	0.984 + 0.000*CL
EN to PAD	t_R	11.872	0.388 + 0.229*CL	0.317 + 0.231*CL	0.296 + 0.232*CL
	t_F	10.870	0.353 + 0.209*CL	0.290 + 0.212*CL	0.266 + 0.212*CL
	t_{PLH}	6.555	1.553 + 0.100*CL	1.560 + 0.100*CL	1.562 + 0.100*CL
	t_{PHL}	6.868	1.500 + 0.107*CL	1.509 + 0.107*CL	1.511 + 0.107*CL
	t_{PLZ}	0.977	0.977 + 0.000*CL	0.977 + 0.000*CL	0.977 + 0.000*CL
	t_{PHZ}	1.070	1.070 + 0.000*CL	1.070 + 0.000*CL	1.070 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.925	0.138 + 0.116*CL	0.133 + 0.116*CL	0.133 + 0.116*CL
	t_F	6.616	0.130 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PLH}	3.372	0.876 + 0.050*CL	0.876 + 0.050*CL	0.876 + 0.050*CL
	t_{PHL}	4.266	0.829 + 0.069*CL	0.826 + 0.069*CL	0.825 + 0.069*CL
TN to PAD	t_R	5.925	0.138 + 0.116*CL	0.133 + 0.116*CL	0.133 + 0.116*CL
	t_F	6.616	0.129 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PLH}	3.549	1.050 + 0.050*CL	1.051 + 0.050*CL	1.052 + 0.050*CL
	t_{PHL}	4.390	0.944 + 0.069*CL	0.946 + 0.069*CL	0.947 + 0.069*CL
	t_{PLZ}	0.829	0.829 + 0.000*CL	0.829 + 0.000*CL	0.829 + 0.000*CL
	t_{PHZ}	0.912	0.912 + 0.000*CL	0.912 + 0.000*CL	0.911 + 0.000*CL
EN to PAD	t_R	5.925	0.138 + 0.116*CL	0.133 + 0.116*CL	0.133 + 0.116*CL
	t_F	6.616	0.129 + 0.130*CL	0.129 + 0.130*CL	0.129 + 0.130*CL
	t_{PLH}	3.636	1.137 + 0.050*CL	1.138 + 0.050*CL	1.139 + 0.050*CL
	t_{PHL}	4.477	1.031 + 0.069*CL	1.033 + 0.069*CL	1.035 + 0.069*CL
	t_{PLZ}	0.914	0.914 + 0.000*CL	0.914 + 0.000*CL	0.914 + 0.000*CL
	t_{PHZ}	0.996	0.997 + 0.000*CL	0.996 + 0.000*CL	0.996 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.982	0.132 + 0.057*CL	0.102 + 0.058*CL	0.090 + 0.058*CL
	t_F	3.313	0.092 + 0.064*CL	0.072 + 0.065*CL	0.070 + 0.065*CL
	t_{PLH}	2.194	0.944 + 0.025*CL	0.946 + 0.025*CL	0.946 + 0.025*CL
	t_{PHL}	2.540	0.840 + 0.034*CL	0.827 + 0.034*CL	0.823 + 0.034*CL
TN to PAD	t_R	2.982	0.132 + 0.057*CL	0.102 + 0.058*CL	0.090 + 0.058*CL
	t_F	3.313	0.075 + 0.065*CL	0.070 + 0.065*CL	0.070 + 0.065*CL
	t_{PLH}	2.370	1.117 + 0.025*CL	1.121 + 0.025*CL	1.121 + 0.025*CL
	t_{PHL}	2.658	0.930 + 0.035*CL	0.933 + 0.034*CL	0.935 + 0.034*CL
	t_{PLZ}	0.854	0.854 + 0.000*CL	0.854 + 0.000*CL	0.854 + 0.000*CL
	t_{PHZ}	1.041	1.042 + 0.000*CL	1.041 + 0.000*CL	1.041 + 0.000*CL
EN to PAD	t_R	2.982	0.132 + 0.057*CL	0.102 + 0.058*CL	0.090 + 0.058*CL
	t_F	3.313	0.075 + 0.065*CL	0.070 + 0.065*CL	0.070 + 0.065*CL
	t_{PLH}	2.458	1.204 + 0.025*CL	1.208 + 0.025*CL	1.209 + 0.025*CL
	t_{PHL}	2.745	1.018 + 0.035*CL	1.021 + 0.034*CL	1.023 + 0.034*CL
	t_{PLZ}	0.941	0.941 + 0.000*CL	0.941 + 0.000*CL	0.941 + 0.000*CL
	t_{PHZ}	1.127	1.127 + 0.000*CL	1.127 + 0.000*CL	1.126 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.022	0.170 + 0.037*CL	0.135 + 0.038*CL	0.111 + 0.038*CL
	t_F	2.217	0.129 + 0.041*CL	0.079 + 0.043*CL	0.058 + 0.043*CL
	t_{PLH}	1.858	1.004 + 0.017*CL	1.024 + 0.017*CL	1.025 + 0.017*CL
	t_{PHL}	1.988	0.889 + 0.022*CL	0.863 + 0.023*CL	0.852 + 0.023*CL
TN to PAD	t_R	2.022	0.170 + 0.037*CL	0.135 + 0.038*CL	0.111 + 0.038*CL
	t_F	2.215	0.066 + 0.043*CL	0.056 + 0.043*CL	0.053 + 0.043*CL
	t_{PLH}	2.034	1.177 + 0.017*CL	1.198 + 0.017*CL	1.201 + 0.017*CL
	t_{PHL}	2.094	0.937 + 0.023*CL	0.942 + 0.023*CL	0.945 + 0.023*CL
	t_{PLZ}	0.878	0.878 + 0.000*CL	0.878 + 0.000*CL	0.878 + 0.000*CL
	t_{PHZ}	1.170	1.171 + 0.000*CL	1.170 + 0.000*CL	1.170 + 0.000*CL
EN to PAD	t_R	2.022	0.170 + 0.037*CL	0.135 + 0.038*CL	0.111 + 0.038*CL
	t_F	2.215	0.066 + 0.043*CL	0.056 + 0.043*CL	0.053 + 0.043*CL
	t_{PLH}	2.122	1.264 + 0.017*CL	1.285 + 0.017*CL	1.289 + 0.017*CL
	t_{PHL}	2.181	1.025 + 0.023*CL	1.030 + 0.023*CL	1.032 + 0.023*CL
	t_{PLZ}	0.964	0.964 + 0.000*CL	0.964 + 0.000*CL	0.964 + 0.000*CL
	t_{PHZ}	1.256	1.257 + 0.000*CL	1.256 + 0.000*CL	1.256 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.567	0.208 + 0.027*CL	0.183 + 0.028*CL	0.157 + 0.028*CL
	t_F	1.684	0.187 + 0.029*CL	0.123 + 0.031*CL	0.088 + 0.032*CL
	t_{PLH}	1.730	1.046 + 0.014*CL	1.092 + 0.013*CL	1.104 + 0.013*CL
	t_{PHL}	1.737	0.946 + 0.015*CL	0.916 + 0.016*CL	0.896 + 0.017*CL
TN to PAD	t_R	1.567	0.207 + 0.027*CL	0.184 + 0.028*CL	0.157 + 0.028*CL
	t_F	1.668	0.069 + 0.032*CL	0.055 + 0.032*CL	0.049 + 0.032*CL
	t_{PLH}	1.906	1.219 + 0.014*CL	1.267 + 0.013*CL	1.279 + 0.013*CL
	t_{PHL}	1.822	0.948 + 0.018*CL	0.956 + 0.017*CL	0.959 + 0.017*CL
	t_{PLZ}	0.900	0.900 + 0.000*CL	0.900 + 0.000*CL	0.900 + 0.000*CL
	t_{PHZ}	1.299	1.300 + 0.000*CL	1.299 + 0.000*CL	1.299 + 0.000*CL
EN to PAD	t_R	1.567	0.207 + 0.027*CL	0.184 + 0.028*CL	0.157 + 0.028*CL
	t_F	1.668	0.069 + 0.032*CL	0.055 + 0.032*CL	0.049 + 0.032*CL
	t_{PLH}	1.994	1.307 + 0.014*CL	1.354 + 0.013*CL	1.367 + 0.013*CL
	t_{PHL}	1.909	1.036 + 0.018*CL	1.043 + 0.017*CL	1.047 + 0.017*CL
	t_{PLZ}	0.985	0.985 + 0.000*CL	0.985 + 0.000*CL	0.985 + 0.000*CL
	t_{PHZ}	1.385	1.386 + 0.000*CL	1.385 + 0.000*CL	1.385 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.262	0.179 + 0.021*CL	0.158 + 0.022*CL	0.136 + 0.023*CL
	t_F	1.445	0.404 + 0.019*CL	0.289 + 0.023*CL	0.228 + 0.024*CL
	t_{PLH}	1.516	0.963 + 0.012*CL	1.004 + 0.010*CL	1.014 + 0.010*CL
	t_{PHL}	1.642	1.032 + 0.012*CL	1.051 + 0.012*CL	1.014 + 0.013*CL
TN to PAD	t_R	1.262	0.179 + 0.021*CL	0.159 + 0.022*CL	0.136 + 0.023*CL
	t_F	1.338	0.065 + 0.025*CL	0.052 + 0.026*CL	0.044 + 0.026*CL
	t_{PLH}	1.692	1.136 + 0.012*CL	1.178 + 0.010*CL	1.189 + 0.010*CL
	t_{PHL}	1.634	0.931 + 0.014*CL	0.939 + 0.014*CL	0.942 + 0.014*CL
	t_{PLZ}	0.993	0.993 + 0.000*CL	0.993 + 0.000*CL	0.993 + 0.000*CL
	t_{PHZ}	1.647	1.647 + 0.000*CL	1.647 + 0.000*CL	1.647 + 0.000*CL
EN to PAD	t_R	1.262	0.179 + 0.021*CL	0.158 + 0.022*CL	0.136 + 0.023*CL
	t_F	1.338	0.065 + 0.025*CL	0.051 + 0.026*CL	0.044 + 0.026*CL
	t_{PLH}	1.780	1.224 + 0.012*CL	1.265 + 0.010*CL	1.277 + 0.010*CL
	t_{PHL}	1.722	1.018 + 0.014*CL	1.026 + 0.014*CL	1.030 + 0.014*CL
	t_{PLZ}	1.079	1.078 + 0.000*CL	1.079 + 0.000*CL	1.079 + 0.000*CL
	t_{PHZ}	1.733	1.734 + 0.000*CL	1.733 + 0.000*CL	1.733 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.095	0.198 + 0.018*CL	0.191 + 0.018*CL	0.171 + 0.018*CL
	t_F	1.294	0.508 + 0.014*CL	0.399 + 0.018*CL	0.318 + 0.020*CL
	t_{PLH}	1.484	0.986 + 0.011*CL	1.040 + 0.009*CL	1.060 + 0.008*CL
	t_{PHL}	1.602	1.072 + 0.011*CL	1.108 + 0.010*CL	1.105 + 0.010*CL
TN to PAD	t_R	1.096	0.198 + 0.018*CL	0.191 + 0.018*CL	0.171 + 0.018*CL
	t_F	1.123	0.071 + 0.021*CL	0.057 + 0.021*CL	0.049 + 0.021*CL
	t_{PLH}	1.661	1.159 + 0.011*CL	1.214 + 0.009*CL	1.236 + 0.008*CL
	t_{PHL}	1.532	0.939 + 0.012*CL	0.950 + 0.012*CL	0.954 + 0.012*CL
	t_{PLZ}	1.023	1.023 + 0.000*CL	1.023 + 0.000*CL	1.023 + 0.000*CL
	t_{PHZ}	1.819	1.819 + 0.000*CL	1.819 + 0.000*CL	1.818 + 0.000*CL
EN to PAD	t_R	1.096	0.198 + 0.018*CL	0.192 + 0.018*CL	0.171 + 0.018*CL
	t_F	1.123	0.070 + 0.021*CL	0.058 + 0.021*CL	0.048 + 0.021*CL
	t_{PLH}	1.748	1.247 + 0.011*CL	1.301 + 0.009*CL	1.323 + 0.008*CL
	t_{PHL}	1.619	1.026 + 0.012*CL	1.038 + 0.012*CL	1.042 + 0.012*CL
	t_{PLZ}	1.108	1.108 + 0.000*CL	1.108 + 0.000*CL	1.108 + 0.000*CL
	t_{PHZ}	1.905	1.905 + 0.000*CL	1.905 + 0.000*CL	1.904 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.978	0.306 + 0.113*CL	0.253 + 0.115*CL	0.215 + 0.115*CL
	t_F	6.654	0.220 + 0.128*CL	0.183 + 0.129*CL	0.170 + 0.130*CL
	t_{PLH}	3.733	1.206 + 0.051*CL	1.235 + 0.050*CL	1.236 + 0.050*CL
	t_{PHL}	4.517	1.070 + 0.069*CL	1.074 + 0.069*CL	1.075 + 0.069*CL
TN to PAD	t_R	5.978	0.306 + 0.113*CL	0.253 + 0.115*CL	0.215 + 0.115*CL
	t_F	6.654	0.220 + 0.128*CL	0.183 + 0.129*CL	0.170 + 0.130*CL
	t_{PLH}	3.908	1.378 + 0.051*CL	1.407 + 0.050*CL	1.410 + 0.050*CL
	t_{PHL}	4.646	1.196 + 0.069*CL	1.201 + 0.069*CL	1.203 + 0.069*CL
	t_{PLZ}	0.806	0.806 + 0.000*CL	0.806 + 0.000*CL	0.806 + 0.000*CL
	t_{PHZ}	0.898	0.898 + 0.000*CL	0.898 + 0.000*CL	0.898 + 0.000*CL
EN to PAD	t_R	5.978	0.306 + 0.113*CL	0.253 + 0.115*CL	0.215 + 0.115*CL
	t_F	6.654	0.220 + 0.128*CL	0.183 + 0.129*CL	0.170 + 0.130*CL
	t_{PLH}	3.995	1.465 + 0.051*CL	1.495 + 0.050*CL	1.498 + 0.050*CL
	t_{PHL}	4.734	1.283 + 0.069*CL	1.289 + 0.069*CL	1.291 + 0.069*CL
	t_{PLZ}	0.893	0.893 + 0.000*CL	0.893 + 0.000*CL	0.893 + 0.000*CL
	t_{PHZ}	0.984	0.984 + 0.000*CL	0.984 + 0.000*CL	0.984 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.384	0.592 + 0.056*CL	0.638 + 0.055*CL	0.612 + 0.055*CL
	t_F	3.454	0.301 + 0.063*CL	0.298 + 0.063*CL	0.267 + 0.064*CL
	t_{PLH}	3.275	1.677 + 0.034*CL	1.866 + 0.028*CL	1.962 + 0.026*CL
	t_{PHL}	2.995	1.159 + 0.038*CL	1.241 + 0.035*CL	1.267 + 0.035*CL
TN to PAD	t_R	3.384	0.593 + 0.056*CL	0.638 + 0.055*CL	0.612 + 0.055*CL
	t_F	3.454	0.305 + 0.063*CL	0.299 + 0.063*CL	0.267 + 0.064*CL
	t_{PLH}	3.450	1.849 + 0.035*CL	2.038 + 0.028*CL	2.136 + 0.026*CL
	t_{PHL}	3.123	1.280 + 0.038*CL	1.365 + 0.035*CL	1.393 + 0.035*CL
	t_{PLZ}	0.825	0.825 + 0.000*CL	0.825 + 0.000*CL	0.825 + 0.000*CL
	t_{PHZ}	1.039	1.040 + 0.000*CL	1.039 + 0.000*CL	1.039 + 0.000*CL
EN to PAD	t_R	3.384	0.593 + 0.056*CL	0.638 + 0.055*CL	0.612 + 0.055*CL
	t_F	3.454	0.305 + 0.063*CL	0.299 + 0.063*CL	0.267 + 0.064*CL
	t_{PLH}	3.537	1.936 + 0.035*CL	2.126 + 0.028*CL	2.223 + 0.026*CL
	t_{PHL}	3.210	1.368 + 0.038*CL	1.453 + 0.035*CL	1.480 + 0.035*CL
	t_{PLZ}	0.912	0.912 + 0.000*CL	0.912 + 0.000*CL	0.912 + 0.000*CL
	t_{PHZ}	1.125	1.125 + 0.000*CL	1.125 + 0.000*CL	1.125 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.714	0.699 + 0.042*CL	0.834 + 0.038*CL	0.881 + 0.037*CL
	t_F	2.679	0.446 + 0.046*CL	0.578 + 0.042*CL	0.613 + 0.041*CL
	t_{PLH}	3.243	1.830 + 0.032*CL	2.073 + 0.023*CL	2.226 + 0.020*CL
	t_{PHL}	2.811	1.266 + 0.033*CL	1.444 + 0.027*CL	1.560 + 0.025*CL
TN to PAD	t_R	2.714	0.699 + 0.042*CL	0.834 + 0.038*CL	0.881 + 0.037*CL
	t_F	2.681	0.465 + 0.046*CL	0.586 + 0.042*CL	0.617 + 0.041*CL
	t_{PLH}	3.418	2.002 + 0.032*CL	2.246 + 0.023*CL	2.400 + 0.020*CL
	t_{PHL}	2.938	1.375 + 0.034*CL	1.565 + 0.027*CL	1.685 + 0.025*CL
	t_{PLZ}	0.888	0.888 + 0.000*CL	0.888 + 0.000*CL	0.888 + 0.000*CL
	t_{PHZ}	1.168	1.169 + 0.000*CL	1.168 + 0.000*CL	1.168 + 0.000*CL
EN to PAD	t_R	2.714	0.699 + 0.042*CL	0.834 + 0.038*CL	0.881 + 0.037*CL
	t_F	2.681	0.465 + 0.046*CL	0.586 + 0.042*CL	0.617 + 0.041*CL
	t_{PLH}	3.505	2.089 + 0.032*CL	2.333 + 0.023*CL	2.487 + 0.020*CL
	t_{PHL}	3.025	1.462 + 0.034*CL	1.653 + 0.027*CL	1.772 + 0.025*CL
	t_{PLZ}	0.974	0.974 + 0.000*CL	0.974 + 0.000*CL	0.974 + 0.000*CL
	t_{PHZ}	1.254	1.255 + 0.000*CL	1.254 + 0.000*CL	1.254 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.191	0.619 + 0.033*CL	0.748 + 0.029*CL	0.805 + 0.028*CL
	t_F	2.066	0.360 + 0.035*CL	0.460 + 0.032*CL	0.497 + 0.031*CL
	t_{PLH}	2.842	1.676 + 0.026*CL	1.890 + 0.019*CL	2.028 + 0.016*CL
	t_{PHL}	2.466	1.287 + 0.025*CL	1.417 + 0.021*CL	1.504 + 0.019*CL
TN to PAD	t_R	2.191	0.619 + 0.033*CL	0.748 + 0.029*CL	0.805 + 0.028*CL
	t_F	2.069	0.387 + 0.035*CL	0.470 + 0.032*CL	0.503 + 0.031*CL
	t_{PLH}	3.017	1.848 + 0.026*CL	2.063 + 0.019*CL	2.202 + 0.016*CL
	t_{PHL}	2.591	1.390 + 0.026*CL	1.534 + 0.021*CL	1.626 + 0.019*CL
	t_{PLZ}	0.886	0.886 + 0.000*CL	0.886 + 0.000*CL	0.886 + 0.000*CL
	t_{PHZ}	1.289	1.290 + 0.000*CL	1.289 + 0.000*CL	1.288 + 0.000*CL
EN to PAD	t_R	2.191	0.619 + 0.033*CL	0.748 + 0.029*CL	0.805 + 0.028*CL
	t_F	2.068	0.387 + 0.035*CL	0.470 + 0.032*CL	0.503 + 0.031*CL
	t_{PLH}	3.105	1.935 + 0.026*CL	2.150 + 0.019*CL	2.289 + 0.016*CL
	t_{PHL}	2.679	1.477 + 0.026*CL	1.622 + 0.021*CL	1.714 + 0.019*CL
	t_{PLZ}	0.973	0.973 + 0.000*CL	0.973 + 0.000*CL	0.973 + 0.000*CL
	t_{PHZ}	1.375	1.376 + 0.000*CL	1.375 + 0.000*CL	1.375 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.887	0.596 + 0.028*CL	0.726 + 0.023*CL	0.787 + 0.022*CL
	t_F	1.612	0.291 + 0.027*CL	0.350 + 0.025*CL	0.368 + 0.025*CL
	t_{PLH}	2.682	1.647 + 0.023*CL	1.856 + 0.017*CL	1.993 + 0.014*CL
	t_{PHL}	2.132	1.245 + 0.019*CL	1.331 + 0.016*CL	1.390 + 0.015*CL
TN to PAD	t_R	1.887	0.596 + 0.028*CL	0.726 + 0.023*CL	0.787 + 0.022*CL
	t_F	1.619	0.321 + 0.027*CL	0.374 + 0.025*CL	0.382 + 0.025*CL
	t_{PLH}	2.857	1.819 + 0.024*CL	2.029 + 0.017*CL	2.167 + 0.014*CL
	t_{PHL}	2.251	1.311 + 0.020*CL	1.430 + 0.016*CL	1.501 + 0.015*CL
	t_{PLZ}	0.939	0.939 + 0.000*CL	0.939 + 0.000*CL	0.939 + 0.000*CL
	t_{PHZ}	1.413	1.413 + 0.000*CL	1.413 + 0.000*CL	1.412 + 0.000*CL
EN to PAD	t_R	1.887	0.596 + 0.028*CL	0.726 + 0.023*CL	0.787 + 0.022*CL
	t_F	1.619	0.321 + 0.027*CL	0.374 + 0.025*CL	0.382 + 0.025*CL
	t_{PLH}	2.944	1.906 + 0.024*CL	2.117 + 0.017*CL	2.255 + 0.014*CL
	t_{PHL}	2.338	1.399 + 0.020*CL	1.518 + 0.016*CL	1.588 + 0.015*CL
	t_{PLZ}	1.025	1.024 + 0.000*CL	1.025 + 0.000*CL	1.025 + 0.000*CL
	t_{PHZ}	1.499	1.500 + 0.000*CL	1.499 + 0.000*CL	1.499 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.829	0.642 + 0.026*CL	0.790 + 0.021*CL	0.875 + 0.019*CL
	t_F	1.440	0.309 + 0.023*CL	0.371 + 0.021*CL	0.401 + 0.021*CL
	t_{PLH}	2.757	1.719 + 0.024*CL	1.943 + 0.016*CL	2.094 + 0.013*CL
	t_{PHL}	2.103	1.315 + 0.017*CL	1.394 + 0.014*CL	1.457 + 0.013*CL
TN to PAD	t_R	1.829	0.642 + 0.026*CL	0.791 + 0.021*CL	0.875 + 0.019*CL
	t_F	1.454	0.339 + 0.023*CL	0.406 + 0.021*CL	0.427 + 0.021*CL
	t_{PLH}	2.932	1.892 + 0.024*CL	2.116 + 0.016*CL	2.268 + 0.013*CL
	t_{PHL}	2.215	1.349 + 0.019*CL	1.476 + 0.015*CL	1.557 + 0.013*CL
	t_{PLZ}	0.938	0.937 + 0.000*CL	0.938 + 0.000*CL	0.938 + 0.000*CL
	t_{PHZ}	1.542	1.542 + 0.000*CL	1.542 + 0.000*CL	1.541 + 0.000*CL
EN to PAD	t_R	1.829	0.642 + 0.026*CL	0.791 + 0.021*CL	0.875 + 0.019*CL
	t_F	1.454	0.339 + 0.023*CL	0.406 + 0.021*CL	0.427 + 0.021*CL
	t_{PLH}	3.019	1.980 + 0.024*CL	2.204 + 0.016*CL	2.356 + 0.013*CL
	t_{PHL}	2.302	1.436 + 0.019*CL	1.564 + 0.015*CL	1.644 + 0.013*CL
	t_{PLZ}	1.024	1.024 + 0.000*CL	1.024 + 0.000*CL	1.024 + 0.000*CL
	t_{PHZ}	1.628	1.628 + 0.000*CL	1.628 + 0.000*CL	1.627 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.351	0.853 + 0.054*CL	1.137 + 0.044*CL	1.330 + 0.040*CL
	t_F	2.850	0.560 + 0.048*CL	0.708 + 0.043*CL	0.768 + 0.042*CL
	t_{PLH}	3.655	1.827 + 0.041*CL	2.122 + 0.031*CL	2.356 + 0.026*CL
	t_{PHL}	3.200	1.528 + 0.036*CL	1.743 + 0.029*CL	1.886 + 0.026*CL
TN to PAD	t_R	3.351	0.853 + 0.054*CL	1.137 + 0.044*CL	1.330 + 0.040*CL
	t_F	2.851	0.572 + 0.047*CL	0.712 + 0.043*CL	0.770 + 0.042*CL
	t_{PLH}	3.830	1.999 + 0.041*CL	2.295 + 0.031*CL	2.530 + 0.026*CL
	t_{PHL}	3.328	1.649 + 0.037*CL	1.868 + 0.029*CL	2.013 + 0.026*CL
	t_{PLZ}	0.897	0.897 + 0.000*CL	0.897 + 0.000*CL	0.897 + 0.000*CL
	t_{PHZ}	1.307	1.308 + 0.000*CL	1.307 + 0.000*CL	1.306 + 0.000*CL
EN to PAD	t_R	3.351	0.853 + 0.054*CL	1.137 + 0.044*CL	1.330 + 0.040*CL
	t_F	2.851	0.572 + 0.047*CL	0.712 + 0.043*CL	0.770 + 0.042*CL
	t_{PLH}	3.918	2.087 + 0.041*CL	2.383 + 0.031*CL	2.617 + 0.026*CL
	t_{PHL}	3.416	1.736 + 0.037*CL	1.956 + 0.029*CL	2.100 + 0.026*CL
	t_{PLZ}	0.984	0.984 + 0.000*CL	0.984 + 0.000*CL	0.984 + 0.000*CL
	t_{PHZ}	1.393	1.394 + 0.000*CL	1.393 + 0.000*CL	1.392 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.013	0.887 + 0.047*CL	1.188 + 0.037*CL	1.399 + 0.032*CL
	t_F	2.401	0.541 + 0.040*CL	0.721 + 0.034*CL	0.813 + 0.032*CL
	t_{PLH}	3.535	1.830 + 0.038*CL	2.137 + 0.028*CL	2.380 + 0.023*CL
	t_{PHL}	2.983	1.556 + 0.031*CL	1.759 + 0.024*CL	1.907 + 0.022*CL
TN to PAD	t_R	3.013	0.887 + 0.047*CL	1.188 + 0.037*CL	1.399 + 0.032*CL
	t_F	2.406	0.588 + 0.038*CL	0.741 + 0.033*CL	0.823 + 0.032*CL
	t_{PLH}	3.710	2.003 + 0.038*CL	2.310 + 0.028*CL	2.554 + 0.023*CL
	t_{PHL}	3.108	1.647 + 0.032*CL	1.873 + 0.025*CL	2.028 + 0.022*CL
	t_{PLZ}	0.951	0.951 + 0.000*CL	0.951 + 0.000*CL	0.951 + 0.000*CL
	t_{PHZ}	1.558	1.559 + 0.000*CL	1.558 + 0.000*CL	1.557 + 0.000*CL
EN to PAD	t_R	3.013	0.887 + 0.047*CL	1.188 + 0.037*CL	1.399 + 0.032*CL
	t_F	2.406	0.589 + 0.038*CL	0.741 + 0.033*CL	0.824 + 0.032*CL
	t_{PLH}	3.797	2.090 + 0.038*CL	2.398 + 0.028*CL	2.641 + 0.023*CL
	t_{PHL}	3.196	1.735 + 0.032*CL	1.961 + 0.025*CL	2.115 + 0.022*CL
	t_{PLZ}	1.038	1.038 + 0.000*CL	1.038 + 0.000*CL	1.038 + 0.000*CL
	t_{PHZ}	1.644	1.645 + 0.000*CL	1.644 + 0.000*CL	1.643 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmot20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.505	0.866 + 0.036*CL	1.080 + 0.029*CL	1.222 + 0.026*CL
	t_F	2.140	0.567 + 0.034*CL	0.736 + 0.028*CL	0.832 + 0.026*CL
	t_{PLH}	3.457	2.039 + 0.032*CL	2.330 + 0.023*CL	2.531 + 0.019*CL
	t_{PHL}	2.950	1.649 + 0.029*CL	1.860 + 0.022*CL	2.011 + 0.019*CL
TN to PAD	t_R	2.505	0.867 + 0.036*CL	1.080 + 0.029*CL	1.222 + 0.026*CL
	t_F	2.143	0.596 + 0.033*CL	0.747 + 0.028*CL	0.838 + 0.026*CL
	t_{PLH}	3.631	2.212 + 0.032*CL	2.503 + 0.023*CL	2.705 + 0.019*CL
	t_{PHL}	3.078	1.761 + 0.029*CL	1.984 + 0.022*CL	2.137 + 0.019*CL
	t_{PLZ}	0.954	0.954 + 0.000*CL	0.954 + 0.000*CL	0.954 + 0.000*CL
	t_{PHZ}	1.557	1.558 + 0.000*CL	1.557 + 0.000*CL	1.556 + 0.000*CL
EN to PAD	t_R	2.505	0.867 + 0.036*CL	1.080 + 0.029*CL	1.222 + 0.026*CL
	t_F	2.143	0.596 + 0.033*CL	0.747 + 0.028*CL	0.838 + 0.026*CL
	t_{PLH}	3.719	2.300 + 0.032*CL	2.591 + 0.023*CL	2.793 + 0.019*CL
	t_{PHL}	3.166	1.849 + 0.029*CL	2.071 + 0.022*CL	2.224 + 0.019*CL
	t_{PLZ}	1.040	1.040 + 0.000*CL	1.040 + 0.000*CL	1.040 + 0.000*CL
	t_{PHZ}	1.643	1.644 + 0.000*CL	1.643 + 0.000*CL	1.643 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.325	0.856 + 0.032*CL	1.065 + 0.025*CL	1.208 + 0.022*CL
	t_F	1.989	0.521 + 0.032*CL	0.706 + 0.026*CL	0.830 + 0.023*CL
	t_{PLH}	3.347	2.013 + 0.030*CL	2.297 + 0.021*CL	2.494 + 0.017*CL
	t_{PHL}	2.818	1.643 + 0.026*CL	1.816 + 0.020*CL	1.957 + 0.017*CL
TN to PAD	t_R	2.325	0.856 + 0.032*CL	1.065 + 0.025*CL	1.209 + 0.022*CL
	t_F	2.005	0.597 + 0.030*CL	0.754 + 0.025*CL	0.859 + 0.023*CL
	t_{PLH}	3.522	2.187 + 0.030*CL	2.470 + 0.021*CL	2.669 + 0.017*CL
	t_{PHL}	2.937	1.693 + 0.028*CL	1.911 + 0.021*CL	2.066 + 0.017*CL
	t_{PLZ}	1.007	1.007 + 0.000*CL	1.007 + 0.000*CL	1.007 + 0.000*CL
	t_{PHZ}	1.810	1.810 + 0.000*CL	1.810 + 0.000*CL	1.809 + 0.000*CL
EN to PAD	t_R	2.325	0.856 + 0.032*CL	1.065 + 0.025*CL	1.208 + 0.022*CL
	t_F	2.005	0.598 + 0.030*CL	0.754 + 0.025*CL	0.859 + 0.023*CL
	t_{PLH}	3.610	2.274 + 0.030*CL	2.558 + 0.021*CL	2.756 + 0.017*CL
	t_{PHL}	3.025	1.780 + 0.028*CL	1.999 + 0.021*CL	2.153 + 0.017*CL
	t_{PLZ}	1.093	1.093 + 0.000*CL	1.093 + 0.000*CL	1.093 + 0.000*CL
	t_{PHZ}	1.896	1.897 + 0.000*CL	1.896 + 0.000*CL	1.896 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.755	0.592 + 0.262*CL	0.466 + 0.266*CL	0.401 + 0.267*CL
	t_F	12.919	0.661 + 0.243*CL	0.534 + 0.248*CL	0.447 + 0.249*CL
	t_{PLH}	7.767	1.815 + 0.119*CL	1.847 + 0.118*CL	1.850 + 0.118*CL
	t_{PHL}	8.099	1.928 + 0.124*CL	1.998 + 0.122*CL	2.006 + 0.122*CL
TN to PAD	t_R	13.755	0.592 + 0.262*CL	0.466 + 0.266*CL	0.401 + 0.267*CL
	t_F	12.919	0.661 + 0.243*CL	0.534 + 0.248*CL	0.447 + 0.249*CL
	t_{PLH}	7.965	2.008 + 0.120*CL	2.042 + 0.118*CL	2.044 + 0.118*CL
	t_{PHL}	8.233	2.058 + 0.124*CL	2.130 + 0.122*CL	2.138 + 0.122*CL
	t_{PLZ}	0.901	0.901 + 0.000*CL	0.901 + 0.000*CL	0.901 + 0.000*CL
	t_{PHZ}	0.883	0.883 + 0.000*CL	0.883 + 0.000*CL	0.883 + 0.000*CL
EN to PAD	t_R	13.755	0.592 + 0.262*CL	0.466 + 0.266*CL	0.401 + 0.267*CL
	t_F	12.919	0.661 + 0.243*CL	0.534 + 0.248*CL	0.447 + 0.249*CL
	t_{PLH}	8.052	2.096 + 0.120*CL	2.130 + 0.118*CL	2.133 + 0.118*CL
	t_{PHL}	8.321	2.146 + 0.124*CL	2.217 + 0.122*CL	2.224 + 0.122*CL
	t_{PLZ}	0.987	0.987 + 0.000*CL	0.987 + 0.000*CL	0.987 + 0.000*CL
	t_{PHZ}	0.969	0.969 + 0.000*CL	0.969 + 0.000*CL	0.969 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.843	0.162 + 0.133*CL	0.151 + 0.134*CL	0.149 + 0.134*CL
	t_F	6.407	0.172 + 0.124*CL	0.148 + 0.125*CL	0.143 + 0.125*CL
	t_{PLH}	3.838	0.878 + 0.059*CL	0.879 + 0.059*CL	0.879 + 0.059*CL
	t_{PHL}	4.035	0.989 + 0.061*CL	0.989 + 0.061*CL	0.989 + 0.061*CL
TN to PAD	t_R	6.843	0.162 + 0.133*CL	0.150 + 0.134*CL	0.150 + 0.134*CL
	t_F	6.407	0.173 + 0.124*CL	0.149 + 0.125*CL	0.143 + 0.125*CL
	t_{PLH}	4.036	1.073 + 0.059*CL	1.075 + 0.059*CL	1.076 + 0.059*CL
	t_{PHL}	4.164	1.111 + 0.061*CL	1.115 + 0.061*CL	1.117 + 0.061*CL
	t_{PLZ}	0.928	0.928 + 0.000*CL	0.928 + 0.000*CL	0.928 + 0.000*CL
	t_{PHZ}	1.006	1.006 + 0.000*CL	1.006 + 0.000*CL	1.006 + 0.000*CL
EN to PAD	t_R	6.843	0.162 + 0.133*CL	0.151 + 0.134*CL	0.149 + 0.134*CL
	t_F	6.407	0.173 + 0.124*CL	0.149 + 0.125*CL	0.143 + 0.125*CL
	t_{PLH}	4.124	1.161 + 0.059*CL	1.162 + 0.059*CL	1.164 + 0.059*CL
	t_{PHL}	4.252	1.199 + 0.061*CL	1.203 + 0.061*CL	1.204 + 0.061*CL
	t_{PLZ}	1.014	1.014 + 0.000*CL	1.014 + 0.000*CL	1.014 + 0.000*CL
	t_{PHZ}	1.092	1.092 + 0.000*CL	1.092 + 0.000*CL	1.092 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.462	0.195 + 0.065*CL	0.153 + 0.066*CL	0.130 + 0.067*CL
	t_F	3.270	0.224 + 0.061*CL	0.197 + 0.061*CL	0.168 + 0.062*CL
	t_{PLH}	2.499	1.004 + 0.030*CL	1.018 + 0.030*CL	1.020 + 0.030*CL
	t_{PHL}	2.695	1.135 + 0.032*CL	1.168 + 0.031*CL	1.172 + 0.030*CL
TN to PAD	t_R	3.463	0.195 + 0.065*CL	0.153 + 0.066*CL	0.130 + 0.067*CL
	t_F	3.271	0.233 + 0.060*CL	0.200 + 0.061*CL	0.169 + 0.062*CL
	t_{PLH}	2.698	1.199 + 0.030*CL	1.215 + 0.030*CL	1.217 + 0.030*CL
	t_{PHL}	2.821	1.241 + 0.032*CL	1.286 + 0.031*CL	1.294 + 0.031*CL
	t_{PLZ}	1.042	1.043 + 0.000*CL	1.042 + 0.000*CL	1.042 + 0.000*CL
	t_{PHZ}	1.260	1.261 + 0.000*CL	1.260 + 0.000*CL	1.260 + 0.000*CL
EN to PAD	t_R	3.463	0.195 + 0.065*CL	0.153 + 0.066*CL	0.130 + 0.067*CL
	t_F	3.271	0.233 + 0.060*CL	0.200 + 0.061*CL	0.169 + 0.062*CL
	t_{PLH}	2.786	1.287 + 0.030*CL	1.302 + 0.030*CL	1.304 + 0.030*CL
	t_{PHL}	2.908	1.329 + 0.032*CL	1.373 + 0.031*CL	1.381 + 0.031*CL
	t_{PLZ}	1.128	1.128 + 0.000*CL	1.128 + 0.000*CL	1.128 + 0.000*CL
	t_{PHZ}	1.346	1.347 + 0.000*CL	1.346 + 0.000*CL	1.346 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.387	0.263 + 0.042*CL	0.235 + 0.043*CL	0.201 + 0.044*CL
	t_F	2.299	0.289 + 0.040*CL	0.286 + 0.040*CL	0.269 + 0.041*CL
	t_{PLH}	2.161	1.102 + 0.022*CL	1.159 + 0.020*CL	1.172 + 0.020*CL
	t_{PHL}	2.381	1.257 + 0.023*CL	1.325 + 0.021*CL	1.355 + 0.021*CL
TN to PAD	t_R	2.387	0.268 + 0.042*CL	0.235 + 0.043*CL	0.201 + 0.044*CL
	t_F	2.303	0.295 + 0.040*CL	0.302 + 0.040*CL	0.277 + 0.041*CL
	t_{PLH}	2.360	1.295 + 0.022*CL	1.354 + 0.020*CL	1.369 + 0.020*CL
	t_{PHL}	2.500	1.322 + 0.025*CL	1.424 + 0.022*CL	1.466 + 0.021*CL
	t_{PLZ}	1.152	1.153 + 0.000*CL	1.152 + 0.000*CL	1.152 + 0.000*CL
	t_{PHZ}	1.514	1.515 + 0.000*CL	1.514 + 0.000*CL	1.514 + 0.000*CL
EN to PAD	t_R	2.387	0.268 + 0.042*CL	0.236 + 0.043*CL	0.201 + 0.044*CL
	t_F	2.303	0.295 + 0.040*CL	0.302 + 0.040*CL	0.277 + 0.041*CL
	t_{PLH}	2.447	1.382 + 0.022*CL	1.442 + 0.020*CL	1.456 + 0.020*CL
	t_{PHL}	2.587	1.410 + 0.025*CL	1.512 + 0.022*CL	1.553 + 0.021*CL
	t_{PLZ}	1.239	1.239 + 0.000*CL	1.239 + 0.000*CL	1.238 + 0.000*CL
	t_{PHZ}	1.600	1.601 + 0.000*CL	1.600 + 0.000*CL	1.600 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.901	0.312 + 0.032*CL	0.322 + 0.032*CL	0.295 + 0.032*CL
	t_F	1.867	0.351 + 0.031*CL	0.368 + 0.030*CL	0.362 + 0.030*CL
	t_{PLH}	2.064	1.176 + 0.019*CL	1.269 + 0.016*CL	1.308 + 0.015*CL
	t_{PHL}	2.305	1.383 + 0.019*CL	1.451 + 0.017*CL	1.503 + 0.016*CL
TN to PAD	t_R	1.902	0.326 + 0.032*CL	0.326 + 0.032*CL	0.297 + 0.032*CL
	t_F	1.879	0.336 + 0.031*CL	0.384 + 0.030*CL	0.383 + 0.030*CL
	t_{PLH}	2.262	1.364 + 0.019*CL	1.462 + 0.016*CL	1.504 + 0.015*CL
	t_{PHL}	2.410	1.383 + 0.022*CL	1.518 + 0.018*CL	1.592 + 0.016*CL
	t_{PLZ}	1.263	1.263 + 0.000*CL	1.263 + 0.000*CL	1.263 + 0.000*CL
	t_{PHZ}	1.768	1.768 + 0.000*CL	1.768 + 0.000*CL	1.767 + 0.000*CL
EN to PAD	t_R	1.902	0.326 + 0.032*CL	0.326 + 0.032*CL	0.297 + 0.032*CL
	t_F	1.879	0.336 + 0.031*CL	0.384 + 0.030*CL	0.383 + 0.030*CL
	t_{PLH}	2.350	1.451 + 0.019*CL	1.550 + 0.016*CL	1.591 + 0.015*CL
	t_{PHL}	2.498	1.470 + 0.022*CL	1.605 + 0.018*CL	1.679 + 0.016*CL
	t_{PLZ}	1.349	1.349 + 0.000*CL	1.349 + 0.000*CL	1.349 + 0.000*CL
	t_{PHZ}	1.853	1.854 + 0.000*CL	1.853 + 0.000*CL	1.853 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.474	0.210 + 0.025*CL	0.193 + 0.026*CL	0.171 + 0.026*CL
	t_F	1.494	0.483 + 0.019*CL	0.385 + 0.022*CL	0.331 + 0.023*CL
	t_{PLH}	1.687	1.054 + 0.013*CL	1.084 + 0.012*CL	1.095 + 0.012*CL
	t_{PHL}	1.940	1.307 + 0.013*CL	1.351 + 0.012*CL	1.354 + 0.012*CL
TN to PAD	t_R	1.479	0.220 + 0.025*CL	0.207 + 0.025*CL	0.183 + 0.026*CL
	t_F	1.446	0.230 + 0.025*CL	0.251 + 0.024*CL	0.242 + 0.024*CL
	t_{PLH}	1.873	1.191 + 0.014*CL	1.251 + 0.012*CL	1.273 + 0.012*CL
	t_{PHL}	1.971	1.201 + 0.017*CL	1.289 + 0.014*CL	1.333 + 0.013*CL
	t_{PLZ}	1.406	1.407 + 0.000*CL	1.406 + 0.000*CL	1.406 + 0.000*CL
	t_{PHZ}	2.040	2.041 + 0.000*CL	2.040 + 0.000*CL	2.040 + 0.000*CL
EN to PAD	t_R	1.479	0.220 + 0.025*CL	0.207 + 0.025*CL	0.182 + 0.026*CL
	t_F	1.446	0.229 + 0.025*CL	0.251 + 0.024*CL	0.242 + 0.024*CL
	t_{PLH}	1.960	1.279 + 0.014*CL	1.339 + 0.012*CL	1.360 + 0.012*CL
	t_{PHL}	2.058	1.289 + 0.017*CL	1.376 + 0.014*CL	1.420 + 0.013*CL
	t_{PLZ}	1.492	1.493 + 0.000*CL	1.492 + 0.000*CL	1.492 + 0.000*CL
	t_{PHZ}	2.127	2.127 + 0.000*CL	2.127 + 0.000*CL	2.126 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.227	0.174 + 0.021*CL	0.159 + 0.021*CL	0.141 + 0.022*CL
	t_F	1.239	0.391 + 0.016*CL	0.312 + 0.019*CL	0.268 + 0.019*CL
	t_{PLH}	1.539	1.014 + 0.011*CL	1.038 + 0.010*CL	1.046 + 0.010*CL
	t_{PHL}	1.740	1.215 + 0.011*CL	1.250 + 0.010*CL	1.251 + 0.010*CL
TN to PAD	t_R	1.231	0.183 + 0.021*CL	0.170 + 0.021*CL	0.150 + 0.022*CL
	t_F	1.200	0.188 + 0.020*CL	0.205 + 0.020*CL	0.196 + 0.020*CL
	t_{PLH}	1.728	1.161 + 0.012*CL	1.210 + 0.010*CL	1.228 + 0.010*CL
	t_{PHL}	1.788	1.150 + 0.014*CL	1.221 + 0.011*CL	1.257 + 0.011*CL
	t_{PLZ}	1.336	1.336 + 0.000*CL	1.336 + 0.000*CL	1.335 + 0.000*CL
	t_{PHZ}	1.813	1.813 + 0.000*CL	1.813 + 0.000*CL	1.812 + 0.000*CL
EN to PAD	t_R	1.232	0.183 + 0.021*CL	0.170 + 0.021*CL	0.151 + 0.022*CL
	t_F	1.201	0.188 + 0.020*CL	0.205 + 0.020*CL	0.197 + 0.020*CL
	t_{PLH}	1.815	1.249 + 0.012*CL	1.298 + 0.010*CL	1.315 + 0.010*CL
	t_{PHL}	1.875	1.237 + 0.014*CL	1.309 + 0.011*CL	1.345 + 0.011*CL
	t_{PLZ}	1.421	1.422 + 0.000*CL	1.421 + 0.000*CL	1.421 + 0.000*CL
	t_{PHZ}	1.899	1.899 + 0.000*CL	1.899 + 0.000*CL	1.898 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.231	0.741 + 0.130*CL	0.747 + 0.130*CL	0.688 + 0.131*CL
	t_F	6.712	0.689 + 0.120*CL	0.661 + 0.121*CL	0.582 + 0.123*CL
	t_{PLH}	5.171	1.869 + 0.069*CL	2.083 + 0.062*CL	2.173 + 0.060*CL
	t_{PHL}	5.232	1.908 + 0.069*CL	2.107 + 0.063*CL	2.167 + 0.061*CL
TN to PAD	t_R	7.231	0.741 + 0.130*CL	0.747 + 0.130*CL	0.687 + 0.131*CL
	t_F	6.712	0.689 + 0.120*CL	0.661 + 0.121*CL	0.582 + 0.123*CL
	t_{PLH}	5.370	2.064 + 0.069*CL	2.279 + 0.062*CL	2.370 + 0.060*CL
	t_{PHL}	5.367	2.039 + 0.069*CL	2.239 + 0.063*CL	2.301 + 0.061*CL
	t_{PLZ}	1.008	1.008 + 0.000*CL	1.008 + 0.000*CL	1.008 + 0.000*CL
	t_{PHZ}	1.063	1.064 + 0.000*CL	1.063 + 0.000*CL	1.063 + 0.000*CL
EN to PAD	t_R	7.231	0.741 + 0.130*CL	0.747 + 0.130*CL	0.687 + 0.131*CL
	t_F	6.712	0.689 + 0.120*CL	0.661 + 0.121*CL	0.582 + 0.123*CL
	t_{PLH}	5.457	2.152 + 0.069*CL	2.366 + 0.062*CL	2.457 + 0.060*CL
	t_{PHL}	5.454	2.127 + 0.069*CL	2.327 + 0.063*CL	2.388 + 0.061*CL
	t_{PLZ}	1.094	1.095 + 0.000*CL	1.094 + 0.000*CL	1.094 + 0.000*CL
	t_{PHZ}	1.149	1.150 + 0.000*CL	1.149 + 0.000*CL	1.149 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot8sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.922	0.683 + 0.066*CL	0.743 + 0.064*CL	0.719 + 0.064*CL
	t_F	3.900	0.736 + 0.065*CL	0.877 + 0.060*CL	0.907 + 0.060*CL
	t_{PLH}	3.705	1.807 + 0.041*CL	2.031 + 0.033*CL	2.147 + 0.031*CL
	t_{PHL}	4.146	1.977 + 0.047*CL	2.278 + 0.037*CL	2.457 + 0.034*CL
TN to PAD	t_R	3.922	0.683 + 0.066*CL	0.743 + 0.064*CL	0.719 + 0.064*CL
	t_F	3.901	0.736 + 0.065*CL	0.877 + 0.060*CL	0.907 + 0.060*CL
	t_{PLH}	3.904	2.005 + 0.041*CL	2.229 + 0.033*CL	2.345 + 0.031*CL
	t_{PHL}	4.278	2.106 + 0.047*CL	2.408 + 0.037*CL	2.588 + 0.034*CL
	t_{PLZ}	1.038	1.038 + 0.000*CL	1.038 + 0.000*CL	1.037 + 0.000*CL
	t_{PHZ}	1.282	1.282 + 0.000*CL	1.282 + 0.000*CL	1.281 + 0.000*CL
EN to PAD	t_R	3.922	0.683 + 0.066*CL	0.743 + 0.064*CL	0.719 + 0.064*CL
	t_F	3.901	0.736 + 0.065*CL	0.877 + 0.060*CL	0.907 + 0.060*CL
	t_{PLH}	3.992	2.092 + 0.041*CL	2.317 + 0.033*CL	2.433 + 0.031*CL
	t_{PHL}	4.365	2.194 + 0.047*CL	2.496 + 0.037*CL	2.675 + 0.034*CL
	t_{PLZ}	1.124	1.124 + 0.000*CL	1.124 + 0.000*CL	1.123 + 0.000*CL
	t_{PHZ}	1.368	1.369 + 0.000*CL	1.368 + 0.000*CL	1.367 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot12sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.161	0.824 + 0.049*CL	0.980 + 0.044*CL	1.039 + 0.042*CL
	t_F	3.320	0.857 + 0.052*CL	1.098 + 0.044*CL	1.234 + 0.042*CL
	t_{PLH}	3.704	2.019 + 0.038*CL	2.312 + 0.028*CL	2.495 + 0.024*CL
	t_{PHL}	4.212	2.185 + 0.045*CL	2.550 + 0.033*CL	2.798 + 0.028*CL
TN to PAD	t_R	3.161	0.824 + 0.049*CL	0.980 + 0.044*CL	1.039 + 0.042*CL
	t_F	3.320	0.863 + 0.052*CL	1.100 + 0.044*CL	1.234 + 0.042*CL
	t_{PLH}	3.904	2.219 + 0.038*CL	2.511 + 0.028*CL	2.694 + 0.024*CL
	t_{PHL}	4.345	2.313 + 0.046*CL	2.680 + 0.033*CL	2.929 + 0.028*CL
	t_{PLZ}	1.038	1.038 + 0.000*CL	1.038 + 0.000*CL	1.037 + 0.000*CL
	t_{PHZ}	1.535	1.536 + 0.000*CL	1.535 + 0.000*CL	1.535 + 0.000*CL
EN to PAD	t_R	3.161	0.824 + 0.049*CL	0.980 + 0.044*CL	1.039 + 0.042*CL
	t_F	3.320	0.863 + 0.052*CL	1.100 + 0.044*CL	1.234 + 0.042*CL
	t_{PLH}	3.991	2.306 + 0.038*CL	2.598 + 0.028*CL	2.781 + 0.024*CL
	t_{PHL}	4.432	2.401 + 0.046*CL	2.768 + 0.033*CL	3.017 + 0.028*CL
	t_{PLZ}	1.124	1.124 + 0.000*CL	1.124 + 0.000*CL	1.123 + 0.000*CL
	t_{PHZ}	1.622	1.623 + 0.000*CL	1.622 + 0.000*CL	1.621 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot16sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.661	0.792 + 0.040*CL	0.958 + 0.034*CL	1.042 + 0.032*CL
	t_F	2.905	0.840 + 0.045*CL	1.094 + 0.036*CL	1.249 + 0.033*CL
	t_{PLH}	3.411	1.941 + 0.033*CL	2.223 + 0.024*CL	2.405 + 0.020*CL
	t_{PHL}	4.049	2.217 + 0.041*CL	2.572 + 0.030*CL	2.820 + 0.025*CL
TN to PAD	t_R	2.661	0.791 + 0.040*CL	0.958 + 0.034*CL	1.042 + 0.032*CL
	t_F	2.907	0.863 + 0.044*CL	1.102 + 0.036*CL	1.253 + 0.033*CL
	t_{PLH}	3.611	2.142 + 0.033*CL	2.423 + 0.024*CL	2.605 + 0.020*CL
	t_{PHL}	4.181	2.336 + 0.042*CL	2.700 + 0.030*CL	2.950 + 0.025*CL
	t_{PLZ}	1.255	1.256 + 0.000*CL	1.255 + 0.000*CL	1.255 + 0.000*CL
	t_{PHZ}	1.780	1.781 + 0.000*CL	1.780 + 0.000*CL	1.780 + 0.000*CL
EN to PAD	t_R	2.661	0.791 + 0.040*CL	0.958 + 0.034*CL	1.042 + 0.032*CL
	t_F	2.907	0.863 + 0.044*CL	1.101 + 0.036*CL	1.253 + 0.033*CL
	t_{PLH}	3.699	2.230 + 0.033*CL	2.510 + 0.024*CL	2.692 + 0.020*CL
	t_{PHL}	4.269	2.424 + 0.042*CL	2.787 + 0.030*CL	3.038 + 0.025*CL
	t_{PLZ}	1.341	1.342 + 0.000*CL	1.341 + 0.000*CL	1.341 + 0.000*CL
	t_{PHZ}	1.867	1.867 + 0.000*CL	1.867 + 0.000*CL	1.866 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot20sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.079	0.632 + 0.031*CL	0.761 + 0.026*CL	0.815 + 0.025*CL
	t_F	2.093	0.509 + 0.034*CL	0.708 + 0.028*CL	0.823 + 0.025*CL
	t_{PLH}	2.819	1.673 + 0.026*CL	1.898 + 0.018*CL	2.042 + 0.016*CL
	t_{PHL}	3.078	1.838 + 0.027*CL	2.040 + 0.021*CL	2.197 + 0.018*CL
TN to PAD	t_R	2.079	0.638 + 0.031*CL	0.763 + 0.026*CL	0.815 + 0.025*CL
	t_F	2.110	0.605 + 0.032*CL	0.765 + 0.027*CL	0.855 + 0.025*CL
	t_{PLH}	3.019	1.869 + 0.026*CL	2.096 + 0.018*CL	2.241 + 0.016*CL
	t_{PHL}	3.197	1.873 + 0.030*CL	2.130 + 0.021*CL	2.304 + 0.018*CL
	t_{PLZ}	1.468	1.468 + 0.000*CL	1.468 + 0.000*CL	1.467 + 0.000*CL
	t_{PHZ}	2.022	2.022 + 0.000*CL	2.022 + 0.000*CL	2.022 + 0.000*CL
EN to PAD	t_R	2.079	0.638 + 0.031*CL	0.763 + 0.026*CL	0.815 + 0.025*CL
	t_F	2.110	0.605 + 0.032*CL	0.765 + 0.027*CL	0.855 + 0.025*CL
	t_{PLH}	3.107	1.957 + 0.026*CL	2.184 + 0.018*CL	2.328 + 0.016*CL
	t_{PHL}	3.284	1.961 + 0.030*CL	2.217 + 0.021*CL	2.392 + 0.018*CL
	t_{PLZ}	1.554	1.555 + 0.000*CL	1.554 + 0.000*CL	1.554 + 0.000*CL
	t_{PHZ}	2.108	2.108 + 0.000*CL	2.108 + 0.000*CL	2.108 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot24sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.606	0.415 + 0.025*CL	0.520 + 0.022*CL	0.554 + 0.021*CL
	t_F	1.593	0.498 + 0.022*CL	0.527 + 0.021*CL	0.564 + 0.021*CL
	t_{PLH}	2.241	1.391 + 0.019*CL	1.539 + 0.014*CL	1.635 + 0.012*CL
	t_{PHL}	2.482	1.707 + 0.016*CL	1.774 + 0.014*CL	1.838 + 0.013*CL
TN to PAD	t_R	1.610	0.451 + 0.024*CL	0.533 + 0.022*CL	0.560 + 0.021*CL
	t_F	1.624	0.431 + 0.025*CL	0.542 + 0.022*CL	0.599 + 0.020*CL
	t_{PLH}	2.439	1.570 + 0.019*CL	1.730 + 0.014*CL	1.830 + 0.012*CL
	t_{PHL}	2.544	1.548 + 0.022*CL	1.731 + 0.016*CL	1.854 + 0.014*CL
	t_{PLZ}	1.481	1.481 + 0.000*CL	1.481 + 0.000*CL	1.481 + 0.000*CL
	t_{PHZ}	2.291	2.291 + 0.000*CL	2.291 + 0.000*CL	2.291 + 0.000*CL
EN to PAD	t_R	1.610	0.451 + 0.024*CL	0.533 + 0.022*CL	0.560 + 0.021*CL
	t_F	1.624	0.431 + 0.025*CL	0.542 + 0.022*CL	0.599 + 0.020*CL
	t_{PLH}	2.526	1.658 + 0.019*CL	1.818 + 0.014*CL	1.917 + 0.012*CL
	t_{PHL}	2.631	1.636 + 0.022*CL	1.819 + 0.016*CL	1.941 + 0.014*CL
	t_{PLZ}	1.567	1.567 + 0.000*CL	1.567 + 0.000*CL	1.567 + 0.000*CL
	t_{PHZ}	2.377	2.377 + 0.000*CL	2.377 + 0.000*CL	2.377 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot12sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.022	1.233 + 0.060*CL	1.547 + 0.050*CL	1.739 + 0.046*CL
	t_F	4.453	1.170 + 0.072*CL	1.614 + 0.057*CL	1.932 + 0.050*CL
	t_{PLH}	4.907	2.629 + 0.051*CL	3.071 + 0.037*CL	3.374 + 0.031*CL
	t_{PHL}	5.229	2.454 + 0.062*CL	2.940 + 0.046*CL	3.298 + 0.039*CL
TN to PAD	t_R	4.022	1.234 + 0.060*CL	1.547 + 0.049*CL	1.739 + 0.046*CL
	t_F	4.456	1.190 + 0.071*CL	1.622 + 0.057*CL	1.936 + 0.050*CL
	t_{PLH}	5.108	2.831 + 0.051*CL	3.271 + 0.037*CL	3.575 + 0.031*CL
	t_{PHL}	5.362	2.573 + 0.062*CL	3.067 + 0.046*CL	3.429 + 0.039*CL
	t_{PLZ}	1.278	1.278 + 0.000*CL	1.278 + 0.000*CL	1.278 + 0.000*CL
	t_{PHZ}	1.820	1.822 + 0.000*CL	1.820 + 0.000*CL	1.820 + 0.000*CL
EN to PAD	t_R	4.022	1.234 + 0.060*CL	1.547 + 0.049*CL	1.739 + 0.046*CL
	t_F	4.456	1.190 + 0.071*CL	1.622 + 0.057*CL	1.937 + 0.050*CL
	t_{PLH}	5.196	2.918 + 0.051*CL	3.359 + 0.037*CL	3.662 + 0.031*CL
	t_{PHL}	5.450	2.661 + 0.062*CL	3.155 + 0.046*CL	3.517 + 0.039*CL
	t_{PLZ}	1.364	1.365 + 0.000*CL	1.364 + 0.000*CL	1.364 + 0.000*CL
	t_{PHZ}	1.906	1.908 + 0.000*CL	1.906 + 0.000*CL	1.906 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot16sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.558	1.144 + 0.053*CL	1.486 + 0.041*CL	1.716 + 0.037*CL
	t_F	3.677	1.243 + 0.054*CL	1.607 + 0.041*CL	1.846 + 0.037*CL
	t_{PLH}	4.331	2.263 + 0.047*CL	2.669 + 0.033*CL	2.968 + 0.027*CL
	t_{PHL}	5.431	3.009 + 0.055*CL	3.522 + 0.038*CL	3.884 + 0.031*CL
TN to PAD	t_R	3.559	1.146 + 0.053*CL	1.488 + 0.041*CL	1.717 + 0.037*CL
	t_F	3.678	1.266 + 0.053*CL	1.614 + 0.041*CL	1.849 + 0.037*CL
	t_{PLH}	4.532	2.463 + 0.047*CL	2.869 + 0.033*CL	3.169 + 0.027*CL
	t_{PHL}	5.564	3.131 + 0.056*CL	3.651 + 0.038*CL	4.016 + 0.031*CL
	t_{PLZ}	1.498	1.499 + 0.000*CL	1.498 + 0.000*CL	1.498 + 0.000*CL
	t_{PHZ}	2.306	2.306 + 0.000*CL	2.306 + 0.000*CL	2.305 + 0.000*CL
EN to PAD	t_R	3.559	1.146 + 0.053*CL	1.488 + 0.041*CL	1.717 + 0.037*CL
	t_F	3.678	1.266 + 0.053*CL	1.614 + 0.041*CL	1.849 + 0.037*CL
	t_{PLH}	4.619	2.551 + 0.047*CL	2.957 + 0.033*CL	3.256 + 0.027*CL
	t_{PHL}	5.652	3.218 + 0.056*CL	3.739 + 0.038*CL	4.103 + 0.031*CL
	t_{PLZ}	1.584	1.585 + 0.000*CL	1.584 + 0.000*CL	1.584 + 0.000*CL
	t_{PHZ}	2.392	2.392 + 0.000*CL	2.392 + 0.000*CL	2.391 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phot20sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.806	1.009 + 0.039*CL	1.233 + 0.031*CL	1.374 + 0.029*CL
	t_F	3.635	1.341 + 0.051*CL	1.717 + 0.038*CL	1.975 + 0.033*CL
	t_{PLH}	3.906	2.283 + 0.037*CL	2.631 + 0.026*CL	2.864 + 0.021*CL
	t_{PHL}	5.625	3.189 + 0.056*CL	3.728 + 0.038*CL	4.108 + 0.030*CL
TN to PAD	t_R	2.806	1.008 + 0.039*CL	1.232 + 0.031*CL	1.373 + 0.029*CL
	t_F	3.636	1.356 + 0.050*CL	1.721 + 0.038*CL	1.977 + 0.033*CL
	t_{PLH}	4.108	2.486 + 0.037*CL	2.833 + 0.026*CL	3.066 + 0.021*CL
	t_{PHL}	5.760	3.317 + 0.056*CL	3.861 + 0.038*CL	4.242 + 0.030*CL
	t_{PLZ}	1.492	1.493 + 0.000*CL	1.492 + 0.000*CL	1.492 + 0.000*CL
	t_{PHZ}	2.300	2.300 + 0.000*CL	2.300 + 0.000*CL	2.299 + 0.000*CL
EN to PAD	t_R	2.806	1.008 + 0.039*CL	1.232 + 0.031*CL	1.373 + 0.029*CL
	t_F	3.636	1.356 + 0.050*CL	1.721 + 0.038*CL	1.977 + 0.033*CL
	t_{PLH}	4.196	2.573 + 0.037*CL	2.920 + 0.026*CL	3.153 + 0.021*CL
	t_{PHL}	5.848	3.405 + 0.056*CL	3.948 + 0.038*CL	4.330 + 0.030*CL
	t_{PLZ}	1.579	1.579 + 0.000*CL	1.579 + 0.000*CL	1.578 + 0.000*CL
	t_{PHZ}	2.386	2.386 + 0.000*CL	2.386 + 0.000*CL	2.385 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot24sh

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.563	1.010 + 0.034*CL	1.230 + 0.027*CL	1.369 + 0.024*CL
	t_F	2.985	0.963 + 0.046*CL	1.355 + 0.033*CL	1.594 + 0.028*CL
	t_{PLH}	3.838	2.320 + 0.035*CL	2.663 + 0.024*CL	2.898 + 0.019*CL
	t_{PHL}	4.711	2.777 + 0.044*CL	3.168 + 0.031*CL	3.466 + 0.025*CL
TN to PAD	t_R	2.563	1.010 + 0.034*CL	1.229 + 0.027*CL	1.369 + 0.024*CL
	t_F	3.004	1.118 + 0.042*CL	1.421 + 0.032*CL	1.631 + 0.027*CL
	t_{PLH}	4.041	2.522 + 0.035*CL	2.864 + 0.024*CL	3.100 + 0.019*CL
	t_{PHL}	4.834	2.819 + 0.046*CL	3.265 + 0.031*CL	3.580 + 0.025*CL
	t_{PLZ}	1.699	1.699 + 0.000*CL	1.699 + 0.000*CL	1.699 + 0.000*CL
	t_{PHZ}	2.798	2.798 + 0.000*CL	2.798 + 0.000*CL	2.798 + 0.000*CL
EN to PAD	t_R	2.563	1.010 + 0.034*CL	1.229 + 0.027*CL	1.369 + 0.024*CL
	t_F	3.004	1.118 + 0.042*CL	1.421 + 0.032*CL	1.631 + 0.027*CL
	t_{PLH}	4.128	2.610 + 0.035*CL	2.952 + 0.024*CL	3.187 + 0.019*CL
	t_{PHL}	4.921	2.907 + 0.046*CL	3.352 + 0.031*CL	3.667 + 0.025*CL
	t_{PLZ}	1.785	1.785 + 0.000*CL	1.785 + 0.000*CL	1.785 + 0.000*CL
	t_{PHZ}	2.884	2.884 + 0.000*CL	2.884 + 0.000*CL	2.884 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmtot2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	12.308	0.580 + 0.237*CL	0.743 + 0.231*CL	0.780 + 0.231*CL
	t_F	12.866	1.293 + 0.237*CL	1.698 + 0.223*CL	1.952 + 0.218*CL
	t_{PLH}	6.392	1.341 + 0.101*CL	1.355 + 0.101*CL	1.369 + 0.100*CL
	t_{PHL}	7.334	1.464 + 0.120*CL	1.664 + 0.113*CL	1.783 + 0.111*CL
TN to PAD	t_R	12.308	0.580 + 0.237*CL	0.744 + 0.231*CL	0.780 + 0.231*CL
	t_F	12.867	1.297 + 0.237*CL	1.698 + 0.223*CL	1.955 + 0.218*CL
	t_{PLH}	6.583	1.529 + 0.101*CL	1.545 + 0.101*CL	1.559 + 0.100*CL
	t_{PHL}	7.481	1.607 + 0.120*CL	1.809 + 0.113*CL	1.930 + 0.111*CL
	t_{PLZ}	0.836	0.836 + 0.000*CL	0.836 + 0.000*CL	0.836 + 0.000*CL
	t_{PHZ}	1.284	1.285 + 0.000*CL	1.284 + 0.000*CL	1.284 + 0.000*CL
EN to PAD	t_R	12.308	0.580 + 0.237*CL	0.744 + 0.231*CL	0.780 + 0.231*CL
	t_F	12.867	1.297 + 0.237*CL	1.698 + 0.223*CL	1.955 + 0.218*CL
	t_{PLH}	6.671	1.617 + 0.101*CL	1.632 + 0.101*CL	1.647 + 0.100*CL
	t_{PHL}	7.568	1.695 + 0.120*CL	1.897 + 0.113*CL	2.017 + 0.111*CL
	t_{PLZ}	0.922	0.922 + 0.000*CL	0.922 + 0.000*CL	0.922 + 0.000*CL
	t_{PHZ}	1.370	1.371 + 0.000*CL	1.370 + 0.000*CL	1.370 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmtot4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.189	0.289 + 0.118*CL	0.306 + 0.118*CL	0.343 + 0.117*CL
	t_F	6.948	0.742 + 0.128*CL	1.029 + 0.118*CL	1.266 + 0.114*CL
	t_{PLH}	3.569	1.047 + 0.051*CL	1.054 + 0.050*CL	1.059 + 0.050*CL
	t_{PHL}	3.940	0.939 + 0.061*CL	0.982 + 0.059*CL	1.077 + 0.057*CL
TN to PAD	t_R	6.189	0.289 + 0.118*CL	0.306 + 0.118*CL	0.343 + 0.117*CL
	t_F	6.950	0.679 + 0.130*CL	1.020 + 0.119*CL	1.269 + 0.114*CL
	t_{PLH}	3.762	1.237 + 0.051*CL	1.245 + 0.050*CL	1.250 + 0.050*CL
	t_{PHL}	4.066	0.994 + 0.063*CL	1.080 + 0.060*CL	1.190 + 0.058*CL
	t_{PLZ}	0.876	0.876 + 0.000*CL	0.876 + 0.000*CL	0.876 + 0.000*CL
	t_{PHZ}	1.639	1.641 + 0.000*CL	1.639 + 0.000*CL	1.638 + 0.000*CL
EN to PAD	t_R	6.189	0.289 + 0.118*CL	0.306 + 0.118*CL	0.343 + 0.117*CL
	t_F	6.950	0.679 + 0.130*CL	1.020 + 0.119*CL	1.269 + 0.114*CL
	t_{PLH}	3.849	1.324 + 0.051*CL	1.332 + 0.050*CL	1.338 + 0.050*CL
	t_{PHL}	4.153	1.082 + 0.063*CL	1.167 + 0.060*CL	1.278 + 0.058*CL
	t_{PLZ}	0.963	0.963 + 0.000*CL	0.963 + 0.000*CL	0.963 + 0.000*CL
	t_{PHZ}	1.725	1.727 + 0.000*CL	1.725 + 0.000*CL	1.724 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmtot6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.157	0.280 + 0.077*CL	0.263 + 0.078*CL	0.261 + 0.078*CL
	t_F	4.918	0.643 + 0.088*CL	0.845 + 0.081*CL	1.023 + 0.078*CL
	t_{PLH}	2.787	1.095 + 0.034*CL	1.111 + 0.034*CL	1.114 + 0.033*CL
	t_{PHL}	3.032	1.030 + 0.040*CL	1.034 + 0.040*CL	1.070 + 0.039*CL
TN to PAD	t_R	4.157	0.281 + 0.077*CL	0.263 + 0.078*CL	0.261 + 0.078*CL
	t_F	4.906	0.490 + 0.092*CL	0.768 + 0.083*CL	0.987 + 0.078*CL
	t_{PLH}	2.980	1.284 + 0.034*CL	1.301 + 0.034*CL	1.306 + 0.033*CL
	t_{PHL}	3.127	0.996 + 0.044*CL	1.067 + 0.041*CL	1.135 + 0.040*CL
	t_{PLZ}	0.908	0.908 + 0.000*CL	0.908 + 0.000*CL	0.908 + 0.000*CL
	t_{PHZ}	2.019	2.022 + 0.000*CL	2.019 + 0.000*CL	2.018 + 0.000*CL
EN to PAD	t_R	4.157	0.281 + 0.077*CL	0.263 + 0.078*CL	0.261 + 0.078*CL
	t_F	4.906	0.490 + 0.092*CL	0.768 + 0.083*CL	0.988 + 0.078*CL
	t_{PLH}	3.067	1.371 + 0.034*CL	1.389 + 0.034*CL	1.393 + 0.033*CL
	t_{PHL}	3.215	1.084 + 0.044*CL	1.155 + 0.041*CL	1.223 + 0.040*CL
	t_{PLZ}	0.993	0.993 + 0.000*CL	0.993 + 0.000*CL	0.993 + 0.000*CL
	t_{PHZ}	2.106	2.108 + 0.000*CL	2.106 + 0.000*CL	2.105 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PvOTyz

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

pmtot4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.508	0.844 + 0.113*CL	0.841 + 0.113*CL	0.810 + 0.114*CL
	t_F	7.061	0.929 + 0.127*CL	1.230 + 0.117*CL	1.438 + 0.112*CL
	t_{PLH}	4.813	2.030 + 0.058*CL	2.212 + 0.052*CL	2.281 + 0.051*CL
	t_{PHL}	4.738	1.524 + 0.067*CL	1.700 + 0.061*CL	1.841 + 0.058*CL
TN to PAD	t_R	6.508	0.845 + 0.113*CL	0.841 + 0.113*CL	0.810 + 0.114*CL
	t_F	7.062	0.934 + 0.127*CL	1.232 + 0.117*CL	1.439 + 0.112*CL
	t_{PLH}	5.023	2.237 + 0.058*CL	2.419 + 0.052*CL	2.490 + 0.051*CL
	t_{PHL}	4.900	1.682 + 0.067*CL	1.860 + 0.061*CL	2.002 + 0.058*CL
	t_{PLZ}	0.879	0.879 + 0.000*CL	0.879 + 0.000*CL	0.879 + 0.000*CL
	t_{PHZ}	1.364	1.365 + 0.000*CL	1.364 + 0.000*CL	1.364 + 0.000*CL
EN to PAD	t_R	6.508	0.845 + 0.113*CL	0.841 + 0.113*CL	0.810 + 0.114*CL
	t_F	7.062	0.934 + 0.127*CL	1.232 + 0.117*CL	1.439 + 0.112*CL
	t_{PLH}	5.110	2.324 + 0.058*CL	2.507 + 0.052*CL	2.577 + 0.051*CL
	t_{PHL}	4.987	1.770 + 0.067*CL	1.948 + 0.061*CL	2.089 + 0.058*CL
	t_{PLZ}	0.965	0.965 + 0.000*CL	0.965 + 0.000*CL	0.965 + 0.000*CL
	t_{PHZ}	1.450	1.451 + 0.000*CL	1.450 + 0.000*CL	1.450 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmtot6sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.705	0.895 + 0.077*CL	0.971 + 0.075*CL	0.964 + 0.075*CL
	t_F	5.334	1.033 + 0.090*CL	1.348 + 0.080*CL	1.546 + 0.076*CL
	t_{PLH}	4.230	2.083 + 0.046*CL	2.322 + 0.038*CL	2.457 + 0.035*CL
	t_{PHL}	4.324	1.742 + 0.055*CL	2.030 + 0.046*CL	2.213 + 0.042*CL
TN to PAD	t_R	4.705	0.895 + 0.077*CL	0.971 + 0.075*CL	0.964 + 0.075*CL
	t_F	5.336	1.044 + 0.090*CL	1.353 + 0.080*CL	1.549 + 0.076*CL
	t_{PLH}	4.440	2.290 + 0.046*CL	2.530 + 0.038*CL	2.666 + 0.035*CL
	t_{PHL}	4.486	1.894 + 0.056*CL	2.188 + 0.046*CL	2.373 + 0.042*CL
	t_{PLZ}	0.879	0.879 + 0.000*CL	0.879 + 0.000*CL	0.879 + 0.000*CL
	t_{PHZ}	1.576	1.578 + 0.000*CL	1.576 + 0.000*CL	1.575 + 0.000*CL
EN to PAD	t_R	4.705	0.895 + 0.077*CL	0.971 + 0.075*CL	0.964 + 0.075*CL
	t_F	5.336	1.044 + 0.090*CL	1.353 + 0.080*CL	1.549 + 0.076*CL
	t_{PLH}	4.527	2.378 + 0.046*CL	2.618 + 0.038*CL	2.754 + 0.035*CL
	t_{PHL}	4.574	1.981 + 0.056*CL	2.275 + 0.046*CL	2.460 + 0.042*CL
	t_{PLZ}	0.966	0.966 + 0.000*CL	0.966 + 0.000*CL	0.966 + 0.000*CL
	t_{PHZ}	1.662	1.664 + 0.000*CL	1.662 + 0.000*CL	1.661 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phtot2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	14.466	0.656 + 0.279*CL	0.835 + 0.273*CL	1.162 + 0.266*CL
	t_F	13.843	1.144 + 0.261*CL	1.661 + 0.244*CL	2.035 + 0.236*CL
	t_{PLH}	7.098	1.093 + 0.120*CL	1.109 + 0.120*CL	1.127 + 0.119*CL
	t_{PHL}	6.936	1.072 + 0.120*CL	1.259 + 0.114*CL	1.385 + 0.111*CL
TN to PAD	t_R	14.466	0.658 + 0.279*CL	0.837 + 0.273*CL	1.160 + 0.266*CL
	t_F	13.844	1.146 + 0.261*CL	1.663 + 0.244*CL	2.036 + 0.236*CL
	t_{PLH}	7.313	1.303 + 0.120*CL	1.322 + 0.120*CL	1.341 + 0.119*CL
	t_{PHL}	7.082	1.209 + 0.120*CL	1.401 + 0.114*CL	1.530 + 0.111*CL
	t_{PLZ}	0.948	0.948 + 0.000*CL	0.948 + 0.000*CL	0.948 + 0.000*CL
	t_{PHZ}	1.271	1.271 + 0.000*CL	1.271 + 0.000*CL	1.270 + 0.000*CL
EN to PAD	t_R	14.466	0.658 + 0.279*CL	0.837 + 0.273*CL	1.160 + 0.266*CL
	t_F	13.844	1.146 + 0.261*CL	1.663 + 0.244*CL	2.036 + 0.236*CL
	t_{PLH}	7.401	1.390 + 0.120*CL	1.409 + 0.120*CL	1.427 + 0.119*CL
	t_{PHL}	7.170	1.297 + 0.120*CL	1.489 + 0.114*CL	1.617 + 0.111*CL
	t_{PLZ}	1.034	1.034 + 0.000*CL	1.034 + 0.000*CL	1.034 + 0.000*CL
	t_{PHZ}	1.357	1.357 + 0.000*CL	1.357 + 0.000*CL	1.357 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phtot4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.223	0.373 + 0.137*CL	0.390 + 0.137*CL	0.431 + 0.136*CL
	t_F	7.411	0.657 + 0.139*CL	0.971 + 0.129*CL	1.252 + 0.123*CL
	t_{PLH}	4.079	1.085 + 0.060*CL	1.094 + 0.060*CL	1.099 + 0.060*CL
	t_{PHL}	4.295	1.159 + 0.064*CL	1.250 + 0.061*CL	1.375 + 0.058*CL
TN to PAD	t_R	7.224	0.375 + 0.137*CL	0.391 + 0.137*CL	0.432 + 0.136*CL
	t_F	7.412	0.646 + 0.140*CL	0.974 + 0.129*CL	1.255 + 0.123*CL
	t_{PLH}	4.294	1.296 + 0.060*CL	1.306 + 0.060*CL	1.313 + 0.060*CL
	t_{PHL}	4.436	1.270 + 0.065*CL	1.381 + 0.061*CL	1.512 + 0.058*CL
	t_{PLZ}	1.061	1.062 + 0.000*CL	1.061 + 0.000*CL	1.061 + 0.000*CL
	t_{PHZ}	1.662	1.663 + 0.000*CL	1.662 + 0.000*CL	1.661 + 0.000*CL
EN to PAD	t_R	7.224	0.375 + 0.137*CL	0.391 + 0.137*CL	0.432 + 0.136*CL
	t_F	7.412	0.646 + 0.140*CL	0.974 + 0.129*CL	1.255 + 0.123*CL
	t_{PLH}	4.382	1.383 + 0.060*CL	1.394 + 0.060*CL	1.401 + 0.060*CL
	t_{PHL}	4.524	1.358 + 0.065*CL	1.468 + 0.061*CL	1.599 + 0.058*CL
	t_{PLZ}	1.147	1.147 + 0.000*CL	1.147 + 0.000*CL	1.147 + 0.000*CL
	t_{PHZ}	1.748	1.749 + 0.000*CL	1.748 + 0.000*CL	1.747 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phtot6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.848	0.357 + 0.090*CL	0.338 + 0.090*CL	0.334 + 0.090*CL
	t_F	5.231	0.561 + 0.096*CL	0.773 + 0.089*CL	0.992 + 0.085*CL
	t_{PLH}	3.156	1.144 + 0.041*CL	1.167 + 0.040*CL	1.172 + 0.040*CL
	t_{PHL}	3.527	1.285 + 0.046*CL	1.382 + 0.043*CL	1.472 + 0.041*CL
TN to PAD	t_R	4.849	0.360 + 0.089*CL	0.339 + 0.090*CL	0.334 + 0.090*CL
	t_F	5.235	0.515 + 0.098*CL	0.767 + 0.089*CL	0.998 + 0.085*CL
	t_{PLH}	3.372	1.352 + 0.041*CL	1.379 + 0.040*CL	1.385 + 0.040*CL
	t_{PHL}	3.659	1.346 + 0.048*CL	1.487 + 0.043*CL	1.592 + 0.041*CL
	t_{PLZ}	1.172	1.172 + 0.000*CL	1.172 + 0.000*CL	1.172 + 0.000*CL
	t_{PHZ}	2.053	2.055 + 0.000*CL	2.053 + 0.000*CL	2.052 + 0.000*CL
EN to PAD	t_R	4.849	0.360 + 0.089*CL	0.339 + 0.090*CL	0.334 + 0.090*CL
	t_F	5.235	0.515 + 0.098*CL	0.767 + 0.089*CL	0.998 + 0.085*CL
	t_{PLH}	3.459	1.440 + 0.041*CL	1.466 + 0.040*CL	1.473 + 0.040*CL
	t_{PHL}	3.746	1.433 + 0.048*CL	1.574 + 0.043*CL	1.680 + 0.041*CL
	t_{PLZ}	1.258	1.258 + 0.000*CL	1.258 + 0.000*CL	1.258 + 0.000*CL
	t_{PHZ}	2.139	2.141 + 0.000*CL	2.139 + 0.000*CL	2.138 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F =0.11ns, CL: Capacitive Load[pF])

phtot4sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.650	1.110 + 0.131*CL	1.099 + 0.131*CL	1.049 + 0.132*CL
	t_F	7.906	1.293 + 0.137*CL	1.647 + 0.125*CL	1.897 + 0.120*CL
	t_{PLH}	5.818	2.487 + 0.070*CL	2.717 + 0.062*CL	2.808 + 0.060*CL
	t_{PHL}	6.206	2.517 + 0.079*CL	2.883 + 0.066*CL	3.146 + 0.061*CL
TN to PAD	t_R	7.650	1.114 + 0.131*CL	1.101 + 0.131*CL	1.051 + 0.132*CL
	t_F	7.907	1.295 + 0.137*CL	1.649 + 0.125*CL	1.897 + 0.120*CL
	t_{PLH}	6.053	2.719 + 0.070*CL	2.950 + 0.062*CL	3.042 + 0.060*CL
	t_{PHL}	6.372	2.679 + 0.079*CL	3.046 + 0.067*CL	3.311 + 0.061*CL
	t_{PLZ}	1.095	1.095 + 0.000*CL	1.095 + 0.000*CL	1.095 + 0.000*CL
	t_{PHZ}	1.480	1.481 + 0.000*CL	1.480 + 0.000*CL	1.480 + 0.000*CL
EN to PAD	t_R	7.650	1.114 + 0.131*CL	1.101 + 0.131*CL	1.051 + 0.132*CL
	t_F	7.907	1.295 + 0.137*CL	1.649 + 0.125*CL	1.897 + 0.120*CL
	t_{PLH}	6.141	2.807 + 0.070*CL	3.038 + 0.062*CL	3.129 + 0.060*CL
	t_{PHL}	6.460	2.767 + 0.079*CL	3.134 + 0.067*CL	3.398 + 0.061*CL
	t_{PLZ}	1.181	1.182 + 0.000*CL	1.181 + 0.000*CL	1.181 + 0.000*CL
	t_{PHZ}	1.566	1.567 + 0.000*CL	1.566 + 0.000*CL	1.566 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phtot6sm

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.583	1.190 + 0.089*CL	1.286 + 0.086*CL	1.273 + 0.086*CL
	t_F	5.971	1.270 + 0.099*CL	1.611 + 0.087*CL	1.848 + 0.082*CL
	t_{PLH}	5.197	2.593 + 0.056*CL	2.905 + 0.046*CL	3.080 + 0.042*CL
	t_{PHL}	5.928	2.914 + 0.066*CL	3.339 + 0.052*CL	3.613 + 0.046*CL
TN to PAD	t_R	5.583	1.194 + 0.089*CL	1.288 + 0.086*CL	1.274 + 0.086*CL
	t_F	5.972	1.271 + 0.099*CL	1.612 + 0.087*CL	1.848 + 0.082*CL
	t_{PLH}	5.433	2.828 + 0.056*CL	3.139 + 0.046*CL	3.315 + 0.042*CL
	t_{PHL}	6.094	3.077 + 0.066*CL	3.503 + 0.052*CL	3.778 + 0.046*CL
	t_{PLZ}	1.094	1.094 + 0.000*CL	1.094 + 0.000*CL	1.094 + 0.000*CL
	t_{PHZ}	1.722	1.724 + 0.000*CL	1.722 + 0.000*CL	1.722 + 0.000*CL
EN to PAD	t_R	5.583	1.194 + 0.089*CL	1.287 + 0.086*CL	1.274 + 0.086*CL
	t_F	5.972	1.271 + 0.099*CL	1.612 + 0.087*CL	1.848 + 0.082*CL
	t_{PLH}	5.520	2.915 + 0.056*CL	3.227 + 0.046*CL	3.403 + 0.042*CL
	t_{PHL}	6.181	3.165 + 0.066*CL	3.591 + 0.052*CL	3.865 + 0.046*CL
	t_{PLZ}	1.180	1.181 + 0.000*CL	1.180 + 0.000*CL	1.180 + 0.000*CL
	t_{PHZ}	1.808	1.810 + 0.000*CL	1.808 + 0.000*CL	1.808 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

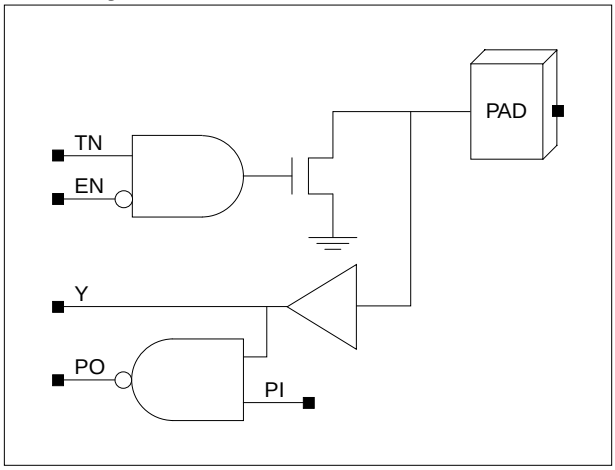
BI-DIRECTIONAL BUFFERS

Cell List

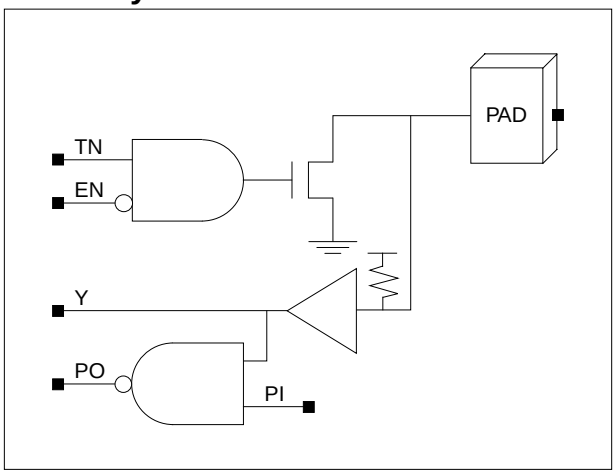
Cell Name	Function Description
PMBaDyz	2.5V Open-Drain Bi-Directional Buffers
PMBaUDyz	2.5V Open-Drain Bi-Directional Buffers with Pull-Up
PHBaDyz	3.3V Open-Drain Bi-Directional Buffers
PHBaUDyz	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PMTBaDyz	5V-Tolerant for 2.5V Open-Drain Bi-Directional Buffers
PMTBaUDyz	5V-Tolerant for 2.5V Open-Drain Bi-Directional Buffers with Pull-Up
PHTBaDyz	5V-Tolerant for 3.3V Open-Drain Bi-Directional Buffers
PHTBaUDyz	5V-Tolerant for 3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PMBaTyz	2.5V Tri-State Bi-Directional Buffers
PMBaDTyz	2.5V Tri-State Bi-Directional Buffers with Pull-Down
PMBaUTyz	2.5V Tri-State Bi-Directional Buffers with Pull-Up
PHBaTyz	3.3V Tri-State Bi-Directional Buffers
PHBaDTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PMTBaTyz	5V-Tolerant for 2.5V Tri-State Bi-Directional Buffers
PMTBaDTyz	5V-Tolerant for 2.5V Tri-State Bi-Directional Buffers with Pull-Down
PMTBaUTyz	5V-Tolerant for 2.5V Tri-State Bi-Directional Buffers with Pull-Up
PHTBaTyz	5V-Tolerant for 3.3V Tri-State Bi-Directional Buffers
PHTBaDTyz	5V-Tolerant for 3.3V Tri-State Bi-Directional Buffers with Pull-Down
PHTBaUTyz	5V-Tolerant for 3.3V Tri-State Bi-Directional Buffers with Pull-Up

Open Drain Bi-Directional Buffers

PvBaDyz

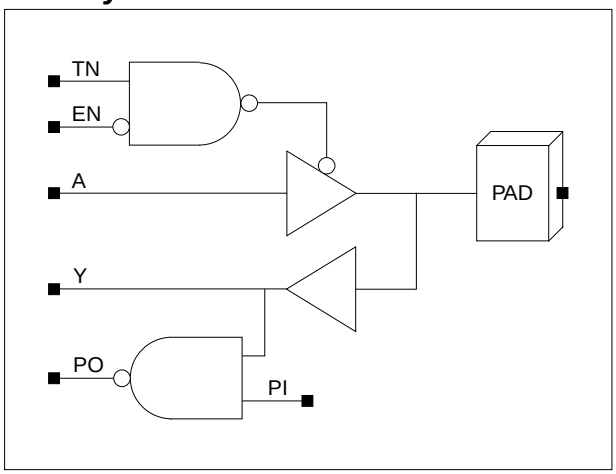


PvBaUDyz

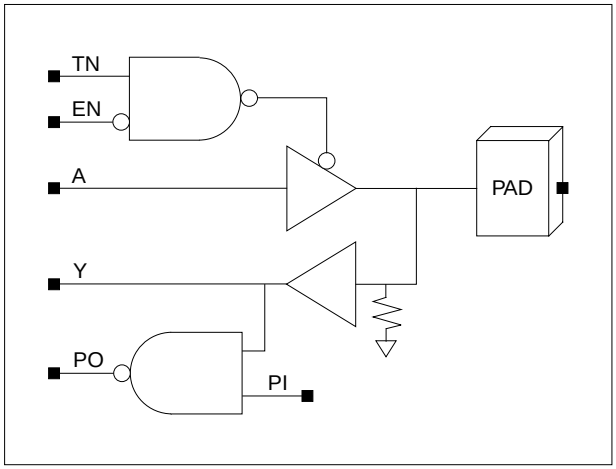


Tri-State Bi-Directional Buffers

PvBaTyz



PvBaDTyz



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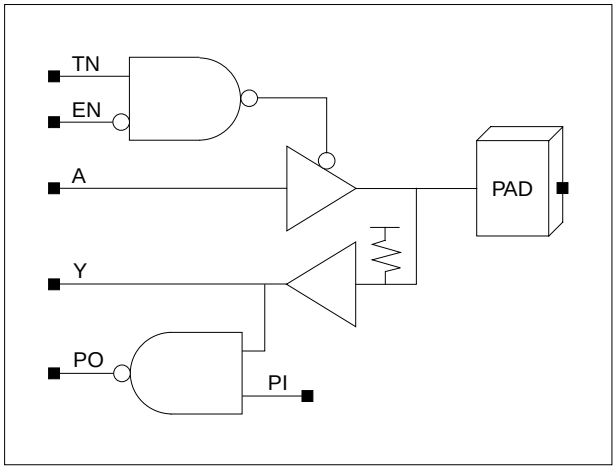


OSCILLATORS

DC Electrical Characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Vih	High level input voltage		0.8×Vdd		Vdd	V
Vil	Low level input voltage		Vss		0.2×Vdd	V
Iih	High level input current	Vin=Vdd	–10		10	µA
Iil	Low level input current	Vin=Vss	–10		10	µA
Cin	Input capacitance				5	pF
Cout	Output capacitance				5	pF

Cell List

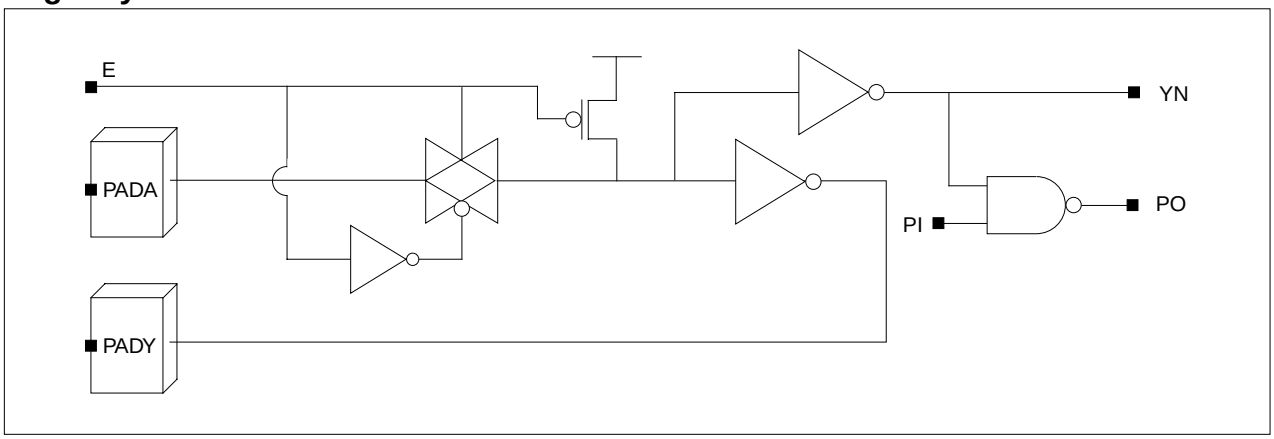
Cell Name	Function Description
phsosck1	3.3V Interface Oscillator Cell with Enable (~ 100kHz)
phsosck17	3.3V Interface Oscillator Cell with Enable and Feedback Resistor 10MΩ (~ 100kHz)
phsoscm1	3.3V Interface Oscillator Cell with Enable (1M ~ 10MHz)
phsoscm2	3.3V Interface Oscillator Cell with Enable (10M ~ 40MHz)
phsoscm3	3.3V Interface Oscillator Cell with Enable (40M ~ 100MHz)
phsoscm16	3.3V Interface Oscillator Cell with Enable and Feedback Resistor 1MΩ (1M ~ 10MHz)
phsoscm26	3.3V Interface Oscillator Cell with Enable and Feedback Resistor 1MΩ (10M ~ 40MHz)
phsoscm36	3.3V Interface Oscillator Cell with Enable and Feedback Resistor 1MΩ (40M ~ 100MHz)

Cell Name	Function Description
pmsosck1	2.5V Interface Oscillator Cell with Enable (~ 100kHz)
pmsoscm1	2.5V Interface Oscillator Cell with Enable (1M ~ 10MHz)
pmsoscm2	2.5V Interface Oscillator Cell with Enable (10M ~ 40MHz)

PHSOSCK1/M1/M2/M3

3.3V Interface Oscillator Cell with Enable

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
phsosck1	*phsoscm1/m2/m3*	*phsosck1*	*phsoscm1/m2/m3*
E	E		
12.57	12.57	2 I/O Slots	2 I/O Slots

Switching Characteristics

phsosck1

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	3059.500	55.250 + 60.085*CL	55.100 + 60.088*CL	55.400 + 60.084*CL
	t_F	2017.000	36.750 + 39.605*CL	36.800 + 39.604*CL	36.800 + 39.604*CL
	t_{PLH}	1298.900	25.325 + 25.471*CL	25.100 + 25.476*CL	25.100 + 25.476*CL
	t_{PHL}	944.450	19.025 + 18.508*CL	18.950 + 18.510*CL	18.800 + 18.512*CL
E to PADY	t_R	3059.500	55.250 + 60.085*CL	55.300 + 60.084*CL	55.000 + 60.088*CL
	t_F	2017.000	36.750 + 39.605*CL	36.800 + 39.604*CL	36.500 + 39.608*CL
	t_{PLH}	1299.100	25.350 + 25.475*CL	25.500 + 25.472*CL	25.200 + 25.476*CL
	t_{PHL}	945.270	19.820 + 18.509*CL	19.810 + 18.509*CL	19.600 + 18.512*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.188	0.165 + 0.010*SL	0.163 + 0.012*SL	0.155 + 0.013*SL
	t_F	0.141	0.117 + 0.013*SL	0.118 + 0.012*SL	0.121 + 0.012*SL
	t_{PLH}	18.403	18.386 + 0.010*SL	18.388 + 0.007*SL	18.416 + 0.006*SL
	t_{PHL}	13.643	13.626 + 0.010*SL	13.628 + 0.008*SL	13.662 + 0.006*SL
E to YN	t_R	0.189	0.164 + 0.013*SL	0.165 + 0.012*SL	0.154 + 0.013*SL
	t_F	0.141	0.114 + 0.016*SL	0.118 + 0.012*SL	0.121 + 0.012*SL
	t_{PLH}	19.284	19.267 + 0.010*SL	19.269 + 0.007*SL	19.299 + 0.006*SL
	t_{PHL}	14.242	14.224 + 0.012*SL	14.227 + 0.008*SL	14.261 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm1

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	22.422	0.505 + 0.438*CL	0.492 + 0.439*CL	0.492 + 0.439*CL
	t_F	21.809	0.464 + 0.427*CL	0.457 + 0.427*CL	0.457 + 0.427*CL
	t_{PLH}	10.617	0.986 + 0.193*CL	0.971 + 0.193*CL	0.959 + 0.193*CL
	t_{PHL}	11.731	0.953 + 0.216*CL	0.937 + 0.216*CL	0.931 + 0.216*CL
E to PADY	t_R	22.422	0.492 + 0.439*CL	0.492 + 0.439*CL	0.492 + 0.439*CL
	t_F	21.833	0.488 + 0.427*CL	0.481 + 0.427*CL	0.481 + 0.427*CL
	t_{PLH}	10.688	1.027 + 0.193*CL	1.026 + 0.193*CL	1.029 + 0.193*CL
	t_{PHL}	12.283	1.483 + 0.216*CL	1.479 + 0.216*CL	1.479 + 0.216*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.154	0.114 + 0.020*SL	0.113 + 0.020*SL	0.095 + 0.021*SL
	t_F	0.144	0.107 + 0.020*SL	0.108 + 0.018*SL	0.091 + 0.019*SL
	t_{PLH}	1.179	1.158 + 0.012*SL	1.160 + 0.010*SL	1.170 + 0.009*SL
	t_{PHL}	0.755	0.732 + 0.014*SL	0.735 + 0.010*SL	0.751 + 0.009*SL
E to YN	t_R	0.155	0.114 + 0.021*SL	0.114 + 0.020*SL	0.095 + 0.021*SL
	t_F	0.142	0.108 + 0.016*SL	0.106 + 0.018*SL	0.090 + 0.019*SL
	t_{PLH}	1.548	1.527 + 0.012*SL	1.529 + 0.010*SL	1.538 + 0.009*SL
	t_{PHL}	1.447	1.424 + 0.014*SL	1.427 + 0.010*SL	1.443 + 0.009*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm2

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	5.034	0.787 + 0.085*CL	0.612 + 0.088*CL	0.456 + 0.091*CL
	t_F	5.328	0.718 + 0.092*CL	0.525 + 0.096*CL	0.353 + 0.098*CL
	t_{PLH}	3.052	1.048 + 0.040*CL	1.033 + 0.040*CL	1.013 + 0.041*CL
	t_{PHL}	3.387	0.981 + 0.048*CL	0.951 + 0.049*CL	0.928 + 0.049*CL
E to PADY	t_R	4.813	0.211 + 0.092*CL	0.179 + 0.093*CL	0.160 + 0.093*CL
	t_F	5.827	1.254 + 0.091*CL	1.120 + 0.094*CL	0.975 + 0.096*CL
	t_{PLH}	3.139	1.086 + 0.041*CL	1.086 + 0.041*CL	1.085 + 0.041*CL
	t_{PHL}	5.881	3.295 + 0.052*CL	3.398 + 0.050*CL	3.434 + 0.049*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.089	0.081 + 0.003*SL	0.081 + 0.004*SL	0.084 + 0.004*SL
	t_F	0.079	0.068 + 0.006*SL	0.069 + 0.005*SL	0.072 + 0.004*SL
	t_{PLH}	1.305	1.298 + 0.004*SL	1.299 + 0.003*SL	1.313 + 0.002*SL
	t_{PHL}	0.936	0.929 + 0.004*SL	0.930 + 0.003*SL	0.945 + 0.002*SL
E to YN	t_R	0.090	0.082 + 0.004*SL	0.082 + 0.004*SL	0.084 + 0.004*SL
	t_F	0.077	0.068 + 0.004*SL	0.067 + 0.005*SL	0.071 + 0.005*SL
	t_{PLH}	1.664	1.658 + 0.004*SL	1.659 + 0.003*SL	1.673 + 0.002*SL
	t_{PHL}	3.155	3.148 + 0.004*SL	3.148 + 0.003*SL	3.163 + 0.003*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm3

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	2.075	0.970 + 0.022*CL	0.946 + 0.023*CL	0.897 + 0.023*CL
	t_F	2.121	0.950 + 0.023*CL	0.918 + 0.024*CL	0.850 + 0.025*CL
	t_{PLH}	1.786	1.028 + 0.015*CL	1.136 + 0.013*CL	1.205 + 0.012*CL
	t_{PHL}	1.869	1.025 + 0.017*CL	1.133 + 0.015*CL	1.185 + 0.014*CL
E to PADY	t_R	1.623	0.346 + 0.026*CL	0.347 + 0.026*CL	0.335 + 0.026*CL
	t_F	5.424	3.961 + 0.029*CL	4.070 + 0.027*CL	4.173 + 0.026*CL
	t_{PLH}	1.969	1.296 + 0.013*CL	1.341 + 0.013*CL	1.373 + 0.012*CL
	t_{PHL}	9.751	8.403 + 0.027*CL	8.577 + 0.023*CL	8.742 + 0.021*CL

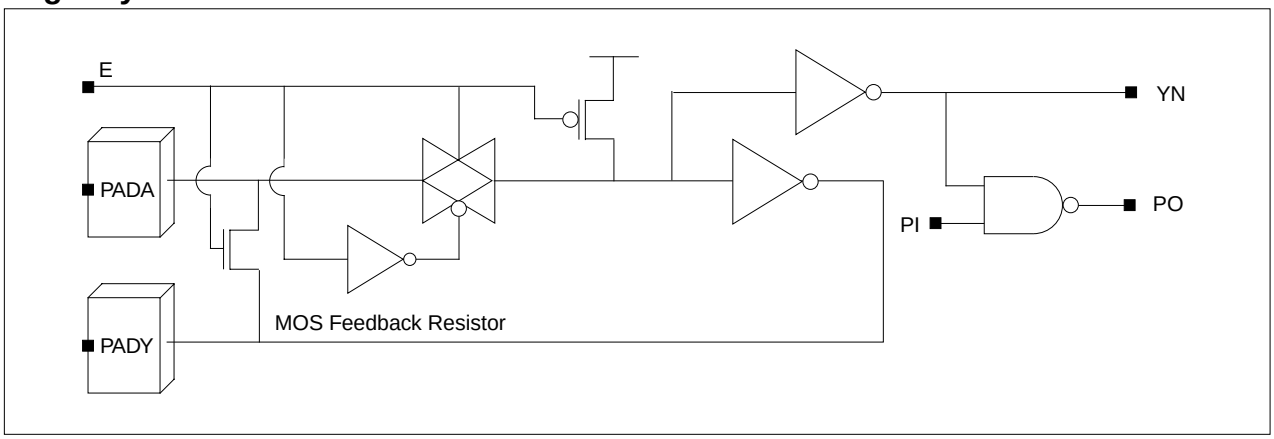
*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.084	0.075 + 0.005*SL	0.076 + 0.004*SL	0.079 + 0.004*SL
	t_F	0.075	0.065 + 0.006*SL	0.066 + 0.005*SL	0.068 + 0.005*SL
	t_{PLH}	1.323	1.317 + 0.004*SL	1.318 + 0.003*SL	1.331 + 0.002*SL
	t_{PHL}	1.236	1.228 + 0.004*SL	1.229 + 0.003*SL	1.243 + 0.002*SL
E to YN	t_R	0.082	0.074 + 0.003*SL	0.073 + 0.004*SL	0.077 + 0.004*SL
	t_F	0.078	0.069 + 0.005*SL	0.069 + 0.005*SL	0.072 + 0.005*SL
	t_{PLH}	1.669	1.663 + 0.003*SL	1.664 + 0.003*SL	1.678 + 0.002*SL
	t_{PHL}	8.877	8.869 + 0.004*SL	8.870 + 0.003*SL	8.885 + 0.002*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
phsosck17	*phsoscm16/m26/m36*	*phsosck17*	*phsoscm16/m26/m36*
E	E		
12.57	12.57	2 I/O Slots	2 I/O Slots

Switching Characteristics

phsosck17

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	3128.700	70.950 + 61.155*CL	74.300 + 61.088*CL	76.400 + 61.060*CL
	t_F	2044.300	44.300 + 40.000*CL	44.500 + 39.996*CL	45.100 + 39.988*CL
	t_{PLH}	1300.600	29.675 + 25.419*CL	28.400 + 25.444*CL	27.200 + 25.460*CL
	t_{PHL}	936.190	20.390 + 18.316*CL	19.370 + 18.336*CL	18.500 + 18.348*CL
E to PADY	t_R	3118.400	53.400 + 61.300*CL	58.000 + 61.208*CL	64.600 + 61.120*CL
	t_F	2016.900	36.900 + 39.600*CL	36.700 + 39.604*CL	36.700 + 39.604*CL
	t_{PLH}	1292.500	22.375 + 25.403*CL	17.300 + 25.504*CL	12.800 + 25.564*CL
	t_{PHL}	938.940	21.890 + 18.341*CL	21.820 + 18.342*CL	22.000 + 18.340*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.189	0.164 + 0.013*SL	0.165 + 0.012*SL	0.154 + 0.013*SL
	t_F	0.141	0.115 + 0.015*SL	0.117 + 0.012*SL	0.122 + 0.012*SL
	t_{PLH}	18.470	18.453 + 0.010*SL	18.455 + 0.007*SL	18.485 + 0.006*SL
	t_{PHL}	13.706	13.689 + 0.010*SL	13.691 + 0.008*SL	13.724 + 0.006*SL
E to YN	t_R	0.189	0.164 + 0.013*SL	0.165 + 0.012*SL	0.154 + 0.013*SL
	t_F	0.141	0.114 + 0.016*SL	0.118 + 0.012*SL	0.121 + 0.012*SL
	t_{PLH}	20.187	20.170 + 0.010*SL	20.172 + 0.007*SL	20.202 + 0.006*SL
	t_{PHL}	15.256	15.238 + 0.012*SL	15.241 + 0.008*SL	15.275 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm16

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	22.481	0.541 + 0.439*CL	0.529 + 0.439*CL	0.529 + 0.439*CL
	t_F	21.863	0.498 + 0.427*CL	0.495 + 0.427*CL	0.492 + 0.427*CL
	t_{PLH}	10.682	1.045 + 0.193*CL	1.030 + 0.193*CL	1.018 + 0.193*CL
	t_{PHL}	11.783	1.000 + 0.216*CL	0.985 + 0.216*CL	0.982 + 0.216*CL
E to PADY	t_R	22.483	0.530 + 0.439*CL	0.531 + 0.439*CL	0.534 + 0.439*CL
	t_F	21.833	0.488 + 0.427*CL	0.479 + 0.427*CL	0.482 + 0.427*CL
	t_{PLH}	10.997	1.324 + 0.193*CL	1.327 + 0.193*CL	1.327 + 0.193*CL
	t_{PHL}	12.556	1.757 + 0.216*CL	1.756 + 0.216*CL	1.753 + 0.216*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.154	0.112 + 0.022*SL	0.114 + 0.020*SL	0.095 + 0.021*SL
	t_F	0.144	0.106 + 0.020*SL	0.108 + 0.018*SL	0.091 + 0.019*SL
	t_{PLH}	1.223	1.202 + 0.012*SL	1.204 + 0.010*SL	1.214 + 0.009*SL
	t_{PHL}	0.794	0.771 + 0.014*SL	0.774 + 0.010*SL	0.790 + 0.009*SL
E to YN	t_R	0.154	0.112 + 0.022*SL	0.114 + 0.020*SL	0.095 + 0.021*SL
	t_F	0.142	0.104 + 0.021*SL	0.107 + 0.018*SL	0.091 + 0.019*SL
	t_{PLH}	1.823	1.802 + 0.012*SL	1.804 + 0.010*SL	1.814 + 0.009*SL
	t_{PHL}	1.711	1.688 + 0.013*SL	1.691 + 0.010*SL	1.707 + 0.009*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm26

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	5.046	0.798 + 0.085*CL	0.623 + 0.088*CL	0.465 + 0.091*CL
	t_F	5.339	0.722 + 0.092*CL	0.531 + 0.096*CL	0.361 + 0.098*CL
	t_{PLH}	3.083	1.075 + 0.040*CL	1.062 + 0.040*CL	1.043 + 0.041*CL
	t_{PHL}	3.411	1.003 + 0.048*CL	0.974 + 0.049*CL	0.952 + 0.049*CL
E to PADY	t_R	4.831	0.234 + 0.092*CL	0.199 + 0.093*CL	0.176 + 0.093*CL
	t_F	5.827	1.254 + 0.091*CL	1.119 + 0.094*CL	0.976 + 0.096*CL
	t_{PLH}	3.435	1.380 + 0.041*CL	1.381 + 0.041*CL	1.380 + 0.041*CL
	t_{PHL}	6.160	3.574 + 0.052*CL	3.677 + 0.050*CL	3.713 + 0.049*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.088	0.080 + 0.003*SL	0.079 + 0.004*SL	0.083 + 0.004*SL
	t_F	0.079	0.069 + 0.005*SL	0.070 + 0.005*SL	0.072 + 0.005*SL
	t_{PLH}	1.329	1.323 + 0.003*SL	1.324 + 0.003*SL	1.338 + 0.002*SL
	t_{PHL}	0.959	0.952 + 0.004*SL	0.953 + 0.003*SL	0.968 + 0.002*SL
E to YN	t_R	0.089	0.080 + 0.005*SL	0.081 + 0.004*SL	0.084 + 0.004*SL
	t_F	0.077	0.067 + 0.006*SL	0.068 + 0.005*SL	0.072 + 0.005*SL
	t_{PLH}	1.947	1.941 + 0.004*SL	1.942 + 0.003*SL	1.956 + 0.002*SL
	t_{PHL}	3.435	3.427 + 0.004*SL	3.428 + 0.003*SL	3.443 + 0.003*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

phsoscm36

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	2.084	0.979 + 0.022*CL	0.955 + 0.023*CL	0.906 + 0.023*CL
	t_F	2.124	0.951 + 0.023*CL	0.919 + 0.024*CL	0.852 + 0.025*CL
	t_{PLH}	1.803	1.045 + 0.015*CL	1.153 + 0.013*CL	1.220 + 0.012*CL
	t_{PHL}	1.883	1.040 + 0.017*CL	1.145 + 0.015*CL	1.197 + 0.014*CL
E to PADY	t_R	1.636	0.360 + 0.026*CL	0.360 + 0.026*CL	0.349 + 0.026*CL
	t_F	5.424	3.961 + 0.029*CL	4.070 + 0.027*CL	4.173 + 0.026*CL
	t_{PLH}	2.232	1.558 + 0.013*CL	1.602 + 0.013*CL	1.635 + 0.012*CL
	t_{PHL}	10.026	8.678 + 0.027*CL	8.852 + 0.023*CL	9.017 + 0.021*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

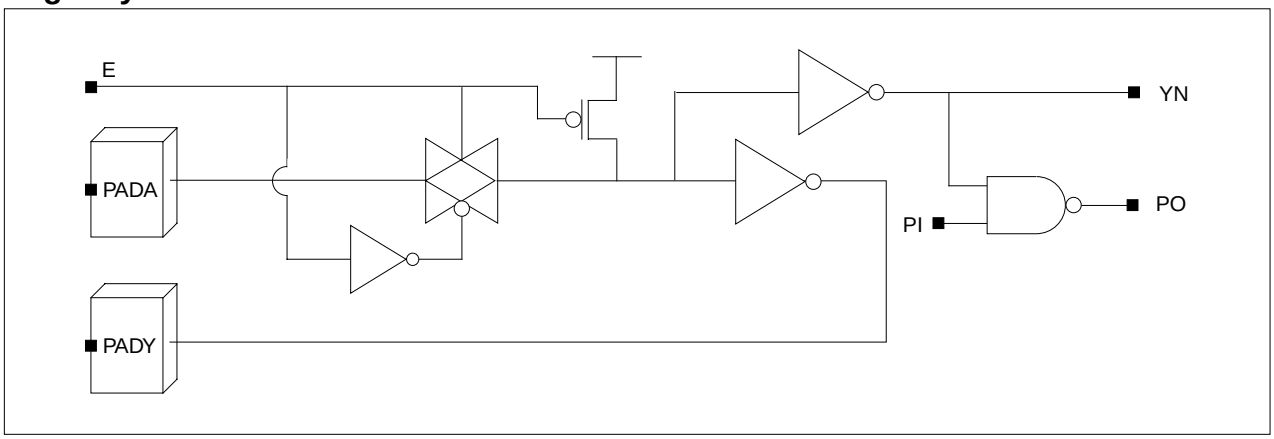
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.084	0.075 + 0.004*SL	0.075 + 0.004*SL	0.079 + 0.004*SL
	t_F	0.075	0.065 + 0.006*SL	0.066 + 0.005*SL	0.068 + 0.005*SL
	t_{PLH}	1.340	1.334 + 0.004*SL	1.335 + 0.003*SL	1.348 + 0.002*SL
	t_{PHL}	1.254	1.247 + 0.004*SL	1.248 + 0.003*SL	1.262 + 0.002*SL
E to YN	t_R	0.084	0.075 + 0.005*SL	0.076 + 0.004*SL	0.079 + 0.004*SL
	t_F	0.079	0.068 + 0.006*SL	0.069 + 0.005*SL	0.072 + 0.004*SL
	t_{PLH}	1.931	1.925 + 0.003*SL	1.926 + 0.003*SL	1.939 + 0.002*SL
	t_{PHL}	9.151	9.144 + 0.004*SL	9.145 + 0.003*SL	9.159 + 0.002*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

PMSOSCK1/M1/M2

2.5V Interface Oscillator Cell with Enable

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
pmsosck1	*pmsoscm1/m2*	*pmsosck1*	*pmsoscm1/m2*
E	E		
12.57	12.57	2 I/O Slots	2 I/O Slots

Switching Characteristics

pmsosck1

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	3635.200	71.450 + 71.275*CL	71.600 + 71.272*CL	71.300 + 71.276*CL
	t_F	2534.200	48.200 + 49.720*CL	48.200 + 49.720*CL	48.200 + 49.720*CL
	t_{PLH}	1528.100	30.625 + 29.950*CL	30.500 + 29.952*CL	30.500 + 29.952*CL
	t_{PHL}	1163.200	25.175 + 22.761*CL	25.200 + 22.760*CL	25.200 + 22.760*CL
E to PADY	t_R	3635.200	71.450 + 71.275*CL	71.600 + 71.272*CL	71.300 + 71.276*CL
	t_F	2534.200	48.200 + 49.720*CL	48.200 + 49.720*CL	48.200 + 49.720*CL
	t_{PLH}	1528.200	30.600 + 29.952*CL	30.600 + 29.952*CL	30.900 + 29.948*CL
	t_{PHL}	1163.900	25.925 + 22.760*CL	25.900 + 22.760*CL	25.900 + 22.760*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.188	0.164 + 0.011*SL	0.163 + 0.012*SL	0.154 + 0.013*SL
	t_F	0.140	0.112 + 0.017*SL	0.117 + 0.012*SL	0.121 + 0.012*SL
	t_{PLH}	20.564	20.547 + 0.010*SL	20.549 + 0.007*SL	20.579 + 0.006*SL
	t_{PHL}	14.475	14.457 + 0.012*SL	14.460 + 0.008*SL	14.494 + 0.006*SL
E to YN	t_R	0.188	0.163 + 0.013*SL	0.164 + 0.012*SL	0.154 + 0.013*SL
	t_F	0.140	0.114 + 0.014*SL	0.116 + 0.012*SL	0.121 + 0.012*SL
	t_{PLH}	21.434	21.417 + 0.010*SL	21.419 + 0.007*SL	21.449 + 0.006*SL
	t_{PHL}	14.838	14.820 + 0.012*SL	14.823 + 0.008*SL	14.857 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

pmsoscm1

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	19.992	0.519 + 0.389*CL	0.476 + 0.390*CL	0.476 + 0.390*CL
	t_F	16.446	0.403 + 0.321*CL	0.378 + 0.321*CL	0.381 + 0.321*CL
	t_{PLH}	9.362	1.010 + 0.167*CL	0.995 + 0.167*CL	0.987 + 0.167*CL
	t_{PHL}	9.339	1.065 + 0.165*CL	1.056 + 0.166*CL	1.051 + 0.166*CL
E to PADY	t_R	19.993	0.476 + 0.390*CL	0.479 + 0.390*CL	0.476 + 0.390*CL
	t_F	16.479	0.429 + 0.321*CL	0.415 + 0.321*CL	0.412 + 0.321*CL
	t_{PLH}	9.385	1.008 + 0.168*CL	1.008 + 0.168*CL	1.004 + 0.168*CL
	t_{PHL}	9.749	1.461 + 0.166*CL	1.460 + 0.166*CL	1.459 + 0.166*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.152	0.112 + 0.020*SL	0.112 + 0.020*SL	0.094 + 0.021*SL
	t_F	0.142	0.107 + 0.018*SL	0.107 + 0.018*SL	0.090 + 0.019*SL
	t_{PLH}	1.184	1.163 + 0.012*SL	1.165 + 0.010*SL	1.175 + 0.009*SL
	t_{PHL}	0.873	0.850 + 0.013*SL	0.853 + 0.010*SL	0.868 + 0.009*SL
E to YN	t_R	0.152	0.112 + 0.021*SL	0.112 + 0.020*SL	0.094 + 0.021*SL
	t_F	0.142	0.108 + 0.017*SL	0.107 + 0.018*SL	0.090 + 0.019*SL
	t_{PLH}	1.497	1.476 + 0.012*SL	1.478 + 0.010*SL	1.488 + 0.009*SL
	t_{PHL}	1.462	1.440 + 0.013*SL	1.442 + 0.010*SL	1.458 + 0.009*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

Switching Characteristics

pmsoscm2

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	5.470	0.737 + 0.095*CL	0.579 + 0.098*CL	0.429 + 0.100*CL
	t_F	4.498	0.673 + 0.077*CL	0.489 + 0.080*CL	0.325 + 0.082*CL
	t_{PLH}	3.217	1.065 + 0.043*CL	1.052 + 0.043*CL	1.035 + 0.044*CL
	t_{PHL}	3.242	1.104 + 0.043*CL	1.089 + 0.043*CL	1.076 + 0.043*CL
E to PADY	t_R	5.278	0.225 + 0.101*CL	0.193 + 0.102*CL	0.174 + 0.102*CL
	t_F	5.010	1.202 + 0.076*CL	1.091 + 0.078*CL	0.965 + 0.080*CL
	t_{PLH}	3.262	1.067 + 0.044*CL	1.068 + 0.044*CL	1.068 + 0.044*CL
	t_{PHL}	5.521	3.179 + 0.047*CL	3.303 + 0.044*CL	3.359 + 0.044*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.2V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.087	0.078 + 0.005*SL	0.079 + 0.004*SL	0.081 + 0.004*SL
	t_F	0.079	0.069 + 0.005*SL	0.070 + 0.005*SL	0.070 + 0.005*SL
	t_{PLH}	1.285	1.279 + 0.004*SL	1.280 + 0.003*SL	1.293 + 0.002*SL
	t_{PHL}	1.023	1.016 + 0.004*SL	1.017 + 0.003*SL	1.031 + 0.002*SL
E to YN	t_R	0.086	0.077 + 0.004*SL	0.078 + 0.004*SL	0.081 + 0.004*SL
	t_F	0.079	0.069 + 0.005*SL	0.070 + 0.005*SL	0.071 + 0.005*SL
	t_{PLH}	1.575	1.569 + 0.004*SL	1.569 + 0.003*SL	1.583 + 0.002*SL
	t_{PHL}	2.963	2.956 + 0.004*SL	2.957 + 0.003*SL	2.971 + 0.002*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 20, *Group3 : 20 < SL

PCI BUFFERS

Overview

PCI buffers are designed for PCI local bus application which is intended for high-performance 32-bit or 64-bit bus architecture.

SEC supports PCI-X input, output and bi-directional buffers for 3.3V and 5V signalling environment.

Features

— Input, output, and bi-directional PCI-X buffers
— PCI-X addendum to the PCI local bus specification compliant
— Operating at up to 133MHz
— Electrically compliant interface in 3.3V and 5V bus environments

Description

Since the introduction of 66MHz timing parameter of the PCI local bus specification in 1994, bandwidth requirements of peripheral devices have steadily grown. PCI-X enable the design old systems and devices that can operate at speeds significantly higher than today's specification allows. Devices can be designed to meet PCI-X requirements and operate as conventional 33MHz and 66MHz PCI devices when installed in those systems.

These PCI-X buffers are designed for 3.3V and 5V environments and compliant with the PCI local bus specification Rev2.2 when they are used in PCI mode. The 5V tolerant PCI mode buffers can be used for 33MHz, 5V environment. These tolerant PCI mode buffers require 5V power for bulk of PMOS driver for 5V bus environment or 3.3V power for 3.3V environment. The PCI-X buffers support PCI mode while SEL=high, Although tolerant PCI buffers support 5V environment, they do not drive 5V.

NOTE: If you want to use PCI buffers, please contact Samsung.

Cell List

Cell Name	Description	Operating Frequency	VIO(note2) Voltage	Operating Voltage	Note
ptbpcix	Bi-direction	Up to 133MHz at PCI-X mode	3.3V	3.3V	1
		Up to 66MHz at 3.3V signaling of PCI mode	3.3V	3.3V	2,3
		Up to 33MHz at 5.0V signaling of PCI mode	5V	3.3	2,3
ptopcix	Driver	Up to 133MHz at PCI-X mode	3.3V	3.3V	1
		Up to 66MHz at 3.3V signaling of PCI mode	3.3V	3.3V	2,3
		Up to 33MHz at 5.0V signaling of PCI mode	5V	3.3	2,3
ptipcix	Receiver	Up to 133MHz at PCI-X mode	3.3V	3.3V	1
		Up to 66MHz at 3.3V signaling of PCI mode	3.3V	3.3V	2,3
		Up to 33MHz at 5.0V signaling of PCI mode	5V	3.3	2,3

NOTES:
1. PCI-X mode condition: SEL = low
2. 3.3V signalling PCI mode condition: SEL = high, VIO = 3.3V (In this case 5V tolerant is not supported)
5.0V signalling PCI mode condition: SEL = high, VIO = 5.0V
3. In 3.3V signalling, the voltage of VIO is 3.3V, which is provided through the VDD5O_PCI power cell
In 5.0V signalling, the voltage of VIO is 3.3V, which is provided through the VDD5O_PCI power cell

Power/Slot Cell Name	Description
vdd1ih_pci	1.2V power cell for internal core and PCI-X I/Os
vdd3op_pci	3.3V power cell for PCI-X I/Os
vdd5o_pci	V_{IO} (3.3V or 5V) power cell for PCI-X I/Os
vss3i_pci	Gnd power cell for internal core;nor used for PCI-X I/Os
vss3op_pci	Gnd power cell for PCI-X I/Os
ev1ih_pci	1.2V ESD protection slot cell for internal core and PCI-X I/Os
ev3op_pci	3.3V ESD protection slot cell for PCI-X I/Os

Electrical Characteristics

DC Characteristics of PCI-X Mode (SEL = low)

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6		3.0	3.6	V
V_{IO}	V_{IO} Voltage		V_{CC}			4.75	5.25	V
V_{ih}	Input High Voltage		$0.5V_{CC}$	V_{CC}+0.5		1.9	V_{IO}+0.5	V
V_{il}	Input Low Voltage		–0.5	$0.35V_{CC}$		–0.5	0.9	V
I_i	Input Leakage Current	$0 < V_{IN} < V_{CC}$	–10	10	$0 < V_{IN} < V_{IO}$	–70	70	µA
V_{oh}	Output High Voltage	I_{OUT} = –500µA	$0.9V_{CC}$	–	I_{OUT} = –2mA	2.4	–	V
V_{ol}	Output Low Voltage	I_{OUT} = 1500µA	–	$0.1V_{CC}$	I_{OUT} = 6mA	–	0.55	V

AC Characteristics of PCI-X Mode (SEL = low)

Symbol	Parameter	Condition	Min	Max	Unit
$I_{oh\ (AC)}$	Switching Current High	$0 < V_{CC}–V_{OUT} \le 3.6V$		$–74(V_{CC}–V_{OUT})$	mA
		$0 < V_{CC}–V_{OUT} \le 1.2V$	$–32(V_{CC}–V_{OUT})$		
		$1.2V < V_{CC}–V_{OUT} \le 1.9V$	$–11(V_{CC}–V_{OUT}) –25.2$		
		$1.9V < V_{CC}–V_{OUT} \le 3.6V$	$–1.8(V_{CC}–V_{OUT}) –42.7$		
$I_{ol\ (AC)}$	Switching Current Low	$0 \le V_{OUT} \le 3.6V$		$100V_{OUT}$	mA
		$0 < V_{OUT} \le 1.3V$	$48V_{OUT}$		
		$1.3V < V_{OUT} \le 3.6V$	$5.7V_{OUT} + 55$		
I_{cl}	Low Current Low	$0 < V_{CC}–V_{OUT} \le 3.6V$	$–40 + (V_{IN}+1)/0.005$		mA
		$–0.8875V < V_{IN} \le –0.625V$	$–25 + (V_{IN}+1)/0.015$		
I_{ch}	High Clamp Current	$0.8875V \le V_{IN}–V_{CC} < 4V$	$40 + (V_{IN}–V_{CC}–1)/0.005$		mA
		$0.625V < V_{IN}–V_{CC} < 0.8875V$	$25 + (V_{IN}–V_{CC}–1)/0.015$		
T_r	Output Rise Time	$PAD(0.3V_{CC})$ to $PAD(0.6V_{CC})$	1.0	6.0	V/ns
T_f	Output Fall Time	$PAD(0.6V_{CC})$ to $PAD(0.3V_{CC})$	1.0	6.0	V/ns
T_{phl}	Output Falling Prop. Delay	$A(0.5V_{CC})$ to $PAD(0.425V_{CC})$	1.5	2.6	ns
T_{plh}	Output Rising Prop. Delay	$A(0.5V_{CC})$ to $PAD(0.425V_{CC})$	1.4	2.6	ns
T_{phi_in}	Output Falling Prop. Delay	$PAD(0.425V_{CC})$ to $Y(0.5V_{CC})$ C_L=1pF	0.35	0.8	ns
T_{plh_in}	Output Rising Prop. Delay	$PAD(0.425V_{CC})$ to $Y(0.5V_{CC})$ C_L=1pF	0.35	0.8	ns

PCI BUFFERS

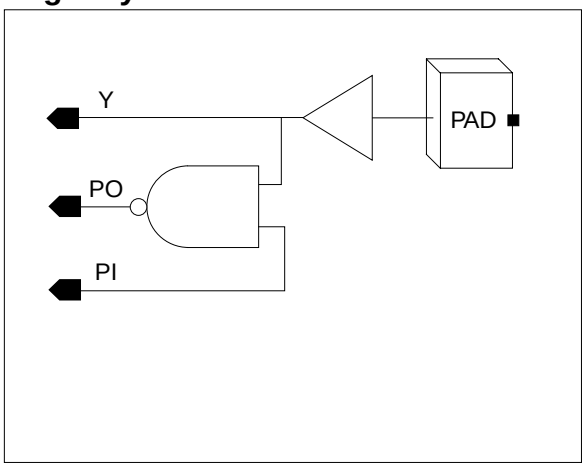
DC Characteristics of PCI Mode (SEL = high)

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6		3.0	3.6	V
V_{IO}	V_{IO} Voltage		V_{CC}			4.75	5.25	V
V_{ih}	Input High Voltage		$0.5V_{CC}$	V_{CC}+0.5		1.9	V_{IO}+0.5	V
V_{il}	Input Low Voltage		–0.5	$0.35V_{CC}$		–0.5	0.9	V
I_i	Input Leakage Current	$0 < V_{IN} < V_{CC}$	–10	10	$0 < Vin < V_{IO}$	–70	70	µA
V_{oh}	Output High Voltage	I_{OUT} = –500µA	$0.9V_{CC}$	–	I_{OUT} = –2mA	2.4	–	V
V_{ol}	Output Low Voltage	I_{OUT} = 1500µA	–	$0.1V_{CC}$	I_{OUT} = 6mA	–	0.55	V

AC Characteristics of PCI Mode (SEL = low)

Symbol	Parameter	3.3V Signaling (66MHz)			5V Signaling (33MHz)			Unit
		Condition	Min	Max	Condition	Min	Max	
$I_{oh\ (AC)}$	Switching current high	$V_{OUT} = 0.3V_{CC}$	$–12V_{CC}$		V_{OUT} = 1.4V	–44		mA
		$V_{OUT} = 0.7V_{CC}$		$–32V_{CC}$	V_{OUT} = 2.4V	–2.33		
		$V_{OUT} = 0.9V_{CC}$	$–1.71V_{CC}$		V_{OUT} = 3.0V		–142	
$I_{ol\ (AC)}$	Switching current low	$V_{OUT} = 0.6V_{CC}$	$16V_{CC}$		V_{OUT} = 2.2V	95		mA
		$V_{OUT} = 0.1V_{CC}$	$2.67V_{CC}$		V_{OUT} = 0.55V	23.9		
		$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	V_{OUT} = 0.71V		206	
I_{cl}	Low clamp current	$–3 < V_{IN} \leq –1$	$–25 + (V_{IN}+1)/0.015$		$–5 < V_{IN} \leq –1$	$–25 + (V_{IN}+1)/0.015$		mA
I_{ch}	High clamp current	$V_{CC}+1 \leq V_{IN} < V_{CC}+4$	$25+(V_{IN}–V_{CC}–1)/0.015$					mA
T_r	Output rise time	$0.3V_{CC}$ to $0.6V_{CC}$	1.0	4.0	PAD($0.4V_{CC}$) to PAD(2.4V)	1.0	5.0	V/ns
T_f	Output fall time	$0.6V_{CC}$ to $0.3V_{CC}$	1.0	4.0	PAD($2.4V_{CC}$) to PAD(0.4V)	1.0	5.0	V/ns
T_{plh}	output falling prop. delay	A($0.5V_{CC}$) to PAD($0.4V_{CC}$)	1.5	3.0	A($0.5V_{CC}$) to PAD(1.4V)	1.0	3.0	ns
T_{phi}	output rising prop. delay	A($0.5V_{CC}$) to PAD($0.4V_{CC}$)	1.5	3.0	A($0.5V_{CC}$) to PAD(1.4V)	1.0	3.0	ns

Logic Symbol



Truth Table

Input Truth Table			
PAD	**PI**	**Y**	**PO**
1	1	1	0
0	x	0	1
1	0	1	1

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F = 1.50ns, SL: Standard Load)

ptipcix

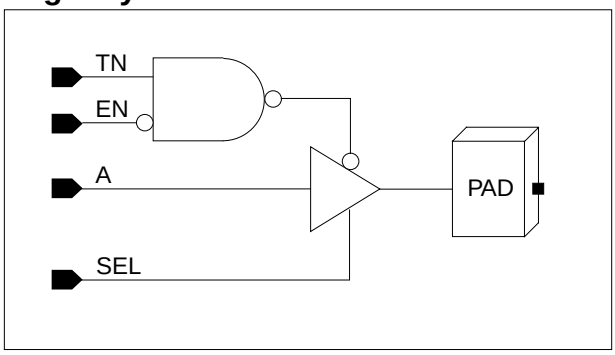
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.483	0.443 + 0.021*SL	0.443 + 0.020*SL	0.448 + 0.020*SL
	t_F	0.145	0.110 + 0.020*SL	0.113 + 0.016*SL	0.126 + 0.015*SL
	t_{PLH}	0.238	0.217 + 0.013*SL	0.220 + 0.009*SL	0.232 + 0.008*SL
	t_{PHL}	0.395	0.371 + 0.017*SL	0.376 + 0.010*SL	0.425 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 17, *Group3 : 17 < SL

PTOPCIX

5V-tolerant PCI-X Output Buffers

Logic Symbol



Truth Table

Output Truth Table			
A	**EN**	**TN**	**PAD**
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	HI-Z

Switching Characteristics

(Typical process, 25°C, 1.2V, t_R/t_F =0.17ns, CL: Capacitive Load[pF])

ptopcix

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.889	0.570 + 0.044*CL	0.419 + 0.049*CL	0.320 + 0.051*CL
	t_F	1.978	0.496 + 0.029*CL	0.439 + 0.031*CL	0.381 + 0.032*CL
	t_{PLH}	2.519	1.557 + 0.018*CL	1.457 + 0.021*CL	1.397 + 0.022*CL
	t_{PHL}	1.703	0.817 + 0.019*CL	0.889 + 0.016*CL	0.909 + 0.016*CL
TN to PAD	t_R	2.827	0.241 + 0.051*CL	0.216 + 0.052*CL	0.184 + 0.053*CL
	t_F	1.895	0.226 + 0.034*CL	0.268 + 0.033*CL	0.265 + 0.033*CL
	t_{PLH}	2.525	1.287 + 0.025*CL	1.328 + 0.024*CL	1.335 + 0.024*CL
	t_{PHL}	1.784	0.836 + 0.020*CL	0.932 + 0.017*CL	0.977 + 0.016*CL
	t_{PLZ}	0.330	0.330 + 0.000*CL	0.330 + 0.000*CL	0.330 + 0.000*CL
	t_{PHZ}	1.778	1.779 + 0.000*CL	1.778 + 0.000*CL	1.778 + 0.000*CL
EN to PAD	t_R	2.827	0.241 + 0.051*CL	0.216 + 0.052*CL	0.184 + 0.053*CL
	t_F	1.895	0.226 + 0.034*CL	0.268 + 0.033*CL	0.265 + 0.033*CL
	t_{PLH}	2.594	1.356 + 0.025*CL	1.397 + 0.024*CL	1.404 + 0.024*CL
	t_{PHL}	1.853	0.905 + 0.020*CL	1.001 + 0.017*CL	1.046 + 0.016*CL
	t_{PLZ}	0.322	0.322 + 0.000*CL	0.322 + 0.000*CL	0.322 + 0.000*CL
	t_{PHZ}	1.769	1.770 + 0.000*CL	1.769 + 0.000*CL	1.769 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Cell List

Cell Type		Cell Name	Supply Voltage	Description
Power	2.5V Interface Digital I/Os	vdd12im	1.2V	1.2V Internal for 2.5V Interface
		vdd12im_core	1.2V	1.2V Core only for 2.5V Interface
		vdd25pm	2.5V	2.5V Pre-Driver
		vdd25om	2.5V	2.5V Output-Driver
		vdd25opm	2.5V	2.5V Output-Driver and Pre-Driver
	3.3V Interface Digital I/Os	vdd12ih	1.2V	1.2V Internal for 3.3V Interface
		vdd12ih_core	1.2V	1.2V Core only for 3.3V Interface
		vdd33ph	3.3V	3.3V Pre-Driver
		vdd33oh	3.3V	3.3V Output-Driver
		vdd33oph	3.3V	3.3V Output-Driver and Pjre-Driver
Ground	2.5V Interface Digital I/Os	vssim		Internal GND for 2.5V Interface
		vsspm		Pre-Driver GND for 2.5V Interface
		vssom		Output-Driver GND for 2.5V Interface
		vssipm		Internal and Pre-Driver GND for 2.5V Interface
		vssopm		Output-Driver and Pre-Driver GND for 2.5V Interface
		vsstm		Total GND for 2.5V Interface
	3.3V Interface Digital I/Os	vssih		Internal GND for 3.3V Interface
		vssph		Pre-Driver GND for 3.3V Interface
		vssoh		Output-Driver GND for 3.3V Interface
		vssiph		Internal and Pre-Driver GND for 3.3V Interface
		vssoph		Output-Driver and Pre-Driver GND for 3.3V Interface
		vssth		Total GND for 3.3V Interface

Cell List (Continued)

Cell Type		Cell Name	Supply Voltage	Description
Power	2.5V Interface Analog I/Os	vdd12im_abb	1.2V	1.2V Internal for 2.5V Internal
		vdd25im_abb	2.5V	2.5V Internal for 2.5V Internal
		vdd25opm_abb	2.5V	2.5V Output-Driver and Pre-Driver
		vdd25tm_abb	2.5V	2.5V Total
	3.3V Interface Analog I/Os	vdd12ih_abb	1.2V	1.2V Internal for 3.3V Interface
		vdd33ih_abb	3.3V	3.3V Internal for 3.3V Interface
		vdd33oph_abb	3.3V	3.3V Output-Driver and Pre-Driver
		vdd33th_abb	3.3V	3.3V Total
Ground	2.5V Interface Analog I/Os	vssoim_abb		Internal GND for 2.5V Interface
		vssopm_abb		Output-Driver and Pre-Driver GND
		vsstm_abb		Total GND Except Bulk-Bias
		vbbm_abb		Bulk-Bias GND
		vssbbm_abb		Total GND Including Bulk-Bias
	3.3V Interface Analog I/Os	vssih_abb		Internal GND for 3.3V Interface
		vssoph_abb		Output-Driver and Pre-Driver GND
		vssth_abb		Total GND Except Bulk-Bias
		vbbh_abb		Bulk-Bias GND
		vssbbh_abb		Total GND Including Bulk-Bias

Analog Input

Cell Name	Function Description
pmia_abb	Analog Input PAD for 2.5V Interface with Separated Bulk-Bias
pmiar10_abb	Analog Input PAD for 2.5V Interface with 10ohm Resistor and Separated Bulk-Bias
pmiar50_abb	Analog Input PAD for 2.5V Interface with 50ohm Resistor and Separated Bulk-Bias
pmnc_abb	Analog No Connection PAD for 2.5V Interface with Separated Bulk-Bias
pmic_abb	Analog CMOS Input PAD for 2.5V Interface with Separated Bulk-Bias
pmicc_abb	Analog CMOS Input PAD for 2.5V Interface with Separated Bulk-Bias and without Nand-Tree
pmicd_abb	Analog CMOS Input PAD for 2.5V Interface with Pull-Down and Separated Bulk-Bias
pmicen_abb	Analog CMOS Input PAD for 2.5V Interface with Separated Bulk-Bias and without Nand-Tree
pmicu_abb	Analog CMOS Input PAD for 2.5V Interface with Pull-Up and Separated Bulk-Bias
pmis_abb	Analog S-CMOS Input PAD for 2.5V Interface with Separated Bulk-Bias
pmisd_abb	Analog S-CMOS Input PAD for 2.5V Interface with Pull-Down and Separated Bulk-Bias
pmisu_abb	Analog S-CMOS Input PAD for 2.5V Interface with Pull-Up and Separated Bulk-Bias
phia_abb	Analog Input PAD for 3.3V Interface with Separated Bulk-Bias
phiar10_abb	Analog Input PAD for 3.3V Interface with10ohm Resistor and Separated Bulk-Bias
phiar50_abb	Analog Input PAD for 3.3V Interface with 10ohm Resistor and Separated Bulk-Bias
phnc_abb	Analog No Connection PAD for 3.3V Interface with Separated Bulk-Bias
phic_abb	Analog CMOS Input PAD for 3.3V Interface with Separate Bulk-Bias
phicc_abb	Analog CMOS Input PAD for 3.3V Interface with Separate Bulk-Bias and without Nand-Tree
phicd_abb	Analog CMOS Input PAD for 3.3V Interface with Pull-Down and Separate Bulk-Bias
phicen_abb	Analog CMOS Input PAD for 3.3V Interface with Separate Bulk-Bias and without Nand-Tree
phicu_abb	Analog CMOS Input PAD for 3.3V Interface with Pull-Up and Separate Bulk-Bias
phis_abb	Analog S-CMOS Input PAD for 3.3V Interface with Separated Bulk-Bias
phisd_abb	Analog S-CMOS Input PAD for 3.3V Interface with Pull-Down and Separated Bulk-Bias
phisu_abb	Analog S-CMOS Input PAD for 3.3V Interface with Pull-Up and Separated Bulk-Bias

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

ANALOG INTERFACE

Analog Output

Cell Name	Function Description
pmoa_abb	Analog Output PAD for 2.5V Interface with Separated Bulk-Bias
pmoar10_abb	Analog Output PAD for 2.5V Interface with 10ohm Resistor and Separated Bulk-Bias
pmoar50_abb	Analog Output PAD for 2.5V Interface with 50ohm Resistor and Separated Bulk-Bias
pmob(1/2/4/8/12)_abb	Analog Normal Output Buffer for 2.5V Interface with Separated Bulk-Bias, 1/2/4/8/12mA Drive
pmot(1/2/4/8/12)_abb	Analog Tri-State Output Buffer for 2.5V Interface with Separated Bulk-Bias, 1/2/4/8/12mA Drive
phoa_abb	Analog Output PAD for 3.3V Interface with Separated Bulk-Bias
phoar10_abb	Analog Output PAD for 3.3V Interface with 10ohm Resistor and Separated Bulk-Bias
phoar50_abb	Analog Output PAD for 3.3V Interface with 50ohm Resistor and Separated Bulk-Bias
phob(1/2/4/8/12)_abb	Analog Normal Output Buffer for 3.3V Interface with Separated Bulk-Bias, 1/2/4/8/12mA Drive
phot(1/2/4/8/12)_abb	Analog Tri-State Output Buffer for 3.3V Interface with Separated Bulk-Bias, 1/2/4/8/12mA Drive
phod4sm_abb	Analog Open-Drain Output Buffer for 3.3V Interface with Separated Bulk-Bias, 4mA Sink Drive

Analog Bi-Direction

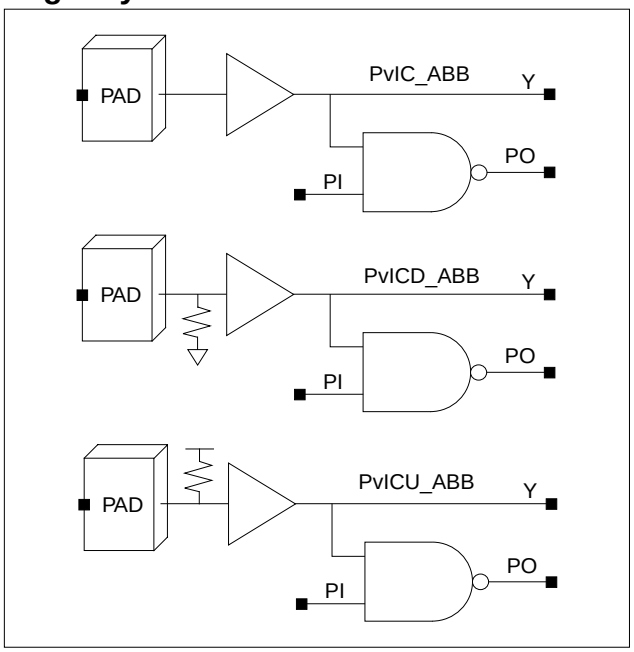
Cell Name	Function Description
pmbct(1/2/4/8)_abb	Analog Bi-Directional Buffer for 2.5V Interface with CMOS Input, Tri-State 1/2/4/8mA Output and Separated Bulk-Bias
phbct(1/2/4/8)_abb	Analog Bi-Directional Buffer for 3.3V Interface with CMOS Input, Tri-State 1/2/4/8mA Output and Separated Bulk-Bias
phbsd4sm_abb	Analog Bi-Directional Buffer for 3.3V Interface with S-CMOS Input, Open-Drain 4mA Slew-Rate Midium Output and Separated Bulk-Bias

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

Cell Availability

2.5V Interface	3.3V Interface
pmic_abb pmicd_abb pmicu_abb	phic_abb phicd_abb phicu_abb

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
pmic_abb/pmicd_abb/pmicu_abb	5.78
phic_abb/phicd_abb/phicu_abb	5.78

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmic_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.108	0.084 + 0.013*SL	0.084 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.088	0.062 + 0.014*SL	0.063 + 0.012*SL	0.061 + 0.013*SL
	t_{PLH}	0.439	0.425 + 0.009*SL	0.426 + 0.007*SL	0.438 + 0.006*SL
	t_{PHL}	0.512	0.495 + 0.011*SL	0.496 + 0.008*SL	0.510 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmicd_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.108	0.084 + 0.012*SL	0.084 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.086	0.062 + 0.011*SL	0.061 + 0.013*SL	0.062 + 0.013*SL
	t_{PLH}	0.474	0.459 + 0.009*SL	0.460 + 0.007*SL	0.472 + 0.006*SL
	t_{PHL}	0.524	0.506 + 0.011*SL	0.507 + 0.008*SL	0.521 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmicu_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.108	0.084 + 0.012*SL	0.084 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.085	0.058 + 0.016*SL	0.060 + 0.013*SL	0.061 + 0.013*SL
	t_{PLH}	0.449	0.434 + 0.009*SL	0.435 + 0.007*SL	0.447 + 0.006*SL
	t_{PHL}	0.546	0.528 + 0.011*SL	0.530 + 0.008*SL	0.543 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phic_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.078 + 0.010*SL	0.078 + 0.010*SL	0.073 + 0.010*SL
	t_F	0.082	0.059 + 0.014*SL	0.061 + 0.011*SL	0.061 + 0.011*SL
	t_{PLH}	0.290	0.278 + 0.007*SL	0.279 + 0.006*SL	0.289 + 0.005*SL
	t_{PHL}	0.636	0.622 + 0.008*SL	0.623 + 0.007*SL	0.634 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phicd_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.078 + 0.010*SL	0.078 + 0.010*SL	0.072 + 0.010*SL
	t_F	0.083	0.060 + 0.013*SL	0.062 + 0.011*SL	0.061 + 0.011*SL
	t_{PLH}	0.332	0.320 + 0.007*SL	0.321 + 0.006*SL	0.331 + 0.005*SL
	t_{PHL}	0.657	0.642 + 0.008*SL	0.643 + 0.007*SL	0.654 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phicu_abb

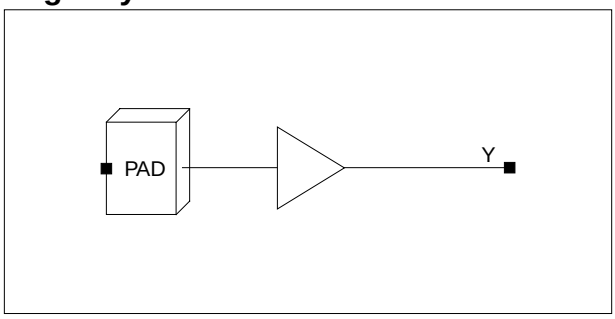
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.078 + 0.010*SL	0.078 + 0.010*SL	0.073 + 0.010*SL
	t_F	0.081	0.060 + 0.009*SL	0.059 + 0.011*SL	0.060 + 0.011*SL
	t_{PLH}	0.292	0.280 + 0.007*SL	0.281 + 0.006*SL	0.291 + 0.005*SL
	t_{PHL}	0.664	0.650 + 0.008*SL	0.650 + 0.007*SL	0.661 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

PMICC_ABB/PHICC_ABB

Analog CMOS Level Input Buffers with Separate Bulk-Bias

Logic Symbol



Truth Table

PAD	Y
0	0
1	1

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmicc_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.091	0.066 + 0.013*SL	0.067 + 0.012*SL	0.060 + 0.013*SL
	t_F	0.072	0.044 + 0.018*SL	0.047 + 0.012*SL	0.044 + 0.013*SL
	t_{PLH}	0.431	0.415 + 0.010*SL	0.417 + 0.007*SL	0.432 + 0.006*SL
	t_{PHL}	0.503	0.484 + 0.012*SL	0.486 + 0.008*SL	0.503 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phicc_abb

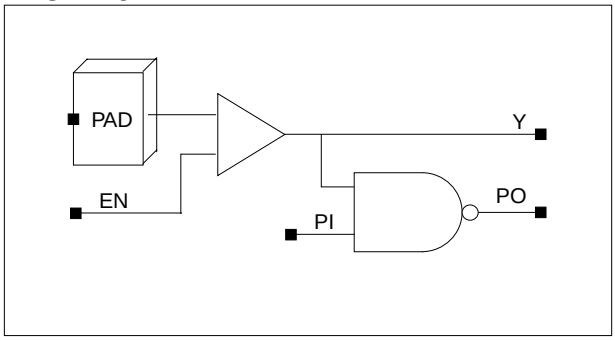
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.083	0.064 + 0.010*SL	0.064 + 0.010*SL	0.058 + 0.010*SL
	t_F	0.066	0.041 + 0.016*SL	0.044 + 0.011*SL	0.045 + 0.011*SL
	t_{PLH}	0.283	0.270 + 0.008*SL	0.271 + 0.006*SL	0.283 + 0.005*SL
	t_{PHL}	0.628	0.612 + 0.009*SL	0.614 + 0.007*SL	0.627 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell Availability

2.5V Interface	3.3V Interface
pmicen_abb	phicen_abb

Logic Symbol



Truth Table

PAD	PI	EN	Y	PO
1	1	1	1	0
0	x	1	0	1
1	0	1	1	1
x	x	0	0	1

Standard Load (SL)

Cell Name	PI	EN
pmicen_abb	5.41	5.53
phicen_abb	5.41	5.53

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmicen_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.188	0.154 + 0.016*SL	0.154 + 0.017*SL	0.143 + 0.018*SL
	t_F	0.156	0.123 + 0.019*SL	0.124 + 0.016*SL	0.120 + 0.016*SL
	t_{PLH}	0.326	0.301 + 0.016*SL	0.304 + 0.011*SL	0.330 + 0.009*SL
	t_{PHL}	0.473	0.447 + 0.016*SL	0.450 + 0.012*SL	0.478 + 0.009*SL
EN to Y	t_R	0.134	0.097 + 0.019*SL	0.098 + 0.018*SL	0.089 + 0.019*SL
	t_F	0.119	0.083 + 0.022*SL	0.086 + 0.016*SL	0.084 + 0.017*SL
	t_{PLH}	0.168	0.146 + 0.013*SL	0.148 + 0.010*SL	0.164 + 0.009*SL
	t_{PHL}	0.225	0.200 + 0.016*SL	0.203 + 0.011*SL	0.226 + 0.009*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phicen_abb

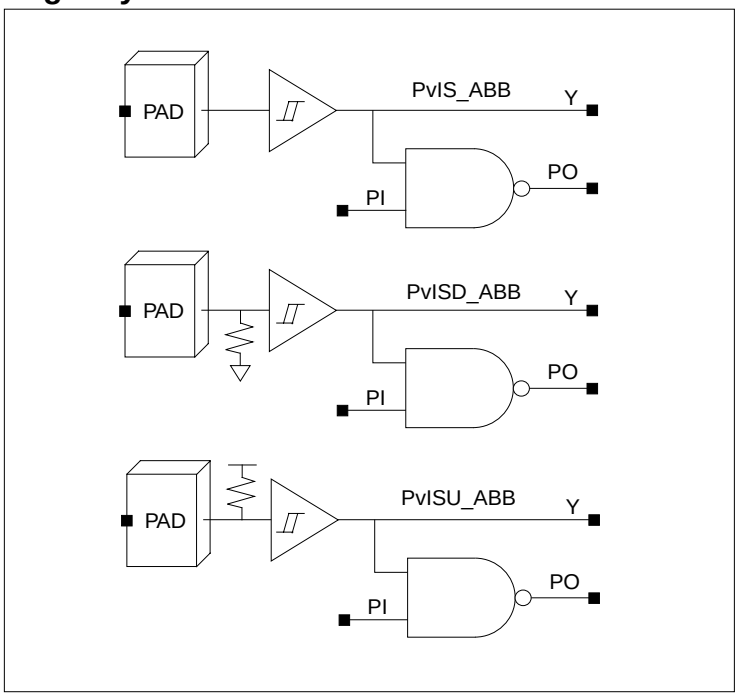
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.161 + 0.011*SL	0.161 + 0.012*SL	0.151 + 0.013*SL
	t_F	0.163	0.136 + 0.014*SL	0.136 + 0.013*SL	0.135 + 0.013*SL
	t_{PLH}	0.275	0.255 + 0.013*SL	0.258 + 0.009*SL	0.280 + 0.007*SL
	t_{PHL}	0.523	0.502 + 0.013*SL	0.504 + 0.010*SL	0.527 + 0.008*SL
EN to Y	t_R	0.119	0.093 + 0.013*SL	0.093 + 0.013*SL	0.089 + 0.014*SL
	t_F	0.120	0.090 + 0.017*SL	0.092 + 0.014*SL	0.092 + 0.014*SL
	t_{PLH}	0.159	0.142 + 0.010*SL	0.144 + 0.008*SL	0.159 + 0.006*SL
	t_{PHL}	0.222	0.201 + 0.013*SL	0.203 + 0.010*SL	0.223 + 0.008*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell Availability

2.5V Interface	3.3V Interface
pmis_abb pmisd_abb pmisu_abb	phis_abb phisd_abb phisu_abb

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
pmis_abb/pmisd_abb/pmisu_abb	5.78
phis_abb/phisd_abb/phisu_abb	5.78

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

pmis_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.108	0.084 + 0.012*SL	0.084 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.086	0.060 + 0.015*SL	0.061 + 0.013*SL	0.061 + 0.013*SL
	t_{PLH}	0.794	0.779 + 0.009*SL	0.780 + 0.007*SL	0.792 + 0.006*SL
	t_{PHL}	0.974	0.956 + 0.011*SL	0.958 + 0.008*SL	0.972 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmisd_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.108	0.084 + 0.012*SL	0.084 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.087	0.060 + 0.016*SL	0.062 + 0.012*SL	0.061 + 0.013*SL
	t_{PLH}	0.803	0.789 + 0.009*SL	0.790 + 0.007*SL	0.802 + 0.006*SL
	t_{PHL}	1.034	1.017 + 0.010*SL	1.018 + 0.008*SL	1.032 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

pmisu_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.109	0.084 + 0.013*SL	0.084 + 0.012*SL	0.081 + 0.013*SL
	t_F	0.087	0.062 + 0.014*SL	0.062 + 0.013*SL	0.062 + 0.013*SL
	t_{PLH}	0.828	0.813 + 0.009*SL	0.815 + 0.007*SL	0.827 + 0.006*SL
	t_{PHL}	0.965	0.948 + 0.011*SL	0.949 + 0.008*SL	0.963 + 0.007*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

phis_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.077 + 0.010*SL	0.078 + 0.010*SL	0.073 + 0.010*SL
	t_F	0.083	0.060 + 0.013*SL	0.062 + 0.011*SL	0.061 + 0.011*SL
	t_{PLH}	0.621	0.609 + 0.007*SL	0.610 + 0.006*SL	0.619 + 0.005*SL
	t_{PHL}	0.996	0.981 + 0.008*SL	0.982 + 0.007*SL	0.993 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phisd_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.078 + 0.010*SL	0.078 + 0.010*SL	0.073 + 0.010*SL
	t_F	0.083	0.062 + 0.011*SL	0.062 + 0.010*SL	0.059 + 0.011*SL
	t_{PLH}	0.645	0.633 + 0.007*SL	0.634 + 0.006*SL	0.643 + 0.005*SL
	t_{PHL}	1.039	1.025 + 0.009*SL	1.026 + 0.007*SL	1.037 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

phisu_abb

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.097	0.078 + 0.010*SL	0.078 + 0.010*SL	0.073 + 0.010*SL
	t_F	0.083	0.061 + 0.012*SL	0.062 + 0.011*SL	0.061 + 0.011*SL
	t_{PLH}	0.642	0.630 + 0.007*SL	0.631 + 0.006*SL	0.640 + 0.005*SL
	t_{PHL}	0.998	0.983 + 0.008*SL	0.984 + 0.007*SL	0.995 + 0.006*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 11, *Group3 : 11 < SL

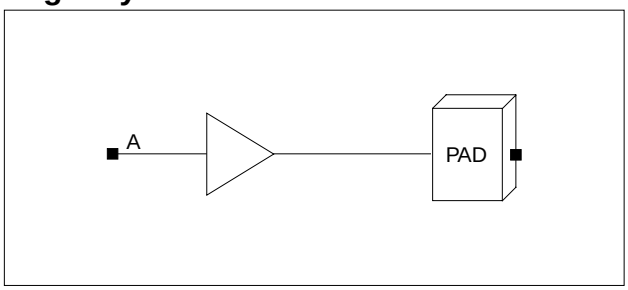
PvOByz_ABB

Analog Normal Output Buffers with Separate Bulk-Bias

Cell Availability

2.5V Interface	3.3V Interface
pmob(1/2/4/8/12)_abb	phob(1/2/4/8/12)_abb

Logic Symbol



Truth Table

A	PAD
0	0
1	1

Standard Load (SL)

Cell Name	A
pmob(1/2/4/8/12)_abb	8.49
phob(1/2/4/8/12)_abb	8.49

Switching Characteristics (Typical process, 25°C, 2.5V, t_R/t_F=0.11ns, CL: Capacitive Load{pF})

pmob1_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	23.608	0.448 + 0.463*CL	0.443 + 0.463*CL	0.442 + 0.463*CL
	t_F	19.017	0.594 + 0.367*CL	0.487 + 0.371*CL	0.451 + 0.371*CL
	t_{PLH}	10.746	0.760 + 0.200*CL	0.761 + 0.200*CL	0.760 + 0.200*CL
	t_{PHL}	10.206	1.214 + 0.180*CL	1.226 + 0.180*CL	1.230 + 0.180*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob2_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	11.853	0.369 + 0.229*CL	0.299 + 0.231*CL	0.275 + 0.232*CL
	t_F	10.852	0.335 + 0.209*CL	0.272 + 0.212*CL	0.248 + 0.212*CL
	t_{PLH}	5.897	0.898 + 0.100*CL	0.904 + 0.100*CL	0.904 + 0.100*CL
	t_{PHL}	6.164	0.799 + 0.107*CL	0.808 + 0.107*CL	0.808 + 0.107*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob4_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.915	0.129 + 0.116*CL	0.124 + 0.116*CL	0.124 + 0.116*CL
	t_F	6.605	0.119 + 0.130*CL	0.118 + 0.130*CL	0.118 + 0.130*CL
	t_{PLH}	2.986	0.490 + 0.050*CL	0.490 + 0.050*CL	0.490 + 0.050*CL
	t_{PHL}	3.781	0.344 + 0.069*CL	0.341 + 0.069*CL	0.340 + 0.069*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F=0.11ns, CL: Capacitive Load{pF})

pmob8_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.978	0.126 + 0.057*CL	0.097 + 0.058*CL	0.085 + 0.058*CL
	t_F	3.308	0.087 + 0.064*CL	0.066 + 0.065*CL	0.065 + 0.065*CL
	t_{PLH}	1.809	0.559 + 0.025*CL	0.561 + 0.025*CL	0.561 + 0.025*CL
	t_{PHL}	2.057	0.357 + 0.034*CL	0.345 + 0.034*CL	0.340 + 0.034*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmob12_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.018	0.166 + 0.037*CL	0.131 + 0.038*CL	0.107 + 0.038*CL
	t_F	2.213	0.125 + 0.041*CL	0.075 + 0.043*CL	0.054 + 0.043*CL
	t_{PLH}	1.472	0.618 + 0.017*CL	0.639 + 0.017*CL	0.640 + 0.017*CL
	t_{PHL}	1.506	0.407 + 0.022*CL	0.381 + 0.023*CL	0.370 + 0.023*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load{pF})

phob1_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	27.264	0.530 + 0.534*CL	0.492 + 0.535*CL	0.490 + 0.535*CL
	t_F	21.073	1.113 + 0.396*CL	0.900 + 0.403*CL	0.747 + 0.407*CL
	t_{PLH}	12.953	1.116 + 0.237*CL	1.119 + 0.237*CL	1.117 + 0.237*CL
	t_{PHL}	12.104	2.326 + 0.197*CL	2.464 + 0.193*CL	2.480 + 0.192*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob2_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.734	0.570 + 0.262*CL	0.445 + 0.266*CL	0.378 + 0.267*CL
	t_F	12.899	0.641 + 0.243*CL	0.514 + 0.248*CL	0.427 + 0.249*CL
	t_{PLH}	7.348	1.396 + 0.119*CL	1.428 + 0.118*CL	1.431 + 0.118*CL
	t_{PHL}	7.576	1.404 + 0.124*CL	1.475 + 0.122*CL	1.482 + 0.122*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob4_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.833	0.152 + 0.133*CL	0.140 + 0.134*CL	0.139 + 0.134*CL
	t_F	6.397	0.162 + 0.124*CL	0.138 + 0.125*CL	0.133 + 0.125*CL
	t_{PLH}	3.434	0.474 + 0.059*CL	0.475 + 0.059*CL	0.475 + 0.059*CL
	t_{PHL}	3.519	0.473 + 0.061*CL	0.474 + 0.061*CL	0.473 + 0.061*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load{pF})

phob8_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.457	0.189 + 0.065*CL	0.147 + 0.066*CL	0.124 + 0.067*CL
	t_F	3.265	0.219 + 0.061*CL	0.191 + 0.061*CL	0.163 + 0.062*CL
	t_{PLH}	2.097	0.602 + 0.030*CL	0.616 + 0.030*CL	0.617 + 0.030*CL
	t_{PHL}	2.180	0.621 + 0.032*CL	0.653 + 0.031*CL	0.657 + 0.030*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phob12_abb

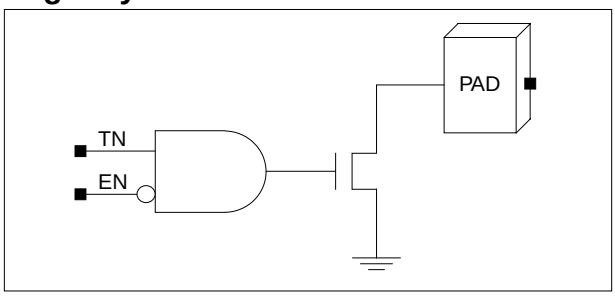
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.383	0.258 + 0.042*CL	0.229 + 0.043*CL	0.196 + 0.044*CL
	t_F	2.295	0.285 + 0.040*CL	0.282 + 0.040*CL	0.264 + 0.041*CL
	t_{PLH}	1.758	0.698 + 0.022*CL	0.756 + 0.020*CL	0.769 + 0.020*CL
	t_{PHL}	1.866	0.742 + 0.023*CL	0.810 + 0.021*CL	0.841 + 0.021*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Cell Availability

3.3V Interface	phod4sm_abb

Logic Symbol



Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Standard Load (SL)

Cell Name	TN	EN
phod4sm_abb	6.00	5.86

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

phod4sm_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.706	0.699 + 0.120*CL	0.662 + 0.121*CL	0.580 + 0.123*CL
	t_{PHL}	4.804	1.476 + 0.069*CL	1.679 + 0.063*CL	1.740 + 0.061*CL
	t_{PLZ}	0.605	0.605 + 0.000*CL	0.605 + 0.000*CL	0.605 + 0.000*CL
EN to PAD	t_F	6.706	0.699 + 0.120*CL	0.662 + 0.121*CL	0.580 + 0.123*CL
	t_{PHL}	4.855	1.526 + 0.069*CL	1.729 + 0.063*CL	1.790 + 0.061*CL
	t_{PLZ}	0.640	0.640 + 0.000*CL	0.640 + 0.000*CL	0.640 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

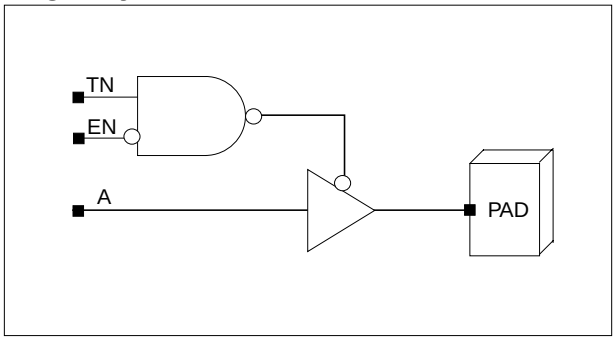
PvOTyz_ABB

Analog Tri-state Output Buffers with Separate Bulk-Bias

Cell Availability

2.5V Interface	3.3V Interface
pmot(1/2/4/8/12)_abb	phot(1/2/4/8/12)_abb

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi - z
0	x	x	Hi - z

Standard Load (SL)

Cell Name	TN	EN	A
pmot(1/2/4/8/12)_abb	8	7.82	11.35
phot(1/2/4/8/12)_abb	8	7.82	11.35

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

pmot1_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	23.608	0.448 + 0.463*CL	0.443 + 0.463*CL	0.442 + 0.463*CL
	t_F	19.017	0.594 + 0.367*CL	0.487 + 0.371*CL	0.451 + 0.371*CL
	t_{PLH}	10.746	0.760 + 0.200*CL	0.761 + 0.200*CL	0.760 + 0.200*CL
	t_{PHL}	10.206	1.214 + 0.180*CL	1.226 + 0.180*CL	1.230 + 0.180*CL
TN to PAD	t_R	23.608	0.448 + 0.463*CL	0.443 + 0.463*CL	0.442 + 0.463*CL
	t_F	19.017	0.594 + 0.367*CL	0.487 + 0.371*CL	0.451 + 0.371*CL
	t_{PLH}	10.810	0.824 + 0.200*CL	0.825 + 0.200*CL	0.824 + 0.200*CL
	t_{PHL}	10.319	1.327 + 0.180*CL	1.339 + 0.180*CL	1.343 + 0.180*CL
	t_{PLZ}	0.617	0.617 + 0.000*CL	0.617 + 0.000*CL	0.617 + 0.000*CL
	t_{PHZ}	0.484	0.484 + 0.000*CL	0.484 + 0.000*CL	0.484 + 0.000*CL
EN to PAD	t_R	23.608	0.448 + 0.463*CL	0.443 + 0.463*CL	0.442 + 0.463*CL
	t_F	19.017	0.594 + 0.367*CL	0.487 + 0.371*CL	0.451 + 0.371*CL
	t_{PLH}	10.864	0.877 + 0.200*CL	0.877 + 0.200*CL	0.880 + 0.200*CL
	t_{PHL}	10.372	1.380 + 0.180*CL	1.393 + 0.180*CL	1.394 + 0.180*CL
	t_{PLZ}	0.655	0.656 + 0.000*CL	0.655 + 0.000*CL	0.655 + 0.000*CL
	t_{PHZ}	0.524	0.524 + 0.000*CL	0.524 + 0.000*CL	0.524 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot2_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	11.853	0.369 + 0.229*CL	0.299 + 0.231*CL	0.275 + 0.232*CL
	t_F	10.852	0.335 + 0.209*CL	0.272 + 0.212*CL	0.248 + 0.212*CL
	t_{PLH}	5.897	0.898 + 0.100*CL	0.904 + 0.100*CL	0.904 + 0.100*CL
	t_{PHL}	6.164	0.799 + 0.107*CL	0.808 + 0.107*CL	0.808 + 0.107*CL
TN to PAD	t_R	11.853	0.369 + 0.229*CL	0.299 + 0.231*CL	0.275 + 0.232*CL
	t_F	10.852	0.335 + 0.209*CL	0.272 + 0.212*CL	0.248 + 0.212*CL
	t_{PLH}	5.961	0.962 + 0.100*CL	0.968 + 0.100*CL	0.968 + 0.100*CL
	t_{PHL}	6.277	0.912 + 0.107*CL	0.920 + 0.107*CL	0.921 + 0.107*CL
	t_{PLZ}	0.520	0.520 + 0.000*CL	0.520 + 0.000*CL	0.520 + 0.000*CL
	t_{PHZ}	0.612	0.613 + 0.000*CL	0.612 + 0.000*CL	0.612 + 0.000*CL
EN to PAD	t_R	11.853	0.369 + 0.229*CL	0.299 + 0.231*CL	0.275 + 0.232*CL
	t_F	10.852	0.335 + 0.209*CL	0.272 + 0.212*CL	0.248 + 0.212*CL
	t_{PLH}	6.014	1.015 + 0.100*CL	1.021 + 0.100*CL	1.022 + 0.100*CL
	t_{PHL}	6.331	0.965 + 0.107*CL	0.973 + 0.107*CL	0.975 + 0.107*CL
	t_{PLZ}	0.560	0.560 + 0.000*CL	0.560 + 0.000*CL	0.560 + 0.000*CL
	t_{PHZ}	0.652	0.652 + 0.000*CL	0.652 + 0.000*CL	0.652 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

pmot4_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.915	0.129 + 0.116*CL	0.124 + 0.116*CL	0.124 + 0.116*CL
	t_F	6.605	0.119 + 0.130*CL	0.118 + 0.130*CL	0.118 + 0.130*CL
	t_{PLH}	2.986	0.490 + 0.050*CL	0.490 + 0.050*CL	0.490 + 0.050*CL
	t_{PHL}	3.781	0.344 + 0.069*CL	0.341 + 0.069*CL	0.340 + 0.069*CL
TN to PAD	t_R	5.915	0.129 + 0.116*CL	0.124 + 0.116*CL	0.124 + 0.116*CL
	t_F	6.605	0.119 + 0.130*CL	0.118 + 0.130*CL	0.118 + 0.130*CL
	t_{PLH}	3.053	0.556 + 0.050*CL	0.556 + 0.050*CL	0.556 + 0.050*CL
	t_{PHL}	3.890	0.447 + 0.069*CL	0.449 + 0.069*CL	0.449 + 0.069*CL
	t_{PLZ}	0.457	0.457 + 0.000*CL	0.457 + 0.000*CL	0.457 + 0.000*CL
	t_{PHZ}	0.543	0.543 + 0.000*CL	0.543 + 0.000*CL	0.543 + 0.000*CL
EN to PAD	t_R	5.915	0.129 + 0.116*CL	0.124 + 0.116*CL	0.124 + 0.116*CL
	t_F	6.605	0.119 + 0.130*CL	0.118 + 0.130*CL	0.118 + 0.130*CL
	t_{PLH}	3.106	0.609 + 0.050*CL	0.609 + 0.050*CL	0.609 + 0.050*CL
	t_{PHL}	3.944	0.501 + 0.069*CL	0.502 + 0.069*CL	0.502 + 0.069*CL
	t_{PLZ}	0.496	0.496 + 0.000*CL	0.496 + 0.000*CL	0.496 + 0.000*CL
	t_{PHZ}	0.582	0.583 + 0.000*CL	0.582 + 0.000*CL	0.582 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

pmot8_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.978	0.126 + 0.057*CL	0.097 + 0.058*CL	0.085 + 0.058*CL
	t_F	3.308	0.087 + 0.064*CL	0.066 + 0.065*CL	0.065 + 0.065*CL
	t_{PLH}	1.809	0.559 + 0.025*CL	0.561 + 0.025*CL	0.561 + 0.025*CL
	t_{PHL}	2.057	0.357 + 0.034*CL	0.345 + 0.034*CL	0.340 + 0.034*CL
TN to PAD	t_R	2.978	0.127 + 0.057*CL	0.097 + 0.058*CL	0.085 + 0.058*CL
	t_F	3.308	0.069 + 0.065*CL	0.065 + 0.065*CL	0.064 + 0.065*CL
	t_{PLH}	1.876	0.625 + 0.025*CL	0.627 + 0.025*CL	0.627 + 0.025*CL
	t_{PHL}	2.161	0.436 + 0.035*CL	0.439 + 0.034*CL	0.439 + 0.034*CL
	t_{PLZ}	0.483	0.483 + 0.000*CL	0.483 + 0.000*CL	0.483 + 0.000*CL
	t_{PHZ}	0.672	0.673 + 0.000*CL	0.672 + 0.000*CL	0.672 + 0.000*CL
EN to PAD	t_R	2.978	0.127 + 0.057*CL	0.097 + 0.058*CL	0.085 + 0.058*CL
	t_F	3.308	0.069 + 0.065*CL	0.065 + 0.065*CL	0.065 + 0.065*CL
	t_{PLH}	1.929	0.678 + 0.025*CL	0.680 + 0.025*CL	0.681 + 0.025*CL
	t_{PHL}	2.214	0.490 + 0.035*CL	0.492 + 0.034*CL	0.493 + 0.034*CL
	t_{PLZ}	0.522	0.522 + 0.000*CL	0.522 + 0.000*CL	0.522 + 0.000*CL
	t_{PHZ}	0.711	0.712 + 0.000*CL	0.711 + 0.000*CL	0.711 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 0.11ns, CL: Capacitive Load[pF])

pmot12_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.018	0.166 + 0.037*CL	0.131 + 0.038*CL	0.107 + 0.038*CL
	t_F	2.213	0.125 + 0.041*CL	0.075 + 0.043*CL	0.054 + 0.043*CL
	t_{PLH}	1.472	0.618 + 0.017*CL	0.639 + 0.017*CL	0.640 + 0.017*CL
	t_{PHL}	1.506	0.407 + 0.022*CL	0.381 + 0.023*CL	0.370 + 0.023*CL
TN to PAD	t_R	2.018	0.166 + 0.037*CL	0.131 + 0.038*CL	0.107 + 0.038*CL
	t_F	2.211	0.062 + 0.043*CL	0.052 + 0.043*CL	0.049 + 0.043*CL
	t_{PLH}	1.539	0.685 + 0.017*CL	0.705 + 0.017*CL	0.707 + 0.017*CL
	t_{PHL}	1.598	0.444 + 0.023*CL	0.448 + 0.023*CL	0.450 + 0.023*CL
	t_{PLZ}	0.506	0.506 + 0.000*CL	0.506 + 0.000*CL	0.506 + 0.000*CL
	t_{PHZ}	0.800	0.801 + 0.000*CL	0.800 + 0.000*CL	0.800 + 0.000*CL
EN to PAD	t_R	2.018	0.166 + 0.037*CL	0.131 + 0.038*CL	0.107 + 0.038*CL
	t_F	2.211	0.062 + 0.043*CL	0.052 + 0.043*CL	0.050 + 0.043*CL
	t_{PLH}	1.592	0.738 + 0.017*CL	0.758 + 0.017*CL	0.760 + 0.017*CL
	t_{PHL}	1.651	0.498 + 0.023*CL	0.502 + 0.023*CL	0.503 + 0.023*CL
	t_{PLZ}	0.546	0.546 + 0.000*CL	0.546 + 0.000*CL	0.546 + 0.000*CL
	t_{PHZ}	0.840	0.841 + 0.000*CL	0.840 + 0.000*CL	0.839 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

phot1_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	31.975	1.170 + 0.616*CL	1.107 + 0.617*CL	1.071 + 0.618*CL
	t_F	28.212	1.417 + 0.536*CL	1.234 + 0.540*CL	1.114 + 0.541*CL
	t_{PLH}	15.344	1.682 + 0.273*CL	1.686 + 0.273*CL	1.683 + 0.273*CL
	t_{PHL}	15.541	2.929 + 0.252*CL	2.941 + 0.252*CL	2.941 + 0.252*CL
TN to PAD	t_R	31.975	1.170 + 0.616*CL	1.107 + 0.617*CL	1.071 + 0.618*CL
	t_F	28.212	1.417 + 0.536*CL	1.234 + 0.540*CL	1.114 + 0.541*CL
	t_{PLH}	15.402	1.741 + 0.273*CL	1.742 + 0.273*CL	1.742 + 0.273*CL
	t_{PHL}	15.640	3.028 + 0.252*CL	3.038 + 0.252*CL	3.044 + 0.252*CL
	t_{PLZ}	0.481	0.481 + 0.000*CL	0.481 + 0.000*CL	0.481 + 0.000*CL
	t_{PHZ}	0.368	0.368 + 0.000*CL	0.368 + 0.000*CL	0.368 + 0.000*CL
EN to PAD	t_R	31.975	1.170 + 0.616*CL	1.107 + 0.617*CL	1.071 + 0.618*CL
	t_F	28.212	1.417 + 0.536*CL	1.234 + 0.540*CL	1.114 + 0.541*CL
	t_{PLH}	15.454	1.792 + 0.273*CL	1.794 + 0.273*CL	1.797 + 0.273*CL
	t_{PHL}	15.692	3.080 + 0.252*CL	3.090 + 0.252*CL	3.096 + 0.252*CL
	t_{PLZ}	0.604	0.604 + 0.000*CL	0.604 + 0.000*CL	0.604 + 0.000*CL
	t_{PHZ}	0.492	0.492 + 0.000*CL	0.492 + 0.000*CL	0.492 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

phot2_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	16.156	0.896 + 0.305*CL	0.804 + 0.307*CL	0.732 + 0.308*CL
	t_F	15.979	1.015 + 0.299*CL	0.863 + 0.302*CL	0.749 + 0.304*CL
	t_{PLH}	8.677	1.819 + 0.137*CL	1.842 + 0.137*CL	1.849 + 0.137*CL
	t_{PHL}	9.560	2.021 + 0.151*CL	2.044 + 0.150*CL	2.047 + 0.150*CL
TN to PAD	t_R	16.156	0.896 + 0.305*CL	0.804 + 0.307*CL	0.732 + 0.308*CL
	t_F	15.979	1.015 + 0.299*CL	0.863 + 0.302*CL	0.749 + 0.304*CL
	t_{PLH}	8.734	1.875 + 0.137*CL	1.900 + 0.137*CL	1.906 + 0.137*CL
	t_{PHL}	9.659	2.120 + 0.151*CL	2.143 + 0.150*CL	2.146 + 0.150*CL
	t_{PLZ}	0.411	0.411 + 0.000*CL	0.411 + 0.000*CL	0.411 + 0.000*CL
	t_{PHZ}	0.427	0.427 + 0.000*CL	0.427 + 0.000*CL	0.427 + 0.000*CL
EN to PAD	t_R	16.156	0.896 + 0.305*CL	0.804 + 0.307*CL	0.732 + 0.308*CL
	t_F	15.979	1.015 + 0.299*CL	0.863 + 0.302*CL	0.749 + 0.304*CL
	t_{PLH}	8.786	1.927 + 0.137*CL	1.951 + 0.137*CL	1.958 + 0.137*CL
	t_{PHL}	9.711	2.172 + 0.151*CL	2.194 + 0.150*CL	2.198 + 0.150*CL
	t_{PLZ}	0.534	0.534 + 0.000*CL	0.534 + 0.000*CL	0.534 + 0.000*CL
	t_{PHZ}	0.549	0.550 + 0.000*CL	0.549 + 0.000*CL	0.549 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

phot4_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.833	0.152 + 0.133*CL	0.140 + 0.134*CL	0.139 + 0.134*CL
	t_F	6.397	0.162 + 0.124*CL	0.138 + 0.125*CL	0.133 + 0.125*CL
	t_{PLH}	3.434	0.474 + 0.059*CL	0.475 + 0.059*CL	0.475 + 0.059*CL
	t_{PHL}	3.519	0.473 + 0.061*CL	0.474 + 0.061*CL	0.473 + 0.061*CL
TN to PAD	t_R	6.833	0.152 + 0.133*CL	0.140 + 0.134*CL	0.139 + 0.134*CL
	t_F	6.397	0.163 + 0.124*CL	0.139 + 0.125*CL	0.133 + 0.125*CL
	t_{PLH}	3.493	0.533 + 0.059*CL	0.534 + 0.059*CL	0.535 + 0.059*CL
	t_{PHL}	3.619	0.570 + 0.061*CL	0.572 + 0.061*CL	0.573 + 0.061*CL
	t_{PLZ}	0.527	0.527 + 0.000*CL	0.527 + 0.000*CL	0.527 + 0.000*CL
	t_{PHZ}	0.606	0.606 + 0.000*CL	0.606 + 0.000*CL	0.605 + 0.000*CL
EN to PAD	t_R	6.833	0.152 + 0.133*CL	0.140 + 0.134*CL	0.139 + 0.134*CL
	t_F	6.397	0.163 + 0.124*CL	0.139 + 0.125*CL	0.133 + 0.125*CL
	t_{PLH}	3.544	0.584 + 0.059*CL	0.585 + 0.059*CL	0.585 + 0.059*CL
	t_{PHL}	3.670	0.621 + 0.061*CL	0.623 + 0.061*CL	0.624 + 0.061*CL
	t_{PLZ}	0.560	0.560 + 0.000*CL	0.560 + 0.000*CL	0.560 + 0.000*CL
	t_{PHZ}	0.639	0.640 + 0.000*CL	0.639 + 0.000*CL	0.639 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

phot8_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.457	0.189 + 0.065*CL	0.147 + 0.066*CL	0.124 + 0.067*CL
	t_F	3.265	0.219 + 0.061*CL	0.191 + 0.061*CL	0.163 + 0.062*CL
	t_{PLH}	2.097	0.602 + 0.030*CL	0.616 + 0.030*CL	0.617 + 0.030*CL
	t_{PHL}	2.180	0.621 + 0.032*CL	0.653 + 0.031*CL	0.657 + 0.030*CL
TN to PAD	t_R	3.457	0.189 + 0.065*CL	0.148 + 0.066*CL	0.124 + 0.067*CL
	t_F	3.265	0.227 + 0.060*CL	0.195 + 0.061*CL	0.164 + 0.062*CL
	t_{PLH}	2.156	0.661 + 0.030*CL	0.675 + 0.030*CL	0.676 + 0.030*CL
	t_{PHL}	2.277	0.701 + 0.032*CL	0.744 + 0.031*CL	0.752 + 0.031*CL
	t_{PLZ}	0.639	0.640 + 0.000*CL	0.639 + 0.000*CL	0.639 + 0.000*CL
	t_{PHZ}	0.858	0.859 + 0.000*CL	0.858 + 0.000*CL	0.858 + 0.000*CL
EN to PAD	t_R	3.457	0.189 + 0.065*CL	0.148 + 0.066*CL	0.124 + 0.067*CL
	t_F	3.265	0.227 + 0.060*CL	0.195 + 0.061*CL	0.164 + 0.062*CL
	t_{PLH}	2.207	0.711 + 0.030*CL	0.726 + 0.030*CL	0.727 + 0.030*CL
	t_{PHL}	2.328	0.751 + 0.032*CL	0.795 + 0.031*CL	0.803 + 0.031*CL
	t_{PLZ}	0.673	0.673 + 0.000*CL	0.673 + 0.000*CL	0.673 + 0.000*CL
	t_{PHZ}	0.892	0.893 + 0.000*CL	0.892 + 0.000*CL	0.892 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F=0.11ns, CL: Capacitive Load[pF])

phot12_abb

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.383	0.258 + 0.042*CL	0.229 + 0.043*CL	0.196 + 0.044*CL
	t_F	2.295	0.285 + 0.040*CL	0.282 + 0.040*CL	0.264 + 0.041*CL
	t_{PLH}	1.758	0.698 + 0.022*CL	0.756 + 0.020*CL	0.769 + 0.020*CL
	t_{PHL}	1.866	0.742 + 0.023*CL	0.810 + 0.021*CL	0.841 + 0.021*CL
TN to PAD	t_R	2.383	0.262 + 0.042*CL	0.230 + 0.043*CL	0.197 + 0.044*CL
	t_F	2.299	0.290 + 0.040*CL	0.297 + 0.040*CL	0.273 + 0.041*CL
	t_{PLH}	1.817	0.756 + 0.022*CL	0.814 + 0.020*CL	0.827 + 0.020*CL
	t_{PHL}	1.956	0.782 + 0.025*CL	0.883 + 0.021*CL	0.923 + 0.021*CL
	t_{PLZ}	0.748	0.749 + 0.000*CL	0.748 + 0.000*CL	0.748 + 0.000*CL
	t_{PHZ}	1.111	1.112 + 0.000*CL	1.111 + 0.000*CL	1.111 + 0.000*CL
EN to PAD	t_R	2.383	0.262 + 0.042*CL	0.230 + 0.043*CL	0.197 + 0.044*CL
	t_F	2.299	0.290 + 0.040*CL	0.297 + 0.040*CL	0.273 + 0.041*CL
	t_{PLH}	1.867	0.806 + 0.022*CL	0.865 + 0.020*CL	0.878 + 0.020*CL
	t_{PHL}	2.007	0.833 + 0.025*CL	0.934 + 0.021*CL	0.974 + 0.021*CL
	t_{PLZ}	0.783	0.783 + 0.000*CL	0.783 + 0.000*CL	0.782 + 0.000*CL
	t_{PHZ}	1.145	1.146 + 0.000*CL	1.145 + 0.000*CL	1.144 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Cell List

Cell Name	Function Description
ev12im	1.2V Internal ESD Protection for 2.5V Interface
ev25pm	2.5V Pre-Driver ESD Protection for 2.5V Interface
ev25om	2.5V Output-Driver ESD Protection for 2.5V Interface
ev25opm	2.5V Pre-Driver and Output-Driver ESD Protection for 2.5V Interface
ev12ih	1.2V Internal ESD Protection for 3.3V Interface
ev33ph	3.3V Pre-Driver ESD Protection for 3.3V Interface
ev33oh	3.3V Output-Driver ESD Protection for 3.3V Interface
ev33oph	3.3V Pre-Driver and Output-Driver ESD Protection for3.3V Interface
ev12im_abb	Analog 1.2V Internal ESD Protection for 2.5V Interface
ev25im_abb	Analog 2.5V Internal ESD Protection for 2.5V Interface
ev25opm_abb	Analog 2.5V Pre-Driver and Output-Driver ESD Protection for 2.5V Interface
ev25tm_abb	Analog 2.5V Internal, Pre-Driver and Output-Driver ESD Protection for 2.5V Interface
ev12ih_abb	Analog 1.2V Internal ESD Protection for 3.3V Interface
ev33ih_abb	Analog3.3V Internal ESD Protection for 3.3V Interface
ev33oph_abb	Analog 3.3V Pre-Driver and Output-Driver ESD Protection for 3.3V Interface
ev33th_abb	Analog 3.3V Internal, Pre-Driver and Output-Driver ESD Protection for 3.3V Interface

Common Slot Cells

Cell List

Cell Name	Function Description
ec0c0	Metal Ring Separator between Different Digital Blocks
ec0c0d	Metal Ring Separator between Different Digital Blocks for Noise Critical Design
ec0ca0	Metal Ring Separator between Digital to Analog
ec0ca0d	Metal Ring Separator between Digital to Analog for Noise Critical Design
eca0ca0	Metal Ring Separator between Different to Analog Blocks
eca0ca0d	Metal Ring Separator between Different to Analog Blocks for Noise Critical Design
eca0ca0_vbb	Metal Ring Separator between Different Analog Blocks with VBB Ring Connected
eca0ca0d_vbb	Metal Ring Separator between Different Analog Blocks for Noise Critical Design with VBB Ring Connected

Compiled Memory

5

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Specialty Memory *

FIFO	Synchronous First-In First-Out Memory
HCSPSRAM	Synchronous Single-Port SRAM (Up to 4Mbits) with Burst Feature
HCVROM	Synchronous Via-1 Programmable ROM (Up to 4Mbits)

* Specialty memory will be supported by on-demand. Additional information about those memories can be obtained from your local Samsung and Design Center or Samsung's worldwide headquarters.

OVERVIEW

This section is an overview of STDH150 compiled memories. STDH150 memories are suitable for high-speed application with best density. Each of these memory types may be customized to satisfy the specific circuit requirements. Each memory uses state-of-the-art design architecture techniques such as automatic power-down techniques, advanced partial activations and process-insensitive circuit designs. The final memory block is implemented as a stand-alone, pitch-matched and customized leafcells. The compiled memory is fully generated by Samsung's memory compiler, called CubicCompiler as a user-configurable compiler. The user defines the memory-related specifications such as word depth, bit per word, column mux type and so on. The compiler then produces any or all of the following items:

- Complete functional model for simulation
- Tabular model for timing and power characteristics
- Automatic generated datasheet including all information for specific memory configuration
- Full GDS and schematic netlist for layout verification
- Phantom cell to use in chip-level floor planning and layout

Additional information about compiled memories can be obtained from your local Samsung and Design Center or Samsung's worldwide headquarters.

COMPILED MEMORY NAMING CONVENTION

In this chapter, we describe the naming convention of memory. The memory name, Figure 5-1 consists of the following convention.

'memory_name':= [memory_code]_[appl_code]_[procs_code]_[opt_code]_[config_code]

Figure 5-1. Compiled Memory Naming Convention

The first string, 'memory_code', means the name of memory type. In STDH150 compiled memory, the available memory types are as follows :

- SPSRAM : Single-Port Synchronous SRAM
- SPSRAMBW : Single-Port Synchronous SRAM with Bit-Write
- SPSRAMR : Single-Port Synchronous SRAM with Redundancy
- DPSRAM : Dual-Port Synchronous SRAM
- DPSRAMBW : Dual-Port Synchronous SRAM with Bit-Write
- DPSRAMR : Dual-Port Synchronous SRAM with Redundancy
- VROM : Synchronous Via-1 Programmable ROM
- SRFRAM : Multi-Port Synchronous Register File
- SRFRAMBW : Multi-Port Synchronous Register File with Bit-Write
- FIFO* : Synchronous First-In First-Out Memory
- CAM : Single-Port Synchronous Binary CAM
- TCAM : Single-Port Synchronous Ternary CAM
- HCSPSRAM* : High-Capacity Single-Port Synchronous SRAM with Burst features
- HCVROM* : High-Capacity Synchronous Via-1 Programmable ROM

The second string, *'appl_code*', means the specific application to suitably support the compiled memory and the application code is one of High-Speed (**HS**)**,** High-Density (**HD**) and Low-Power (**LP**).

The third string, *'proc_code'*, represents the process and the process code is one of High-speed process (**H**), Generic process (**G**), and Low-Power process (**L**). If there is no process code, it means that the memory is developed under Generic process. If the process code is set to '**L**', it means that the memory is developed under Low-Power process.

The fourth string, *'opt_code'*, represents the number of read and write ports for multi-port memory and the option code is composed of the following convention:

'opt_code' = <n>r<m>w

Currently this field is only used for SRFRAM, where n is the total number of read ports and m is the total number of write ports.

The last string, *'config_code'*, represents the configuration of the memory to be specified. This configuration code is composed of the following convention:

'config_code' = <WORD> x <BPW> m <YMUX> b <BANK>

Where, WORD is the word depth, BPW is bit per word, YMUX is the available column mux type and BANK is the number of bank to be used.

For example, '*spsram_hdh_1024x32m16*' refers to a High-Density single-port synchronous SRAM with 1024 words, 32 bits and 16 column mux under High-speed process. Second, '*srfram_hdh_1r1w_32x32m2*' refers to a High-Density two-port (1-read/1-write) synchronous register file with 32 word, 32 bits and 2 column mux, under High-speed process.

CHARACTERISTICS FOR TIMING AND POWER

STDH150 compiled memories are fully optimized under 1.2V ± 0.1V supply voltage. Compiled memory in this section has been characterized using typical-process at 25 degree and 1.2V supply. The values of worst-case and best-case can be calculated by using the local derating factor derived from the following equation:

$$t_{WC}(t_{BC}) = K_{P_local} \times K_{V_local} \times K_{T_local} \times t_{NOM}$$

Where,

t_{WC} is a worst-case propagation delay

t_{BC} is a best-case propagation delay

t_{NOM} is a typical-case propagation delay characterized under typical-process, 25 degree and 1.2V supply

K_{P_local} is a local process factor corresponding to each memory type.

K_{V_local} is a local voltage derating factor corresponding to each memory type.

K_{T_local} is a local temperature derating factor corresponding to each memory type.

Note that K_{P_local}, K_{V_local} and K_{T_local} are only used in compiled memories.

A two-dimensional timing table look-up model has been adopted to yield more accuracy. Based on the combination of input slopes and output loads, the propagation delay is measured from the input crossing 50% V_{DD} to the output crossing 50% V_{DD}. The timing values reported in the tables are also taken from the same voltage level as the switching characteristics with 0.2ns for input slope and 10SL(Standard Load) for output load.

In STDH150, four kinds of power consumptions are available-the dynamic read power consumption, the dynamic write power consumption, the standby power consumption and the static leakage power consumption. The dynamic power consumption for read mode and write mode is measured on the condition that 50% switching activities for all inputs are applied except that OEN (Output Enable Negative) is tied to low. The total power consumption can be calculated by the following equation:

$$P_{total} = ((SA_{read} \times P_{read}) + (SA_{write} \times P_{write})) \times f_{MAX}$$

Where,

P_{total} is the total power consumption in microwatts

P_{read} is the read power consumption in microwatts per MHz

P_{write} is the write power consumption in microwatts per MHz

SA_{read} is the input switching activity under a read access on every cycle

SA_{write} is the input switching activity under a write access on every cycle

f_{MAX} is the memory clock frequency in MHz.

The value of SA_{read} or SA_{write} is between 0 and 1. Also, the sum of SA_{read} and SA_{write} must be less than or equal to 1.

The dynamic power values reported in the tables are also taken from 50% switching activity, SA=0.5. In dual-port or multi-port memory, the power consumption is measured on the condition that only one port is in active mode and the other port is isolated. The power consumption for standby mode is measured on the condition that CSN (Chip Select Negative) is in disable, other inputs are in stable and only CK switches. During standby mode, other inputs such as address, data-in and control pins are stable and only CK is toggled. It means the power consumed on the condition that the memory is deselected.

The static leakage power cosumption is measured on the condition that all inputs including CK and outputs are stable. Because there are no switching activities in memory, the process leakage power is only consumed. The static leakage power consumption is independent of the memory clock frequency.

BUILT-IN SELF TEST AND BUILT-IN REDUNDANCY-ANALYSIS

Samsung provides engineering design services to support Built-In Self-Test (BIST) and Built-In Redundancy-Analysis (BIRA) for the compiled memory.

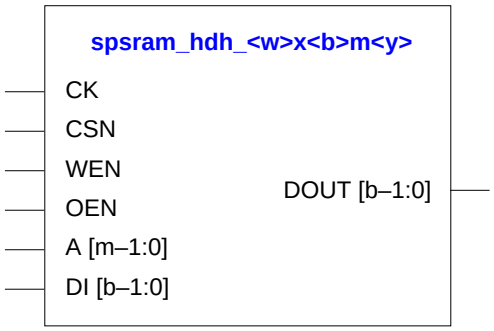
BIST is the recommended test solution for compiled memories. Samsung BIST circuits are designed to detect a set of fault types, such as stuck-at faults, transition faults, coupling faults and address decoder faults that adversely impact the functionality of the memory block. Although several memories of the same types or the different types exist together in a circuit, Samsung supports the BIST for all to the memories as a single architecture.

BIRA design service is also provided to test redundancy RAMs with testers. BIRA tests a SRAM and generates fail information after redundancy analysis. The fail information gathered by tester is automatically processed and transferred to the laser repair machine. For multiple redundancy RAMs, Samsung BIRA architecture has an integration module to support parallel testing, minimum test pin usage and optimized logic tester interface.

For more detailed information regarding to the BIST and BIRA, please contact your local Samsung and Design Center or Samsung's worldwide headquarters.

NOTE

Logic Symbol



NOTES:
1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

SPSRAM_HDH is a single-port synchronous static RAM which is provided as a compiler. SPSRAM_HDH is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAM_HDH Function Table

CK	CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

SPSRAM_HDH

High-Density Single-Port Synchronous Static RAM

Parameter Description

SPSRAM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

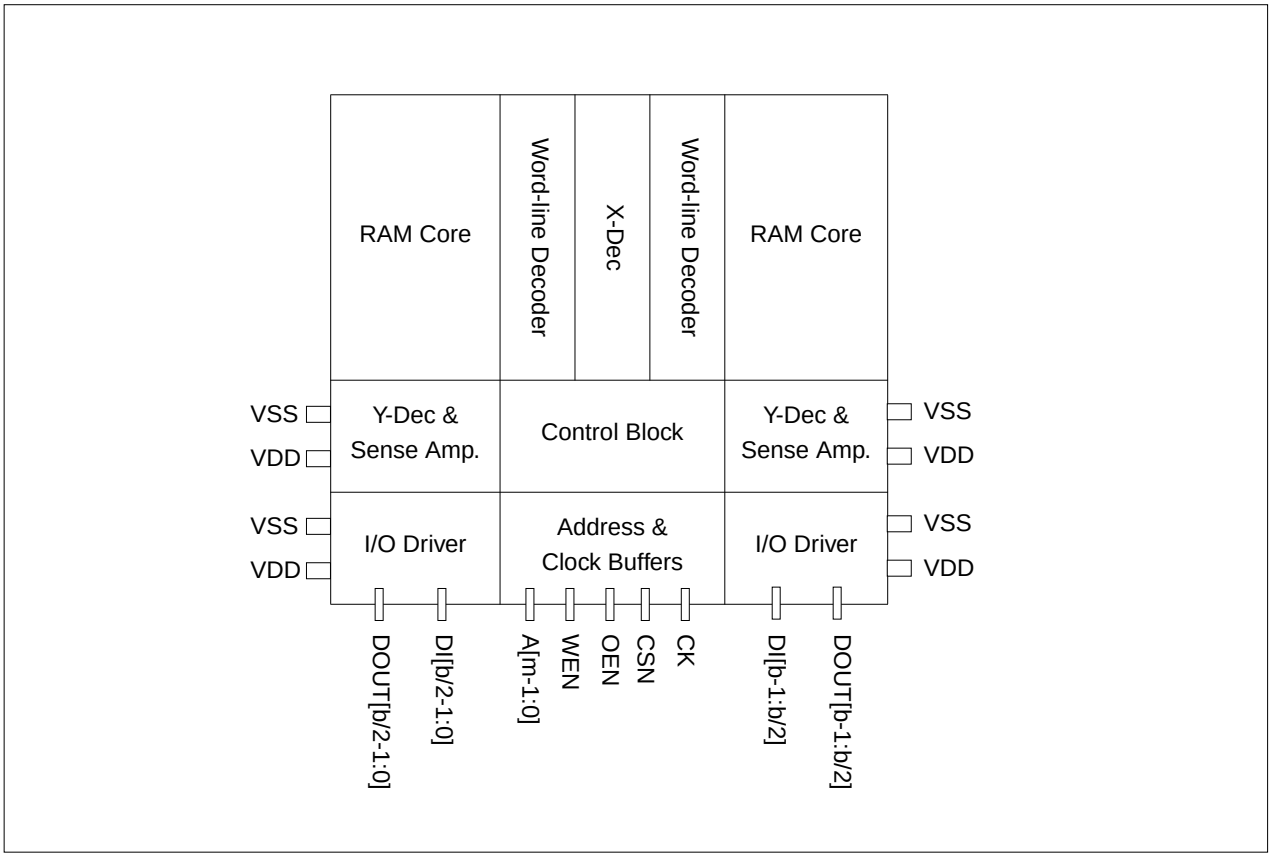
Unit: [SL]

CK	CSN	WEN	OEN	A	DI	DOUT
11.80	5.90	7.60	8.40	5.70	3.60	12.10

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagrams

SPSRAM_HDH has the dual-array architecture. In this architecture, the multiple power ports are located on the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in SPSRAM_HDH is permitted only for Metal-5 or upper layers.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPSRAM_HDH.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (µW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (µA)			
Static_leakage	The static leakage power consumption while CSN is high and other signals including CK are in stable.		
Definition for Area (µm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**128**	**512**	**512**	**512**	**2048**	**2048**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
Timing (ns)								
t_{cyc}	1.00	0.99	0.98	1.07	1.07	1.07	1.58	1.62
t_{ckl}	0.34	0.34	0.33	0.36	0.36	0.36	0.37	0.37
t_{ckh}	0.32	0.32	0.32	0.31	0.31	0.30	0.31	0.30
t_{as}	0.36	0.36	0.35	0.38	0.38	0.38	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.27	0.23	0.30	0.28	0.24	0.28	0.24
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.24	0.22	0.19	0.24	0.23	0.21	0.23	0.20
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.77	0.79	0.82	0.84	0.86	0.90	1.41	1.42
t_{da}	0.63	0.64	0.66	0.67	0.69	0.73	1.24	1.27
t_{dz}	0.12	0.14	0.18	0.12	0.14	0.18	0.14	0.18
t_{zd}	0.22	0.24	0.28	0.22	0.24	0.28	0.24	0.28
t_{od}	0.30	0.32	0.36	0.30	0.32	0.36	0.32	0.36
Power (µW/MHz)								
Power_read	28.34	50.53	94.91	28.14	49.63	92.61	66.30	124.20
Power_write	23.44	40.84	75.64	30.35	54.07	101.51	77.68	147.18
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	40.540	56.722	89.085	91.998	119.570	174.713	370.962	517.224
Area (µm)								
Width	251.61	431.04	789.88	251.61	431.04	789.88	431.04	789.88
Height	149.44	149.44	149.44	318.40	318.40	318.40	994.24	994.24

NOTES:

1. Standby power is measured on the condition that SPSRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SPSRAM_HDH

High-Density Single-Port Synchronous Static RAM

Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**256**	**1024**	**1024**	**1024**	**4096**	**4096**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{cyc}	1.00	0.99	0.97	1.08	1.09	1.10	1.58	1.63
t_{ckl}	0.35	0.35	0.35	0.36	0.36	0.37	0.37	0.37
t_{ckh}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{as}	0.37	0.37	0.37	0.38	0.38	0.39	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.29	0.26	0.30	0.29	0.26	0.29	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.24	0.23	0.21	0.24	0.23	0.21	0.23	0.21
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.78	0.80	0.83	0.85	0.88	0.92	1.42	1.45
t_{da}	0.61	0.63	0.66	0.70	0.71	0.75	1.25	1.26
t_{dz}	0.11	0.13	0.16	0.11	0.13	0.16	0.16	0.16
t_{zd}	0.21	0.23	0.26	0.21	0.23	0.26	0.26	0.26
t_{od}	0.29	0.31	0.34	0.29	0.31	0.34	0.35	0.37
Power (µW/MHz)								
Power_read	24.07	41.96	77.74	25.96	45.29	83.95	58.96	109.64
Power_write	20.25	34.46	62.89	22.13	37.92	69.51	62.13	116.11
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	37.618	50.876	77.393	89.076	113.724	163.021	365.116	505.533
Area (µm)								
Width	251.55	430.99	789.88	251.55	430.99	789.88	430.99	789.88
Height	139.44	139.44	139.44	308.40	308.40	308.40	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**2048**	**2048**	**4096**	**4096**	**8192**	**8192**
bpw	**16**	**32**	**16**	**32**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{cyc}	1.00	0.99	1.05	1.03	1.18	1.19	1.59	1.64
t_{ckl}	0.34	0.33	0.34	0.31	0.37	0.37	0.37	0.37
t_{ckh}	0.32	0.33	0.31	0.31	0.31	0.31	0.31	0.31
t_{as}	0.36	0.35	0.36	0.33	0.39	0.39	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.26	0.29	0.27	0.29	0.27	0.29	0.27
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.22	0.19	0.23	0.20	0.23	0.21	0.23	0.21
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.80	0.83	0.87	0.91	0.99	1.00	1.45	1.48
t_{da}	0.65	0.67	0.70	0.73	0.85	0.85	1.28	1.27
t_{dz}	0.12	0.15	0.12	0.15	0.12	0.15	0.12	0.15
t_{zd}	0.22	0.25	0.22	0.25	0.22	0.25	0.22	0.25
t_{od}	0.31	0.34	0.32	0.32	0.32	0.37	0.32	0.32
Power (µW/MHz)								
Power_read	40.51	75.26	36.30	65.82	40.99	74.76	53.21	98.07
Power_write	34.30	62.64	37.88	69.16	45.34	83.86	48.30	90.12
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	47.953	71.548	110.801	157.176	194.599	271.346	362.193	499.688
Area (µm)								
Width	430.90	71.548	430.90	789.88	430.90	789.88	430.90	789.88
Height	139.44	139.44	308.40	308.40	533.68	533.68	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

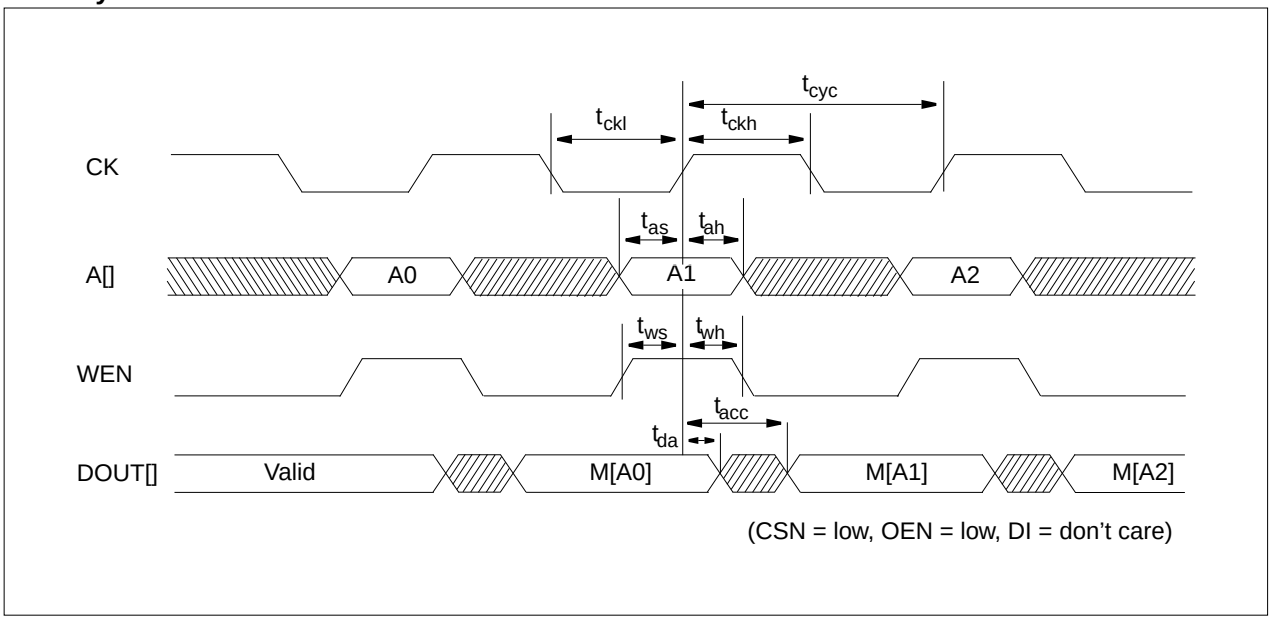
Parameters								
words	**1024**	**1024**	**4096**	**4096**	**8192**	**8192**	**16384**	**16384**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{cyc}	1.01	1.02	1.06	1.07	1.20	1.23	1.60	1.63
t_{ckl}	0.35	0.35	0.36	0.37	0.37	0.37	0.35	0.33
t_{ckh}	0.31	0.31	0.31	0.31	0.31	0.31	0.32	0.34
t_{as}	0.37	0.37	0.38	0.39	0.39	0.39	0.37	0.35
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.28	0.30	0.28	0.30	0.28	0.28	0.25
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.23	0.20	0.23	0.21	0.23	0.21	0.21	0.16
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.85	0.90	0.93	0.95	1.06	1.11	1.47	1.50
t_{da}	0.68	0.69	0.75	0.76	0.91	0.87	1.27	1.29
t_{dz}	0.12	0.14	0.12	0.14	0.12	0.14	0.12	0.14
t_{zd}	0.22	0.24	0.22	0.24	0.22	0.24	0.22	0.24
t_{od}	0.30	0.33	0.29	0.31	0.29	0.31	0.29	0.31
Power (µW/MHz)								
Power_read	31.54	56.63	36.36	66.33	42.79	78.91	51.17	94.31
Power_write	32.79	59.87	36.16	66.36	38.10	69.10	47.81	88.99
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	46.492	68.625	109.340	154.253	193.137	268.424	360.732	496.765
Area (µm)								
Width	430.71	789.88	430.71	789.88	430.71	789.88	430.71	789.88
Height	139.44	139.44	308.40	308.40	533.68	533.68	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

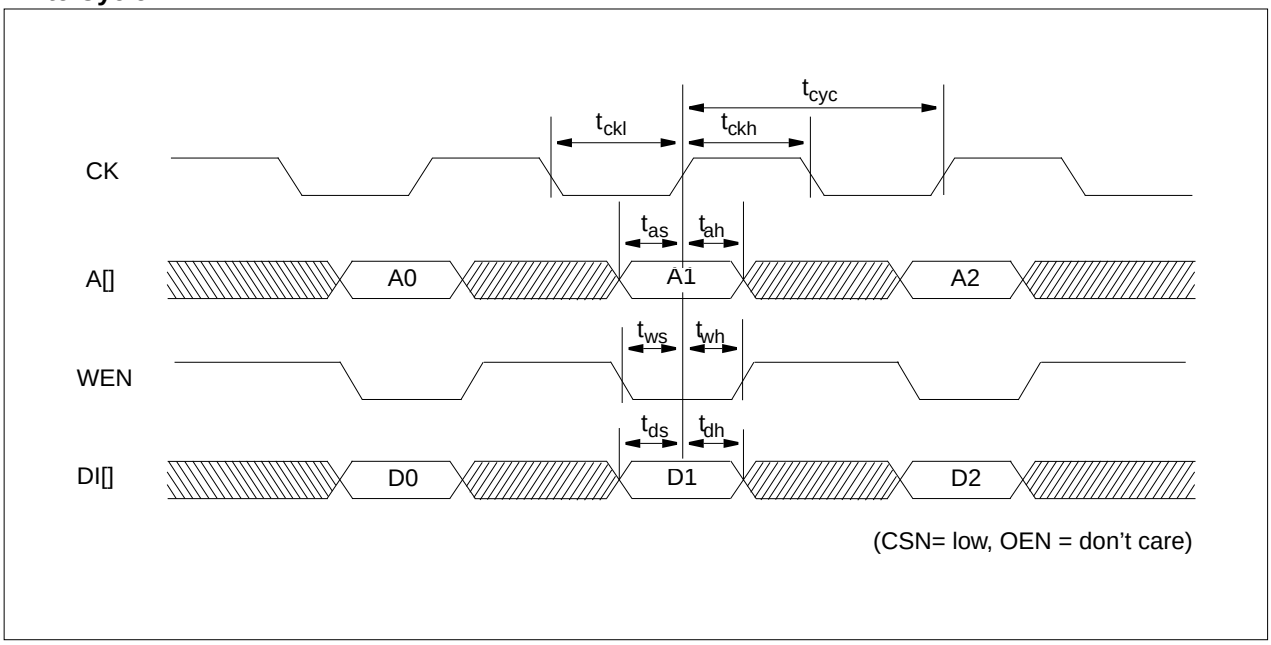
Timing Diagrams

Read Cycle



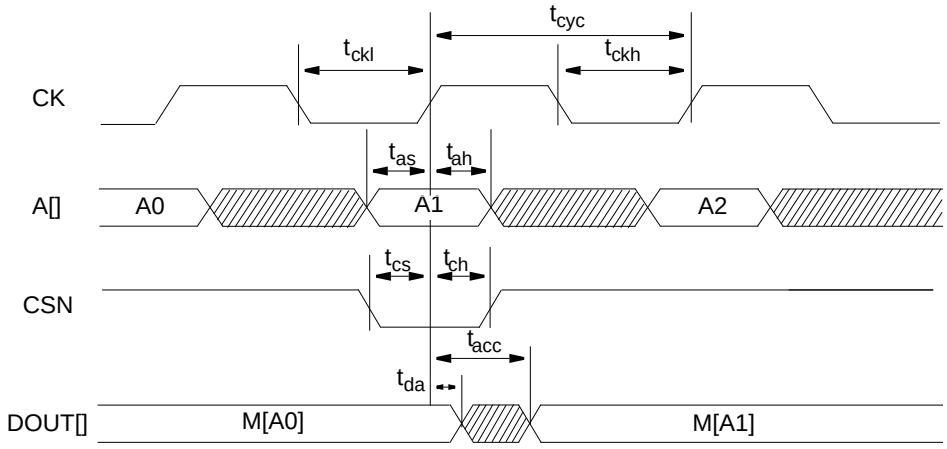
(CSN = low, OEN = low, DI = don't care)

Write Cycle



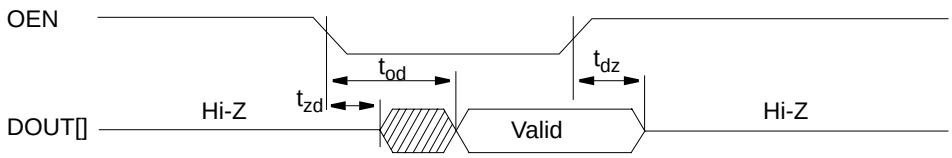
(CSN= low, OEN = don't care)

Read Cycle with CSN Controlled



(OEN = low, WEN = high, DI = don’t care)

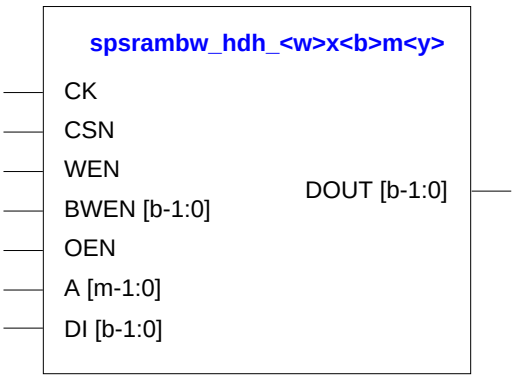
OEN Controlled Output Enable



(CK, A, WEN, DI, CSN = don’t care)

NOTE: “don't care” means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Bit-Write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to128 number of bit per word

Function Description

SPSRAMBW_HDH is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW_HDH is intended for use in high-density applications. Basically, its functionality is exactly same as SPSRAM_HDH except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. When the individual bit of BWEN[] is low, the data on the corresponding write data bit of DI[] are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HDH. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMBW_HDH Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

SPSRAMBW_HDH

High-Density Single-Port Synchronous Static RAM with Bit-Write

Parameter Description

SPSRAMBW_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux =(y) 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

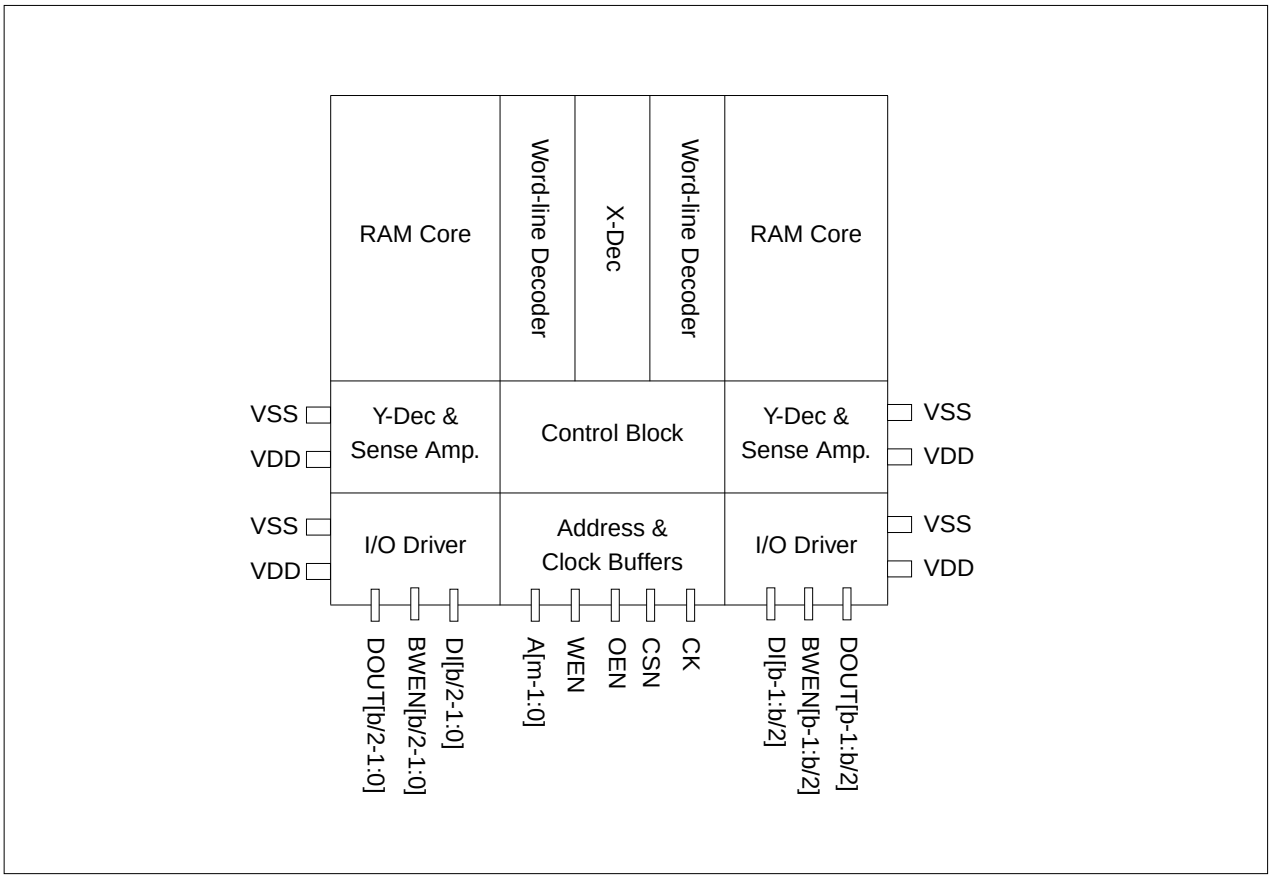
Unit: [SL]

CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
11.80	5.90	7.60	3.60	8.40	5.70	3.60	12.10

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagrams

SPSRAMBW_HDH has the dual-array architecture. In this architecture, the multiple power ports are located on the bottom edge of both right-and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



SPSRAMBW_HDH

High-Density Single-Port Synchronous Static RAM with Bit-Write

Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in SPSRAMBW_HDH is permitted for only Metal-5 or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMBW_HDH.

4. A byte-write or word-write operation with SPSRAMBW_HDH. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_HDH. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time

Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.

Definition for Static Leakage Current Consumption (μA)	
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.

Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

SPSRAMBW_HDH

High-Density Single-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=4** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**128**	**512**	**512**	**512**	**2048**	**2048**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
Timing (ns)								
t_{cyc}	1.00	0.99	0.98	1.07	1.07	1.07	1.58	1.62
t_{ckl}	0.34	0.34	0.33	0.36	0.36	0.36	0.37	0.37
t_{ckh}	0.32	0.32	0.32	0.31	0.31	0.30	0.31	0.30
t_{as}	0.36	0.36	0.35	0.38	0.38	0.38	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.27	0.23	0.30	0.28	0.24	0.28	0.24
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.24	0.22	0.19	0.24	0.23	0.21	0.23	0.20
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.26	0.24	0.19	0.27	0.25	0.21	0.25	0.21
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.77	0.79	0.82	0.84	0.86	0.90	1.41	1.42
t_{da}	0.63	0.64	0.66	0.67	0.69	0.73	1.24	1.27
t_{dz}	0.12	0.14	0.18	0.12	0.14	0.18	0.14	0.18
t_{zd}	0.22	0.24	0.28	0.22	0.24	0.28	0.24	0.28
t_{od}	0.30	0.32	0.36	0.30	0.32	0.36	0.32	0.36
Power (µW/MHz)								
Power_read	28.34	50.53	94.91	28.14	49.63	92.61	66.30	124.20
Power_write	24.42	42.84	79.66	31.33	56.05	105.49	79.59	151.03
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	40.540	56.722	89.085	91.998	119.570	174.713	370.962	517.224
Area (µm)								
Width	251.61	431.04	789.88	251.61	431.04	789.88	431.04	789.88
Height	149.44	149.44	149.44	318.40	318.40	318.40	994.24	994.24

NOTES:

1. Standby power is measured on the condition that SPSRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**256**	**1024**	**1024**	**1024**	**4096**	**4096**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{cyc}	1.00	0.99	0.97	1.08	1.09	1.10	1.58	1.63
t_{ckl}	0.35	0.35	0.35	0.36	0.36	0.37	0.37	0.37
t_{ckh}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{as}	0.37	0.37	0.37	0.38	0.38	0.39	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.29	0.26	0.30	0.29	0.26	0.29	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.24	0.23	0.21	0.24	0.23	0.21	0.23	0.21
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.26	0.22	0.28	0.26	0.22	0.26	0.23
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.78	0.80	0.83	0.85	0.88	0.92	1.42	1.45
t_{da}	0.61	0.63	0.66	0.70	0.71	0.75	1.25	1.26
t_{dz}	0.11	0.13	0.16	0.11	0.13	0.16	0.16	0.16
t_{zd}	0.21	0.23	0.26	0.21	0.23	0.26	0.26	0.26
t_{od}	0.29	0.31	0.34	0.29	0.31	0.34	0.35	0.37
Power (µW/MHz)								
Power_read	24.07	41.96	77.74	25.96	45.29	83.95	58.96	109.64
Power_write	20.71	35.43	64.86	22.59	38.88	71.45	63.10	118.08
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	37.618	50.876	77.393	89.076	113.724	163.021	365.116	505.533
Area (µm)								
Width	251.55	430.99	789.88	251.55	430.99	789.88	430.99	789.88
Height	139.44	139.44	139.44	308.40	308.40	308.40	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**2048**	**2048**	**4096**	**4096**	**8192**	**8192**
bpw	**16**	**32**	**16**	**32**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{cyc}	1.00	0.99	1.05	1.03	1.18	1.19	1.59	1.64
t_{ckl}	0.34	0.33	0.34	0.31	0.37	0.37	0.37	0.37
t_{ckh}	0.32	0.33	0.31	0.31	0.31	0.31	0.31	0.31
t_{as}	0.36	0.35	0.36	0.33	0.39	0.39	0.39	0.39
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.26	0.29	0.27	0.29	0.27	0.29	0.27
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.22	0.19	0.23	0.20	0.23	0.21	0.23	0.21
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.24	0.29	0.26	0.28	0.26	0.28	0.26
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.80	0.83	0.87	0.91	0.99	1.00	1.45	1.48
t_{da}	0.65	0.67	0.70	0.73	0.85	0.85	1.28	1.27
t_{dz}	0.12	0.15	0.12	0.15	0.12	0.15	0.12	0.15
t_{zd}	0.22	0.25	0.22	0.25	0.22	0.25	0.22	0.25
t_{od}	0.31	0.34	0.32	0.32	0.32	0.37	0.32	0.32
Power (µW/MHz)								
Power_read	40.51	75.26	36.30	65.82	40.99	74.76	53.21	98.07
Power_write	34.77	63.60	38.34	70.12	45.84	84.89	49.75	91.06
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	47.953	71.548	110.801	157.176	194.599	271.346	362.193	499.688
Area (µm)								
Width	430.90	789.88	430.90	789.88	430.90	789.88	430.90	789.88
Height	139.44	139.44	308.40	308.40	533.68	533.68	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

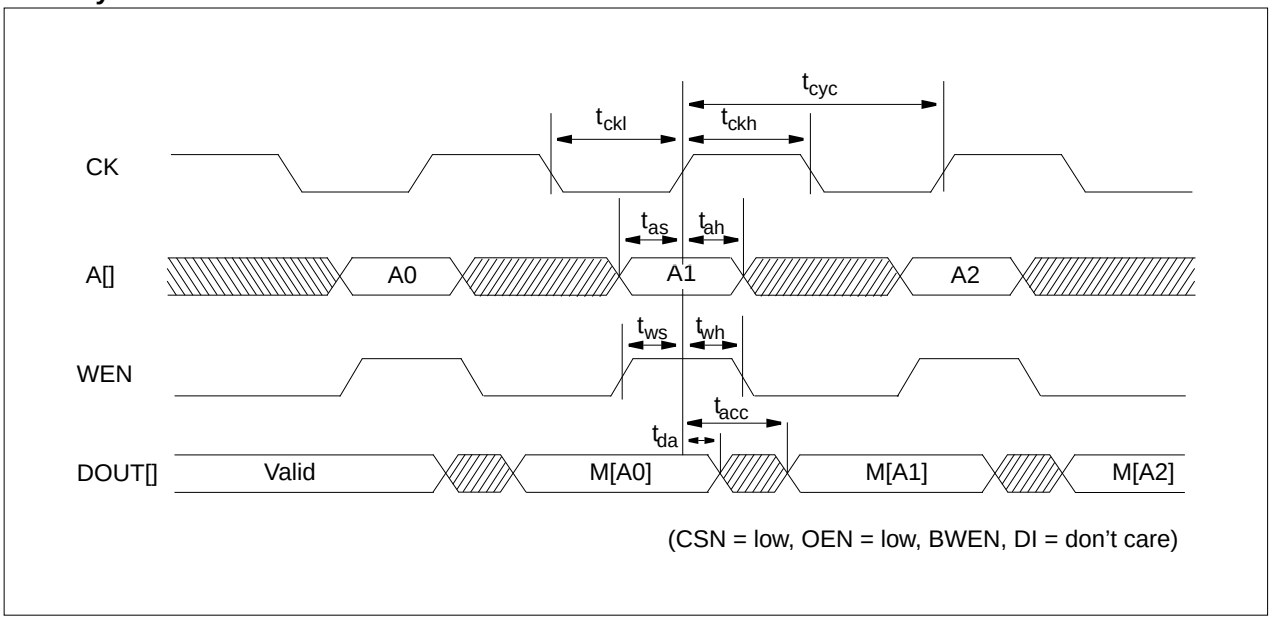
Parameters								
words	**1024**	**1024**	**4096**	**4096**	**8192**	**8192**	**16384**	**16384**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{cyc}	1.01	1.02	1.06	1.07	1.20	1.23	1.60	1.63
t_{ckl}	0.35	0.35	0.36	0.37	0.37	0.37	0.35	0.33
t_{ckh}	0.31	0.31	0.31	0.31	0.31	0.31	0.32	0.34
t_{as}	0.37	0.37	0.38	0.39	0.39	0.39	0.37	0.35
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.30	0.28	0.30	0.28	0.30	0.28	0.28	0.25
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.23	0.20	0.23	0.21	0.23	0.21	0.21	0.16
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.30	0.28	0.30	0.28	0.30	0.28	0.29	0.25
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.85	0.90	0.93	0.95	1.06	1.11	1.47	1.50
t_{da}	0.68	0.69	0.75	0.76	0.91	0.87	1.27	1.29
t_{dz}	0.12	0.14	0.12	0.14	0.12	0.14	0.12	0.14
t_{zd}	0.22	0.24	0.22	0.24	0.22	0.24	0.22	0.24
t_{od}	0.30	0.33	0.29	0.31	0.29	0.31	0.29	0.31
Power (µW/MHz)								
Power_read	31.54	56.63	36.36	66.33	42.79	78.91	51.17	94.31
Power_write	33.01	60.35	36.40	66.87	38.32	69.57	48.04	89.48
Power_standby	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Static Leakage (µA)								
Static_leakage	46.492	68.625	109.340	154.253	193.137	268.424	360.732	496.765
Area (µm)								
Width	430.71	789.88	430.71	789.88	430.71	789.88	430.71	789.88
Height	139.44	139.44	308.40	308.40	533.68	533.68	984.24	984.24

NOTES:

1. Standby power is measured on the condition that SPSRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

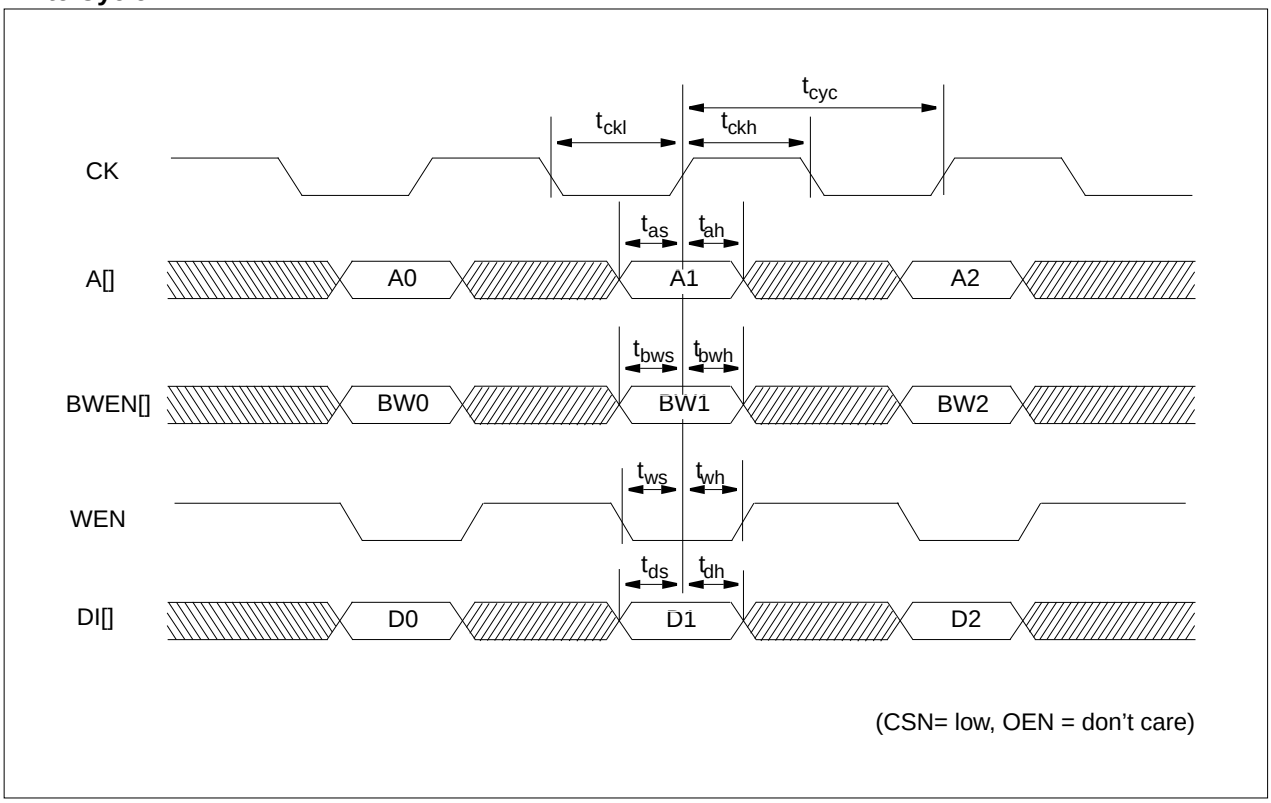
Timing Diagrams

Read Cycle



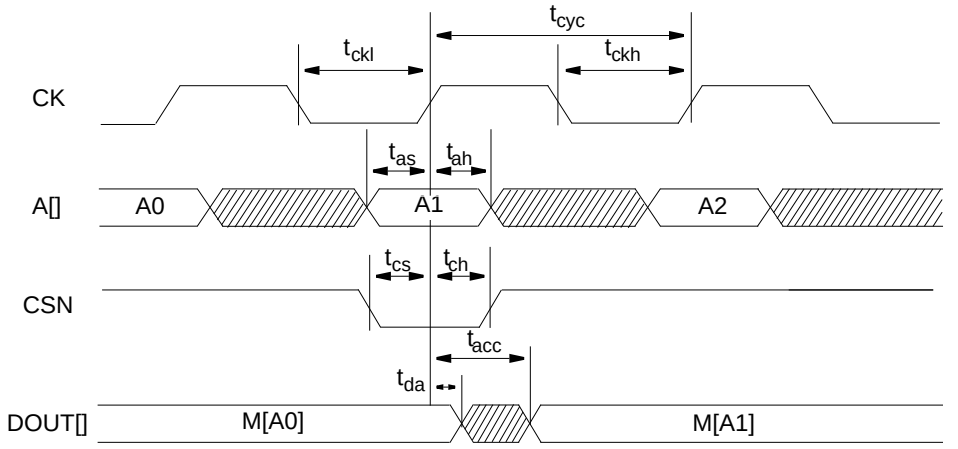
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle



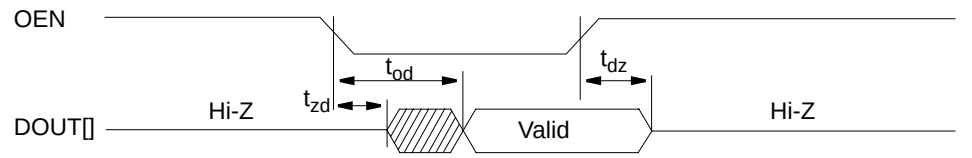
(CSN= low, OEN = don't care)

Read Cycle with CSN Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

OEN Controlled Output Enable



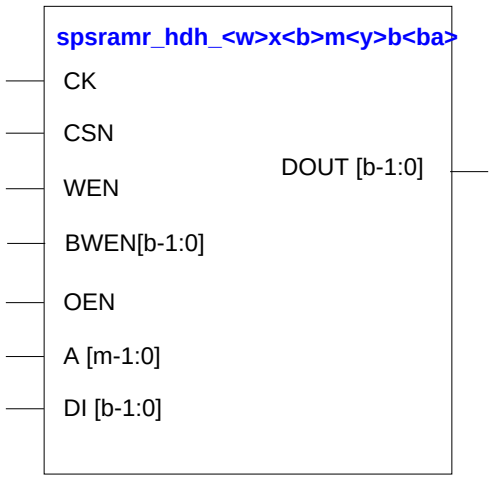
(CSN, CK, A, WEN, BWEN, DI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

SPSRAMR_HDH

High-Density Single-Port Synchronous Static RAM with Redundancy

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- High-capacity application
- Heuristic row-redundancy available
- Bit-write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- 64Kbits ~ 1Mbits capacity
- 2K ~ 32K number of words
- 8 ~ 128 number of bits per word

Function Description

SPSRAMR_HDH is a repairable single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMR_HDH is intended for use in high-capacity applications. Basically, its functionality is exactly same as SPSRAMBW_HDH. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. When the individual bit of BWEN[] is low, the data on the corresponding write data bit of DI[] are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HDH. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMR_HDH Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L/H	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

SPSRAMR_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	2048	4096	8192
		Max	4096	8192	16384
		Step	64	128	256
	ba = 2	Min	4096	8192	16384
		Max	8192	16384	32768
		Step	128	256	512
Bpw (b)		Min	32	16	8
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

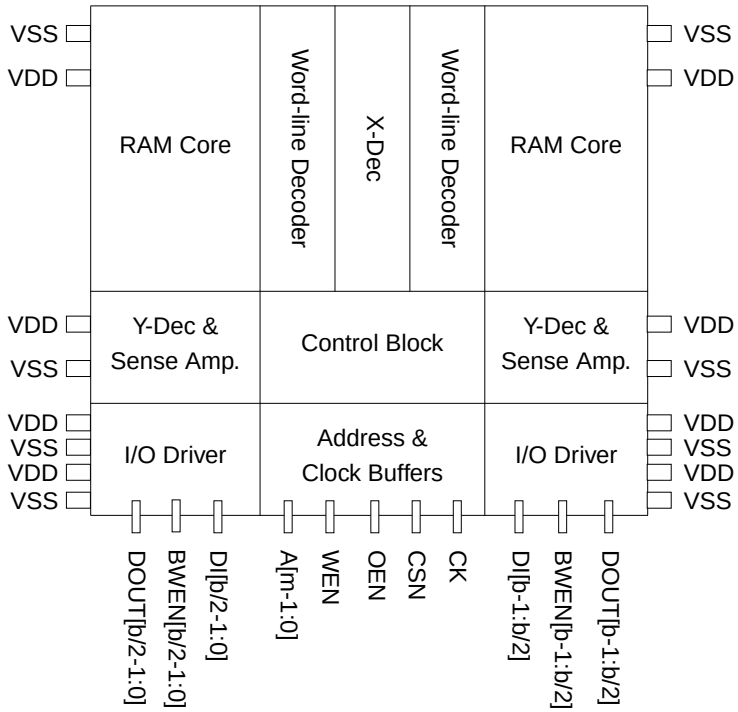
	CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
ba = 1	7.28	1.75	4.5	3.4	3.2	4.7	3.4	17.7
ba = 2	7.28	1.75	4.5	3.4	3.2	4.7	3.4	17.7

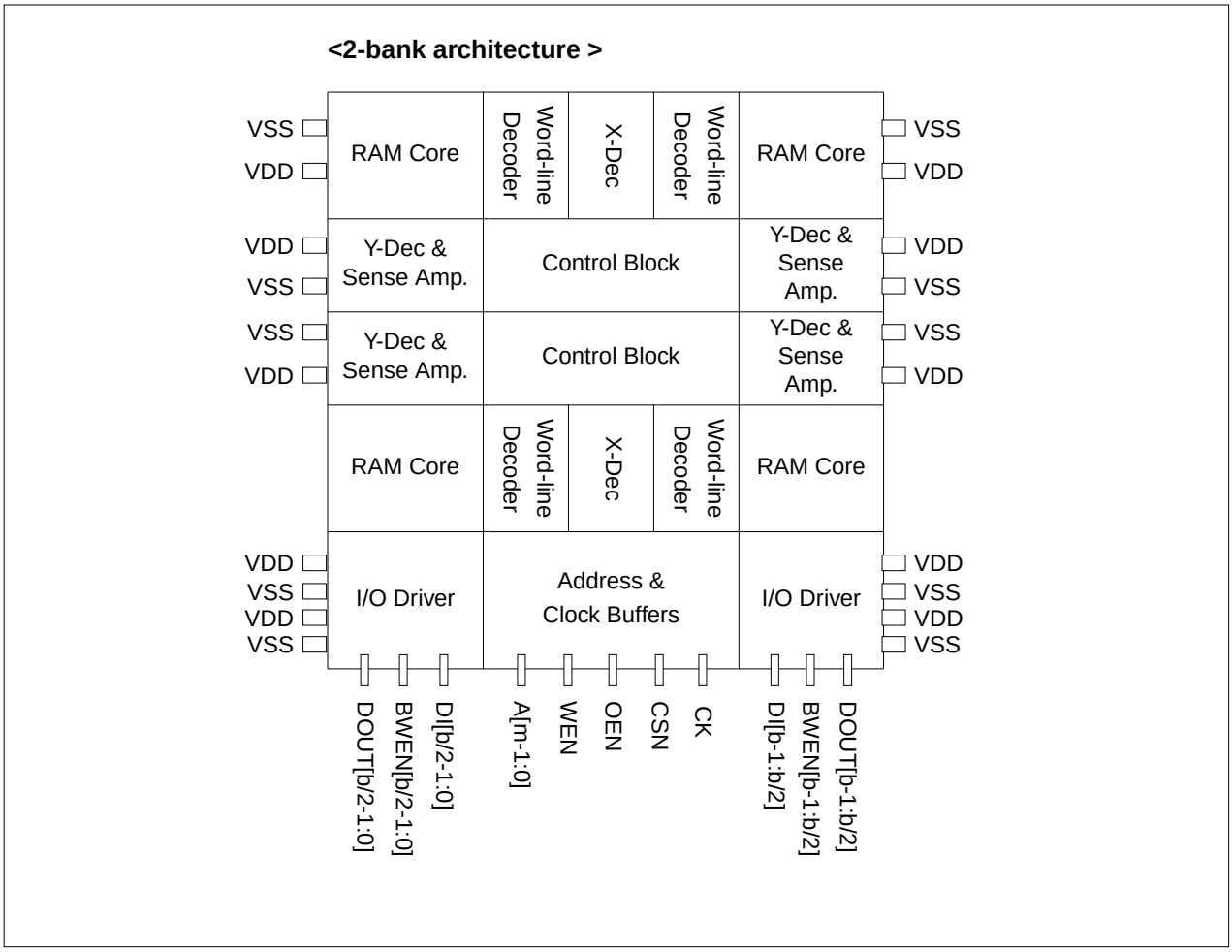
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

Block Diagrams

SPSRAMR_HDH has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAMR_HDH compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. Regardless of architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of (both right-and left-sides) of memory and all signal ports are located on the bottom sides of memory.

<1-bank architecture>





Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in SPSRAMR_HDH is permitted for only Metal-5 or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMR_HDH.

4. A byte-write or word-write operation with SPSRAMR_HDH. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAMR_HDH. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (μA)			
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**2048**	**2048**	**2048**	**4096**	**4096**	**4096**	**8192**	**8192**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
bank	**1**	**1**	**1**	**1**	**1**	**1**	**2**	**2**
Timing (ns)								
t_{cyc}	1.44	1.48	1.50	1.76	1.79	1.84	1.91	1.95
t_{ckl}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ckh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{as}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.41	0.40	0.39	0.41	0.40	0.38	0.40	0.38
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.43	0.42	0.41	0.43	0.42	0.41	0.42	0.40
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.21	1.23	1.27	1.54	1.57	1.62	1.68	1.73
t_{da}	0.85	0.86	0.86	1.17	1.19	1.21	1.24	1.25
t_{dz}	0.09	0.10	0.11	0.09	0.10	0.11	0.10	0.11
t_{zd}	0.19	0.20	0.21	0.19	0.20	0.21	0.20	0.21
t_{od}	0.22	0.25	0.30	0.22	0.25	0.30	0.25	0.30
Power (µW/MHz)								
Power_read	56.25	87.47	182.90	66.12	118.00	221.76	161.74	302.43
Power_write	60.61	107.70	201.87	71.44	129.42	245.39	168.13	315.72
Power_standby	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
Static Leakage (µA)								
Static_leakage	309.598	413.468	621.209	513.232	679.727	1012.718	1216.002	1803.251
Area (µm)								
Width	490.82	849.62	1567.22	490.82	849.62	1567.22	849.62	1567.22
Height	565.48	570.17	579.56	1016.04	1025.43	1044.20	2015.77	2053.32

NOTES:

1. Standby power is measured on the condition that SPSRAMR_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**4096**	**4096**	**4096**	**8192**	**8192**	**8192**	**16384**	**16384**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
bank	**1**	**1**	**1**	**1**	**1**	**1**	**2**	**2**
Timing (ns)								
t_{cyc}	1.43	1.45	1.49	1.78	1.80	1.83	1.90	1.94
t_{ckl}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ckh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{as}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.41	0.40	0.39	0.41	0.41	0.39	0.40	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.43	0.43	0.41	0.43	0.43	0.41	0.42	0.41
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.20	1.22	1.27	1.55	1.57	1.61	1.68	1.72
t_{da}	0.85	0.85	0.86	1.20	1.20	1.21	1.24	1.25
t_{dz}	0.09	0.09	0.10	0.09	0.09	0.10	0.09	0.10
t_{zd}	0.19	0.19	0.20	0.19	0.19	0.20	0.19	0.20
t_{od}	0.22	0.24	0.27	0.22	0.24	0.27	0.24	0.27
Power (µW/MHz)								
Power_read	49.14	84.08	153.95	58.99	103.56	192.68	140.04	258.90
Power_write	50.19	86.65	159.58	57.31	100.80	187.79	135.85	250.74
Power_standby	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
Static Leakage (µA)								
Static_leakage	303.352	400.976	596.225	506.985	667.235	987.734	1203.510	1778.267
Area (µm)								
Width	490.82	849.62	1567.22	490.82	849.62	1567.22	849.62	1567.22
Height	565.48	570.17	579.56	1016.04	1025.43	1044.20	2015.77	2053.32

NOTES:

1. Standby power is measured on the condition that SPSRAMR_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

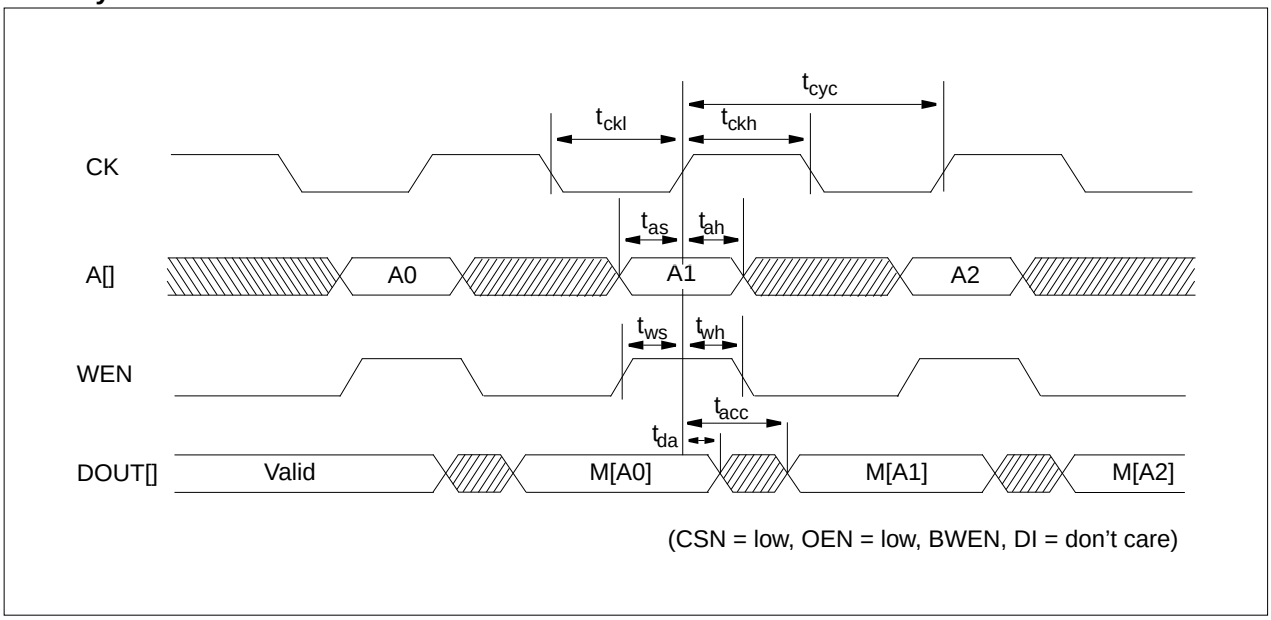
*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**8192**	**8192**	**8192**	**16384**	**16384**	**16384**	**32768**	**32768**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
bank	**1**	**1**	**1**	**1**	**1**	**1**	**2**	**2**
Timing (ns)								
t_{cyc}	1.44	1.46	1.50	1.79	1.81	1.84	1.92	1.96
t_{ckl}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ckh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{as}	0.40	0.40	0.40	0.40	0.40	0.40	0.41	0.41
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.42	0.41	0.40	0.41	0.41	0.40	0.41	0.40
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.44	0.43	0.42	0.44	0.43	0.42	0.43	0.42
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.22	1.24	1.28	1.56	1.58	1.62	1.70	1.74
t_{da}	0.85	0.86	0.86	1.20	1.20	1.20	1.24	1.25
t_{dz}	0.09	0.09	0.10	0.09	0.09	0.10	0.09	0.10
t_{zd}	0.10	0.13	0.20	0.19	0.13	0.20	0.13	0.20
t_{od}	0.22	0.23	0.26	0.22	0.23	0.26	0.23	0.26
Power (µW/MHz)								
Power_read	45.33	76.65	139.29	55.22	96.24	178.30	128.69	236.29
Power_write	44.65	75.40	136.91	49.66	85.61	157.50	117.88	214.95
Power_standby	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
Static Leakage (µA)								
Static_leakage	300.229	394.730	583.733	503.862	660.989	975.242	1197.264	1765.775
Area (µm)								
Width	490.82	849.62	1567.22	490.82	849.62	1567.22	849.62	1567.22
Height	565.48	570.17	579.56	1016.04	1025.43	1044.20	2015.77	2053.32

NOTES:
1. Standby power is measured on the condition that SPSRAMR_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

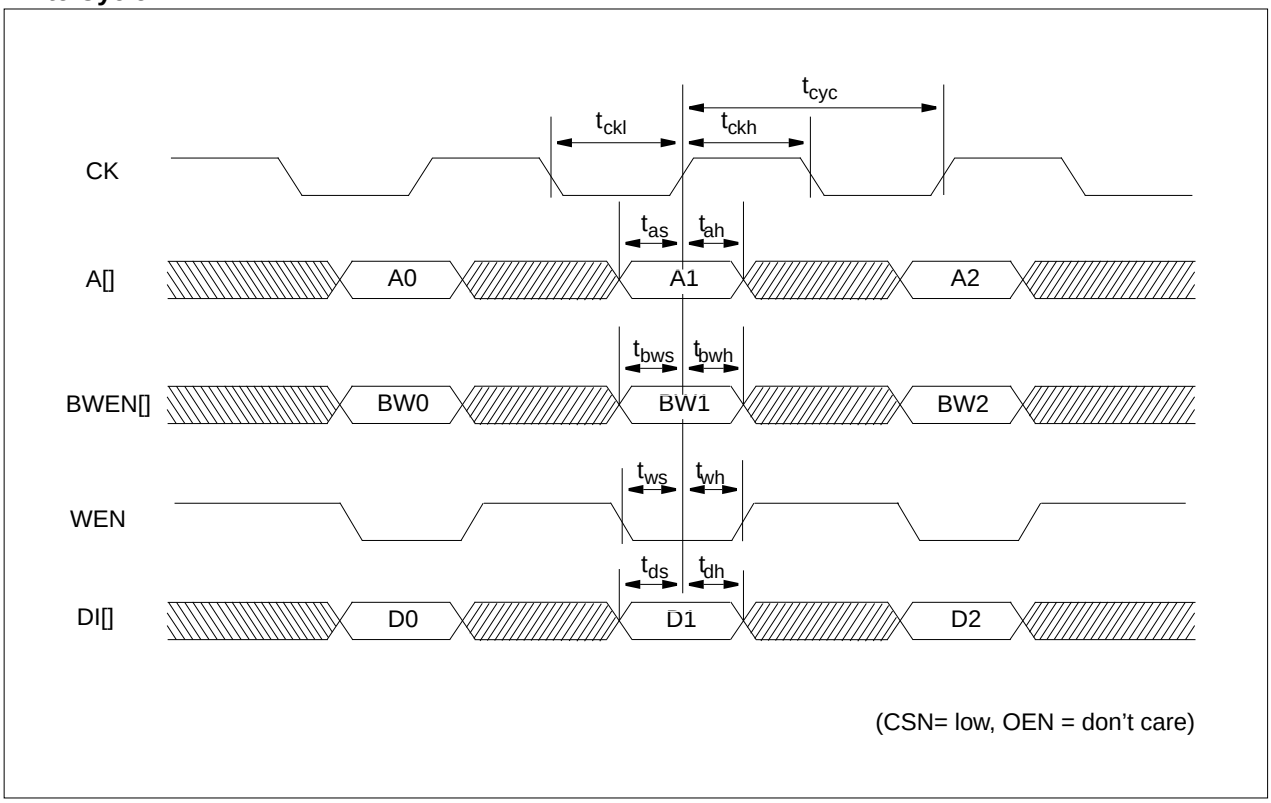
Timing Diagrams

Read Cycle



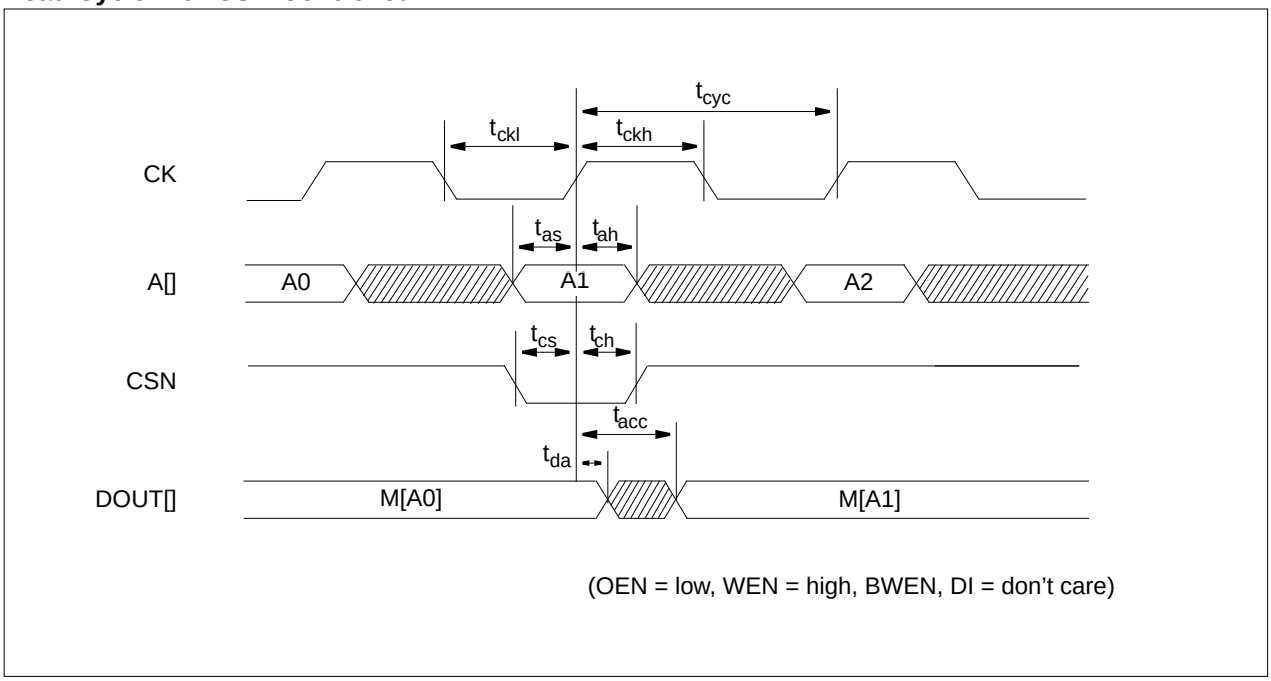
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle

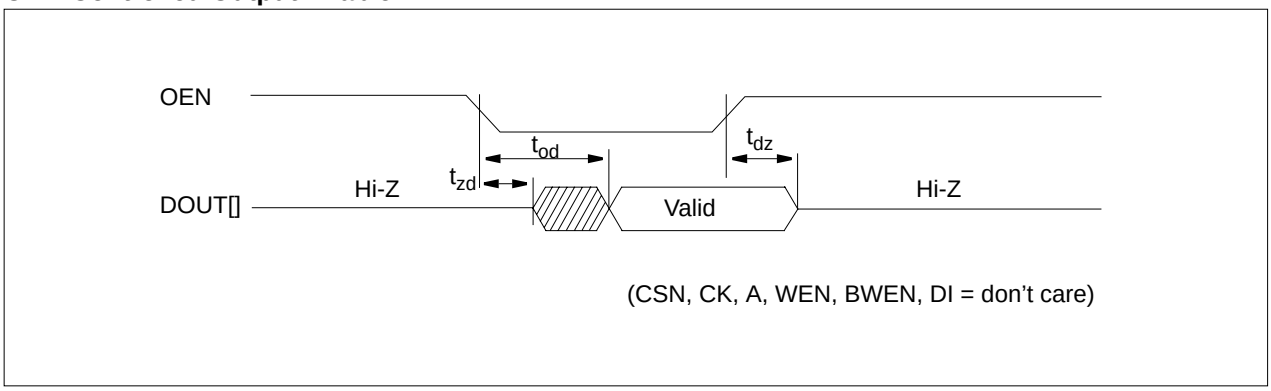


(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



OEN-Controlled Output Enable

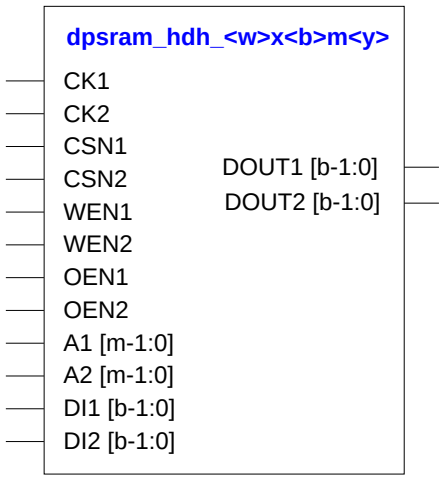


NOTE: "don't care" means the condition that these pins are in normal operation mode.

DPSRAM_HDH

High-Density Dual-Port Synchronous Static RAM

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM_HDH is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM_HDH is intended for use in high-density applications. Each port is fully independent. On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. The data on DI1[](DI2[]) is written into the memory location specified on A1[](A2[]). During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAM_HDH Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

Parameter Description

DPSRAM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [] A2 []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [] DI2 []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [] DOUT2 []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
7.83	2.42	2.42	2.35	2.42	3.37	6.55

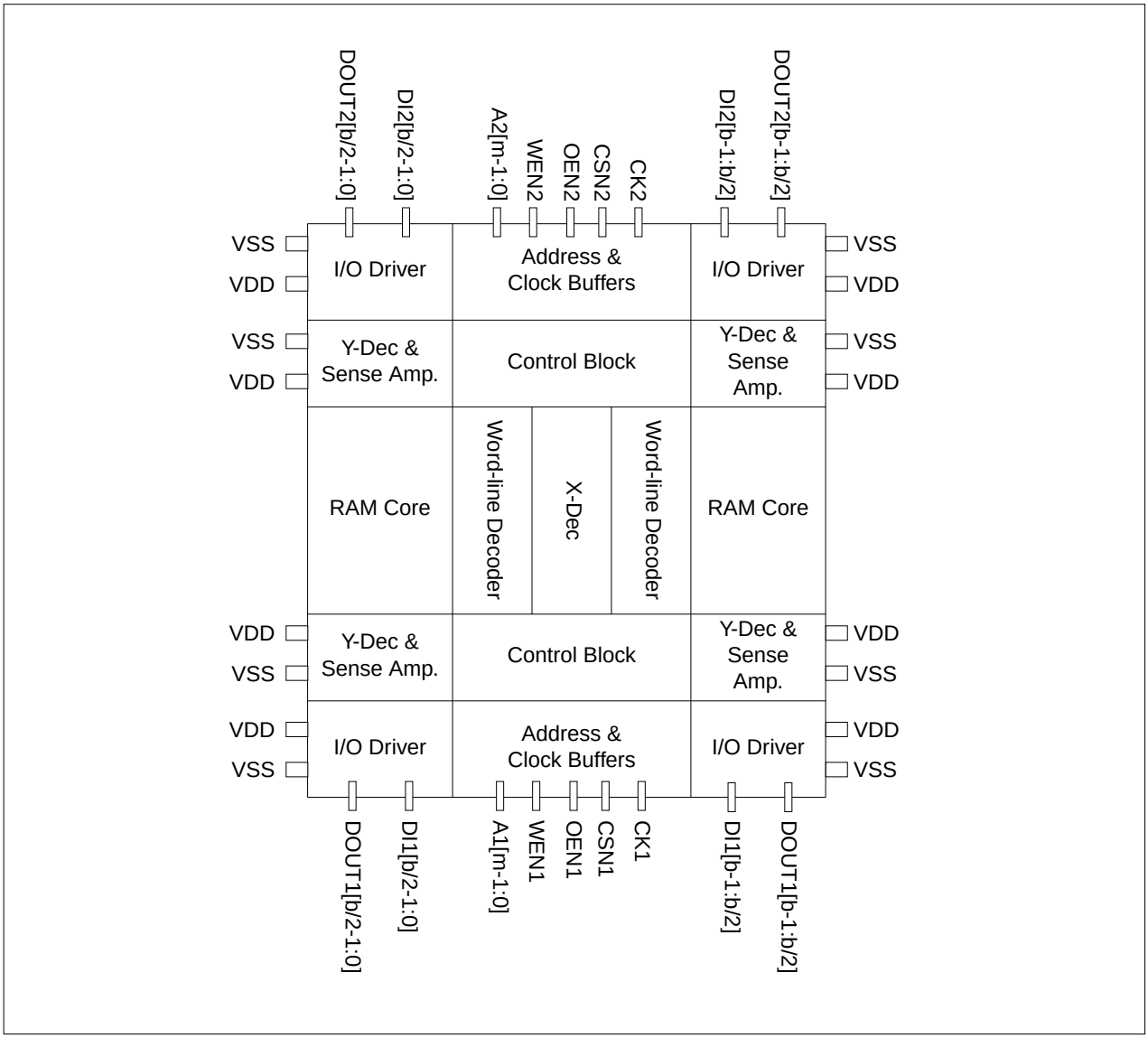
NOTE: Each pin's capacitance is exactly same regardless of available mux types.

DPSRAM_HDH

High-Density Dual-Port Synchronous Static RAM

Block Diagram

DPSRAM_HDH supports only 1-bank architecture. The multiple power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAM_HDH has two symmetrical signal ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in DPSRAM_HDH is permitted for Metal-5 or upper metal layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAM_HDH.

4. Contention mode in same address access. In DPSRAM_HDH, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operations, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM_HDH has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

DPSRAM_HDH

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Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (μA)			
Static_leakage	The static leakage power consumption while CSN is high and other signals including CK are in stable.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**64**	**256**	**256**	**256**	**1024**	**1024**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
Timing (ns)								
t_{cyc}	0.94	0.98	1.00	0.95	0.98	1.01	1.28	1.31
t_{ckl}	0.27	0.27	0.33	0.27	0.27	0.33	0.27	0.33
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.13	0.14
t_{cc}	0.48	0.52	0.57	0.48	0.52	0.58	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.25	0.26	0.28	0.25	0.26	0.25	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.74	0.77	0.80	0.75	0.78	0.81	1.08	1.11
t_{da}	0.59	0.62	0.62	0.60	0.62	0.62	0.92	0.92
t_{dz}	0.21	0.26	0.31	0.21	0.26	0.31	0.26	0.31
t_{zd}	0.25	0.30	0.35	0.25	0.30	0.35	0.30	0.35
t_{od}	0.28	0.33	0.37	0.28	0.33	0.37	0.33	0.37
Power (µW/MHz)								
Power_read	28.35	51.69	98.13	28.58	52.05	98.71	61.50	116.49
Power_write	29.46	54.39	104.80	32.40	60.17	115.97	84.35	162.67
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	90.483	151.367	282.905	128.134	204.036	380.269	414.712	769.723
Area (µm)								
Width	367.76	634.00	1189.76	367.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	195.32	299.00	299.00	299.00	713.72	713.72

NOTES:

1. In power consumption of DPSRAM_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAM_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

DPSRAM_HDH

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Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**128**	**512**	**512**	**512**	**2048**	**2048**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{cyc}	0.95	0.98	1.01	0.96	0.99	1.01	1.29	1.31
t_{ckl}	0.28	0.29	0.30	0.28	0.29	0.30	0.30	0.30
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.48	0.52	0.57	0.48	0.52	0.58	0.83	0.89
t_{as}	0.26	0.28	0.29	0.27	0.28	0.29	0.28	0.29
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.27	0.27	0.29	0.27	0.27	0.27	0.27
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.75	0.78	0.81	0.75	0.78	0.81	1.08	1.11
t_{da}	0.60	0.62	0.62	0.60	0.63	0.63	0.93	0.93
t_{dz}	0.19	0.22	0.25	0.19	0.22	0.25	0.22	0.25
t_{zd}	0.23	0.26	0.29	0.23	0.26	0.29	0.26	0.29
t_{od}	0.26	0.29	0.32	0.26	0.29	0.32	0.29	0.32
Power (µW/MHz)								
Power_read	25.55	45.23	84.65	25.76	45.54	85.16	55.01	102.85
Power_write	25.11	44.81	84.29	26.69	47.85	90.24	62.58	118.27
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	73.585	117.572	215.314	111.236	170.240	312.677	380.916	702.132
Area (µm)								
Width	367.76	634.00	1189.76	367.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	195.32	299.00	299.00	299.00	713.72	713.72

NOTES:

1. In power consumption of DPSRAM_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAM_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**
bpw	**16**	**32**	**16**	**32**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{cyc}	0.99	1.02	1.00	1.03	1.09	1.12	1.30	1.32
t_{ckl}	0.26	0.28	0.27	0.28	0.26	0.28	0.27	0.28
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.52	0.57	0.52	0.58	0.61	0.67	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.79	0.82	0.80	0.82	0.89	0.92	1.10	1.12
t_{da}	0.63	0.63	0.64	0.64	0.73	0.73	0.94	0.94
t_{dz}	0.20	0.23	0.20	0.23	0.20	0.23	0.20	0.23
t_{zd}	0.24	0.27	0.24	0.27	0.24	0.27	0.24	0.27
t_{od}	0.27	0.30	0.27	0.30	0.27	0.30	0.27	0.30
Power (µW/MHz)								
Power_read	39.70	73.62	40.00	74.11	43.22	79.96	49.43	91.81
Power_write	37.95	70.49	39.52	73.49	41.94	77.72	49.50	92.42
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	99.108	178.386	151.776	275.749	222.002	405.567	362.452	665.204
Area (µm)								
Width	634.00	1189.76	634.00	1189.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	299.00	299.00	437.24	437.24	713.72	713.72

NOTES:

1. In power consumption of DPSRAM_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAM_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

DPSRAM_HDH

High-Density Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

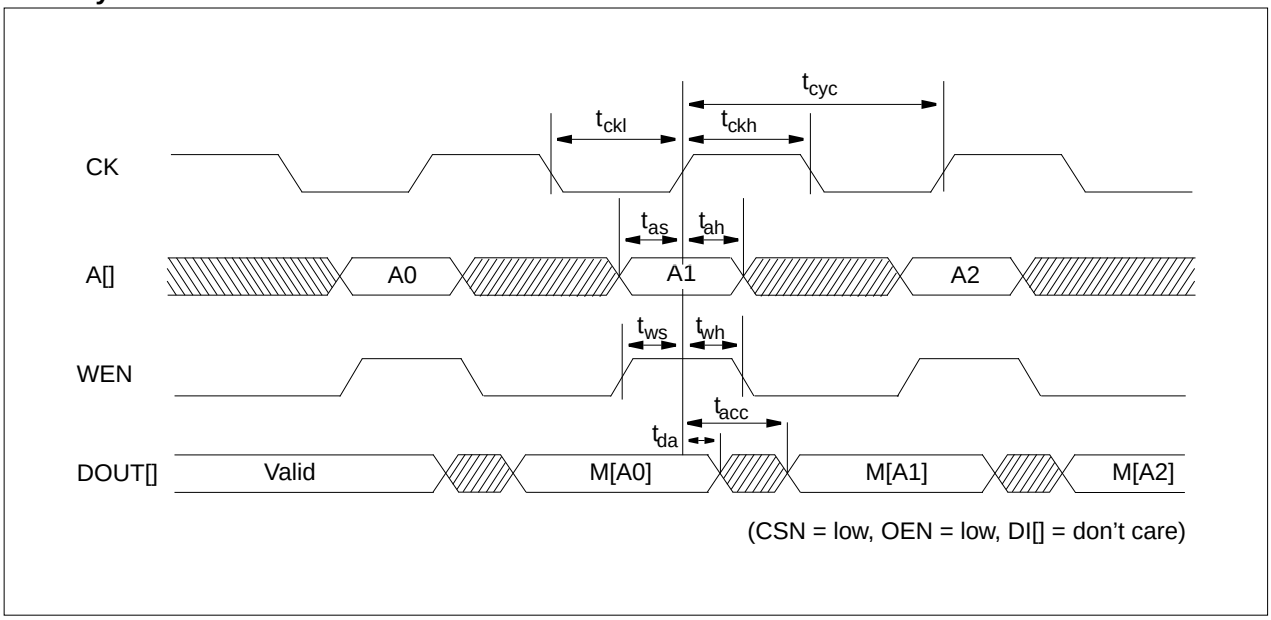
Parameters								
words	**512**	**512**	**2048**	**2048**	**4096**	**4096**	**8192**	**8192**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{cyc}	1.01	1.04	1.02	1.05	1.11	1.14	1.32	1.34
t_{ckl}	0.26	0.28	0.26	0.28	0.26	0.28	0.27	0.28
t_{ckh}	0.14	0.13	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.52	0.57	0.52	0.58	0.61	0.67	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.26
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.81	0.84	0.82	0.84	0.91	0.94	1.12	1.14
t_{da}	0.65	0.65	0.66	0.66	0.75	0.75	0.96	0.96
t_{dz}	0.19	0.21	0.19	0.21	0.19	0.21	0.19	0.21
t_{zd}	0.23	0.25	0.23	0.25	0.23	0.25	0.23	0.25
t_{od}	0.26	0.28	0.26	0.28	0.26	0.28	0.26	0.28
Power (µW/MHz)								
Power_read	36.90	68.18	37.18	68.66	40.45	74.47	46.59	86.28
Power_write	34.24	63.54	35.27	65.28	36.91	67.64	43.04	79.41
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	70.413	120.997	123.082	218.360	193.307	348.179	333.757	607.815
Area (µm)								
Width	634.00	1189.76	634.00	1189.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	299.00	299.00	437.24	437.24	713.72	713.72

NOTES:

1. In power consumption of DPSRAM_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAM_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

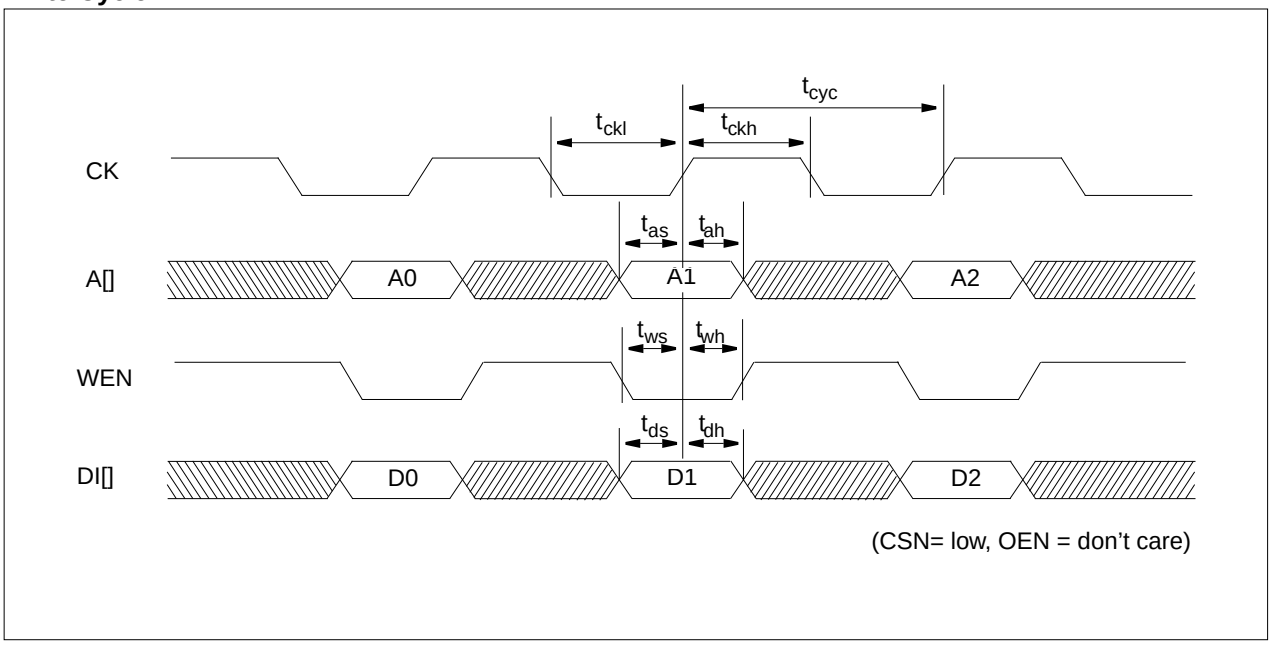
Timing Diagrams

Read Cycle



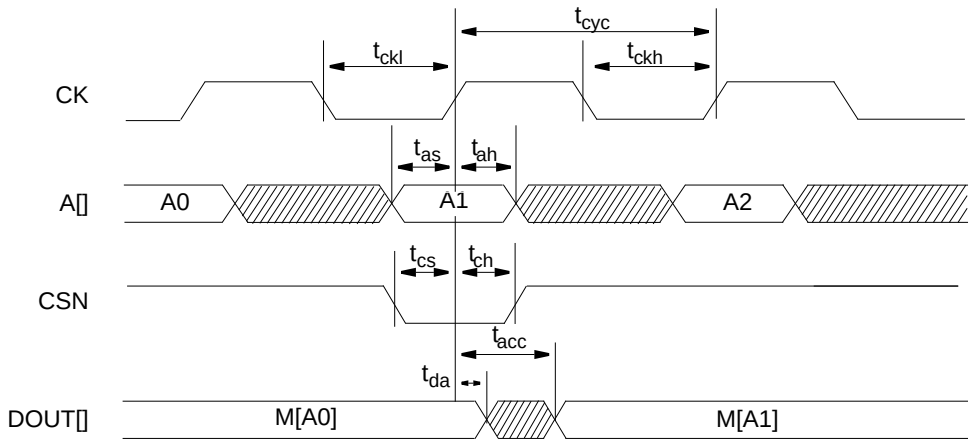
(CSN = low, OEN = low, DI[] = don't care)

Write Cycle



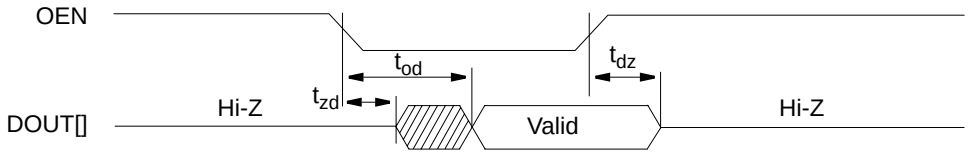
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



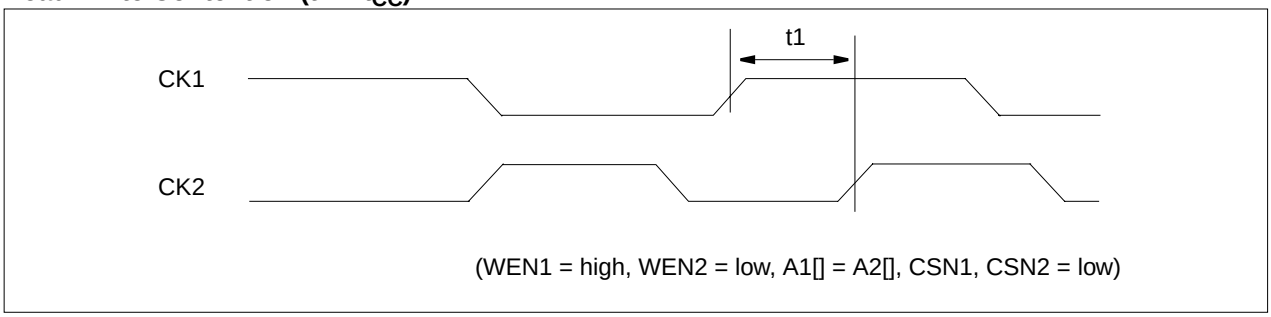
(OEN = low, WEN = high, DI[] = don't care)

OEN-Controlled Output Enable



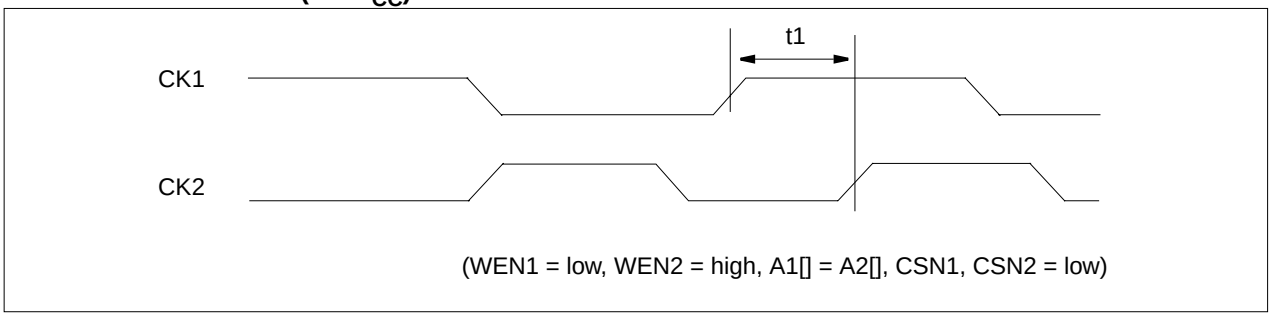
(CSN, CK, A[], WEN, DI[] = don't care)

Read-Write Contention (t1 < t_{CC})



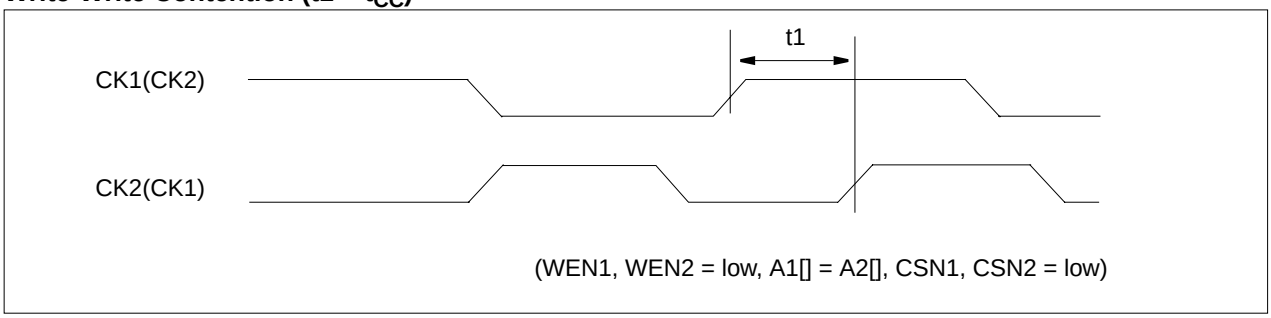
In the read-write contention (A1[] = A2[]), DOUT1[] is UNKNOWN while the write data is valid.

Write-Read Contention (t1 < t_{CC})



In the write-read contention (A1[] = A2[]), the write data is valid while DOUT2[] is UNKNOWN.

Write-Write Contention (t1 < t_{CC})



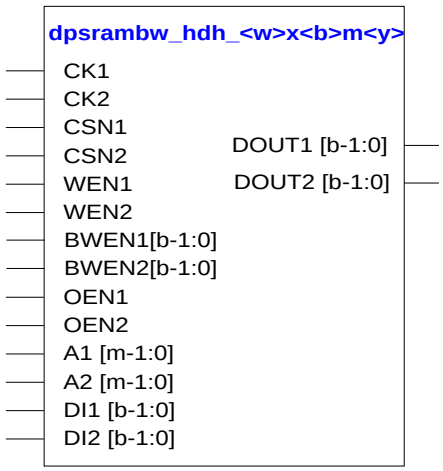
In the write-write contention (A1[] = A2[]), the write data is unpredictable.

NOTE: “don’t care” means the condition that these pins are in normal operation mode.

DPSRAMBW_HDH

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMBW_HDH is a dual-port synchronous static RAM with bit-write capability which is provided as a compiler. DPSRAMBW_HDH is intended for use in high-density applications. Each port is fully independent. Basically, its functionality is exactly same as DPSRAM_HDH except a bit-write operation which is controlled by BWEN1[](BWEN2[]), named bit-write enable signal bus. Each bit of BWEN1[](BWEN2[]) enables or disable the write operation of its corresponding bit in DI1[](DI2[]). On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. When the individual bit of BWEN1[](BWEN2[]) is low, the data on the corresponding write data bit of DI1[](DI2[]) are written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[]) are high, any data in DI1[](DI2[]) are not written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEM2[]) are low, the data in DI1[](DI2[]) are written into the memory location specified on A1[](A2[]), which is exactly same as the write operation in DPSRAM_HDH. During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAMBW_HDH Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	BWEN1 BWEN2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	All L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	All H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

DPSRAMBW_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN1[] BWEN2[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [] A2 []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [] DI2 []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [] DOUT2 []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT
7.83	2.42	2.42	2.35	2.42	3.37	3.37	6.55

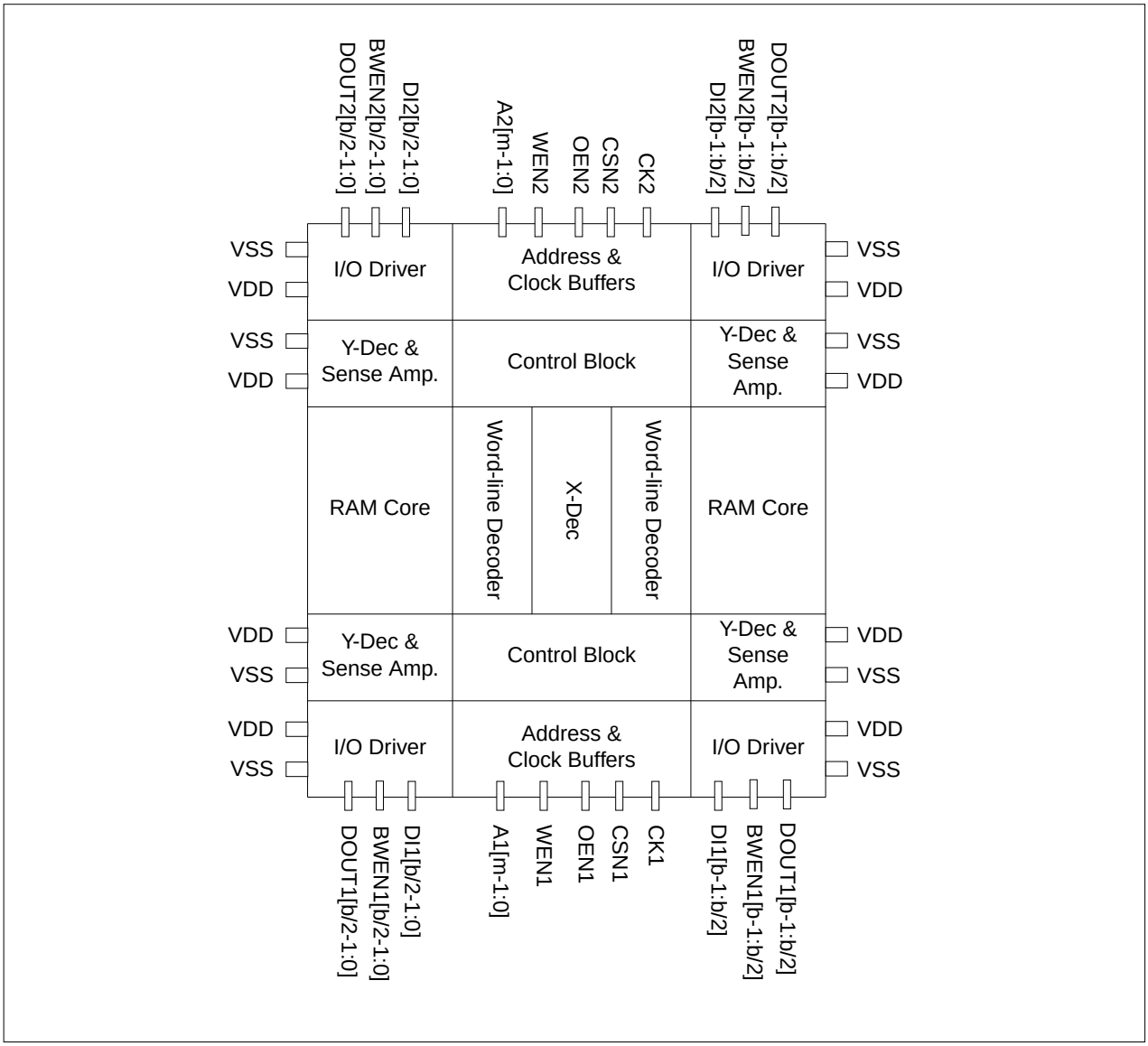
NOTE: Each pin's capacitance is exactly same regardless of available mux types.

DPSRAMBW_HDH

High-Density Dual-Port Synchronous Static RAM Bit-Write

Block Diagram

DPSRAMBW_HDH supports only 1-bank architecture. The multiple power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAMBW_HDH has two symmetrical signal ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in DPSRAMBW_HDH is permitted for Metal-5 layer or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAMBW_HDH.

4. Contention mode in same address access. In DPSRAMBW_HDH, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAMBW_HDH has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. A byte-write or word-write operation with DPSRAMBW_HDH. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as DPSRAM_HDH. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

DPSRAMBW_HDH

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{bws}	BWEN setup time	t_{bwh}	BWEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, other signals in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (μA)			
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**64**	**256**	**256**	**256**	**1024**	**1024**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
Timing (ns)								
t_{cyc}	0.94	0.98	1.00	0.95	0.98	1.01	1.28	1.31
t_{ckl}	0.27	0.27	0.33	0.27	0.27	0.33	0.27	0.33
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.13	0.14
t_{cc}	0.48	0.52	0.57	0.48	0.52	0.58	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.25	0.26	0.28	0.25	0.26	0.25	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.25	0.26	0.28	0.25	0.26	0.25	0.26
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.74	0.77	0.80	0.75	0.78	0.81	1.08	1.11
t_{da}	0.59	0.62	0.62	0.60	0.62	0.62	0.92	0.92
t_{dz}	0.21	0.26	0.31	0.21	0.26	0.31	0.26	0.31
t_{zd}	0.25	0.30	0.35	0.25	0.30	0.35	0.30	0.35
t_{od}	0.28	0.33	0.37	0.28	0.33	0.37	0.33	0.37
Power (µW/MHz)								
Power_read	28.35	51.69	98.13	28.58	52.05	98.71	61.50	116.49
Power_write	31.38	58.43	113.02	34.32	64.21	124.15	88.38	170.85
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	90.483	151.367	282.905	128.134	204.036	380.269	414.712	769.723
Area (µm)								
Width	367.76	634.00	1189.76	367.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	195.32	299.00	299.00	299.00	713.72	713.72

NOTES:

1. In power consumption of DPSRAMBW_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMBW_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

DPSRAMBW_HDH

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**128**	**512**	**512**	**512**	**2048**	**2048**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{cyc}	0.95	0.98	1.01	0.96	0.99	1.01	1.29	1.31
t_{ckl}	0.28	0.29	0.30	0.28	0.29	0.30	0.30	0.30
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.48	0.52	0.57	0.48	0.52	0.58	0.83	0.89
t_{as}	0.26	0.28	0.29	0.27	0.28	0.29	0.28	0.29
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.27	0.27	0.29	0.27	0.27	0.27	0.27
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.29	0.27	0.27	0.29	0.27	0.27	0.27	0.27
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.75	0.78	0.81	0.75	0.78	0.81	1.08	1.11
t_{da}	0.60	0.62	0.62	0.60	0.63	0.63	0.93	0.93
t_{dz}	0.19	0.22	0.25	0.19	0.22	0.25	0.22	0.25
t_{zd}	0.23	0.26	0.29	0.23	0.26	0.29	0.26	0.29
t_{od}	0.26	0.29	0.32	0.26	0.29	0.32	0.29	0.32
Power (µW/MHz)								
Power_read	25.55	45.23	84.65	25.76	45.54	85.16	55.01	102.85
Power_write	26.01	46.81	88.42	27.59	49.85	94.37	64.58	122.41
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	73.585	117.572	215.314	111.236	170.240	312.677	380.916	702.132
Area (µm)								
Width	367.76	634.00	1189.76	367.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	195.32	299.00	299.00	299.00	713.72	713.72

NOTES:

1. In power consumption of DPSRAMBW_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMBW_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**
bpw	**16**	**32**	**16**	**32**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{cyc}	0.99	1.02	1.00	1.03	1.09	1.12	1.30	1.32
t_{ckl}	0.26	0.28	0.27	0.28	0.26	0.28	0.27	0.28
t_{ckh}	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.52	0.57	0.52	0.58	0.61	0.67	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.79	0.82	0.80	0.82	0.89	0.92	1.10	1.12
t_{da}	0.63	0.63	0.64	0.64	0.73	0.73	0.94	0.94
t_{dz}	0.20	0.23	0.20	0.23	0.20	0.23	0.20	0.23
t_{zd}	0.24	0.27	0.24	0.27	0.24	0.27	0.24	0.27
t_{od}	0.27	0.30	0.27	0.30	0.27	0.30	0.27	0.30
Power (µW/MHz)								
Power_read	39.70	73.62	40.00	74.11	43.22	79.96	49.43	91.81
Power_write	38.93	72.58	40.50	75.58	42.92	79.82	50.47	94.51
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	99.108	178.386	151.776	275.749	222.002	405.567	362.452	665.204
Area (µm)								
Width	634.00	1189.76	634.00	1189.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	299.00	299.00	437.24	437.24	713.72	713.72

NOTES:

1. In power consumption of DPSRAMBW_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMBW_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

DPSRAMBW_HDH

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

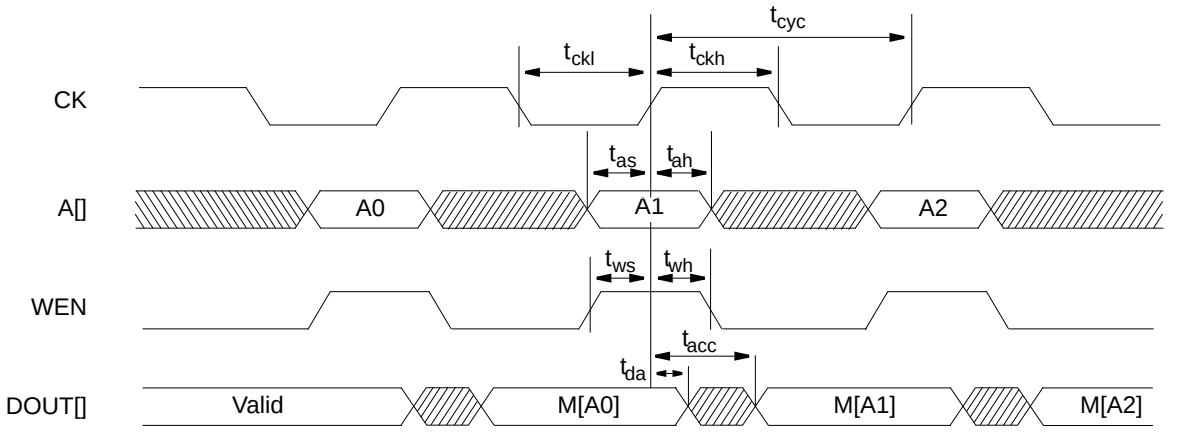
Parameters								
words	**512**	**512**	**2048**	**2048**	**4096**	**4096**	**8192**	**8192**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{cyc}	1.01	1.04	1.02	1.05	1.11	1.14	1.32	1.34
t_{ckl}	0.26	0.28	0.26	0.28	0.26	0.28	0.27	0.28
t_{ckh}	0.14	0.13	0.14	0.14	0.14	0.14	0.14	0.14
t_{cc}	0.52	0.57	0.52	0.58	0.61	0.67	0.83	0.89
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.26
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.81	0.84	0.82	0.84	0.91	0.94	1.12	1.14
t_{da}	0.65	0.65	0.66	0.66	0.75	0.75	0.96	0.96
t_{dz}	0.19	0.21	0.19	0.21	0.19	0.21	0.19	0.21
t_{zd}	0.23	0.25	0.23	0.25	0.23	0.25	0.23	0.25
t_{od}	0.26	0.28	0.26	0.28	0.26	0.28	0.26	0.28
Power (µW/MHz)								
Power_read	36.90	68.18	37.18	68.66	40.45	74.47	46.59	86.28
Power_write	34.70	64.61	35.73	66.35	37.37	68.71	43.50	80.48
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)								
Static_leakage	70.413	120.997	123.082	218.360	193.307	348.179	333.757	607.815
Area (µm)								
Width	634.00	1189.76	634.00	1189.76	634.00	1189.76	634.00	1189.76
Height	195.32	195.32	299.00	299.00	437.24	437.24	713.72	713.72

NOTES:

1. In power consumption of DPSRAMBW_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMBW_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

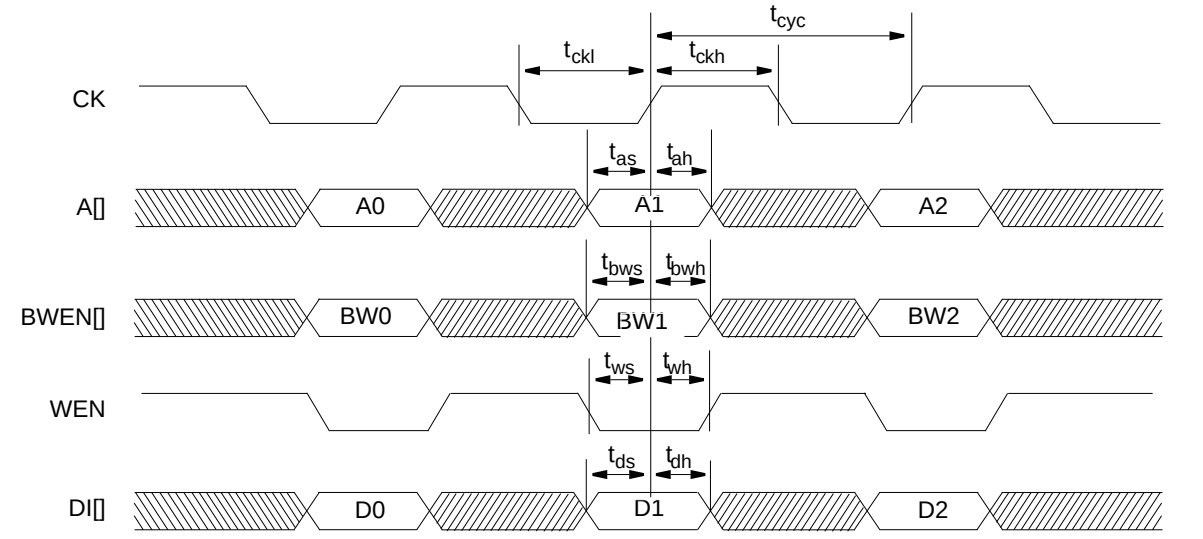
Timing Diagrams

Read Cycle



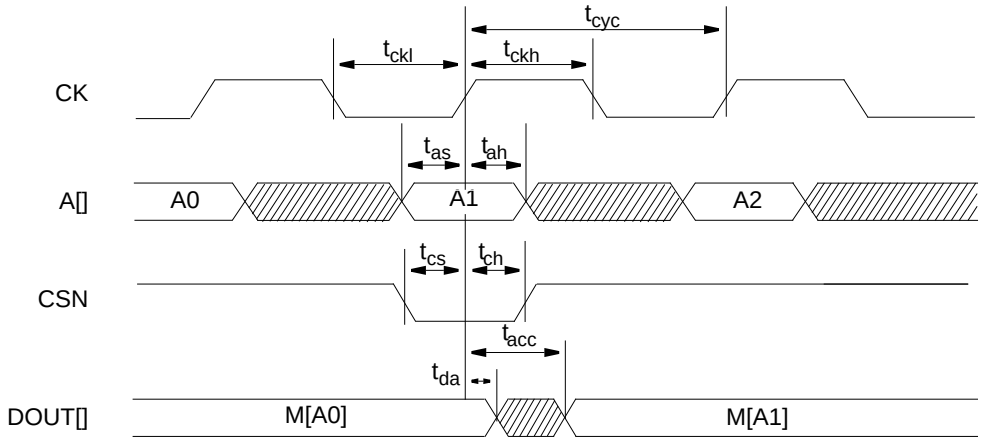
(CSN = low, OEN = low, DI[], BWEN[]= don't care)

Write Cycle



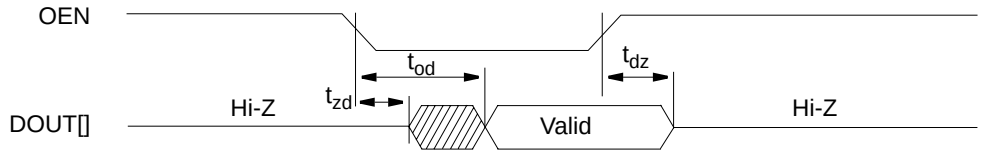
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



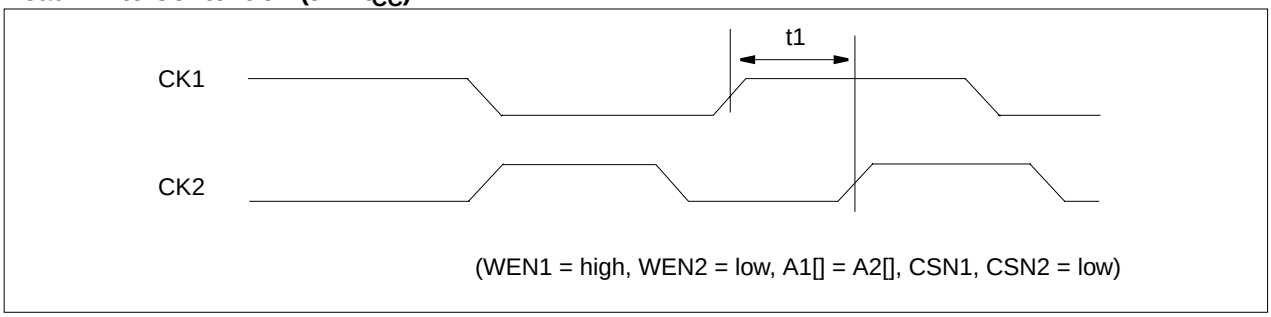
(OEN = low, WEN = high, DI[], BWEN[] = don't care)

OEN-Controlled Output Enable



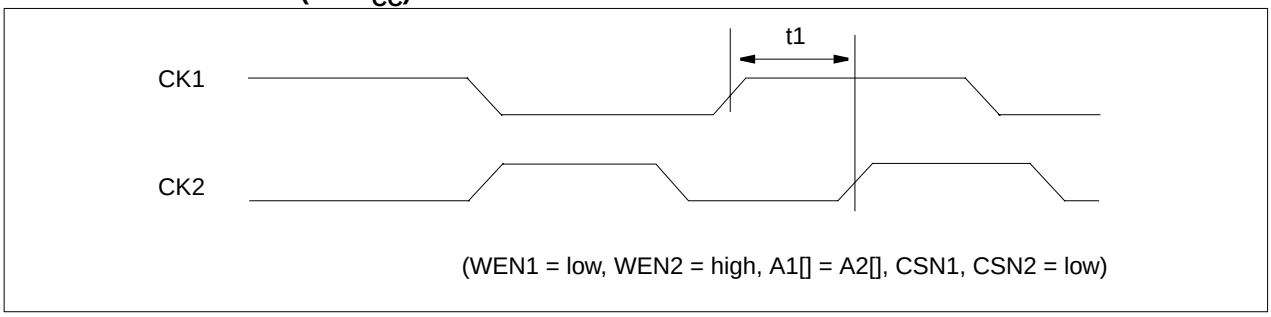
(CSN, CK, A[], WEN, DI[], BWEN[] = don't care)

Read-Write Contention (t1 < t_{CC})



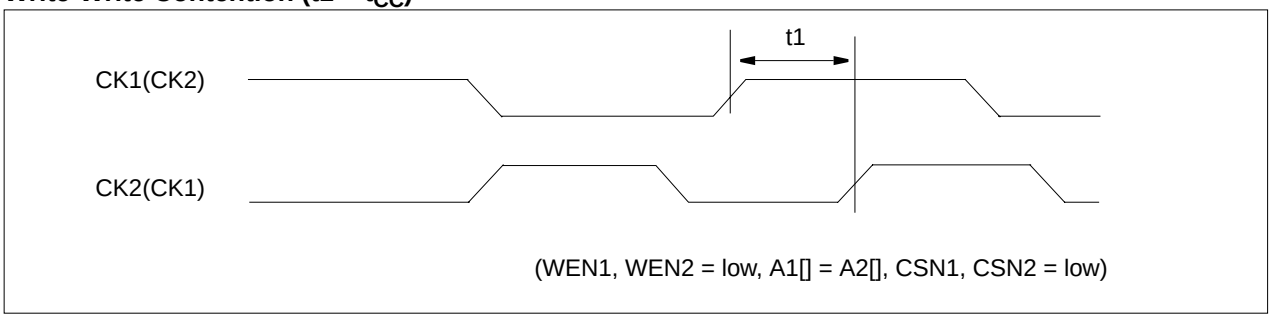
In the read-write contention (A1[] = A2[]), DOUT1[] is UNKNOWN while the write data is valid.

Write-Read Contention (t1 < t_{CC})



In the write-read contention (A1[] = A2[]), the write data is valid while DOUT2[] is UNKNOWN.

Write-Write Contention (t1 < t_{CC})



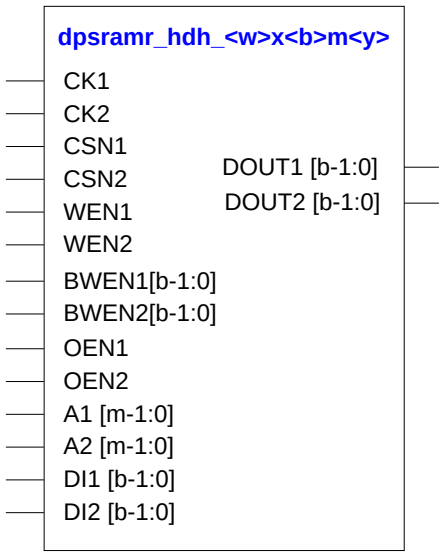
In the write-write contention (A1[] = A2[]), the write data is unpredictable.

NOTE: “don’t care” means the condition that these pins are in normal operation mode.

DPSRAMR_HDH

High-Density Dual-Port Synchronous Static RAM with Redundancy

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Heuristic row-redundancy available
- Separated data I/O
- Bit-write capability
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- 16Kbits ~ 256Kbits capacity
- 128 ~ 16K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMR_HDH is a dual-port synchronous static RAM with redundancy which is provided as a compiler. DPSRAMR_HDH is intended for use in high-density applications. Each port is fully independent. Basically, its functionality is exactly same as DPSRAMBW_HDH. Each bit of BWEN1[](BWEN2[]) enables or disable the write operation of its corresponding bit in DI1[] (DI2[]). On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. The data bits in DI1[](DI2[]), which their corresponding bit (s) in BWEN1[](BWEN2[]) are low, are written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[]) are high, any data in DI1[](DI2[]) are not written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[] are low, the data in DI1[](DI2[]) are written into the memory location specified on A1[](A2[]), which is exactly same as the write operation in DPSRAM_HDH. During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAMR_HDH Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	BWEN1 BWEN2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Write-write cycle
↑	L	L	L	Valid	X	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operatoin
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

DPSRAMR_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	128	256	512	1024
	Max	2048	4096	8192	16384
	Step	32	64	128	256
Bpw (b)	Min	8	4	2	1
	Max	128	64	32	16
	Step	1	1	1	1

NOTE: Capacity(w b) => 16K bits.

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN1 BWEN2	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [] A2 []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [] DI2 []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [] DOUT2 []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

DPSRAMR_HDH

High-Density Dual-Port Synchronous Static RAM with Redundancy

Pin Capacitance

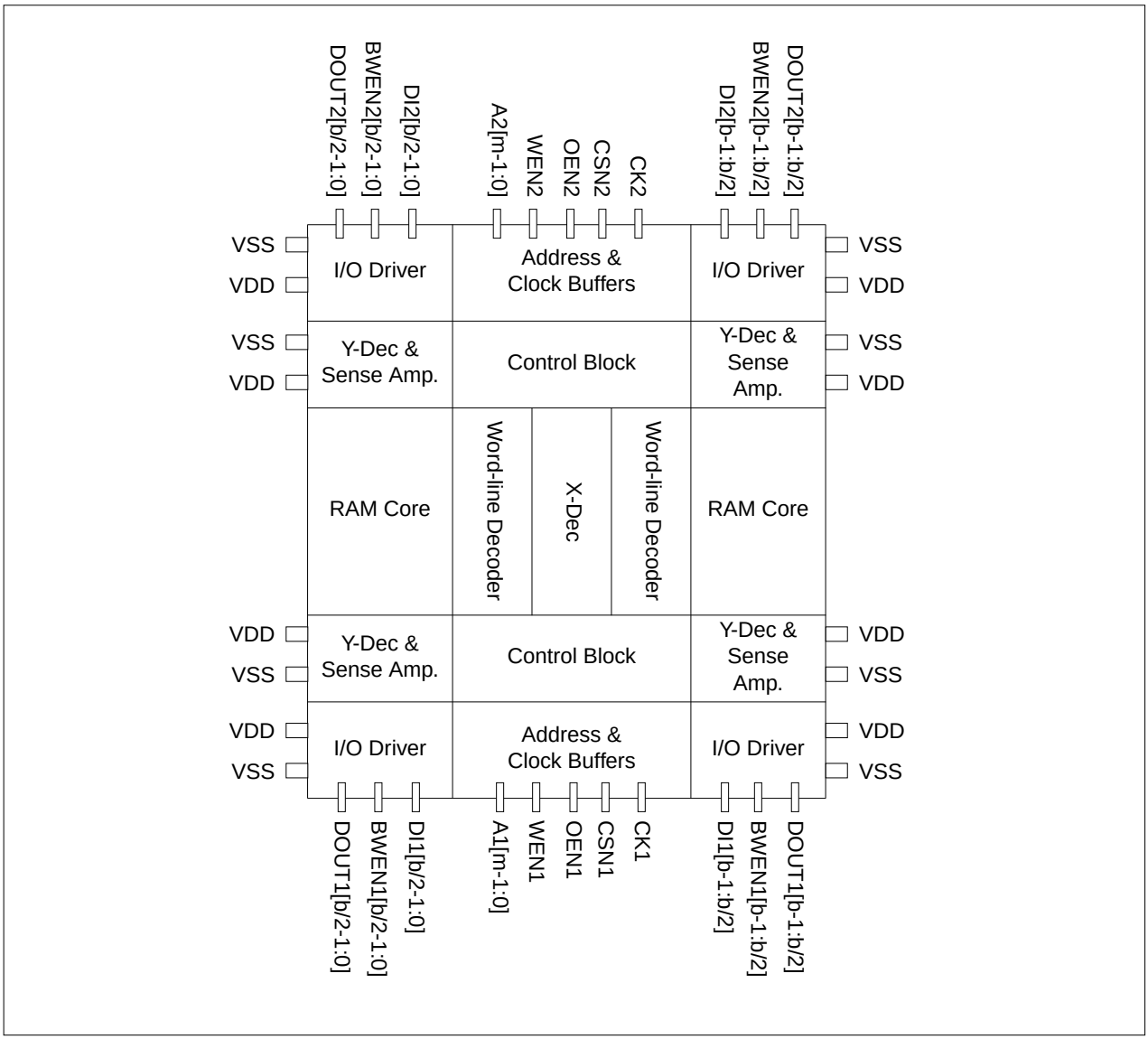
(Unit = SL)

CK	CSN	WEN	BWEN	OEN	A1	DI1	DOUT1
7.83	2.42	2.42	3.37	2.35	2.42	3.37	6.55

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagram

DPSRAMR_HDH supports only 1-bank architecture. The multiple power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAMR_HDH has two symmetrical signal ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in DPSRAMR_HDH is permitted for Metal-5 or upper metal layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAMR_HDH.

4. Contention mode in same address access. In DPSRAMR_HDH, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operations, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAMR_HDH has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. A byte-write or word-write operation with DPSRAMR_HDH. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte(8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In wore-write operation, the functionality is exactly same as DPSRAM_HDH. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{bws}	BWEN setup time	t_{bwh}	BWEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (μA)			
Static_leakage	The static leakage power consumption while CSN is high and other signals including CK are in stable.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**128**	**512**	**768**	**1024**	**1536**	**2048**	**2048**
bpw	**128**	**32**	**48**	**64**	**96**	**8**	**128**
Timing (ns)							
t_{cyc}	1.01	1.08	1.18	1.33	1.72	2.41	2.59
t_{ckl}	0.34	0.32	0.32	0.32	0.33	0.32	0.33
t_{ckh}	0.13	0.13	0.13	0.13	0.13	0.13	0.13
t_{cc}	0.59	0.64	0.73	0.89	1.23	1.54	1.69
t_{as}	0.28	0.29	0.29	0.29	0.29	0.29	0.29
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.21	0.22	0.22	0.21	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.26	0.28	0.26	0.25	0.26	0.30	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.16	0.16	0.17	0.17	0.17	0.16	0.17
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.26	0.28	0.26	0.25	0.26	0.30	0.26
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.81	0.87	0.97	1.12	1.45	1.77	1.85
t_{da}	0.62	0.73	0.82	0.96	1.27	1.63	1.67
t_{dz}	0.31	0.21	0.24	0.26	0.27	0.17	0.31
t_{zd}	0.35	0.25	0.28	0.30	0.31	0.22	0.35
t_{od}	0.37	0.28	0.31	0.33	0.34	0.25	0.38
Power (µW/MHz)							
Power_read	102.46	33.42	47.90	65.30	107.76	19.21	162.01
Power_write	123.93	41.63	65.78	93.34	164.24	24.13	258.07
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)							
Static_leakage	315.451	178.687	287.040	415.416	854.433	318.900	1290.455
Area (µm)							
Width	1215.48	393.48	526.60	659.72	949.24	193.80	1215.48
Height	246.20	453.56	591.80	730.04	1032.30	1284.92	1334.84

NOTES:

1. In power consumption of DPSRAMR_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMR_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

DPSRAMR_HDH

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Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**256**	**1024**	**1536**	**2048**	**3072**	**4096**	**4096**
bpw	**64**	**16**	**24**	**32**	**48**	**4**	**64**
Timing (ns)							
t_{cyc}	1.02	1.10	1.19	1.31	1.73	2.42	2.57
t_{ckl}	0.34	0.32	0.32	0.32	0.33	0.32	0.33
t_{ckh}	0.13	0.13	0.13	0.13	0.13	0.13	0.13
t_{cc}	0.58	0.63	0.72	0.89	1.24	1.55	1.68
t_{as}	0.31	0.29	0.29	0.30	0.30	0.29	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.27	0.29	0.28	0.27	0.28	0.31	0.27
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.17	0.16	0.17	0.17	0.17	0.16	0.17
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.27	0.29	0.28	0.27	0.28	0.31	0.27
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.82	0.90	0.98	1.12	1.45	1.78	1.86
t_{da}	0.63	0.75	0.83	0.97	1.28	1.63	1.68
t_{dz}	0.26	0.20	0.21	0.23	0.23	0.17	0.26
t_{zd}	0.29	0.23	0.25	0.26	0.27	0.21	0.30
t_{od}	0.32	0.26	0.28	0.29	0.30	0.24	0.33
Power (µW/MHz)							
Power_read	89.08	30.63	43.31	58.87	97.86	19.13	148.55
Power_write	96.50	32.70	49.68	68.32	116.66	20.24	181.54
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)							
Static_leakage	247.859	161.789	261.693	381.620	803.739	314.676	1222.864
Area (µm)							
Width	1215.48	393.48	526.60	659.72	949.24	193.80	1215.48
Height	246.20	453.56	591.80	730.04	1032.16	1284.67	1334.84

NOTES:

1. In power consumption of DPSRAMR_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMR_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**512**	**2048**	**3072**	**4096**	**6144**	**8192**	**8192**
bpw	**32**	**8**	**12**	**16**	**24**	**2**	**32**
Timing (ns)							
t_{cyc}	1.03	1.10	1.20	1.34	1.73	2.43	2.58
t_{ckl}	0.31	0.32	0.32	0.32	0.32	0.32	0.32
t_{ckh}	0.13	0.13	0.13	0.13	0.13	0.13	0.13
t_{cc}	0.59	0.64	0.73	0.89	1.24	1.55	1.68
t_{as}	0.28	0.29	0.28	0.29	0.29	0.29	0.29
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.21	0.22	0.21	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.30	0.29	0.28	0.29	0.31	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.17	0.17	0.16	0.17	0.17	0.16	0.17
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.30	0.29	0.28	0.29	0.31	0.28
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.83	0.91	0.99	1.13	1.48	1.80	1.87
t_{da}	0.64	0.76	0.84	0.98	1.30	1.65	1.69
t_{dz}	0.23	0.19	0.20	0.21	0.21	0.17	0.23
t_{zd}	0.27	0.23	0.24	0.25	0.25	0.21	0.27
t_{od}	0.30	0.25	0.26	0.27	0.28	0.24	0.29
Power (µW/MHz)							
Power_read	78.32	27.92	39.20	53.42	89.83	18.46	137.72
Power_write	79.14	27.02	40.02	53.71	89.91	17.66	139.51
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)							
Static_leakage	210.931	152.557	247.845	363.156	776.043	312.368	1185.936
Area (µm)							
Width	1215.48	393.48	526.60	659.72	949.24	193.80	1215.48
Height	246.20	453.56	591.80	730.04	1031.86	1284.15	1334.84

NOTES:

1. In power consumption of DPSRAMR_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMR_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

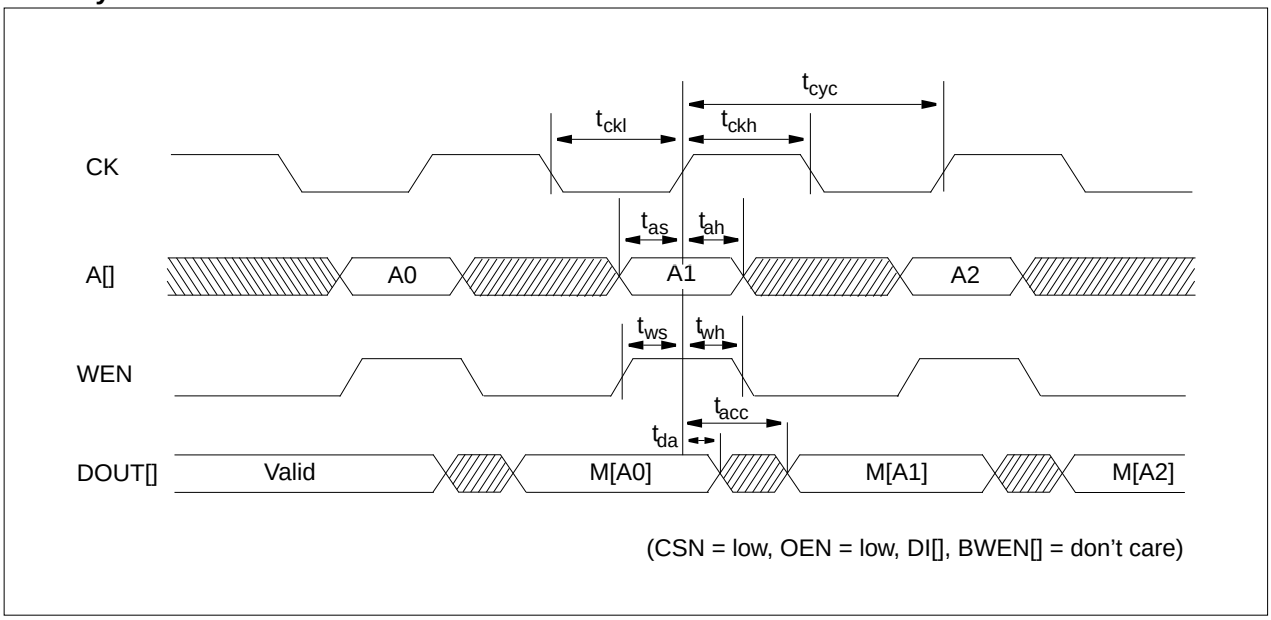
Parameters							
words	**1024**	**4096**	**6144**	**8192**	**12288**	**16384**	**16384**
bpw	**16**	**4**	**6**	**8**	**12**	**1**	**16**
Timing (ns)							
t_{cyc}	1.05	1.14	1.22	1.37	1.72	2.41	2.59
t_{ckl}	0.31	0.32	0.32	0.32	0.32	0.32	0.32
t_{ckh}	0.13	0.13	0.13	0.13	0.13	0.13	0.13
t_{cc}	0.60	0.64	0.74	0.89	1.25	1.55	1.69
t_{as}	0.28	0.29	0.29	0.29	0.29	0.29	0.29
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.22	0.21	0.22	0.22	0.22	0.22	0.22
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.28	0.30	0.29	0.29	0.29	0.31	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.28	0.30	0.29	0.29	0.29	0.31	0.28
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	0.85	0.93	1.01	1.16	1.49	1.82	1.89
t_{da}	0.67	0.78	0.86	1.00	1.32	1.67	1.71
t_{dz}	0.21	0.18	0.18	0.19	0.20	0.17	0.21
t_{zd}	0.26	0.22	0.23	0.23	0.25	0.21	0.26
t_{od}	0.29	0.25	0.26	0.26	0.27	0.24	0.28
Power (µW/MHz)							
Power_read	72.88	26.55	37.14	50.66	85.76	18.16	132.36
Power_write	70.26	24.18	35.07	46.62	76.76	16.36	118.63
Power_standby	0.83	0.83	0.83	0.83	0.83	0.83	0.83
Static Leakage (µA)							
Static_leakage	153.543	138.210	226.324	334.461	733.002	308.781	1128.547
Area (µm)							
Width	1215.48	393.48	526.60	659.72	949.24	193.80	1215.48
Height	246.20	453.56	591.80	730.04	1031.21	1283.00	1334.84

NOTES:

1. In power consumption of DPSRAMR_HDH, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that DPSRAMR_HDH is deselected and only CK switches.
3. Static leakage current is measured on the condition that all input and output signals are stable.

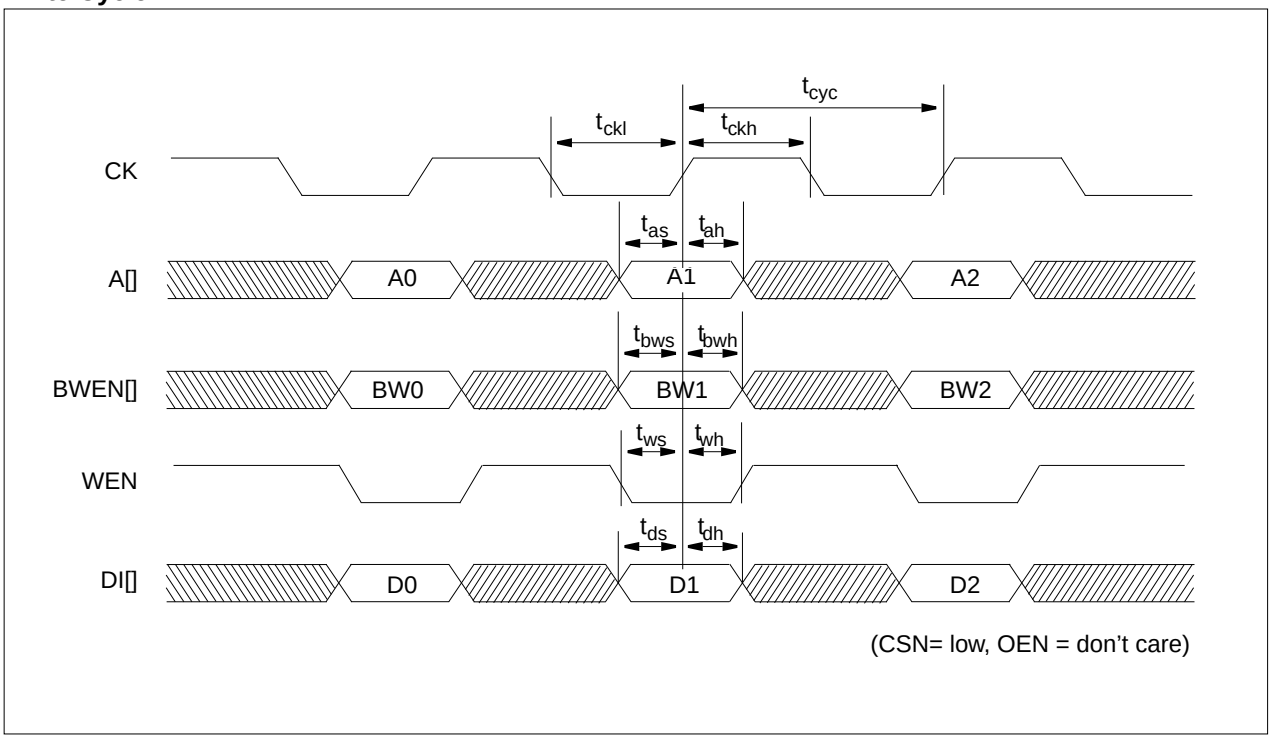
Timing Diagrams

Read Cycle



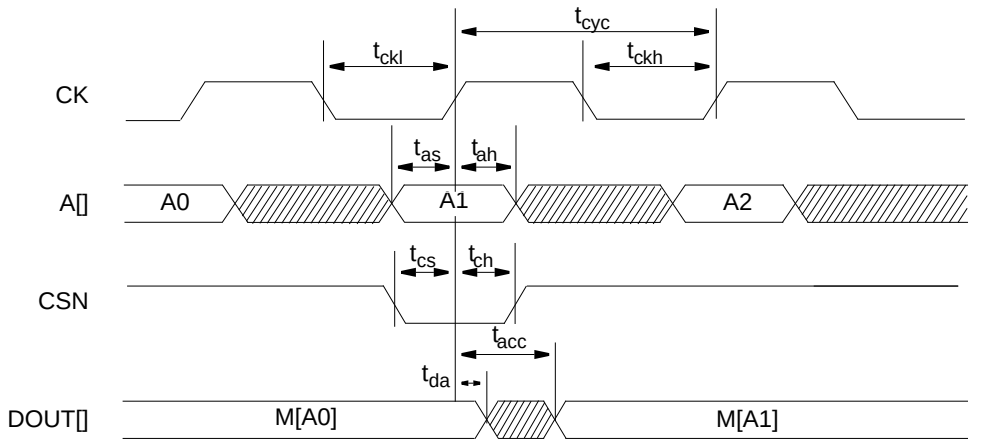
(CSN = low, OEN = low, DI[], BWEN[] = don't care)

Write Cycle



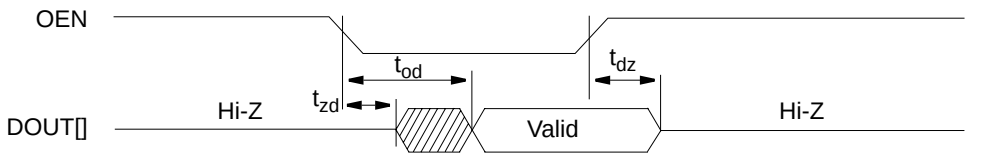
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



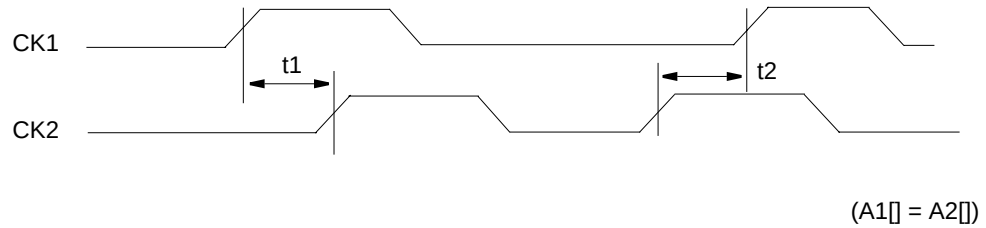
(OEN = low, WEN = high, DI[], BWEN[] = don't care)

OEN-Controlled Output Enable



(CSN=low, CK, A[], WEN, DI[], BWEN[] = don't care)

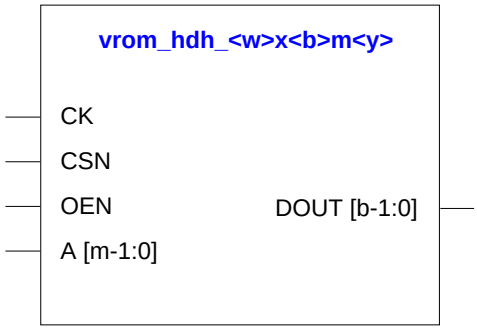
Contention Mode (t1, t2 < t_{CC})



(A1[] = A2[])

NOTE:"don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Suitable for low-power application
- Via-1 programmable code available
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Near zero hold time
- Flexible aspect ratio
- Up to 1Mbits capacity
- Up to 32K number of words
- Up to 128 number of bit per word

Function Description

VROM_HDH is a synchronous via-1 programmable ROM which is provided as a compiler. VROM_HDH is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

VROM_HD Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

VROM_HDH

High-Density Synchronous Via-1 Programmable ROM

Parameter Description

VROM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), amd Column mux(y).

Parameters		Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words(w)	Min	64	128	256
	Max	8192	16384	32768
	Step	64	128	256
Bpw(b)	Min	2	2	2
	Max	128	64	32
	Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A []	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

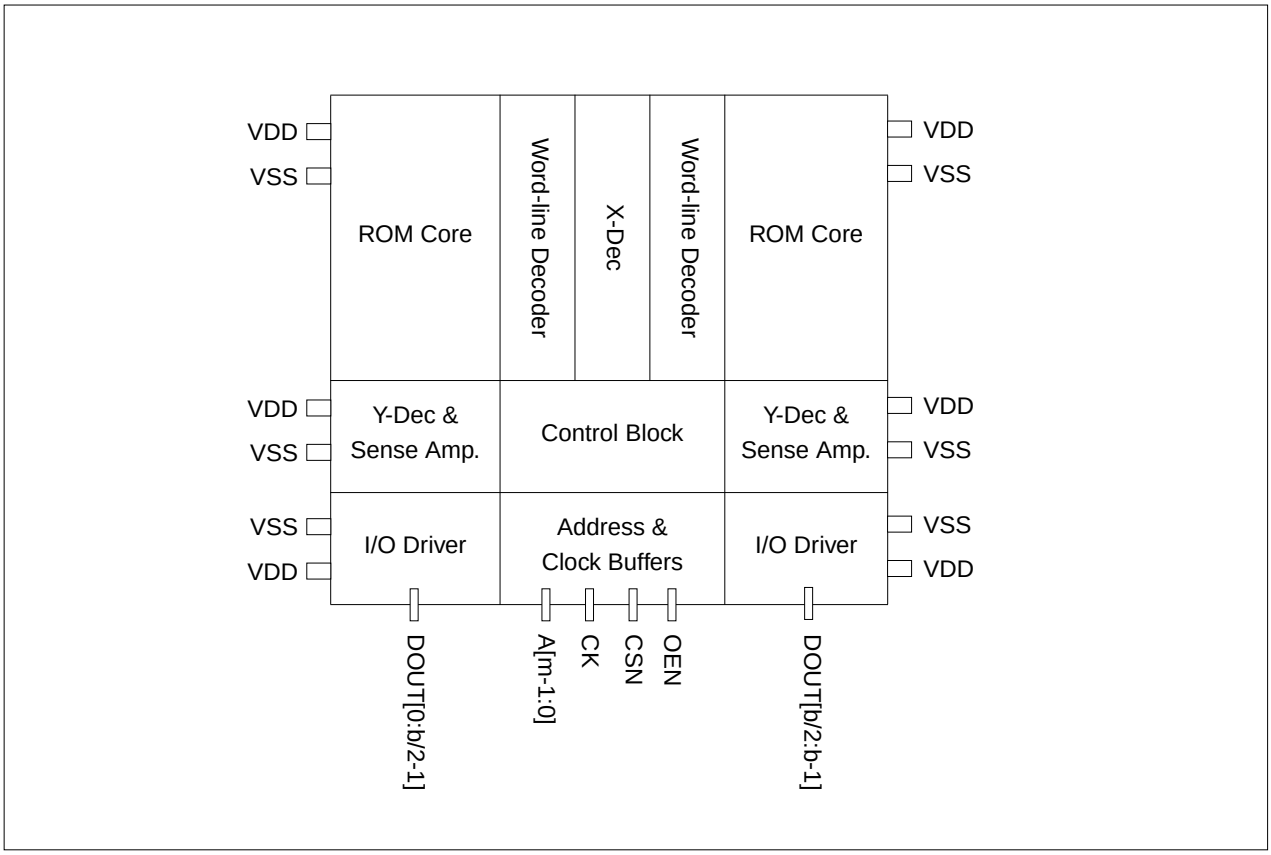
Unit: [SL]

CK	CSN	OEN	A	DOUT
3.40	0.73	0.97	0.73	4.85

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagrams

VROM_HDH has the dual-array architectures. In architecture, the multiple power ports are located on the top-edge and the bottom edge and the middle edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in VROM_HDH is permitted for Metal-5 or upper layers.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of VROM_HDH.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time from	t_{od}	OEN to valid data output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high, other signals are in stable and only CK is toggled.		
Definition for Static Leakage Current Consumption (μA)			
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**512**	**2048**	**2048**	**2048**	**8192**	**8192**
bpw	**32**	**64**	**128**	**32**	**64**	**128**	**64**	**128**
Timing (ns)								
t_{cyc}	2.04	2.10	2.22	2.32	2.38	2.49	3.39	3.51
t_{ckl}	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{as}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.65	1.71	1.83	1.93	1.98	2.10	3.00	3.12
t_{da}	1.24	1.30	1.42	1.51	1.57	1.68	2.58	2.69
t_{dz}	0.19	0.22	0.27	0.19	0.22	0.27	0.22	0.27
t_{zd}	0.27	0.30	0.35	0.27	0.30	0.35	0.30	0.35
t_{od}	0.30	0.32	0.38	0.30	0.32	0.38	0.32	0.38
Power (µW/MHz)								
Power_read	50.09	84.88	155.63	74.11	130.35	243.83	275.77	527.82
Power_standby	1.65	1.65	1.65	1.65	1.65	1.65	1.65	1.65
Static Leakage (µA)								
Static_leakage	72.984	86.401	113.235	205.590	239.867	308.421	853.732	1089.165
Area (µm)								
Width	268.98	409.54	686.66	268.98	409.54	686.66	409.54	686.66
Height	208.64	208.64	208.64	377.60	377.60	377.60	1053.44	1053.44

NOTES:

1. Standby power is measured on the condition that VROM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

VROM_HDH

High-Density Synchronous Via-1 Programmable ROM

Reference Table

*** For Ymux=16** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**1024**	**4096**	**4096**	**4096**	**16384**	**16384**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{cyc}	2.06	2.12	2.24	2.34	2.40	2.52	3.42	3.53
t_{ckl}	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{as}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.67	1.73	1.85	1.95	2.01	2.12	3.02	3.14
t_{da}	1.24	1.30	1.42	1.51	1.57	1.68	2.58	2.69
t_{dz}	0.17	0.19	0.23	0.17	0.19	0.23	0.19	0.23
t_{zd}	0.26	0.28	0.31	0.26	0.28	0.31	0.28	0.31
t_{od}	0.28	0.30	0.34	0.28	0.30	0.34	0.30	0.34
Power (µW/MHz)								
Power_read	45.40	75.41	136.82	69.51	120.99	255.14	266.40	508.93
Power_standby	1.65	1.65	1.65	1.65	1.65	1.65	1.65	1.65
Static Leakage (µA)								
Static_leakage	71.170	82.773	105.980	203.776	236.239	301.166	850.104	1081.909
Area (µm)								
Width	268.98	409.54	686.66	268.98	409.54	686.66	409.54	686.66
Height	208.64	208.64	208.64	377.60	377.60	377.60	1053.44	1053.44

NOTES:

1. Standby power is measured on the condition that VROM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=32** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

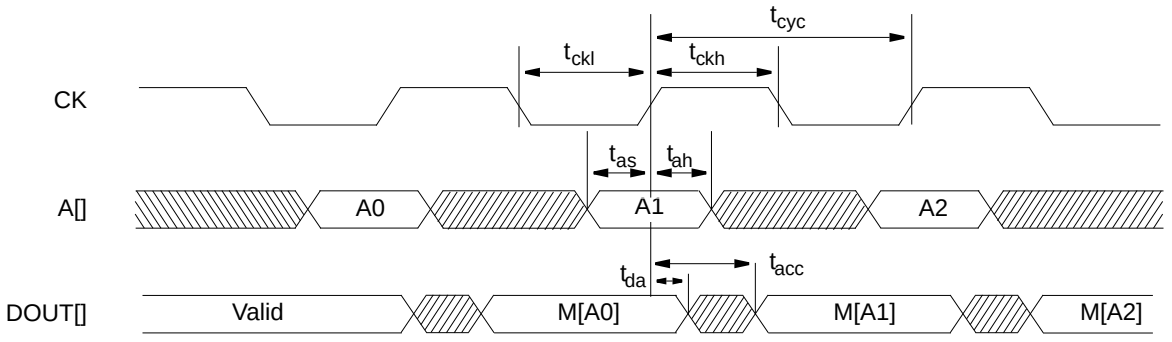
Parameters								
words	**2048**	**2048**	**8192**	**8192**	**16384**	**16384**	**32768**	**32768**
bpw	**16**	**32**	**16**	**32**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{cyc}	2.17	2.29	2.44	2.56	2.78	2.90	3.46	3.58
t_{ckl}	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{as}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.77	1.90	2.05	2.17	2.39	2.51	3.07	3.19
t_{da}	1.31	1.43	1.58	1.70	1.92	2.03	2.59	2.70
t_{dz}	0.18	0.21	0.18	0.21	0.18	0.21	0.18	0.21
t_{zd}	0.26	0.29	0.26	0.29	0.26	0.29	0.26	0.29
t_{od}	0.29	0.32	0.29	0.32	0.29	0.32	0.29	0.32
Power (µW/MHz)								
Power_read	70.98	127.92	116.58	216.33	168.74	318.44	261.89	499.85
Power_standby	1.65	1.65	1.65	1.65	1.65	1.65	1.65	1.65
Static Leakage (µA)								
Static_leakage	80.959	102.352	234.425	297.538	439.047	577.785	848.290	1078.281
Area (µm)								
Width	409.54	686.66	409.54	686.66	409.54	686.66	409.54	686.66
Height	208.64	208.64	377.60	377.60	602.88	602.88	1053.44	1053.44

NOTES:

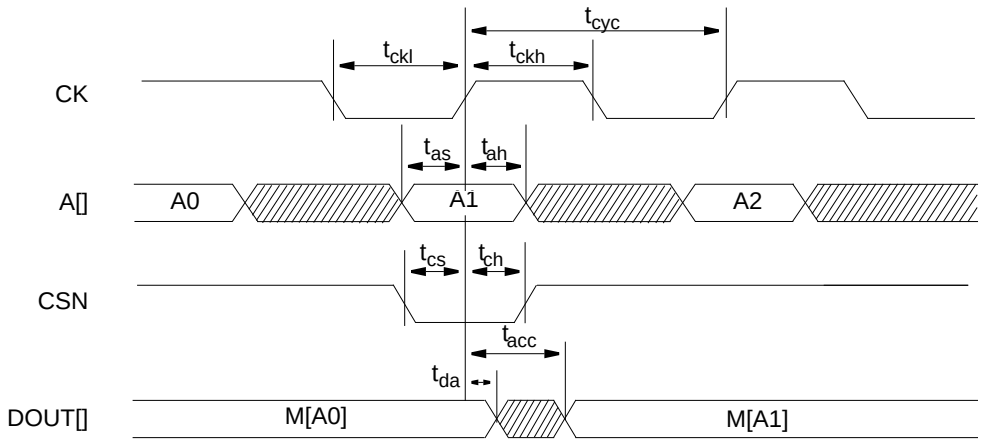
1. Standby power is measured on the condition that VROM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Timing Diagrams

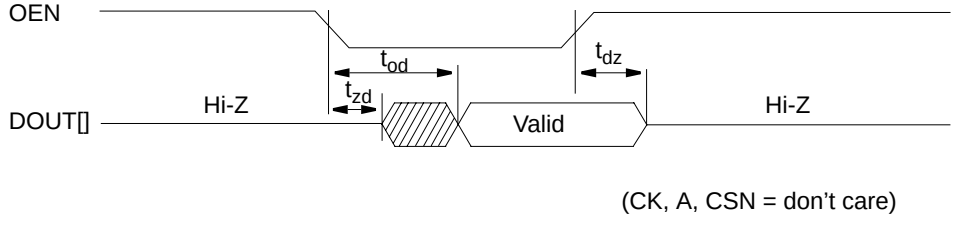
Read Cycle



Read Cycle with CSN-Controlled

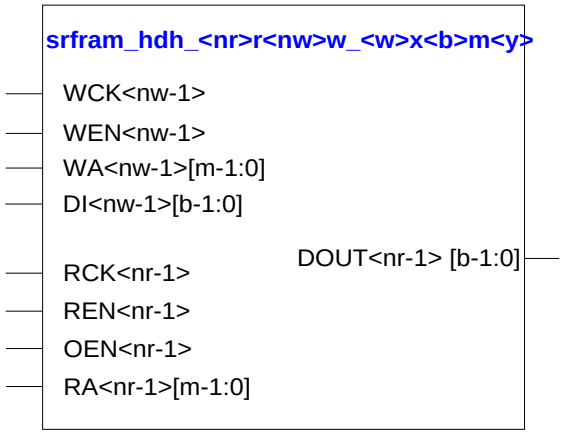


OEN Controlled Output Enable



NOTE: “don't care” means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Writes(nw) is the number of write ports(1-to-2).
5. Reads(nr) is the number of read ports(1-to-2).
6. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous read/write operation
- Fully independent ports
- Latched inputs and outputs
- Flexible aspect ratio
- Asynchronous tri-state output
- Two ports(1-read and 1-write) available
- Three ports(2-read and 1-write) available
- Four ports(2-read and 2-write) available
- Up to 16Kbits capacity
- Up to 1024 number of words
- Up to 64 number of bits per word

Function Description

SRFRAM_HDH is a multi-port synchronous register file which is provided as a compiler. SRFRAM_HDH is intended for use in high-density applications. It allows maximum 4 ports with configurable 1-to-2 read ports and 1-to-2 write ports. All read and write ports are fully independent. On the rising edge of WCK, the write cycle is initiated when WEN is low. The data bits in DI[] are written into the memory location specified on WA[]. During the write cycle, DOUT[] remains stable. If WEN is high, WA[] and DI[] are disabled. It is called “write standby mode”. On the rising edge of RCK, the read cycle is initiated when REN is low. the data stored in the memory location specified on RA[] become valid through DOUT[] after a delay. If REN is high, RA[] is disabled and DOUT[] remains stable with the previous data output. It is called “read standby mode”. When OEN is high, DOUT[] is placed in a high-impedance state.

SRFRAM_HDH Function Table

WCK	WEN	WA	DI	RCK	RA	REN	OEN	DOUT	Comment
X	H	X	X	X	X	H	L	DOUT(t-1)	De-selected (standby mode)
X	H	X	X	X	X	X	X	X	Write standby mode
↑	L	Valid	Valid	X	X	X	X	X	Write cycle
X	X	X	X	X	X	H	L	DOUT(t-1)	Read standby mode
X	X	X	X	↑	Valid	L	L	MEM(RA)	Read cycle
X	X	X	X	X	X	X	H	Z	Unconditional tri-state output

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Parameter Description

SRFRAM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y), Number of read ports(nr) and Number of write ports(nw).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8
Words(w)	Min	4	8	16
	Max	256	512	1024
	Step	2	4	8
Bpw(b)	Min	1	1	1
	Max	64	32	16
	Step	1	1	1
Write ports(nw)		1, 2		
Read ports(nr)		1, 2		

Pin Descriptions

Name	I/O	Description
WCK<nw-1>	Write Clock	Write Clock input on each write port. WEN, WA[] and DI[] are latched into the RAM on the rising edge of WCK. If WEN is low on the rising edge of WCK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in write standby mode.
WEN<nw-1>	Write Enable	Write Enable input on each write port. WEN is latched into the RAM on the rising edge of WCK.When WEN is low, the write mode is enabled. When WEN is high, it prevents the write-operation. It is called “write standby mode”.
WA<nw-1>[]	Write Address	Write Address bus on each write port. It specifies the location in which the data will be written in the write-operation. WA[] is latched at the rising edge of WCK.
DI<nw-1>[]	Data Input	Data Input bus on each write port. It contains data values to be written into the memory during the write-cycle. DI[] is latched at the rising edge of WCK.
RCK<nr-1>	Read Clock	Read Clock input on each read port. REN and RA[] are latched into the RAM on the rising edge of RCK. If REN is low on the rising edge of RCK, the RAM is in read mode. If REN is high on the rising edge of RCK, the RAM is in read standby mode.
REN<nr-1>	Read Enable	Read Enable input on each read port. REN is latched into the RAM on the rising edge of RCK. When REN is low, read is enabled. When REN is high, read is disabled and DOUT[] remains in the previous state. It is called “read standby mode”
OEN<nr-1>	Data Output Enable	Output Enable input on each read port. The low state enables output drivers and the high state disables output to go to the Hi-Z state.
RA<nr-1>[]	Read Address	Read Address bus on each read port. It specifies the location to be read in the read-operation. RA[] is latched at the rising edge of RCK.
DOUT<nr-1>[]	Data Output	Data Output bus on each read port. When REN and OEN are low, it presents the data word stored in the location specified by RA[] after the rising edge of RCK. When REN is high and OEN is low, DOUT[] remains in the previous state. When OEN is high, DOUT[] is in the high-impedance state regardless of REN.

Pin Capacitance

Unit: [SL]

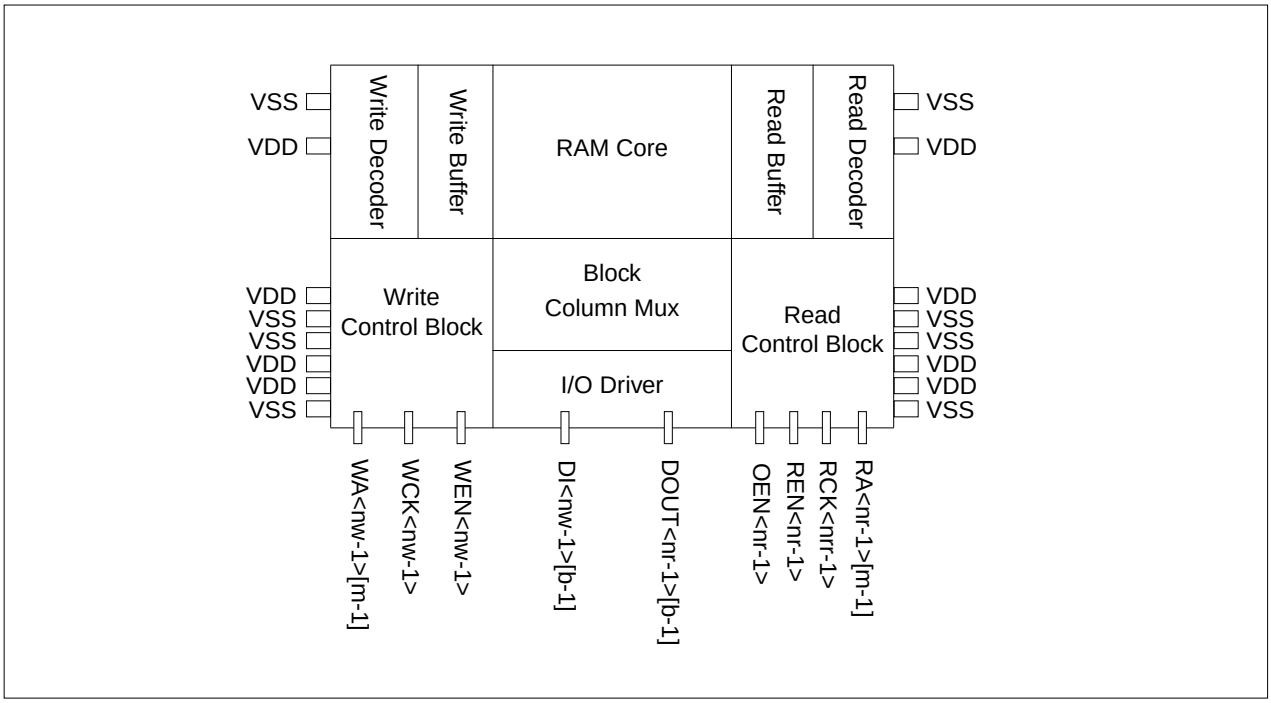
WCK	WEN	WA	DI	RCK	REN	OEN	RA	DOUT
4.32	1.82	1.82	1.82	4.32	1.82	4.44	1.82	12.54

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Block Diagrams

SRFRAM_HDH supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting over-the-cell routing. In SRFRAM_HDH, the over-the-cell routing is permitted for Metal-4 or upper layers. Namely, while doing layout on the chip-level, any signals to be routed can be crossed over the area of register file generated by SRFRAM_HDH compiler.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SRFRAM_HDH.

4. Contention mode under same addresses (RA[]=WA[] or WA0[] = WA1[]). In SRFRAM_HDH, simultaneous operations by both ports on the same addresses (RA[]=WA[] or WA0[] = WA1[]) such as read/write, write/read and write/write operation, cause a contention problem. Simultaneous operations are defined as the state in which both ports are enabled and both address buses are equal. SRFRAM_HDH has no scheme preventing the contention mode. Due to the simultaneous operations, silicon will behave unpredictably. A write operation cannot complete and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports.

5. Power reduction during standby mode. SRFRAM_HDH provides two types of standby modes – the write standby mode and the read standby mode. While in the write standby mode, WA[] and DI[] are blocked even though the transitions of those signals occur. While in the read standby mode, RA[] is blocked even though its transition occurs. So, you can reduce the power consumption in SRFRAM_HDH by properly using two standby modes in your design.

Characteristics

Definition for AC Timing (ns)	
Symbol	**Description**
t_{rcyc}	Min RCK cycle time (rise to rise)
t_{rckl}	Min RCK pulse width low
t_{rckh}	Min RCK pulse width high
t_{wcyc}	Min WCK cycle time (rise to rise)
t_{wckl}	Min WCK pulse width low
t_{wckh}	Min WCK pulse width high
t_{was}	WA setup to WCK rise
t_{wah}	WA hold from WCK rise
t_{ws}	WEN setup to WCK rise
t_{wh}	WEN hold from WCK rise
t_{ds}	DI setup to WCK rise
t_{dh}	DI hold from WCK rise
t_{ras}	RA setup to RCK rise
t_{rah}	RA hold from RCK rise
t_{rs}	REN setup to RCK rise
t_{rh}	REN hold from RCK rise
t_{cc}	Min CK to CK setup time (rise to rise) in read-write, write-read or write-write contention mode.
t_{da}	Output hold time from RCK rise to DOUT Unknown
t_{acc}	Delay from RCK rise to DOUT transition
t_{zd}	Output hold time from OEN fall to DOUT unknown
t_{dz}	Delay from OEN rise to DOUT Transition from Driven to Hi-Z
t_{od}	Delay from OEN fall to DOUT Transition from Hi-Z to Driven
Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_w_standby	The write standby power consumption while WEN is high, other signals are in stable and only WCK is toggled.
Power_r_standby	The read standby power consumption while REN is high, other signals are in stable and only RCK is toggled.
Definition for Static Leakage Current Consumption (μA)	
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.
Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Reference Table

*** For Ymux=2(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.10	1.20
t_{rckl}	0.32	0.32	0.32	0.35	0.35	0.35	0.46	0.46
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{wcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.10	1.20
t_{wckl}	0.32	0.32	0.32	0.35	0.35	0.35	0.46	0.46
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{cc}	0.62	0.64	0.67	0.66	0.68	0.72	0.85	0.89
t_{ras}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.20	0.14	0.16	0.20	0.16	0.20
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.52	0.54	0.60	0.57	0.58	0.64	0.74	0.79
t_{da}	0.42	0.44	0.50	0.47	0.48	0.54	0.63	0.69
t_{dz}	0.10	0.11	0.16	0.10	0.11	0.16	0.11	0.16
t_{zd}	0.12	0.12	0.18	0.12	0.12	0.17	0.12	0.17
t_{od}	0.15	0.17	0.23	0.15	0.17	0.23	0.17	0.23
Power (µW/MHz)								
Power_read	7.46	12.55	23.03	8.23	13.93	25.52	17.96	32.83
Power_write	8.43	13.80	25.13	9.74	16.16	29.49	24.55	45.24
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	14.506	19.096	28.276	25.836	33.128	47.712	89.257	125.457
Area (µm)								
Width	238.24	376.48	652.96	238.24	376.48	652.96	376.48	652.96
Height	59.92	59.92	59.92	101.68	101.68	101.68	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=4(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.91	0.90	0.91	0.97	0.97	0.97	1.14	1.12
t_{rckl}	0.45	0.45	0.45	0.48	0.48	0.48	0.57	0.56
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{wcyc}	0.91	0.90	0.91	0.97	0.97	0.97	1.10	1.12
t_{wckl}	0.45	0.45	0.45	0.48	0.48	0.48	0.14	0.56
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.57	0.55
t_{cc}	0.62	0.64	0.67	0.66	0.68	0.72	0.55	0.89
t_{ras}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.13	0.15	0.18	0.13	0.15	0.18	0.15	0.18
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.58	0.60	0.65	0.62	0.64	0.70	0.79	0.84
t_{da}	0.48	0.50	0.56	0.52	0.54	0.60	0.69	0.75
t_{dz}	0.10	0.10	0.14	0.10	0.10	0.14	0.10	0.14
t_{zd}	0.11	0.11	0.15	0.11	0.11	0.15	0.11	0.15
t_{od}	0.15	0.16	0.20	0.15	0.16	0.20	0.16	0.20
Power (µW/MHz)								
Power_read	5.53	8.65	15.29	5.97	9.37	16.52	11.54	20.29
Power_write	6.47	9.84	17.20	7..24	11.11	19.45	15.66	27.66
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	12.661	15.407	20.897	23.992	29.439	40.334	85.567	118.079
Area (µm)								
Width	238.24	376.48	652.96	238.24	376.48	652.96	376.48	652.96
Height	59.92	59.92	59.92	101.68	101.68	101.68	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Reference Table

*** For Ymux=8(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.16	1.16	1.22	1.20	1.29	1.27	1.33	1.34
t_{rckl}	0.58	0.58	0.61	0.60	0.65	0.63	0.66	0.67
t_{rckh}	0.36	0.36	0.40	0.40	0.45	0.45	0.55	0.55
t_{wcyc}	1.16	1.16	1.22	1.20	1.29	1.27	1.33	1.34
t_{wckl}	0.58	0.58	0.61	0.60	0.65	0.63	0.66	0.67
t_{wckh}	0.36	0.36	0.40	0.40	0.45	0.45	0.55	0.55
t_{cc}	0.64	0.67	0.68	0.72	0.74	0.78	0.85	0.89
t_{ras}	0.16	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.17	0.14	0.13	0.14	0.17	0.14	0.17
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.66	0.71	0.70	0.75	0.75	0.81	0.84	0.90
t_{da}	0.56	0.61	0.60	0.65	0.65	0.71	0.74	0.80
t_{dz}	0.10	0.12	0.10	0.12	0.10	0.12	0.10	0.12
t_{zd}	0.11	0.14	0.11	0.14	0.11	0.14	0.11	0.14
t_{od}	0.15	0.19	0.15	0.19	0.15	0.19	0.15	0.19
Power (µW/MHz)								
Power_read	6.31	10.62	6.72	11.29	7.26	12.19	8.01	13.39
Power_write	7.49	12.52	8.22	13.73	9.19	15.34	10.85	18.15
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	13.562	17.208	27.594	36.644	46.304	62.559	83.723	114.389
Area (µm)								
Width	376.48	652.96	376.48	652.96	376.48	652.96	376.48	652.96
Height	59.92	59.92	101.68	101.68	157.36	157.36	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=2(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.12	1.22
t_{rckl}	0.31	0.31	0.31	0.35	0.34	0.34	0.46	0.46
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{wcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.12	1.22
t_{wckl}	0.31	0.31	0.31	0.35	0.34	0.34	0.46	0.46
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{cc}	0.62	0.64	0.69	0.67	0.69	0.74	0.86	0.91
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.53	0.55	0.62	0.57	0.59	0.67	0.75	0.83
t_{da}	0.43	0.45	0.52	0.47	0.49	0.57	0.65	0.73
t_{dz}	0.11	0.11	0.18	0.11	0.11	0.18	0.11	0.18
t_{zd}	0.12	0.13	0.19	0.12	0.13	0.19	0.13	0.19
t_{od}	0.15	0.18	0.25	0.15	0.18	0.25	0.18	0.25
Power (µW/MHz)								
Power_read	7.63	12.90	23.66	8.34	14.18	25.91	17.97	32.82
Power_write	9.48	15.50	28.20	11.14	18.41	33.45	28.90	52.91
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	21.608	28.342	41.809	39.511	51.205	74.593	142.658	205.731
Area (µm)								
Width	318.32	486.64	823.28	318.32	486.64	823.28	486.64	823.28
Height	88.68	88.68	88.68	135.72	135.72	135.72	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Reference Table

*** For Ymux=4(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.89	0.88	0.87	0.95	0.95	0.94	1.13	1.12
t_{rckl}	0.44	0.44	0.44	0.48	0.47	0.47	0.56	0.54
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{wcyc}	0.89	0.88	0.87	0.95	0.95	0.94	1.13	1.12
t_{wckl}	0.44	0.44	0.44	0.48	0.47	0.47	0.56	0.54
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{cc}	0.62	0.64	0.69	0.67	0.69	0.74	0.86	0.91
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.17	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.15	0.19	0.14	0.15	0.19	0.15	0.19
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.58	0.61	0.68	0.63	0.65	0.72	0.81	0.88
t_{da}	0.49	0.51	0.58	0.53	0.55	0.62	0.71	0.78
t_{dz}	0.10	0.10	0.15	0.10	0.10	0.15	0.10	0.15
t_{zd}	0.11	0.12	0.17	0.11	0.12	0.17	0.12	0.16
t_{od}	0.15	0.17	0.22	0.15	0.17	0.22	0.17	0.22
Power (µW/MHz)								
Power_read	5.66	8.91	15.77	6.07	9.58	16.90	11.65	20.48
Power_write	7.52	11.49	20.15	8.52	13.08	22.90	18.86	33.12
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	19.068	23.262	31.649	36.971	46.125	64.433	137.578	195.571
Area (µm)								
Width	318.32	486.64	823.28	318.32	486.64	823.28	486.64	823.28
Height	88.68	88.68	88.68	135.72	135.72	135.72	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=8(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.13	1.12	1.19	1.16	1.27	1.23	1.31	1.31
t_{rckl}	0.57	0.56	0.60	0.58	0.63	0.61	0.66	0.66
t_{rckh}	0.36	0.36	0.40	0.40	0.46	0.46	0.56	0.56
t_{wcyc}	1.13	1.12	1.19	1.16	1.27	1.23	1.31	1.31
t_{wckl}	0.57	0.56	0.60	0.58	0.63	0.61	0.66	0.66
t_{wckh}	0.36	0.36	0.40	0.40	0.46	0.46	0.56	0.56
t_{cc}	0.64	0.69	0.69	0.74	0.75	0.80	0.86	0.91
t_{ras}	0.17	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.17	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.15	0.18	0.15	0.18	0.15	0.18	0.15	0.18
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.67	0.74	0.71	0.79	0.77	0.84	0.87	0.94
t_{da}	0.57	0.64	0.61	0.69	0.67	0.74	0.77	0.84
t_{dz}	0.10	0.14	0.10	0.14	0.10	0.14	0.10	0.14
t_{zd}	0.11	0.15	0.11	0.15	0.11	0.15	0.11	0.15
t_{od}	0.16	0.20	0.16	0.20	0.16	0.20	0.16	0.20
Power (µW/MHz)								
Power_read	6.51	11.00	6.90	11.63	7.42	12.47	8.16	13.66
Power_write	8.89	14.95	9.82	16.46	11.08	18.47	13.25	22.08
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	20.722	26.569	43.585	59.353	74.069	103.066	135.038	190.491
Area (µm)								
Width	486.64	823.28	486.64	823.28	486.64	823.28	486.64	823.28
Height	88.68	88.68	135.72	135.72	198.44	198.44	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Reference Table

*** For Ymux=2(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.73	0.73	0.83	0.85	0.85	0.95	1.27	1.37
t_{rckl}	0.32	0.32	0.31	0.36	0.36	0.35	0.49	0.50
t_{rckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{wcyc}	0.73	0.73	0.83	0.85	0.85	0.95	1.27	1.37
t_{wckl}	0.32	0.32	0.31	0.36	0.36	0.35	0.49	0.50
t_{wckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{cc}	0.63	0.66	0.71	0.70	0.72	0.78	0.95	1.01
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.17	0.15	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.23	0.14	0.17	0.23	0.17	0.23
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.54	0.57	0.65	0.60	0.63	0.71	0.84	0.92
t_{da}	0.45	0.47	0.56	0.50	0.53	0.61	0.73	0.82
t_{dz}	0.11	0.12	0.20	0.11	0.12	0.20	0.12	0.20
t_{zd}	0.12	0.14	0.22	0.12	0.14	0.22	0.14	0.22
t_{od}	0.16	0.19	0.27	0.16	0.19	0.27	0.19	0.27
Power (µW/MHz)								
Power_read	7.82	13.25	24.29	8.71	14.85	27.14	19.79	35.87
Power_write	8.72	14.39	26.42	10.22	17.09	31.34	27.08	50.01
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	29.280	38.727	57.622	52.727	68.365	99.642	186.917	267.722
Area (µm)								
Width	402.24	604.48	1008.96	402.24	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	107.84	167.36	167.36	167.36	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=4(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.91	0.90	0.88	0.99	0.98	0.96	1.27	1.28
t_{rckl}	0.46	0.45	0.44	0.50	0.49	0.48	0.61	0.63
t_{rckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{wcyc}	0.91	0.90	0.88	0.99	0.98	0.96	1.27	1.28
t_{wckl}	0.46	0.45	0.44	0.50	0.49	0.48	0.61	0.63
t_{wckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{cc}	0.63	0.66	0.71	0.70	0.72	0.78	0.95	1.01
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.17	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.60	0.63	0.71	0.65	0.65	0.77	0.89	0.97
t_{da}	0.50	0.53	0.61	0.56	0.58	0.67	0.79	0.87
t_{dz}	0.10	0.11	0.17	0.10	0.11	0.17	0.11	0.17
t_{zd}	0.11	0.12	0.18	0.11	0.12	0.18	0.12	0.18
t_{od}	0.15	0.17	0.24	0.15	0.17	0.24	0.17	0.24
Power (µW/MHz)								
Power_read	5.80	9.16	16.18	6.30	9.98	17.60	12.62	22.09
Power_write	7.00	10.85	19.23	7.88	12.31	21.79	17.70	31.52
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	25.588	31.344	42.855	49.035	60.982	84.875	179.534	252.955
Area (µm)								
Width	402.24	604.48	1008.96	402.24	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	107.84	167.36	167.36	167.36	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAM_HDH

High-Density Multi-Port Synchronous Register File

Reference Table

*** For Ymux=8(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

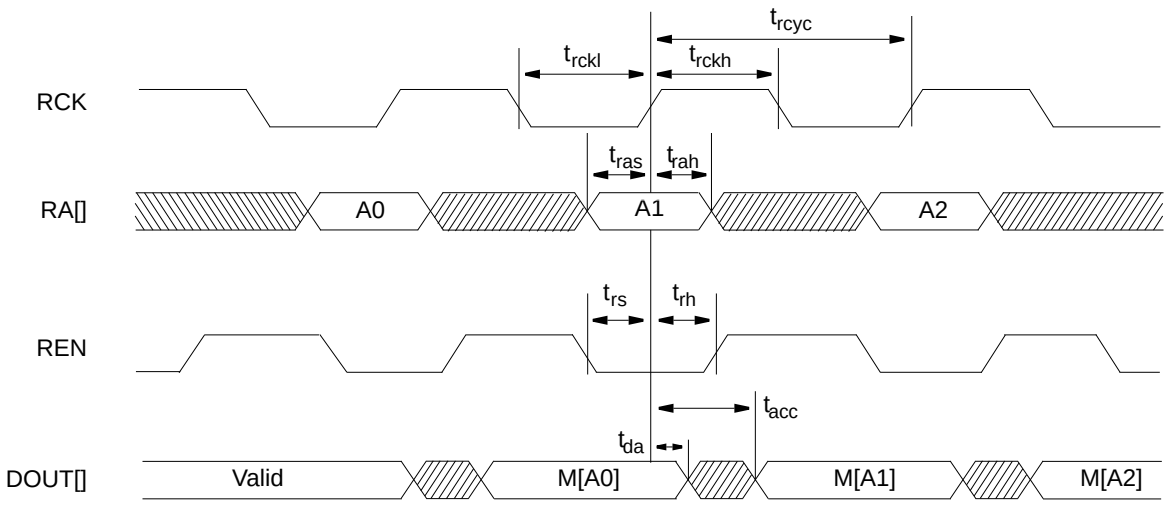
Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.16	1.13	1.20	1.17	1.26	1.22	1.51	1.55
t_{rckl}	0.58	0.56	0.60	0.58	0.63	0.61	0.76	0.78
t_{rckh}	0.37	0.37	0.42	0.42	0.50	0.50	0.64	0.64
t_{wcyc}	1.16	1.13	1.20	1.17	1.26	1.22	1.51	1.55
t_{wckl}	0.58	0.56	0.60	0.58	0.63	0.61	0.76	0.78
t_{wckh}	0.37	0.37	0.42	0.42	0.50	0.50	0.64	0.64
t_{cc}	0.66	0.72	0.72	0.78	0.80	0.86	0.95	1.01
t_{ras}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.15	0.20	0.15	0.20	0.15	0.20	0.15	0.20
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.69	0.77	0.74	0.83	0.81	0.90	0.94	1.03
t_{da}	0.59	0.68	0.64	0.73	0.71	0.80	0.84	0.93
t_{dz}	0.10	0.15	0.10	0.15	0.10	0.15	0.10	0.15
t_{zd}	0.11	0.16	0.11	0.16	0.11	0.16	0.11	0.16
t_{od}	0.16	0.22	0.16	0.22	0.16	0.22	0.16	0.22
Power (µW/MHz)								
Power_read	6.70	11.30	7.17	12.08	7.79	13.12	8.72	14.58
Power_write	8.36	14.19	9.19	15.58	10.31	17.43	12.29	20.84
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	27.652	35.471	57.290	77.491	96.807	133.518	175.842	245.571
Area (µm)								
Width	604.48	1008.96	604.48	1008.96	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	167.36	167.36	246.72	246.72	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAM_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

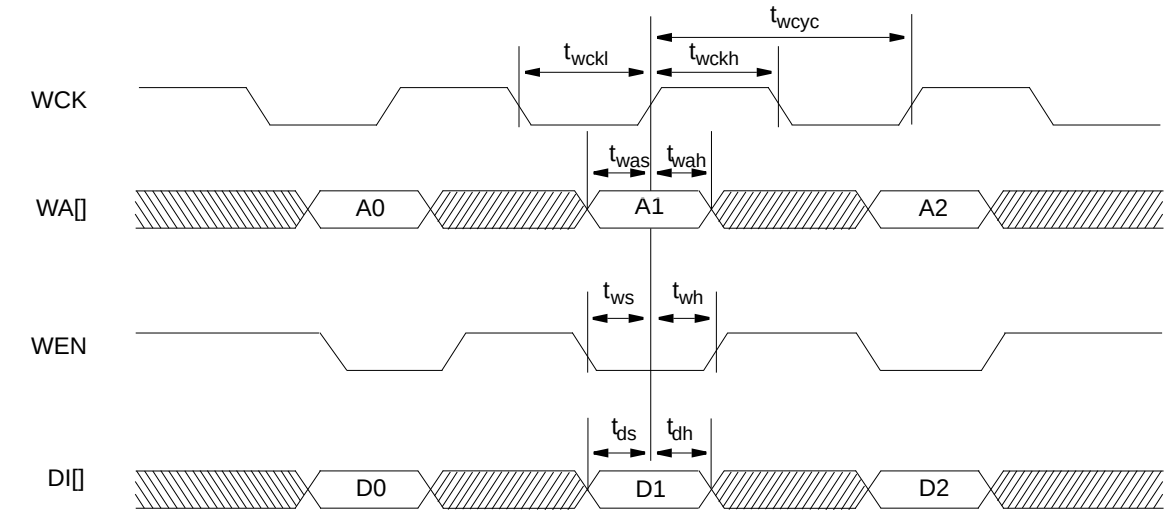
Timing Diagrams

Read Cycle



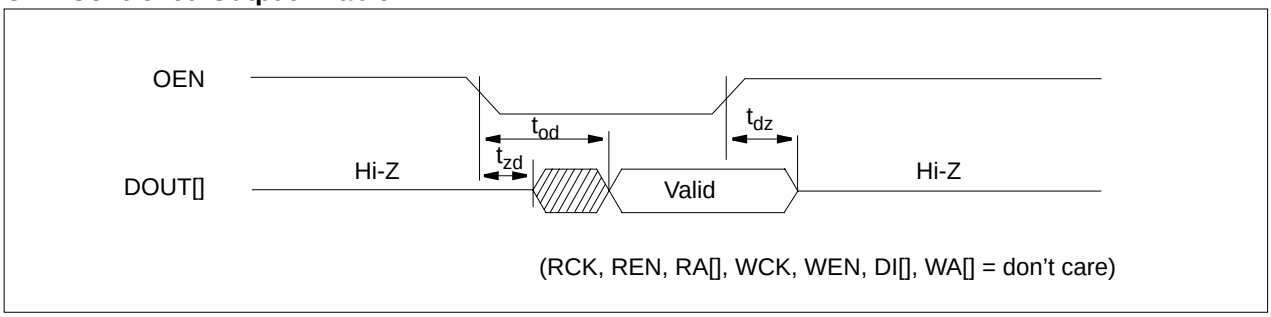
(OEN, REN = low, WCK, WEN, DI[], WA[] = don't care)

Write Cycle

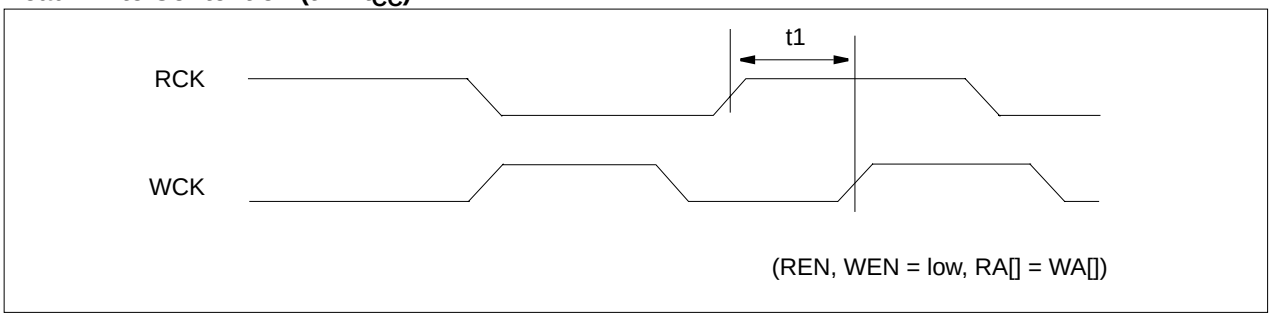


(RCK, REN, OEN, RA[] = don't care)

OEN Controlled Output Enable

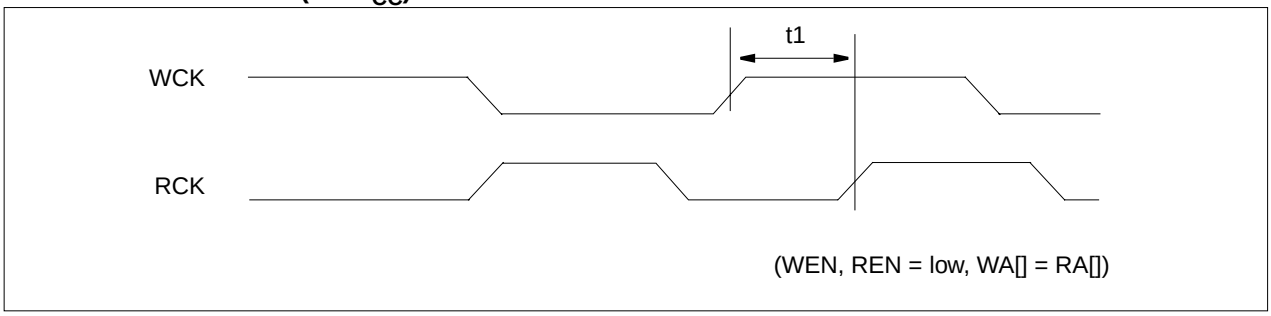


Read-Write Contention (t1 < t_{CC})



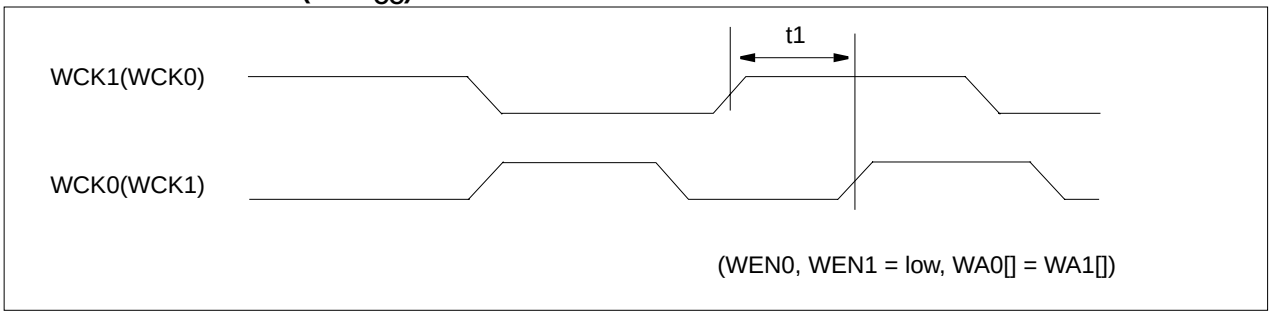
In the read-write contention (RA[] = WA[]), DOUT[] is UNKNOWN while the write data is valid.

Write-Read Contention (t1 < t_{CC})



In the write-read contention (WA[] = RA[]), the write data is valid while DOUT[] is UNKNOWN.

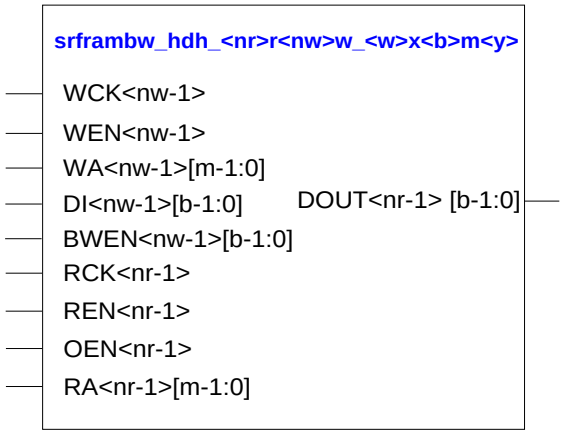
Write-Write Contention (t1 < t_{CC})



In the write-write contention (WA0[] = WA1[]), the write data is unpredictable.

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Writes(nw) is the number of write ports(1-to-2).
5. Reads(nr) is the number of read ports(1-to-2).
6. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Bit-write capability
- Separated data I/O
- Synchronous read/write operation
- Fully independent ports
- Latched inputs and outputs
- Flexible aspect ratio
- Asynchronous tri-state output
- Two ports(1-read and 1-write) available
- Three ports(2-read and 1-write) available
- Four ports(2-read and 2-write) available
- Up to 16Kbits capacity
- Up to 1024 number of words
- Up to 64 number of bits per word

Function Description

SRFRAMBW_HDH is a multi-port synchronous register file with bit-write capability which is provided as a compiler. SRFRAMBW_HDH is intended for use in high-density applications. It allows maximum 4 ports with configurable 1-to-2 read ports and 1-to-2 write ports. All read and write ports are fully independent. Basically, its functionality is exactly same as SRFRAM_HDH except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of WCK, the write cycle is initiated when WEN is low. When the individual bit of BWEN[] is low, the data on the corresponding write data bit of DI[] are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on WA[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on WA[], which is exactly same as the write operation in SRFRAM_HDH. During the write cycle, DOUT[] remains stable. If WEN is high, WA[] and DI[] are disabled. It is called “write standby mode”. On the rising edge of RCK, the read cycle is initiated when REN is low. the data stored in the memory location specified on RA[] become valid through DOUT[] after a delay. If REN is high, RA[] is disabled and DOUT[] remains stable with the previous data output. It is called “read standby mode”. When OEN is high, DOUT[] is placed in a high-impedance state.

SRFRAMBW_HDH Function Table

WCK	WEN	BWEN	WA	DI	RCK	RA	REN	OEN	DOUT	Comment
X	H	X	X	X	X	X	H	L	DOUT(t-1)	De-selected (standby mode)
X	H	X	X	X	X	X	X	X	X	Write standby mode
↑	L	L	Valid	Valid	X	X	X	X	X	Bit write cycle
↑	L	All L	Valid	Valid	X	X	X	X	X	Word write cycle
↑	L	All H	Valid	Valid	X	X	X	X	DOUT(t-1)	No write operation
X	X	X	X	X	X	X	H	L	DOUT(t-1)	Read standby mode
X	X	X	X	X	↑	Valid	L	L	MEM(RA)	Read cycle
X	X	X	X	X	X	X	X	H	Z	Unconditional tri-state output

Parameter Description

SRFRAMBW_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y), Number of read ports(nr) and Number of write ports(nw).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8
Words(w)	Min	4	8	16
	Max	256	512	1024
	Step	2	4	8
Bpw(b)	Min	1	1	1
	Max	64	32	16
	Step	1	1	1
Write ports(nw)		1, 2		
Read ports(nr)		1, 2		

Pin Descriptions

Name	I/O	Description
WCK<nw-1>	Write Clock	Write Clock input on each write port. WEN, WA[] and DI[] are latched into the RAM on the rising edge of WCK. If WEN is low on the rising edge of WCK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in write standby mode.
WEN<nw-1>	Write Enable	Write Enable input on each write port. WEN is latched into the RAM on the rising edge of WCK.When WEN is low, the write mode is enabled. When WEN is high, it prevents the write-operation. It is called “write standby mode”.
WA<nw-1>[]	Write Address	Write Address bus on each write port. It specifies the location in which the data will be written in the write-operation. WA[] is latched at the rising edge of WCK.
BWEN<nw-1>[]	Bit Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising of WCK. Each bit of BWEN[] enables and disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on WA[], but DI[1] is not written.
DI<nw-1>[]	Data Input	Data Input bus on each write port. It contains data values to be written into the memory during the write-cycle. DI[] is latched at the rising edge of WCK.
RCK<nr-1>	Read Clock	Read Clock input on each read port. REN and RA[] are latched into the RAM on the rising edge of RCK. If REN is low on the rising edge of RCK, the RAM is in read mode. If REN is high on the rising edge of RCK, the RAM is in read standby mode.
REN<nr-1>	Read Enable	Read Enable input on each read port. REN is latched into the RAM on the rising edge of RCK. When REN is low, read is enabled. When REN is high, read is disabled and DOUT[] remains in the previous state. It is called “read standby mode”
OEN<nr-1>	Data Output Enable	Output Enable input on each read port. The low state enables output drivers and the high state disables output to go to the Hi-Z state.
RA<nr-1>[]	Read Address	Read Address bus on each read port. It specifies the location to be read in the read-operation. RA[] is latched at the rising edge of RCK.
DOUT<nr-1>[]	Data Output	Data Output bus on each read port. When REN and OEN are low, it presents the data word stored in the location specified by RA[] after the rising edge of RCK. When REN is high and OEN is low, DOUT[] remains in the previous state. When OEN is high, DOUT[] is in the high-impedance state regardless of REN.

Pin Capacitance

Unit: [SL]

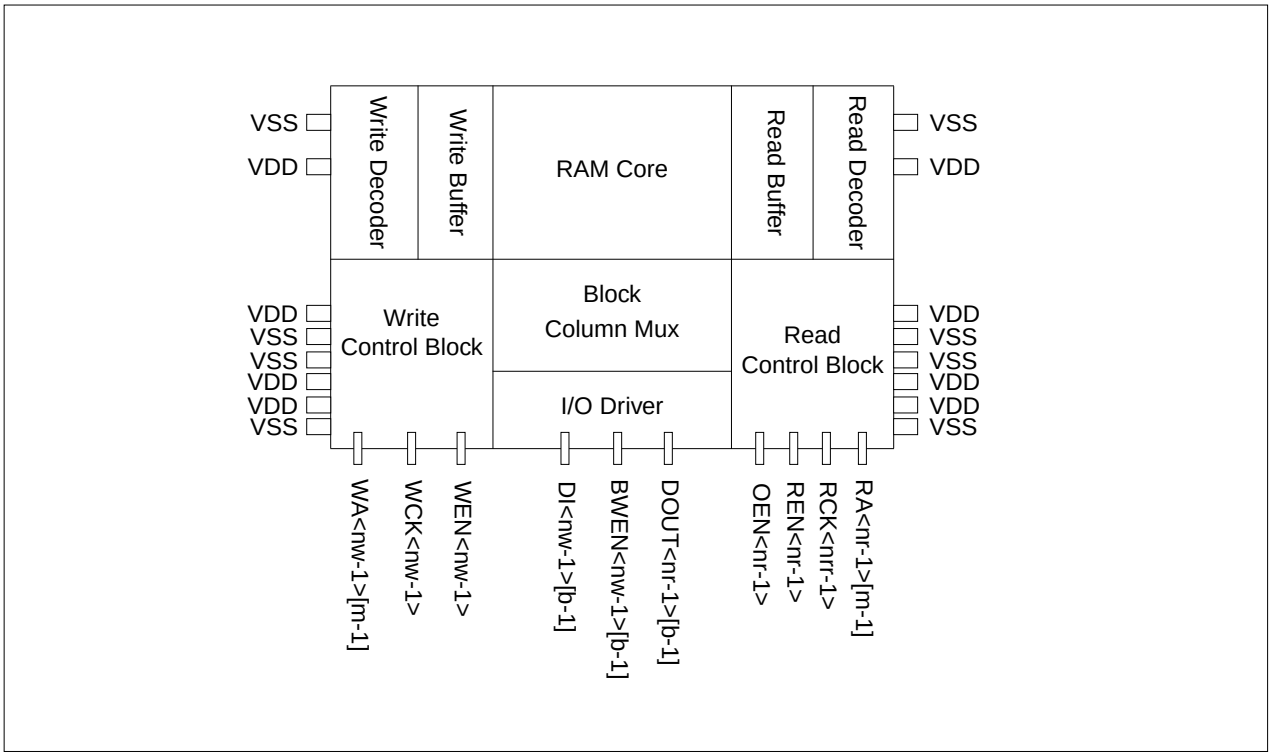
WCK	WEN	WA	DI	BWEN	RCK	REN	OEN	RA	DOUT
4.32	1.82	1.82	1.82	1.82	4.32	1.82	4.44	1.82	12.54

SRFRAMBW_HDH

High-Density Multi-Port Synchronous Register File with Bit-Write

Block Diagrams

SRFRAMBW_HDH supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting over-the-cell routing. In SRFRAMBW_HDH, the over-the-cell routing is permitted for Metal-4 or upper layers. Namely, while doing layout on the chip-level, any signals to be routed can be crossed over the area of register file generated by SRFRAMBW_HDH compiler.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SRFRAMBW_HDH.

4. Contention mode under same addresses (RA[]=WA[] or WA0[] = WA1[]). In SRFRAMBW_HDH, simultaneous operations by both ports on the same address (RA[]=WA[] or WA0[] = WA1[]) such as read/write, write/read and write/write operation, cause a contention problem. Simultaneous operations are defined as the state in which both ports are enabled and both address buses are equal. SRFRAMBW_HDH has no scheme preventing the contention mode. Due to the simultaneous operations, silicon will behave unpredictably. A write operation cannot complete and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports.

5. A byte-write or word-write operation with SRFRAMBW_HDH
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SRFRAM_HDH. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

6. Power reduction during standby mode. SRFRAMBW_HDH provides two types of standby modes – the write standby mode and the read standby mode. While in the write standby mode, WA[] and DI[] are blocked even though the transitions of those signals occur. While in the read standby mode, RA[] is blocked even though its transition occurs. So, you can reduce the power consumption in SRFRAMBW_HDH by properly using two standby modes in your design.

SRFRAMBW_HDH

High-Density Multi-Port Synchronous Register File with Bit-Write

Characteristics

Definition for AC Timing (ns)	
Symbol	**Description**
t_{rcyc}	Min RCK cycle time (rise to rise)
t_{rckl}	Min RCK pulse width low
t_{rckh}	Min RCK pulse width high
t_{wcyc}	Min WCK cycle time (rise to rise)
t_{wckl}	Min WCK pulse width low
t_{wckh}	Min WCK pulse width high
t_{was}	WA setup to WCK rise
t_{wah}	WA hold from WCK rise
t_{ws}	WEN setup to WCK rise
t_{wh}	WEN hold from WCK rise
t_{bws}	BWEN setup to WCK rise
t_{bwh}	BWEN hold from WCK rise
t_{ds}	DI setup to WCK rise
t_{dh}	DI hold from WCK rise
t_{ras}	RA setup to RCK rise
t_{rah}	RA hold from RCK rise
t_{rs}	REN setup to RCK rise
t_{rh}	REN hold from RCK rise
t_{cc}	Min CK to CK setup time (rise to rise) in read-write, write-read or write-write contention mode.
t_{da}	Output hold time from RCK rise to DOUT Unknown
t_{acc}	Delay from RCK rise to DOUT transition
t_{zd}	Output hold time from OEN fall to DOUT unknown
t_{dz}	Delay from OEN rise to DOUT Transition from Driven to Hi-Z
t_{od}	Delay from OEN fall to DOUT Transition from Hi-Z to Driven
Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_w_standby	The write standby power consumption while WEN is high, other signals are in stable and only WCK is toggled.
Power_r_standby	The read standby power consumption while REN is high, other signals are in stable and only RCK is toggled.
Definition for Static Leakage Current Consumption (μA)	
Static_leakage	The static leakage power consumption while CSN is high and all signals including CK are in stable.
Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=2(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.10	1.20
t_{rckl}	0.32	0.32	0.32	0.35	0.35	0.35	0.46	0.46
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{wcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.10	1.20
t_{wckl}	0.32	0.32	0.32	0.35	0.35	0.35	0.46	0.46
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{cc}	0.62	0.64	0.67	0.66	0.68	0.72	0.85	0.89
t_{ras}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.16	0.20	0.14	0.16	0.20	0.16	0.20
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.20	0.14	0.16	0.20	0.16	0.20
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.52	0.54	0.60	0.57	0.58	0.64	0.74	0.79
t_{da}	0.42	0.44	0.50	0.47	0.48	0.54	0.63	0.69
t_{dz}	0.10	0.11	0.16	0.10	0.11	0.16	0.11	0.16
t_{zd}	0.12	0.12	0.18	0.12	0.12	0.17	0.12	0.17
t_{od}	0.15	0.17	0.23	0.15	0.17	0.23	0.17	0.23
Power (µW/MHz)								
Power_read	7.46	12.55	23.03	8.23	13.93	25.52	17.96	32.83
Power_write	8.43	13.80	25.13	9.74	16.16	29.49	24.55	45.24
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	14.506	19.096	28.276	25.836	33.128	47.712	89.257	125.457
Area (µm)								
Width	238.24	376.48	652.96	238.24	376.48	652.96	376.48	652.96
Height	59.92	59.92	59.92	101.68	101.68	101.68	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAMBW_HDH

High-Density Multi-Port Synchronous Register File with Bit-Write

Reference Table

*** For Ymux=4(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.91	0.90	0.91	0.97	0.97	0.97	1.14	1.12
t_{rckl}	0.45	0.45	0.45	0.48	0.48	0.48	0.57	0.56
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.55	0.55
t_{wcyc}	0.91	0.90	0.91	0.97	0.97	0.97	1.10	1.12
t_{wckl}	0.45	0.45	0.45	0.48	0.48	0.48	0.14	0.56
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.57	0.55
t_{cc}	0.62	0.64	0.67	0.66	0.68	0.72	0.55	0.89
t_{ras}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.13	0.15	0.18	0.13	0.15	0.18	0.15	0.18
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.13	0.15	0.18	0.13	0.15	0.18	0.15	0.18
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.58	0.60	0.65	0.62	0.64	0.70	0.79	0.84
t_{da}	0.48	0.50	0.56	0.52	0.54	0.60	0.69	0.75
t_{dz}	0.10	0.10	0.14	0.10	0.10	0.14	0.10	0.14
t_{zd}	0.11	0.11	0.15	0.11	0.11	0.15	0.11	0.15
t_{od}	0.15	0.16	0.20	0.15	0.16	0.20	0.16	0.20
Power (µW/MHz)								
Power_read	5.53	8.65	15.29	5.97	9.37	16.52	11.54	20.29
Power_write	6.47	9.84	17.20	7..24	11.11	19.45	15.66	27.66
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	12.661	15.407	20.897	23.992	29.439	40.334	85.567	118.079
Area (µm)								
Width	238.24	376.48	652.96	238.24	376.48	652.96	376.48	652.96
Height	59.92	59.92	59.92	101.68	101.68	101.68	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=8(nr=1, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.16	1.16	1.22	1.20	1.29	1.27	1.33	1.34
t_{rckl}	0.58	0.58	0.61	0.60	0.65	0.63	0.66	0.67
t_{rckh}	0.36	0.36	0.40	0.40	0.45	0.45	0.55	0.55
t_{wcyc}	1.16	1.16	1.22	1.20	1.29	1.27	1.33	1.34
t_{wckl}	0.58	0.58	0.61	0.60	0.65	0.63	0.66	0.67
t_{wckh}	0.36	0.36	0.40	0.40	0.45	0.45	0.55	0.55
t_{cc}	0.64	0.67	0.68	0.72	0.74	0.78	0.85	0.89
t_{ras}	0.16	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.17	0.14	0.13	0.14	0.17	0.14	0.17
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.17	0.14	0.13	0.14	0.17	0.14	0.17
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.66	0.71	0.70	0.75	0.75	0.81	0.84	0.90
t_{da}	0.56	0.61	0.60	0.65	0.65	0.71	0.74	0.80
t_{dz}	0.10	0.12	0.10	0.12	0.10	0.12	0.10	0.12
t_{zd}	0.11	0.14	0.11	0.14	0.11	0.14	0.11	0.14
t_{od}	0.15	0.19	0.15	0.19	0.15	0.19	0.15	0.19
Power (µW/MHz)								
Power_read	6.31	10.62	6.72	11.29	7.26	12.19	8.01	13.39
Power_write	7.49	12.52	8.22	13.73	9.19	15.34	10.85	18.15
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	13.562	17.208	27.594	36.644	46.304	62.559	83.723	114.389
Area (µm)								
Width	376.48	652.96	376.48	652.96	376.48	652.96	376.48	652.96
Height	59.92	59.92	101.68	101.68	157.36	157.36	268.72	268.72

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAMBW_HDH

High-Density Multi-Port Synchronous Register File with Bit-Write

Reference Table

*** For Ymux=2(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.12	1.22
t_{rckl}	0.31	0.31	0.31	0.35	0.34	0.34	0.46	0.46
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{wcyc}	0.72	0.72	0.82	0.80	0.80	0.90	1.12	1.22
t_{wckl}	0.31	0.31	0.31	0.35	0.34	0.34	0.46	0.46
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{cc}	0.62	0.64	0.69	0.67	0.69	0.74	0.86	0.91
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.53	0.55	0.62	0.57	0.59	0.67	0.75	0.83
t_{da}	0.43	0.45	0.52	0.47	0.49	0.57	0.65	0.73
t_{dz}	0.11	0.11	0.18	0.11	0.11	0.18	0.11	0.18
t_{zd}	0.12	0.13	0.19	0.12	0.13	0.19	0.13	0.19
t_{od}	0.15	0.18	0.25	0.15	0.18	0.25	0.18	0.25
Power (µW/MHz)								
Power_read	7.63	12.90	23.66	8.34	14.18	25.91	17.97	32.82
Power_write	9.48	15.50	28.20	11.14	18.41	33.45	28.90	52.91
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	21.608	28.342	41.809	39.511	51.205	74.593	142.658	205.731
Area (µm)								
Width	318.32	486.64	823.28	318.32	486.64	823.28	486.64	823.28
Height	88.68	88.68	88.68	135.72	135.72	135.72	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=4(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.89	0.88	0.87	0.95	0.95	0.94	1.13	1.12
t_{rckl}	0.44	0.44	0.44	0.48	0.47	0.47	0.56	0.54
t_{rckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{wcyc}	0.89	0.88	0.87	0.95	0.95	0.94	1.13	1.12
t_{wckl}	0.44	0.44	0.44	0.48	0.47	0.47	0.56	0.54
t_{wckh}	0.36	0.36	0.36	0.40	0.40	0.40	0.56	0.56
t_{cc}	0.62	0.64	0.69	0.67	0.69	0.74	0.86	0.91
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.17	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.15	0.19	0.14	0.15	0.19	0.15	0.19
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.15	0.19	0.14	0.15	0.19	0.15	0.19
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.58	0.61	0.68	0.63	0.65	0.72	0.81	0.88
t_{da}	0.49	0.51	0.58	0.53	0.55	0.62	0.71	0.78
t_{dz}	0.10	0.10	0.15	0.10	0.10	0.15	0.10	0.15
t_{zd}	0.11	0.12	0.17	0.11	0.12	0.17	0.12	0.16
t_{od}	0.15	0.17	0.22	0.15	0.17	0.22	0.17	0.22
Power (µW/MHz)								
Power_read	5.66	8.91	15.77	6.07	9.58	16.90	11.65	20.48
Power_write	7.52	11.49	20.15	8.52	13.08	22.90	18.86	33.12
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	19.068	23.262	31.649	36.971	46.125	64.433	137.578	195.571
Area (µm)								
Width	318.32	486.64	823.28	318.32	486.64	823.28	486.64	823.28
Height	88.68	88.68	88.68	135.72	135.72	135.72	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

SRFRAMBW_HDH

High-Density Multi-Port Synchronous Register File with Bit-Write

Reference Table

*** For Ymux=8(nr=2, nw=1)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.13	1.12	1.19	1.16	1.27	1.23	1.31	1.31
t_{rckl}	0.57	0.56	0.60	0.58	0.63	0.61	0.66	0.66
t_{rckh}	0.36	0.36	0.40	0.40	0.46	0.46	0.56	0.56
t_{wcyc}	1.13	1.12	1.19	1.16	1.27	1.23	1.31	1.31
t_{wckl}	0.57	0.56	0.60	0.58	0.63	0.61	0.66	0.66
t_{wckh}	0.36	0.36	0.40	0.40	0.46	0.46	0.56	0.56
t_{cc}	0.64	0.69	0.69	0.74	0.75	0.80	0.86	0.91
t_{ras}	0.17	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.17	0.16	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.15	0.18	0.15	0.18	0.15	0.18	0.15	0.18
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.15	0.18	0.15	0.18	0.15	0.18	0.15	0.18
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.67	0.74	0.71	0.79	0.77	0.84	0.87	0.94
t_{da}	0.57	0.64	0.61	0.69	0.67	0.74	0.77	0.84
t_{dz}	0.10	0.14	0.10	0.14	0.10	0.14	0.10	0.14
t_{zd}	0.11	0.15	0.11	0.15	0.11	0.15	0.11	0.15
t_{od}	0.16	0.20	0.16	0.20	0.16	0.20	0.16	0.20
Power (µW/MHz)								
Power_read	6.51	11.00	6.90	11.63	7.42	12.47	8.16	13.66
Power_write	8.89	14.95	9.82	16.46	11.08	18.47	13.25	22.08
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	20.722	26.569	43.585	59.353	74.069	103.066	135.038	190.491
Area (µm)								
Width	486.64	823.28	486.64	823.28	486.64	823.28	486.64	823.28
Height	88.68	88.68	135.72	135.72	198.44	198.44	323.88	323.88

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=2(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**16**	**16**	**16**	**64**	**64**	**64**	**256**	**256**
bpw	**16**	**32**	**64**	**16**	**32**	**64**	**32**	**64**
Timing (ns)								
t_{rcyc}	0.73	0.73	0.83	0.85	0.85	0.95	1.27	1.37
t_{rckl}	0.32	0.32	0.31	0.36	0.36	0.35	0.49	0.50
t_{rckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{wcyc}	0.73	0.73	0.83	0.85	0.85	0.95	1.27	1.37
t_{wckl}	0.32	0.32	0.31	0.36	0.36	0.35	0.49	0.50
t_{wckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{cc}	0.63	0.66	0.71	0.70	0.72	0.78	0.95	1.01
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.17	0.15	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.16	0.23	0.14	0.17	0.23	0.17	0.23
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.23	0.14	0.17	0.23	0.17	0.23
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.54	0.57	0.65	0.60	0.63	0.71	0.84	0.92
t_{da}	0.45	0.47	0.56	0.50	0.53	0.61	0.73	0.82
t_{dz}	0.11	0.12	0.20	0.11	0.12	0.20	0.12	0.20
t_{zd}	0.12	0.14	0.22	0.12	0.14	0.22	0.14	0.22
t_{od}	0.16	0.19	0.27	0.16	0.19	0.27	0.19	0.27
Power (µW/MHz)								
Power_read	7.82	13.25	24.29	8.71	14.85	27.14	19.79	35.87
Power_write	8.72	14.39	26.42	10.22	17.09	31.34	27.08	50.01
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	29.280	38.727	57.622	52.727	68.365	99.642	186.917	267.722
Area (µm)								
Width	402.24	604.48	1008.96	402.24	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	107.84	167.36	167.36	167.36	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=4(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**32**	**32**	**128**	**128**	**128**	**512**	**512**
bpw	**8**	**16**	**32**	**8**	**16**	**32**	**16**	**32**
Timing (ns)								
t_{rcyc}	0.91	0.90	0.88	0.99	0.98	0.96	1.27	1.28
t_{rckl}	0.46	0.45	0.44	0.50	0.49	0.48	0.61	0.63
t_{rckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{wcyc}	0.91	0.90	0.88	0.99	0.98	0.96	1.27	1.28
t_{wckl}	0.46	0.45	0.44	0.50	0.49	0.48	0.61	0.63
t_{wckh}	0.37	0.37	0.37	0.42	0.42	0.42	0.64	0.64
t_{cc}	0.63	0.66	0.71	0.70	0.72	0.78	0.95	1.01
t_{ras}	0.16	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.16	0.17	0.16	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.17	0.15	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.14	0.16	0.21	0.14	0.16	0.21	0.16	0.21
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.60	0.63	0.71	0.65	0.65	0.77	0.89	0.97
t_{da}	0.50	0.53	0.61	0.56	0.58	0.67	0.79	0.87
t_{dz}	0.10	0.11	0.17	0.10	0.11	0.17	0.11	0.17
t_{zd}	0.11	0.12	0.18	0.11	0.12	0.18	0.12	0.18
t_{od}	0.15	0.17	0.24	0.15	0.17	0.24	0.17	0.24
Power (µW/MHz)								
Power_read	5.80	9.16	16.18	6.30	9.98	17.60	12.62	22.09
Power_write	7.00	10.85	19.23	7.88	12.31	21.79	17.70	31.52
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	25.588	31.344	42.855	49.035	60.982	84.875	179.534	252.955
Area (µm)								
Width	402.24	604.48	1008.96	402.24	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	107.84	167.36	167.36	167.36	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

Reference Table

*** For Ymux=8(nr=2, nw=2)**(Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

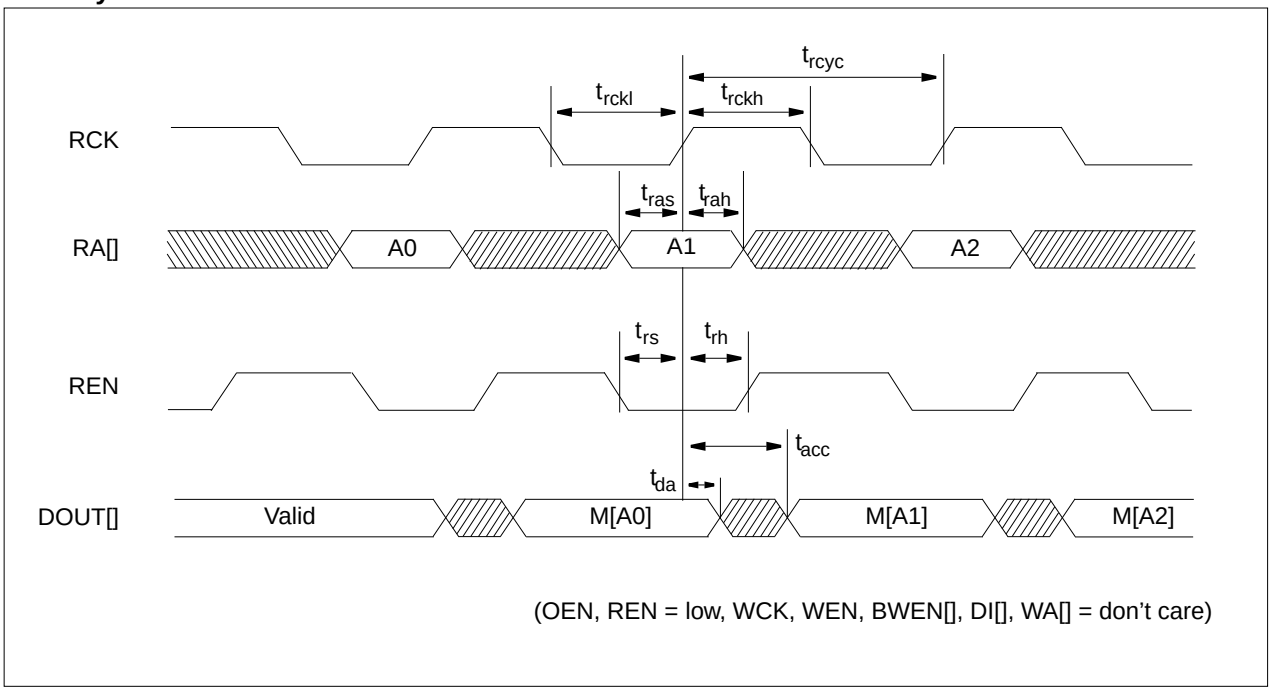
Parameters								
words	**64**	**64**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**8**	**16**	**8**	**16**	**8**	**16**	**8**	**16**
Timing (ns)								
t_{rcyc}	1.16	1.13	1.20	1.17	1.26	1.22	1.51	1.55
t_{rckl}	0.58	0.56	0.60	0.58	0.63	0.61	0.76	0.78
t_{rckh}	0.37	0.37	0.42	0.42	0.50	0.50	0.64	0.64
t_{wcyc}	1.16	1.13	1.20	1.17	1.26	1.22	1.51	1.55
t_{wckl}	0.58	0.56	0.60	0.58	0.63	0.61	0.76	0.78
t_{wckh}	0.37	0.37	0.42	0.42	0.50	0.50	0.64	0.64
t_{cc}	0.66	0.72	0.72	0.78	0.80	0.86	0.95	1.01
t_{ras}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{rah}	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
t_{was}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.17
t_{wah}	0.15	0.15	0.15	0.17	0.15	0.15	0.15	0.15
t_{bws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{bwh}	0.15	0.20	0.15	0.20	0.15	0.20	0.15	0.20
t_{ds}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{dh}	0.15	0.20	0.15	0.20	0.15	0.20	0.15	0.20
t_{ws}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{rh}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{acc}	0.69	0.77	0.74	0.83	0.81	0.90	0.94	1.03
t_{da}	0.59	0.68	0.64	0.73	0.71	0.80	0.84	0.93
t_{dz}	0.10	0.15	0.10	0.15	0.10	0.15	0.10	0.15
t_{zd}	0.11	0.16	0.11	0.16	0.11	0.16	0.11	0.16
t_{od}	0.16	0.22	0.16	0.22	0.16	0.22	0.16	0.22
Power (µW/MHz)								
Power_read	6.70	11.30	7.17	12.08	7.79	13.12	8.72	14.58
Power_write	8.36	14.19	9.19	15.58	10.31	17.43	12.29	20.84
Power_r_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Power_w_standby	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
Static Leakage (µA)								
Static_leakage	27.652	35.471	57.290	77.491	96.807	133.518	175.842	245.571
Area (µm)								
Width	604.48	1008.96	604.48	1008.96	604.48	1008.96	604.48	1008.96
Height	107.84	107.84	167.36	167.36	246.72	246.72	405.44	405.44

NOTES:

1. Standby power is measured on the condition that SRFRAMBW_HDH is deselected and only CK switches.
2. Static leakage current is measured on the condition that all input and output signals are stable.

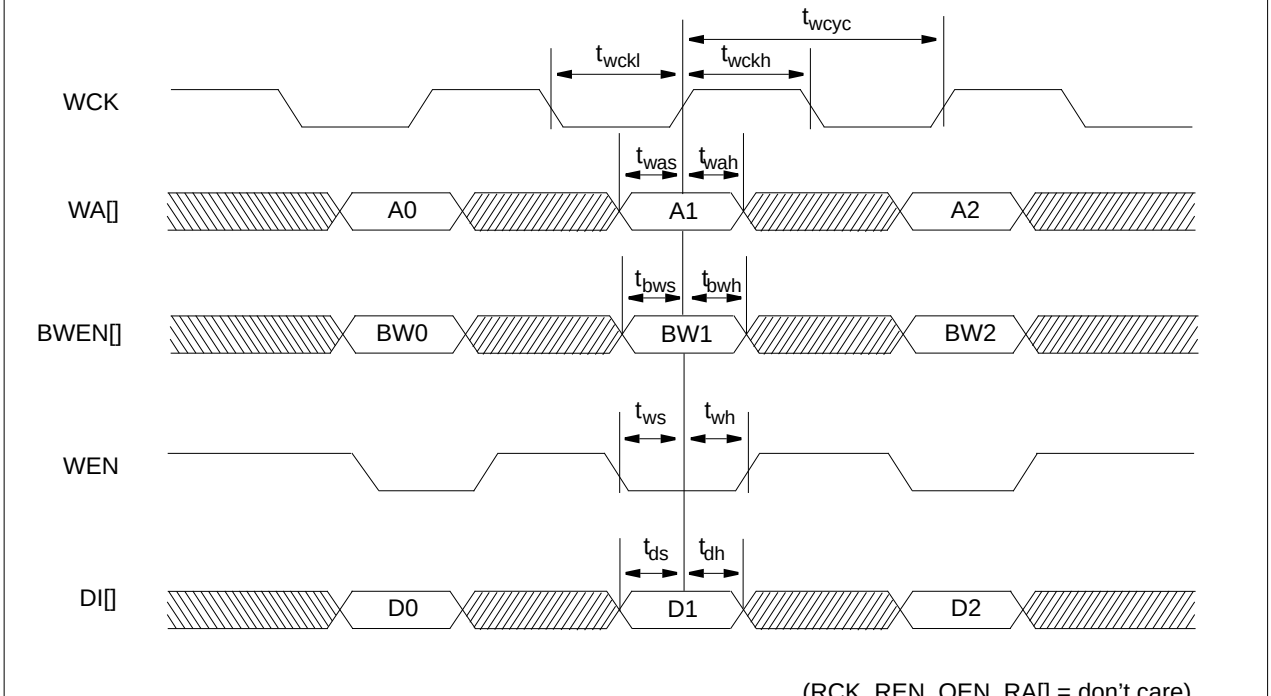
Timing Diagrams

Read Cycle



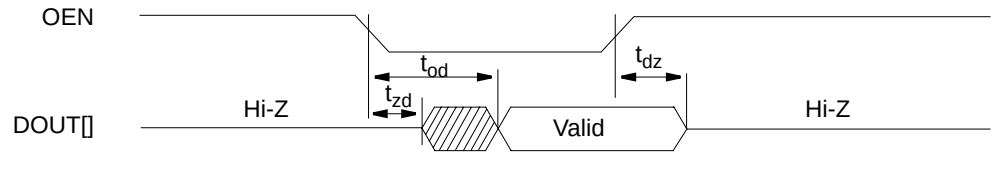
(OEN, REN = low, WCK, WEN, BWEN[], DI[], WA[] = don't care)

Write Cycle



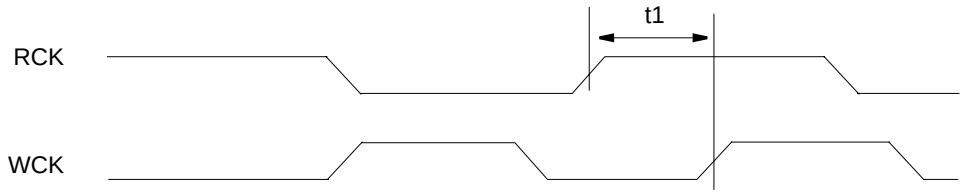
(RCK, REN, OEN, RA[] = don't care)

OEN Controlled Output Enable



(RCK, REN, RA[], WCK, WEN, BWEN[], DI[], WA[] = don't care)

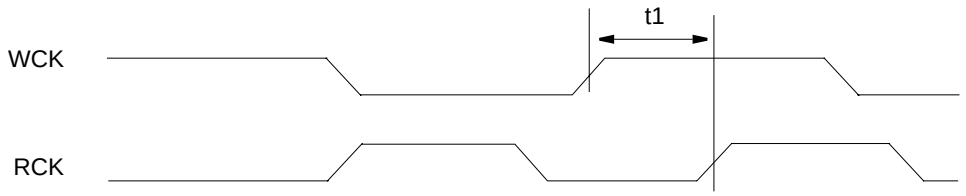
Read-Write Contention (t1 < t_{CC})



(REN, WEN = low, RA[] = WA[])

In the read-write contention (RA[] = WA[]), DOUT[] is UNKNOWN while the write data is valid.

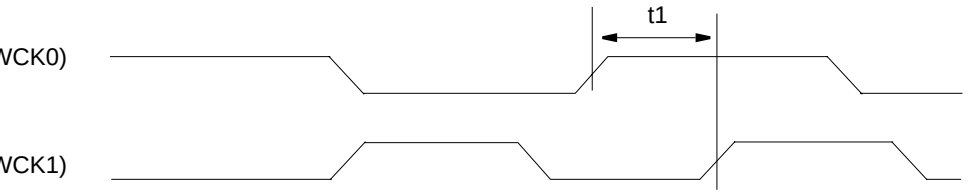
Write-Read Contention (t1 < t_{CC})



(WEN, REN = low, WA[] = RA[])

In the write-read contention (WA[] = RA[]), the write data is valid while DOUT[] is UNKNOWN.

Write-Write Contention (t1 < t_{CC})



(WEN0, WEN1 = low, WA0[] = WA1[])

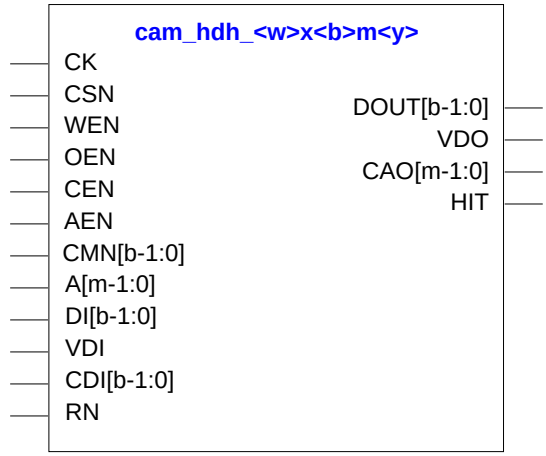
In the write-write contention (WA0[] = WA1[]), the write data is unpredictable.

NOTE: "don't care" means the condition that these pins are in normal operation mode.

CAM_HDH

High-Density Single-Port Synchronous Binary CAM

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density Binary CAM application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Single cycle compare operation
- Low noise output optimization
- Global hit/miss
- Built-in priority address encoder
- Asynchronous reset control for all the valid-bits
- Up to 32K bits capacity
- Up to 512 number of words
- Up to 64 number of bit per word

Function Description

CAM_HDH is a single-port synchronous Binary CAM which is provided as a compiler. CAM_HDH is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low and CEN and RN are high. The data on DI[] is written to the addressed CAM location and VDI overwrites the valid bit associated with CAM entry with the state selected by A[], and DOUT[], VDO, CAO[] and HIT remains stable during a normal write access cycle. On the rising edge of CK, the read cycle begins when WEN is high and CSN is low and CEN and RN are high. The data at DOUT[] become valid after a delay and VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry. On the rising edge of CK, the compare cycle starts when CSN and CEN are low and RN are high, All valid data entries in the CAM are simultaneously searched for the match pattern (CDI[]) defined by mask pattern(CMN[]). CDI[] bits are considered as matched bits at all times, if the corresponding bits of the applied CMN[] are in low states. Each CAM entry can be excluded from the compare function by setting the associated valid bit to a low state by the use of VDI. If one or more entries match with the masked CMN[] pattern, HIT will be asserted and CAO[] will contain the lowest one of all matched addresses by the built-in priority address encoder. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[], VDO, CAO[] and HIT remains stable. When OEN is high, DOUT[] and VDO are placed in a high-impedance state. When AEN is high, CAO[] is placed in a high-impedance state. On the falling edge of RN, all the valid-bits are invalidated and settled to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.

CAM_HDH Function Table

CK	CSN	RN	WEN	AEN	OEN	A	DI/ VDI	CDI	CMN	CEN	DOUT/ VDO	HIT	CAO	Comment
X	X	L	X	L	L	X	X	X	X	X	X	X	X	Reset
X	H	H	X	L	L	X	X	X	X	X	UNCH	UNCH	UNCH	Idle
X	X	X	X	H	H	X	X	X	X	X	Z	UNCH	Z	Tri-state
↑	L	H	L	L	L	Valid	Valid	X	X	H	UNCH	UNCH	UNCH	Write
↑	L	H	H	L	L	Valid	X	X	X	H	Data-out	UNCH	UNCH	Read
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	1	Lowest of all matched addresses	Matched compare cycle
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	0	0	Missed compare cycle

NOTES:

1. DOUT and VDO are high impedance when OEN is high.
2. CAO is high impedance when AEN is high.
3. HIT is 1 if matched or 0 if not.
4. Match pattern is defined by CDI, bit-wise enabled by CMN.

Parameter Description

CAM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w) and Number of bit per word(b) and Column mux(y).

Parameters	Min	Max	Step	Note
Address Inputs(m)	3	9	1	Words(w) is limited to one of (8, 16, 32, 64, 128, 256, 512).
Words (w)	8	512	Note	
Bpw (b)	2	64	1	
Mux(y)	1	1	-	
Capacity	16	32K	-	

CAM_HDH

High-Density Single-Port Synchronous Binary CAM

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[], DI[], CDI[], CMN[], VDI and CEN are latched into the CAM on the rising edge of CK. If CSN and WEN are low and CEN and RN are high on the rising edge of CK, the CAM is in write mode. If CSN is low and WEN is high and CEN and RN are high on the rising edge of CK, the CAM is in read mode. If CSN and CEN are low and RN is high on the rising edge of CK, the CAM is in compare mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the CAM on the rising edge of CK. When CSN is low and RN is high, the CAM is enabled for reading, writing or comparing, depending on the state of WEN and CEN. When CSN is high and RN is high, the CAM goes to the standby mode and is disabled for reading or writing or comparing. DOUT[], VDO, HIT and CAO[] remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the CAM on the rising edge of CK depending on the state of CEN. When CSN and WEN is low and CEN and RN are high, data are written to the addressed location and DOUT[], VDO, HIT and CAO[] remains stable. When CSN is low and WEN is high and CEN and RN are high, data from the addressed word are present at DOUT[] and VDO, whereas HIT and CAO[] remains stable.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT[] and VDO are disabled and go to high-impedance state.
CEN	Compare Enable	Compare enable input. The compare enable is latched into the CAM on the rising edge of CK. When CSN and CEN is low and RN is high, the CAM match function is activated. When CSN is low and CEN and RN are high, only read-write accesses are permitted.
AEN	Address Output Enable	Address output enable input. The address output enable is asynchronously operated regardless of any input. When AEN is high, CAO[] is disabled and goes to high-impedance state.
CMN [ ]	Compare Mask Input	Compare mask input bus. CMN[] defines the pattern which enables the CDI[] pattern to be used for the CAM match function. If the CMN[] bit is low, the corresponding CDI[] bit will be interpreted as a wild card.
A [ ]	Address	Address input bus. The address is latched into the CAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
VDI	Valid Bit Input	Valid Bit Input. VDI overwrites the valid bit associated with the CAM entry with the state selected by A[], during a normal write access cycle. Valid Bit Input are latched on the rising edge of CK.
CDI [ ]	Compare Data Input	Compare Data input bus. Compare-data are latched on the rising edge of CK and define the data pattern to be matched with the CAM entries, in conjunction to CMN[].
RN	Reset Enable	Reset Enable. RN, if low, invalidates all the CAM entries by setting all the valid-bits, one per entry, to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the CAM is in read mode. Data output remains previous data output while the CAM is in write mode and compare mode.
VDO	Valid Bit Output	Valid bit output. VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry.
CAO [ ]	Address Output	Address output bus. CAO[] presents the address of the matched entry, in a single match case. In a multiple-match case, CAO[] is the lowest one of all matched addresses by the built-in priority address encoder.
HIT	Match Output	Match Output. HIT indicates one or more CAM entries matched the masked CDI[], if high.

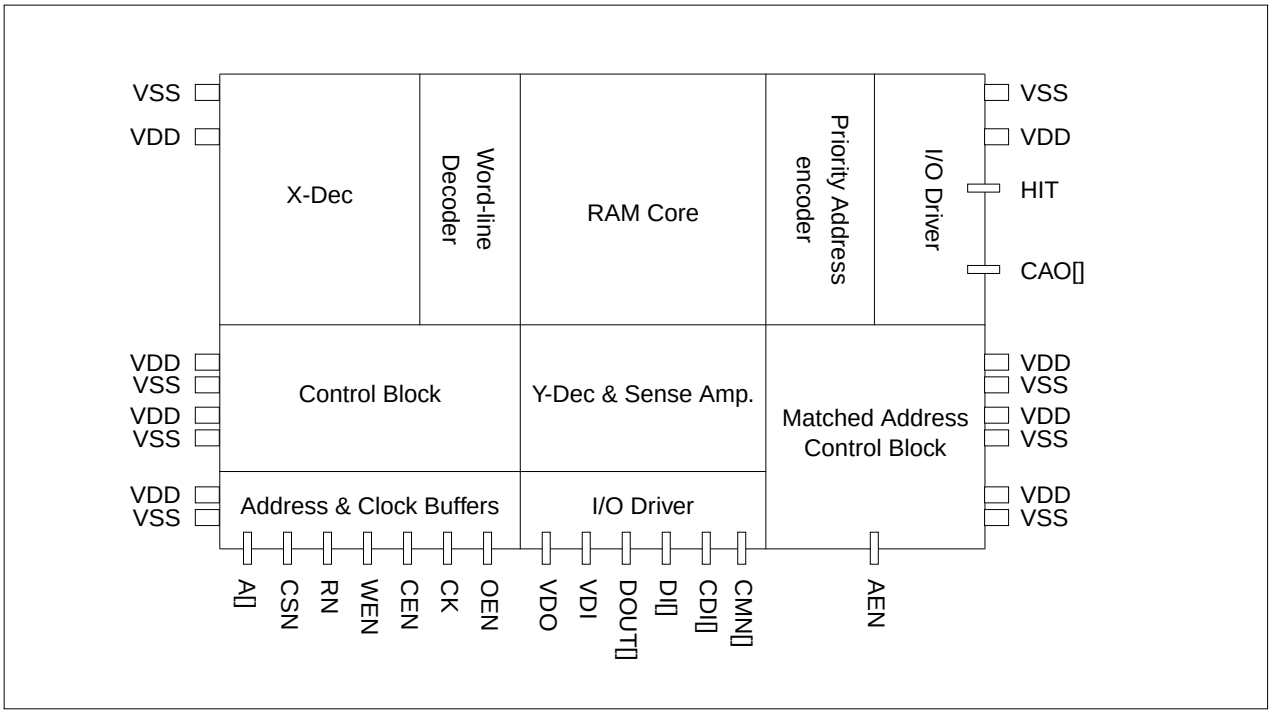
Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	CEN	AEN	CMN	A
4.2388	0.8541	1.2653	0.8854	1.1502	1.1502	1.2653	1.2653
DI	**VDI**	**CDI**	**RN**	**DOUT**	**CDO**	**CAO**	
1.2655	1.2655	1.2653	0.8267	3.0522	3.0522	3.0522	

Block Diagrams

CAM_HDH supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports except HIT and CAO are located on the bottom of the memory. HIT and CAO are located on the right-edge of the memory.



CAM_HDH

High-Density Single-Port Synchronous Binary CAM

Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in CAM_HDH is permitted only for Metal-5 layer or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of CAM_HDH.

4. Power reduction during standby mode. The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{da}	De-access time
t_{ckl}	Clock pulse width low	t_{vdacc}	Validity data access time
t_{ckh}	Clock pulse width high	t_{vdda}	Validity data de-access time
t_{as}	Address setup time	t_{caacc}	Matched address access time
t_{ah}	Address hold time	t_{cada}	Matched address de-access time
t_{cs}	CSN setup time	t_{htacc}	Global Hit/Miss access time
t_{ch}	CSN hold time	t_{htda}	Global Hit/Miss de-access time
t_{ds}	Data-In setup time	t_{dz}	DOUT drive to high-Z time
t_{dh}	Data-In hold time	t_{zd}	DOUT high-Z to drive time
t_{ws}	WEN setup time	t_{od}	OEN to valid output time
t_{wh}	WEN hold time	t_{vddz}	VDO drive to high-Z time
t_{ces}	CEN setup time	t_{vdzd}	VDO high-Z to drive time
t_{ceh}	CEN hold time	t_{vdod}	OEN to valid output time for VDO
t_{cms}	CMN setup time	t_{cadz}	CAO drive to high-Z time
t_{cmh}	CMN hold time	t_{cazd}	CAO high-Z to drive time
t_{vds}	VDI setup time	t_{caod}	AEN to valid output time for CAO
t_{vdh}	VDI hold time	t_{rn}	Min RN pulse width low
t_{cds}	CDI setup time	t_{rns}	RN setup time
t_{cdh}	CDI hold time	t_{rnh}	RN hold time
t_{acc}	Data access time		

Definition for Power Consumption (µW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_compare	The dynamic average power consumption while in a compare cycle
Power_reset	The dynamic average power consumption while in a reset mode
Power_standby	The standby power consumption while CSN and RN are high, OEN and AEN are low and other signals are in stable except that CK is toggled
Static Leakage Current Consumption (uA)	
Static_leakage	The static leakage power consumption while CSN is high and other signals including CK are in stable.
Definition for Area (µm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

CAM_HDH

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Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**8**	**8**	**8**	**8**	**8**	**8**
Timing (ns)						
t_{cyc}	1.76	1.78	1.82	1.91	2.39	3.78
t_{ckl}	0.31	0.32	0.32	0.33	0.33	0.33
t_{ckh}	0.53	0.53	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.31	0.32	0.32	0.33	0.33	0.33
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.15	0.15	0.15	0.15	0.15	0.15
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.15	0.15	0.15	0.15	0.15	0.15
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	0.97	1.00	1.05	1.14	1.34	1.82
t_{da}	0.58	0.61	0.66	0.75	0.95	1.43
t_{dz}	0.12	0.12	0.12	0.12	0.12	0.12
t_{zd}	0.13	0.13	0.13	0.13	0.13	0.13
t_{od}	0.47	0.47	0.47	0.47	0.47	0.47
t_{vdacc}	0.97	1.00	1.05	1.14	1.34	1.82
t_{vdda}	0.58	0.61	0.66	0.75	0.95	1.43
t_{vddz}	0.12	0.12	0.12	0.12	0.12	0.12
t_{vdzd}	0.13	0.13	0.13	0.13	0.13	0.13
t_{vdod}	0.47	0.47	0.47	0.47	0.47	0.47
t_{caacc}	1.30	1.34	1.48	1.60	1.99	2.55
t_{cada}	0.56	0.58	0.61	0.68	0.90	1.30
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.47	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.21	1.27	1.36	1.47	1.75	2.16
t_{htda}	0.56	0.58	0.61	0.68	0.90	1.30
t_{rn}	1.16	1.18	1.22	1.31	1.79	3.18
t_{rns}	0.31	0.32	0.32	0.33	0.33	0.33
t_{rnh}	1.16	1.18	1.22	1.31	1.79	3.18
Power (µW/MHz)						
Power_write	6.38	7.56	9.85	14.48	23.91	44.00
Power_read	6.10	7.08	8.83	12.22	19.16	34.54
Power_compare	18.64	23.86	33.19	51.06	85.18	118.15
Power_standby	1.07	1.45	2.17	3.59	6.40	12.01
Power_reset	1.30	1.85	2.97	5.27	10.08	21.55
Static_current (µA)						
Static_current	17.971	23.864	35.440	58.303	103.734	194.526
Area (µm)						
Width	144.68	159.28	173.88	188.48	203.09	217.69
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**16**	**16**	**16**	**16**	**16**	**16**
Timing (ns)						
t_{cyc}	1.84	1.86	1.89	1.96	2.14	3.80
t_{ckl}	0.32	0.32	0.32	0.33	0.33	0.33
t_{ckh}	0.53	0.53	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.33
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.00	1.02	1.07	1.16	1.36	1.85
t_{da}	0.60	0.63	0.68	0.77	0.97	1.46
t_{dz}	0.13	0.13	0.13	0.13	0.13	0.13
t_{zd}	0.15	0.15	0.15	0.15	0.15	0.15
t_{od}	0.48	0.49	0.48	0.48	0.49	0.48
t_{vdacc}	1.00	1.02	1.07	1.16	1.36	1.85
t_{vdda}	0.60	0.63	0.68	0.77	0.97	1.46
t_{vddz}	0.13	0.13	0.13	0.13	0.13	0.13
t_{vdzd}	0.15	0.15	0.15	0.15	0.15	0.15
t_{vdod}	0.48	0.49	0.48	0.48	0.49	0.48
t_{caacc}	1.36	1.41	1.55	1.68	2.08	2.64
t_{cada}	0.63	0.65	0.68	0.75	0.99	1.43
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.47	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.27	1.34	1.43	1.55	1.83	2.25
t_{htda}	0.63	0.65	0.68	0.75	0.99	1.43
t_{rn}	1.24	1.26	1.29	1.36	1.81	3.20
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.33
t_{rnh}	1.24	1.26	1.29	1.36	1.81	3.20
Power (μW/MHz)						
Power_write	8.85	10.60	14.13	21.16	35.37	65.00
Power_read	8.53	10.04	12.63	17.51	27.41	48.88
Power_compare	27.81	35.49	49.72	77.18	129.41	167.37
Power_standby	1.67	2.37	3.74	6.44	11.80	22.51
Power_reset	1.60	2.31	3.75	6.69	12.77	26.76
Static_current (μA)						
Static_current	29.120	37.070	52.800	83.960	145.860	269.520
Area (μm)						
Width	181.16	195.76	210.36	224.96	239.57	254.17
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

CAM_HDH

High-Density Single-Port Synchronous Binary CAM

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**32**	**32**	**32**	**32**	**32**	**32**
Timing (ns)						
t_{cyc}	2.11	2.13	2.17	2.23	2.51	3.84
t_{ckl}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ckh}	0.53	0.53	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.20	0.20	0.20	0.20	0.20	0.20
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.20	0.20	0.20	0.20	0.20	0.20
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.20	0.20	0.20	0.20	0.20	0.20
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.20	0.20	0.20	0.20	0.20	0.20
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.04	1.06	1.11	1.21	1.41	1.89
t_{da}	0.65	0.67	0.72	0.82	1.02	1.50
t_{dz}	0.16	0.16	0.16	0.16	0.16	0.16
t_{zd}	0.17	0.17	0.17	0.17	0.17	0.17
t_{od}	0.51	0.51	0.51	0.51	0.51	0.51
t_{vdacc}	1.04	1.06	1.11	1.21	1.41	1.89
t_{vdda}	0.65	0.67	0.72	0.82	1.02	1.50
t_{vddz}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdzd}	0.17	0.17	0.17	0.17	0.17	0.17
t_{vdod}	0.51	0.51	0.51	0.51	0.51	0.51
t_{caacc}	1.48	1.52	1.66	1.80	2.21	2.78
t_{cada}	0.74	0.76	0.80	0.88	1.12	1.57
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.47	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.39	1.46	1.54	1.67	1.97	2.39
t_{htda}	0.74	0.76	0.80	0.88	1.12	1.57
t_{rn}	1.51	1.53	1.57	1.63	1.91	3.24
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.34
t_{rnh}	1.51	1.53	1.57	1.63	1.91	3.24
Power (μW/MHz)						
Power_read	13.86	16.80	22.67	34.38	57.92	106.09
Power_write	13.40	15.95	20.17	27.91	43.48	76.64
Power_compare	45.80	57.72	80.53	124.70	208.71	268.95
Power_standby	2.85	4.16	6.75	11.87	22.91	42.50
Power_reset	2.18	3.19	5.24	9.39	17.91	36.81
Static_current (μA)						
Static_current	51.240	63.160	86.860	133.950	227.440	414.160
Area (μm)						
Width	254.12	268.72	283.32	297.92	312.53	327.13
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

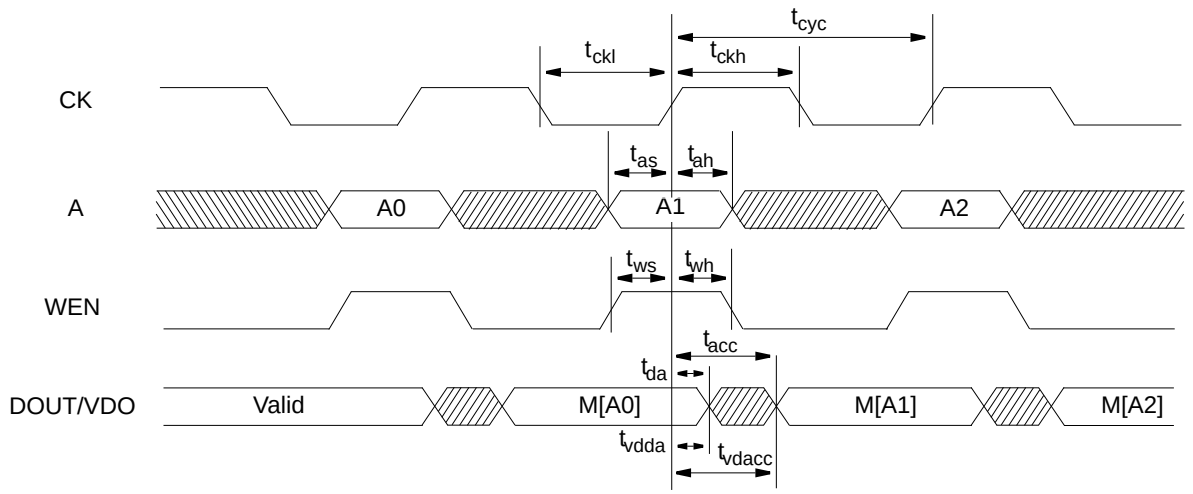
Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**64**	**64**	**64**	**64**	**64**	**64**
Timing (ns)						
t_{cyc}	2.58	2.61	2.65	2.72	3.01	3.92
t_{ckl}	0.31	0.32	0.32	0.33	0.33	0.34
t_{ckh}	0.53	0.52	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.11	1.14	1.20	1.30	1.50	1.98
t_{da}	0.72	0.75	0.81	0.91	1.11	1.59
t_{dz}	0.21	0.21	0.21	0.21	0.21	0.21
t_{zd}	0.21	0.21	0.21	0.21	0.21	0.21
t_{od}	0.55	0.55	0.55	0.55	0.55	0.55
t_{vdacc}	1.11	1.14	1.20	1.30	1.50	1.98
t_{vdda}	0.72	0.75	0.81	0.91	1.11	1.59
t_{vddz}	0.21	0.21	0.21	0.21	0.21	0.21
t_{vdzd}	0.21	0.21	0.21	0.21	0.21	0.21
t_{vdod}	0.55	0.55	0.55	0.55	0.55	0.55
t_{caacc}	1.69	1.73	1.87	2.02	2.44	3.02
t_{cada}	0.96	0.98	1.02	1.10	1.35	1.81
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.46	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.60	1.67	1.76	1.89	2.19	2.64
t_{htda}	0.96	0.98	1.02	1.10	1.35	1.81
t_{rn}	1.98	2.01	2.05	2.12	2.41	3.32
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.34
t_{rnh}	1.98	2.01	2.05	2.12	2.41	3.32
Power (µW/MHz)						
Power_write	24.48	29.69	40.10	61.02	103.11	188.26
Power_read	23.32	27.91	35.36	48.86	75.71	132.08
Power_compare	81.49	100.42	137.77	210.72	351.36	483.74
Power_standby	5.21	7.71	12.71	22.64	42.48	82.10
Power_reset	3.34	4.96	8.21	14.76	28.09	56.59
Static_current (µA)						
Static_current	95.400	115.190	154.710	233.380	389.560	701.430
Area (µm)						
Width	400.04	414.64	429.24	443.84.	458.45	473.05
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

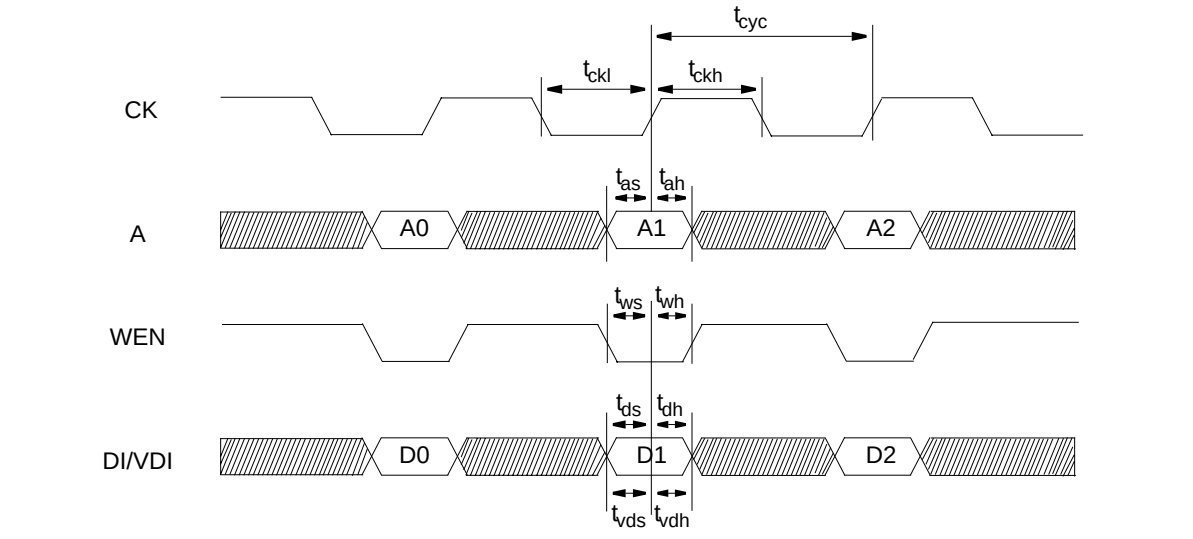
Timing Diagrams

Read Cycle



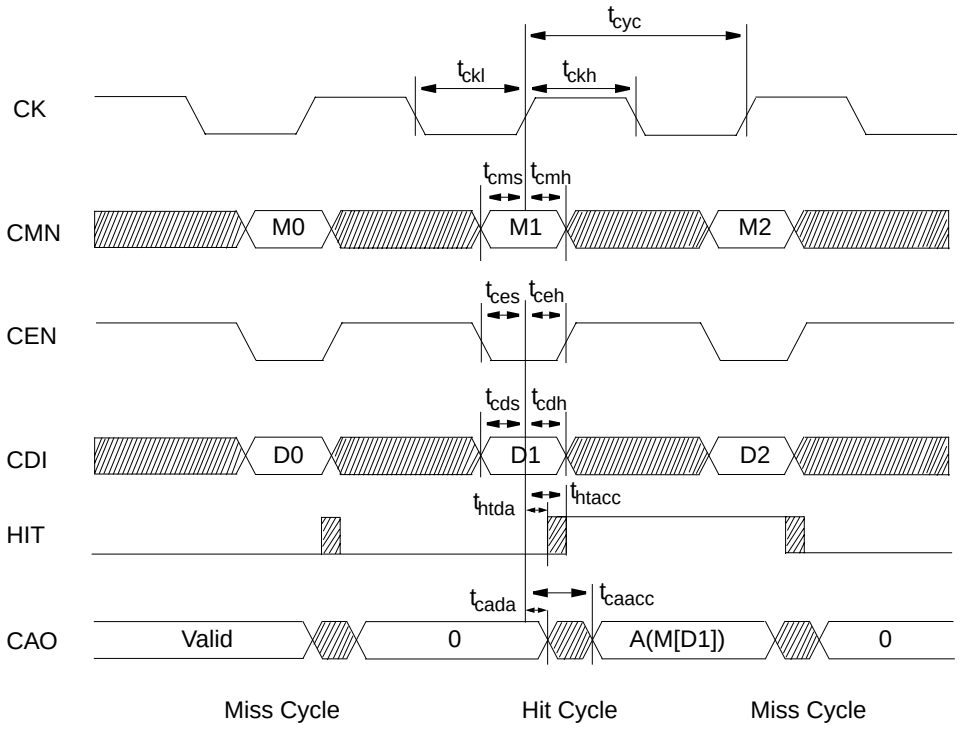
(RN=high, CSN=low, OEN=low, CEN=high, AEN, DI, VDI, CDI, CMN= don't care)

Write Cycle



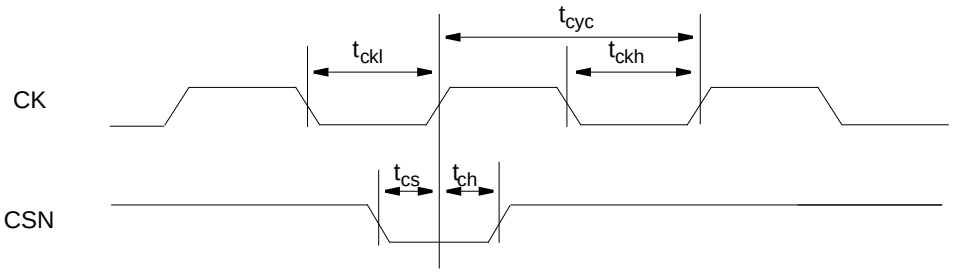
(RN = high, CSN = low, CEN = high, OEN, AEN, CDI, CMN = don't care)

Compare Cycle



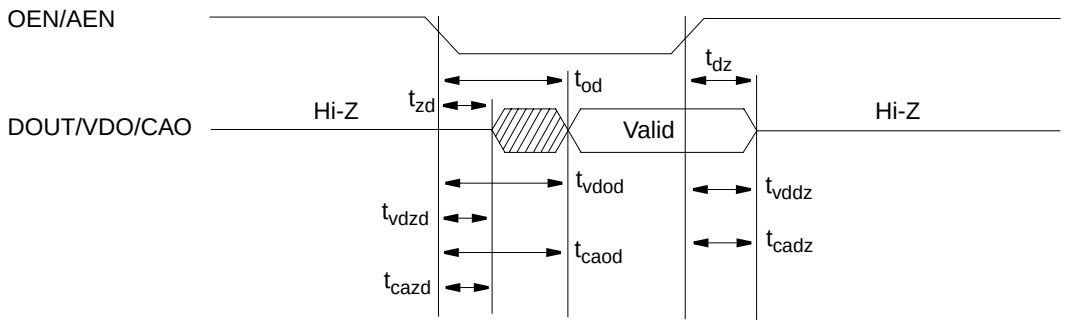
(RN = high, CSN = low, A, WEN, OEN, AEN, DI = don't care)

CSN Controlled



(RN, WEN, OEN CEN, AEN, A, DI, VDI, CDI, CMN = valid)

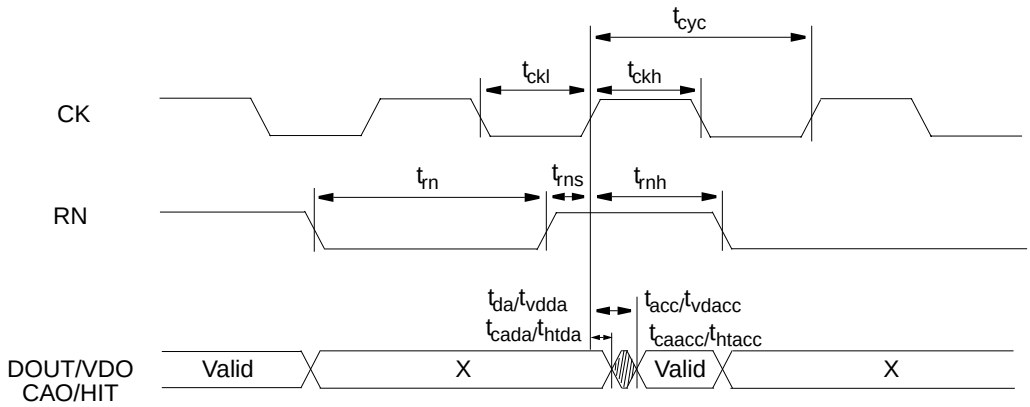
OEN/AEN Controlled Output Enable



(RN, CK, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = don't care)

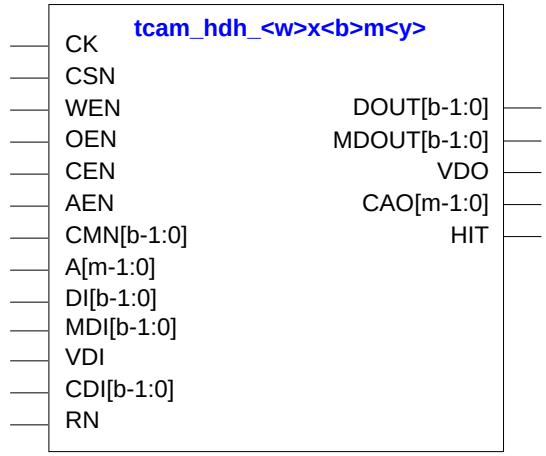
NOTE: "don't care" means the condition that these pins are in normal operation mode.

RN Controlled Reset Mode



(OEN, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = valid)

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density Ternary CAM application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Single cycle compare operation
- Low noise output optimization
- Global hit/miss
- Built-in priority address encoder
- Asynchronous reset control for all the valid-bits
- Up to 32Kbits capacity
- Up to 512 number of words
- Up to 64 number of bit per word

Function Description

TCAM_HDH is a single-port synchronous Ternary CAM which is provided as a compiler. TCAM_HDH is intended for use in high-density applications. TCAM_HDH stores a ”don’t care” state in addition to the 0s and 1s stored in a binary CAM. In a ternary CAM, for each word in the CAM data array, there is a corresponding word in the mask array. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low and CEN and RN are high. The data on DI[] are written to the addressed CAM data information location, the data on MDI[] are written to the addressed CAM mask information location, and VDI overwrites the valid bit associated with CAM entry with the state selected by A[]. DOUT[], MDOUT[], VDO, CAO[] and HIT remain stable during a normal write access cycle. On the rising edge of CK, the read cycle begins when WEN is high and CSN is low and CEN and RN are high. The data information at DOUT[] and the mask information at MDOUT[] become valid after a delay and VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry. On the rising edge of CK, the compare cycle starts when CSN and CEN are low and RN are high, All valid data entries in the CAM with a local mask array are simultaneously searched for the match pattern (CDI[]) defined by global mask pattern(CMN[]). The masking can be global or local. Global masks apply to all words of the CAM while a local mask applies only to a particular word of the CAM. CDI[] bits are considered as matched bits at all times, if the corresponding bits of the applied CMN[] are in low states. A single bit or multiple bits of a word can be ignored during a search operation. Each CAM entry can be excluded from the compare function by setting the associated valid bit to a low state by the use of VDI. If one or more entries match with the globally masked CMN[] pattern and the local mask array, HIT will be asserted and CAO[] will contain the lowest one of all matched addresses by the built-in priority address encoder. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[], MDOUT[], VDO, CAO[] and HIT remains stable. When OEN is high, DOUT[], MDOUT[], VDO are placed in a high-impedance state. When AEN is high, CSO[] is placed in a high-impedance state. On the falling edge of RN, all the valid-bits are invalidated and setted to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.

TCAM_HDH

High-Density Single-Port Synchronous Ternary CAM

TCAM_HDH Function Table

CK	CSN	RN	WEN	AEN	OEN	A	DI/ MDI/ VDI	CDI	CMN	CEN	DOUT/ MDOUT/ VDO	HIT	CAO	Comment
X	X	L	X	L	L	X	X	X	X	X	X	X	X	Reset
X	H	H	X	L	L	X	X	X	X	X	UNCH	UNCH	UNCH	Idle
X	X	X	X	H	H	X	X	X	X	X	Z	UNCH	Z	Tri-state
↑	L	H	L	L	L	Valid	Valid	X	X	H	UNCH	UNCH	UNCH	Write
↑	L	H	H	L	L	Valid	X	X	X	H	Data-out	UNCH	UNCH	Read
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	1	Lowest of all matched addresses	Matched compare cycle
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	0	0	Missed compare cycle

NOTES:

1. DOUT and MDOUT and VDO are high impedance when OEN is high.
2. CAO is high impedance when AEN is high.
3. HIT is 1 if matched or 0 if not.
4. Match pattern is defined by CDI, bit-wise enabled by CMN and local mask array.

Parameter Description

TCAM_HDH is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w) and Number of bit per word(b) and Column mux(y).

Parameters	Min	Max	Step	Note
Address Inputs(m)	3	9	1	Words(w) is limited to one of (8, 16, 32, 64, 128, 256, 512).
Words (w)	8	512	Note	
Bpw (b)	2	64	1	
Mux(y)	1	1	-	
Capacity	16	32K	-	

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[], DI[], CDI[], CMN[], VDI and CEN are latched into the CAM on the rising edge of CK. If CSN and WEN are low and CEN and RN are high on the rising edge of CK, the CAM is in write mode. If CSN is low and WEN is high and CEN and RN are high on the rising edge of CK, the CAM is in read mode. If CSN and CEN are low and RN is high on the rising edge of CK, the CAM is in compare mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the CAM on the rising edge of CK. When CSN is low and RN is high, the CAM is enabled for reading, writing or comparing, depending on the state of WEN and CEN. When CSN is high and RN is high, the CAM goes to the standby mode and is disabled for reading or writing or comparing. DOUT[], VDO, HIT and CAO[] remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the CAM on the rising edge of CK depending on the state of CEN. When CSN and WEN is low and CEN and RN are high, data are written to the addressed location and DOUT[], VDO, HIT and CAO[] remains stable. When CSN is low and WEN is high and CEN and RN are high, data from the addressed word are present at DOUT[] and VDO, whereas HIT and CAO[] remains stable.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT[] and VDO are disabled and go to high-impedance state.
CEN	Compare Enable	Compare enable input. The compare enable is latched into the CAM on the rising edge of CK. When CSN and CEN is low and RN is high, the CAM match function is activated. When CSN is low and CEN and RN are high, only read-write accesses are permitted.
AEN	Address Output Enable	Address output enable input. The address output enable is asynchronously operated regardless of any input. When AEN is high, CAO[] is disabled and goes to high-impedance state.
CMN [ ]	Compare Mask Input	Compare mask input bus. CMN[] defines the pattern which enables the CDI[] pattern to be used for the CAM match function. If the CMN[] bit is low, the corresponding CDI[] bit will be interpreted as a wild card.
A [ ]	Address	Address input bus. The address is latched into the CAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
MDI [ ]	Mask Data Input	Mask data input bus. Mask data are latched on the rising edge of CK. Mask data input is written into the addressed mask information location in write mode.
VDI	Valid Bit Input	Valid Bit Input. VDI overwrites the valid bit associated with the CAM entry with the state selected by A[], during a normal write access cycle. Valid Bit Input are latched on the rising edge of CK.
CDI [ ]	Compare Data Input	Compare Data input bus. Compare-data are latched on the rising edge of CK and define the data pattern to be matched with the CAM entries, in conjunction to CMN[].
RN	Reset Enable	Reset Enable. RN, if low, invalidates all the CAM entries by setting all the valid-bits, one per entry, to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the CAM is in read mode. Data output remains previous data output while the CAM is in write mode and compare mode.
MDOUT [ ]	Mask Data Output	Mask data output bus. Mask data output is valid after the rising edge of CK while the CAM is in read mode. Mask data output remains previous mask data output while the CAM is in write mode and compare mode.
VDO	Valid Bit Output	Valid bit output. VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry.
CAO [ ]	Address Output	Address output bus. CAO[] presents the address of the matched entry, in a single match case. In a multiple-match case, CAO[] is the lowest one of all matched addresses by the built-in priority address encoder.
HIT	Match Output	Match Output. HIT indicates one or more CAM entries matched the masked CDI[], if high.

TCAM_HDH

High-Density Single-Port Synchronous Ternary CAM

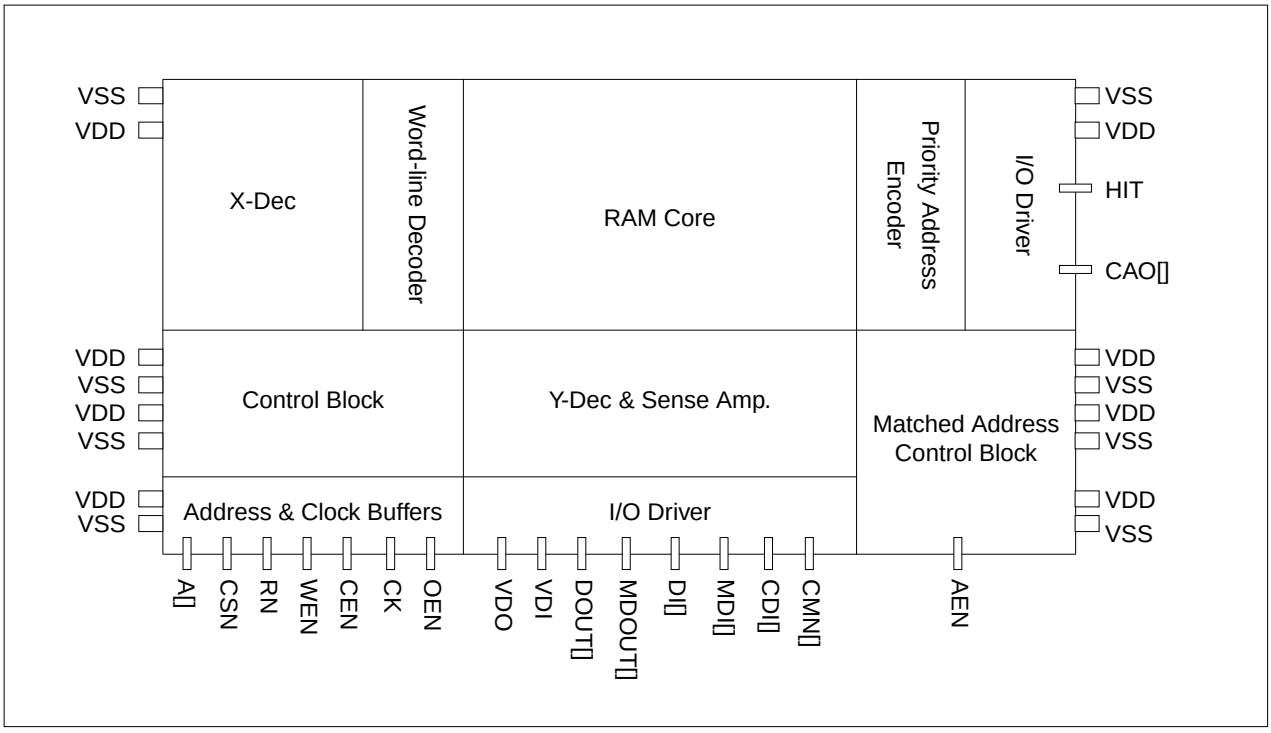
Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	CEN	AEN	CMN	A	DI
4.2388	0.8541	1.2653	0.8854	1.1502	1.1502	1.2653	1.2653	1.2655
MDI	**VDI**	**CDI**	**RN**	**DOUT**	**MDOUT**	**CDO**	**CAO**	
1.2655	1.2655	1.2653	0.8267	3.0522	3.0522	3.0522	3.0522	

Block Diagrams

TCAM_HDH supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports except HIT and CAO are located on the bottom of the memory. HIT and CAO are located on the right-edge of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in TCAM_HDH is permitted only for Metal-5 layer or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of TCAM_HDH.

4. Power reduction during standby mode. The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{mds}	Mask data-In setup time
t_{mdh}	Mask data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{ces}	CEN setup time
t_{ceh}	CEN hold time	t_{cms}	CMN setup time
t_{cmh}	CMN hold time	t_{vds}	VDI setup time
t_{vdh}	VDI hold time	t_{cds}	CDI setup time
t_{cdh}	CDI hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{macc}	Mask data access time
t_{mda}	Mask data de-access time	t_{vdacc}	Validity data access time
t_{vdda}	Validity data de-access time	t_{caacc}	Matched address access time
t_{cada}	Matched address de-access time	t_{htacc}	Global Hit/Miss access time
t_{htda}	Global Hit/Miss de-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{mdz}	MOUT drive to high-Z time
t_{mzd}	MDOUT high-Z to drive time	t_{od}	OEN to valid output time
t_{vddz}	VDO drive to high-Z time	t_{vdzd}	VDO high-Z to drive time
t_{vdod}	OEN to valid output time for VDO	t_{cadz}	CAO drive to high-Z time
t_{cazd}	CAO high-Z to drive time	t_{caod}	AEN to valid output time for CAO
t_{rn}	Min RN pulse width low	t_{rns}	RN setup time
t_{rnh}	RN hold time	t_{mod}	OEN to valid mask data output time

Definition for Power Consumption (µW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_compare	The dynamic average power consumption while in a compare cycle
Power_reset	The dynamic average power consumption while in a reset mode
Power_standby	The standby power consumption while CSN and RN are high, OEN and AEN are low and other signals are in stable except that CK is toggled
Static Leakage Current Consumption (uA)	
Static_leakage	The static leakage power consumption while CSN is high and other signals including CK are in stable.
Definition for Area (µm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**8**	**8**	**8**	**8**	**8**	**8**
Timing (ns)						
t_{cyc}	1.81	1.84	1.88	1.97	2.45	3.87
t_{ckl}	0.31	0.32	0.32	0.33	0.33	0.33
t_{ckh}	0.53	0.53	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.31	0.32	0.32	0.33	0.33	0.33
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{mds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{mdh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.17	0.17	0.17	0.17	0.17	0.17
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.01	1.03	1.08	1.18	1.38	1.86
t_{da}	0.62	0.64	0.69	0.79	0.98	1.47
t_{dz}	0.12	0.12	0.12	0.12	0.12	0.12
t_{zd}	0.14	0.14	0.14	0.14	0.14	0.14
t_{od}	0.48	0.48	0.48	0.48	0.48	0.48
t_{macc}	1.01	1.03	1.08	1.18	1.38	1.86
t_{mda}	0.62	0.64	0.69	0.79	0.98	1.47
t_{mdz}	0.12	0.12	0.12	0.12	0.12	0.12
t_{mzd}	0.14	0.14	0.14	0.14	0.14	0.14
t_{mod}	0.48	0.48	0.48	0.48	0.48	0.48
t_{vdacc}	1.01	1.03	1.08	1.18	1.38	1.86
t_{vdda}	0.62	0.64	0.69	0.79	0.98	1.47
t_{vddz}	0.12	0.12	0.12	0.12	0.12	0.12
t_{vdzd}	0.14	0.14	0.14	0.14	0.14	0.14
t_{vdod}	0.48	0.48	0.48	0.48	0.48	0.48
t_{caacc}	1.32	1.37	1.50	1.63	2.02	2.58
t_{cada}	0.59	0.61	0.64	0.71	0.93	1.36
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.46	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.23	1.30	1.38	1.50	1.77	2.23
t_{htda}	0.59	0.61	0.64	0.71	0.93	1.36
t_{rn}	1.21	1.24	1.28	1.37	1.85	3.27
t_{rns}	0.31	0.32	0.32	0.33	0.33	0.33
t_{rnh}	1.21	1.24	1.28	1.37	1.85	3.27

Reference Table (continued)

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**8**	**8**	**8**	**8**	**8**	**8**
Power (µW/MHz)						
Power_write	7.77	9.25	12.13	17.88	29.54	53.95
Power_read	7.53	8.65	10.47	13.84	20.73	36.20
Power_compare	19.96	25.95	36.89	57.79	98.29	123.76
Power_standby	1.06	1.38	1.98	3.14	5.43	10.00
Power_reset	1.29	1.80	2.85	4.98	9.50	20.35
Static_current (µA)						
Static_current	19.761	25.561	36.963	59.476	104.076	193.096
Area (µm)						
Width	174.92	189.52	204.12	218.72	233.33	247.93
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**16**	**16**	**16**	**16**	**16**	**16**
Timing (ns)						
t_{cyc}	1.95	1.97	2.01	2.07	2.47	3.90
t_{ckl}	0.32	0.32	0.32	0.33	0.33	0.33
t_{ckh}	0.53	0.53	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.33
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.18	0.18	0.18	0.18	0.18	0.18
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.19	0.19	0.19	0.19	0.19	0.19
t_{mds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{mdh}	0.19	0.19	0.19	0.19	0.19	0.19
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.19	0.19	0.19	0.19	0.19	0.19
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.18	0.18	0.18	0.18	0.18	0.18
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.04	1.06	1.11	1.21	1.41	1.89
t_{da}	0.65	0.67	0.72	0.82	1.02	1.50
t_{dz}	0.14	0.14	0.14	0.14	0.14	0.14
t_{zd}	0.16	0.16	0.16	0.16	0.16	0.16
t_{od}	0.50	0.50	0.50	0.50	0.50	0.50
t_{macc}	1.04	1.06	1.11	1.21	1.41	1.89
t_{mda}	0.65	0.67	0.72	0.82	1.02	1.50
t_{mdz}	0.14	0.14	0.14	0.14	0.14	0.14
t_{mzd}	0.16	0.16	0.16	0.16	0.16	0.16
t_{mod}	0.50	0.50	0.50	0.50	0.50	0.50
t_{vdacc}	1.04	1.06	1.11	1.21	1.41	1.89
t_{vdda}	0.65	0.67	0.72	0.82	1.02	1.50
t_{vddz}	0.14	0.14	0.14	0.14	0.14	0.14
t_{vdzd}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdod}	0.50	0.50	0.50	0.50	0.50	0.50
t_{caacc}	1.41	1.45	1.59	1.73	2.13	2.69
t_{cada}	0.68	0.70	0.74	0.81	1.05	1.48
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.20	0.28
t_{caod}	0.46	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.32	1.39	1.47	1.60	1.89	2.41
t_{htda}	0.68	0.70	0.74	0.81	1.05	1.48
t_{rn}	1.35	1.37	1.41	1.47	1.87	3.30
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.33
t_{rnh}	1.35	1.37	1.41	1.47	1.87	3.30

Reference Table (continued)

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**16**	**16**	**16**	**16**	**16**	**16**
Power (μW/MHz)						
Power_write	11.39	13.71	18.29	27.39	45.70	83.24
Power_read	11.18	12.96	15.64	20.43	30.13	51.56
Power_compare	29.75	38.39	54.71	85.98	146.43	178.51
Power_standby	1.64	2.21	3.31	5.47	9.76	18.30
Power_reset	1.58	2.22	3.51	6.15	11.67	24.46
Static_current (μA)						
Static_current	32.670	40.430	55.780	86.150	146.230	266.010
Area (μm)						
Width	241.64	256.24	270.84	285.44	300.05	314.65
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**32**	**32**	**32**	**32**	**32**	**32**
Timing (ns)						
t_{cyc}	2.27	2.29	2.33	2.40	2.69	3.95
t_{ckl}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ckh}	0.53	0.52	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.15
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.21	0.21	0.21	0.21	0.21	0.21
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.22	0.22	0.22	0.22	0.22	0.22
t_{mds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{mdh}	0.22	0.22	0.22	0.22	0.22	0.22
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.22	0.22	0.22	0.22	0.22	0.22
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.21	0.21	0.21	0.21	0.21	0.21
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.09	1.12	1.17	1.27	1.47	1.95
t_{da}	0.70	0.73	0.78	0.88	1.08	1.56
t_{dz}	0.18	0.18	0.18	0.18	0.18	0.18
t_{zd}	0.19	0.19	0.19	0.19	0.19	0.19
t_{od}	0.53	0.53	0.53	0.53	0.53	0.53
t_{macc}	1.09	1.12	1.17	1.27	1.47	1.95
t_{mda}	0.70	0.73	0.78	0.88	1.08	1.56
t_{mdz}	0.18	0.18	0.18	0.18	0.18	0.18
t_{mzd}	0.19	0.19	0.19	0.19	0.19	0.19
t_{mod}	0.53	0.53	0.53	0.53	0.53	0.53
t_{vdacc}	1.09	1.12	1.17	1.27	1.47	1.95
t_{vdda}	0.70	0.73	0.78	0.88	1.08	1.56
t_{vddz}	0.18	0.18	0.18	0.18	0.18	0.18
t_{vdzd}	0.19	0.19	0.19	0.19	0.19	0.19
t_{vdod}	0.53	0.53	0.53	0.53	0.53	0.53
t_{caacc}	1.57	1.61	1.75	1.89	2.30	2.89
t_{cada}	0.85	0.87	0.91	0.99	1.23	1.67
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.46	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.48	1.54	1.63	1.77	2.06	2.64
t_{htda}	0.85	0.87	0.91	0.99	1.23	1.67
t_{rn}	1.67	1.69	1.73	1.80	2.09	3.35
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.34
t_{rnh}	1.67	1.69	1.73	1.81	2.09	3.35

Reference Table (continued)

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**32**	**32**	**32**	**32**	**32**	**32**
Power (µW/MHz)						
Power_write	18.84	22.82	30.69	46.35	77.79	141.42
Power_read	18.56	21.89	25.95	33.53	48.68	81.72
Power_compare	48.11	60.52	84.48	131.28	223.27	296.44
Power_standby	2.79	3.83	5.89	9.96	18.05	34.18
Power_reset	2.14	3.02	4.79	8.39	15.79	32.48
Static_current (µA)						
Static_current	58.380	69.910	92.920	138.550	228.610	408.000
Area (µm)						
Width	375.08	389.68	404.28	418.88	433.49	448.09
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

Reference Table

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**64**	**64**	**64**	**64**	**64**	**64**
Timing (ns)						
t_{cyc}	2.88	2.91	2.95	3.03	3.32	4.07
t_{ckl}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ckh}	0.52	0.52	0.52	0.52	0.52	0.52
t_{as}	0.16	0.16	0.16	0.16	0.16	0.16
t_{ah}	0.11	0.12	0.13	0.14	0.14	0.14
t_{cs}	0.32	0.32	0.32	0.33	0.33	0.34
t_{ch}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ces}	0.19	0.19	0.19	0.20	0.20	0.20
t_{ceh}	0.25	0.25	0.25	0.25	0.25	0.25
t_{cms}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cmh}	0.28	0.28	0.28	0.28	0.28	0.28
t_{ds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{dh}	0.30	0.30	0.30	0.30	0.30	0.30
t_{mds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{mdh}	0.30	0.30	0.30	0.30	0.30	0.30
t_{vds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{vdh}	0.30	0.30	0.30	0.30	0.30	0.30
t_{cds}	0.16	0.16	0.16	0.16	0.16	0.16
t_{cdh}	0.28	0.28	0.28	0.28	0.28	0.28
t_{ws}	0.16	0.16	0.16	0.16	0.16	0.16
t_{wh}	0.11	0.12	0.13	0.14	0.14	0.15
t_{acc}	1.20	1.23	1.29	1.39	1.60	2.08
t_{da}	0.81	0.84	0.90	1.00	1.20	1.69
t_{dz}	0.25	0.25	0.25	0.25	0.25	0.25
t_{zd}	0.25	0.25	0.25	0.25	0.25	0.25
t_{od}	0.59	0.59	0.59	0.59	0.59	0.59
t_{macc}	1.20	1.23	1.29	1.39	1.60	2.08
t_{mda}	0.81	0.84	0.90	1.00	120	1.69
t_{mdz}	0.25	0.25	0.25	0.25	0.25	0.25
t_{mzd}	0.25	0.25	0.25	0.25	0.25	0.25
t_{mod}	0.59	0.59	0.59	0.59	0.59	0.59
t_{vdacc}	1.20	1.23	1.29	1.39	1.60	2.08
t_{vdda}	0.81	0.84	0.90	1.00	1.20	1.69
t_{vddz}	0.25	0.25	0.25	0.25	0.25	0.25
t_{vdzd}	0.25	0.25	0.25	0.25	0.25	0.25
t_{vdod}	0.59	0.59	0.59	0.59	0.59	0.59
t_{caacc}	1.87	1.91	2.05	2.20	2.61	3.25
t_{cada}	1.19	1.20	1.24	1.33	1.57	2.00
t_{cadz}	0.11	0.11	0.12	0.14	0.18	0.27
t_{cazd}	0.13	0.13	0.14	0.16	0.19	0.28
t_{caod}	0.47	0.47	0.48	0.50	0.53	0.62
t_{htacc}	1.78	1.85	1.94	2.07	2.37	3.00
t_{htda}	1.19	1.20	1.24	1.33	1.57	2.00
t_{rn}	2.28	2.31	2.35	2.43	2.72	3.47
t_{rns}	0.32	0.32	0.32	0.33	0.33	0.34
t_{rnh}	2.28	2.31	2.35	2.43	2.72	3.47

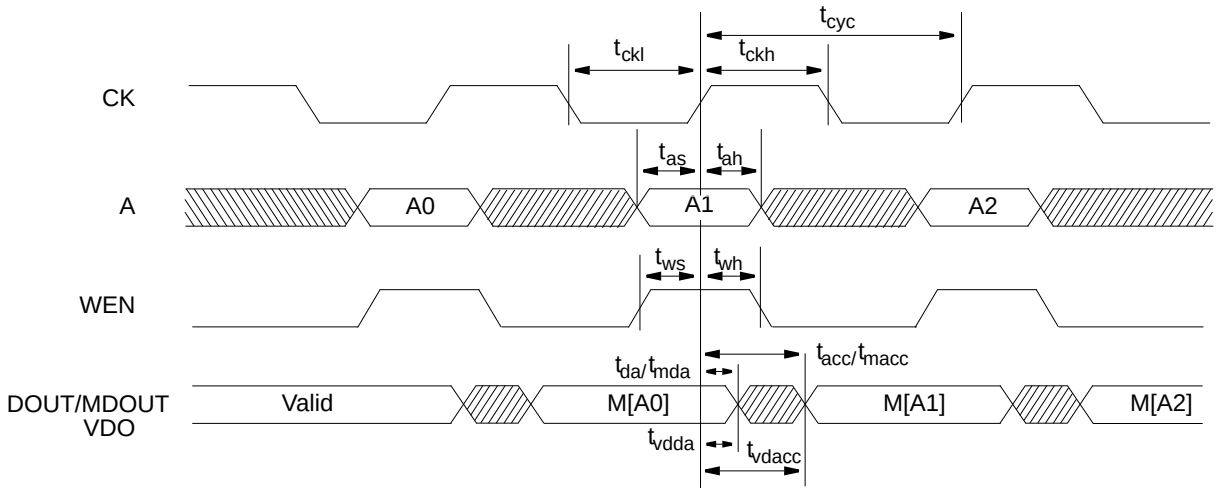
Reference Table (continued)

*** For Ymux=1** (Typical process, 1.2V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**64**	**64**	**64**	**64**	**64**	**64**
Power (μW/MHz)						
Power_read	35.24	42.16	56.39	85.06	142.71	258.46
Power_write	35.03	38.96	46.50	59.73	85.88	142.06
Power_compare	87.90	105.88	142.39	216.64	365.34	543.63
Power_standby	5.07	7.05	11.02	18.88	34.52	65.73
Power_reset	3.27	4.61	7.34	12.83	24.01	48.23
Static_current (μA)						
Static_current	109.730	128.800	167.010	242.940	392.640	690.530
Area (μm)						
Width	641.96	656.56	671.16	685.76	700.37	714.97
Height	232.80	285.60	391.20	602.40	1024.80	1869.60

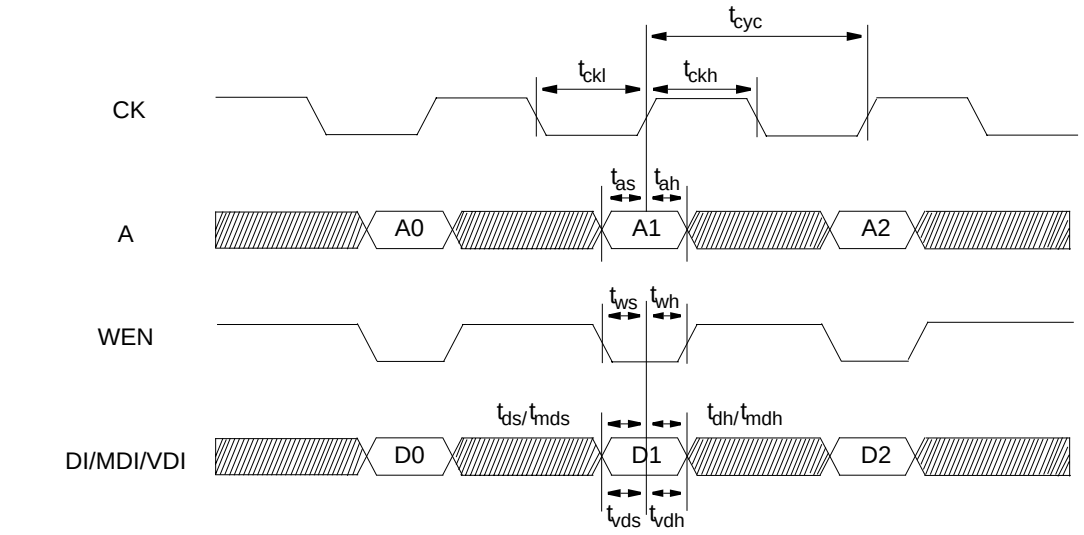
Timing Diagrams

Read Cycle



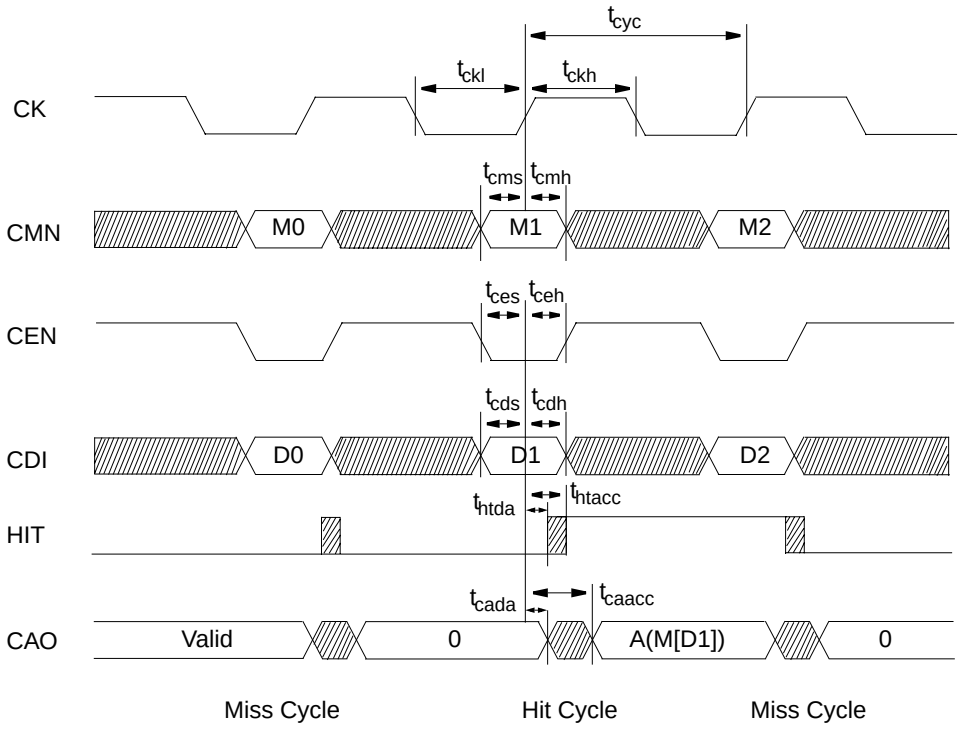
(RN=high, CSN=low, OEN=low, CEN=high, AEN, DI, MDI, VDI, CDI, CMN = don't care)

Write Cycle



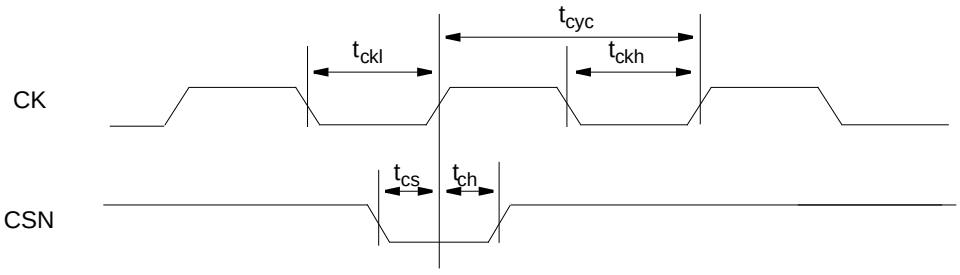
(RN = high, CSN = low, CEN = high, OEN, AEN, CDI, CMN = don't care)

Compare Cycle



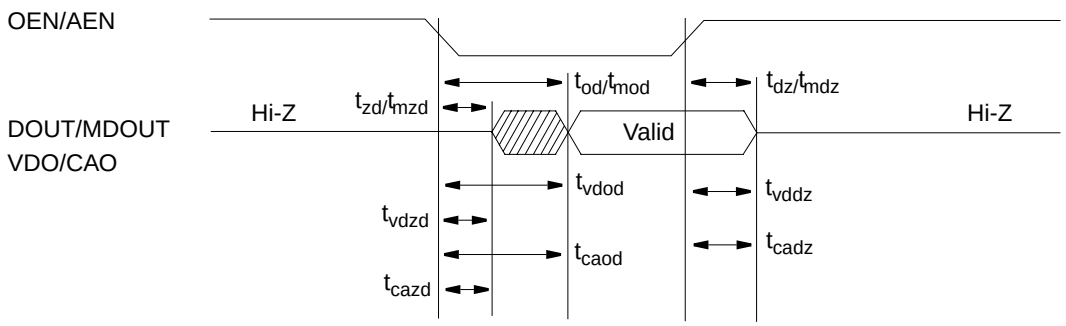
(RN = high, CSN = low, A, WEN, OEN, AEN, DI, MDI = don't care)

CSN Controlled



(RN, WEN, OEN CEN, AEN, A, DI, MDI, VDI, CDI, CMN = valid)

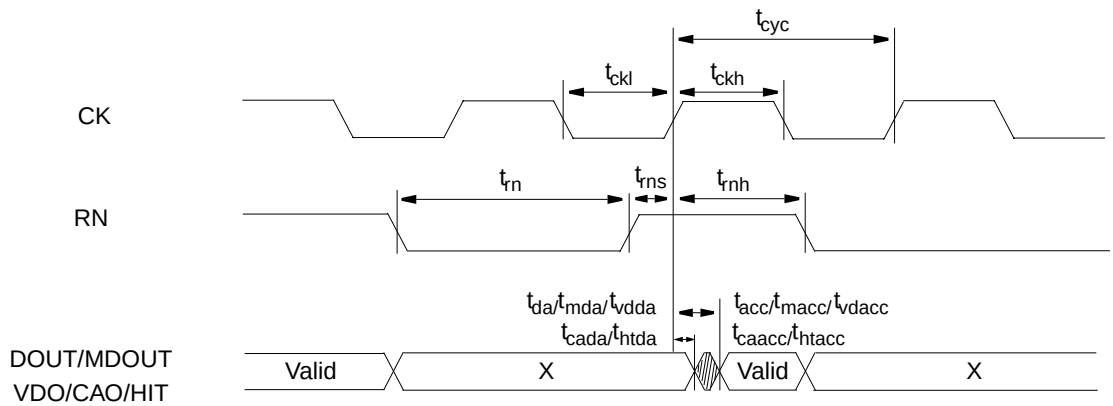
OEN/AEN Controlled Output Enable



(RN, CK, CSN, WEN, CEN, AEN, CMN, A, DI, MDI, VDI, CDI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

RN Controlled Reset Mode



(OEN, CSN, WEN, CEN, AEN, CMN, A, DI, MDI, VDI, CDI = valid)

PLL

6

Contents

PLL2113X 6-1

GENERAL DESCRIPTION

The pll2113x is a Phase Locked Loop (PLL) frequency synthesizer. The PLL provides frequency multiplication capabilities. Its output clock frequency FOUT is related to the input clock frequency FIN by the following equation:

$$FOUT = (m \times FIN) / (p \times 2^S)$$

where FOUT is the output clock frequency. FIN is the input clock frequency. m, p and s are the values for programmable dividers. pll2113x consists of a Phase Frequency Detector(PFD), a Charge Pump, an Off-chip Loop Filter, a Voltage Controlled Oscillator (VCO), a 6-bit Pre-divider, an 8-bit Main-divider and 2-bit Post-scaler as will be shown in functional block diagram.

FEATURES

- 0.13um CMOS device technology
- 1.2V single power supply
- Output frequency range: 50M ~ 300MHz
- Jitter: ±150ps at 300MHz
- Duty ratio: 40% to 60% (All tuned range)
- Power down mode
- Off-chip loop filter
- Frequency is changed by programmable divider

NOTES:

1. Don't set the P or M value as zero, that is, setting the P=000000, M=00000000 can cause malfunction of the PLL.
2. The proper range of P and M: $1 \le P \le 62$, $1 \le M \le 248$ (refer to page6 function description)
3. The P and M must be selected considering stability of PLL and VCO output frequency range.
4. **Please contact SEC application engineer for proper selection of the P, M, S values of the PLL.**

Ver_1.0.3 (May. 2003)
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FUNCTIONAL BLOCK DIAGRAM

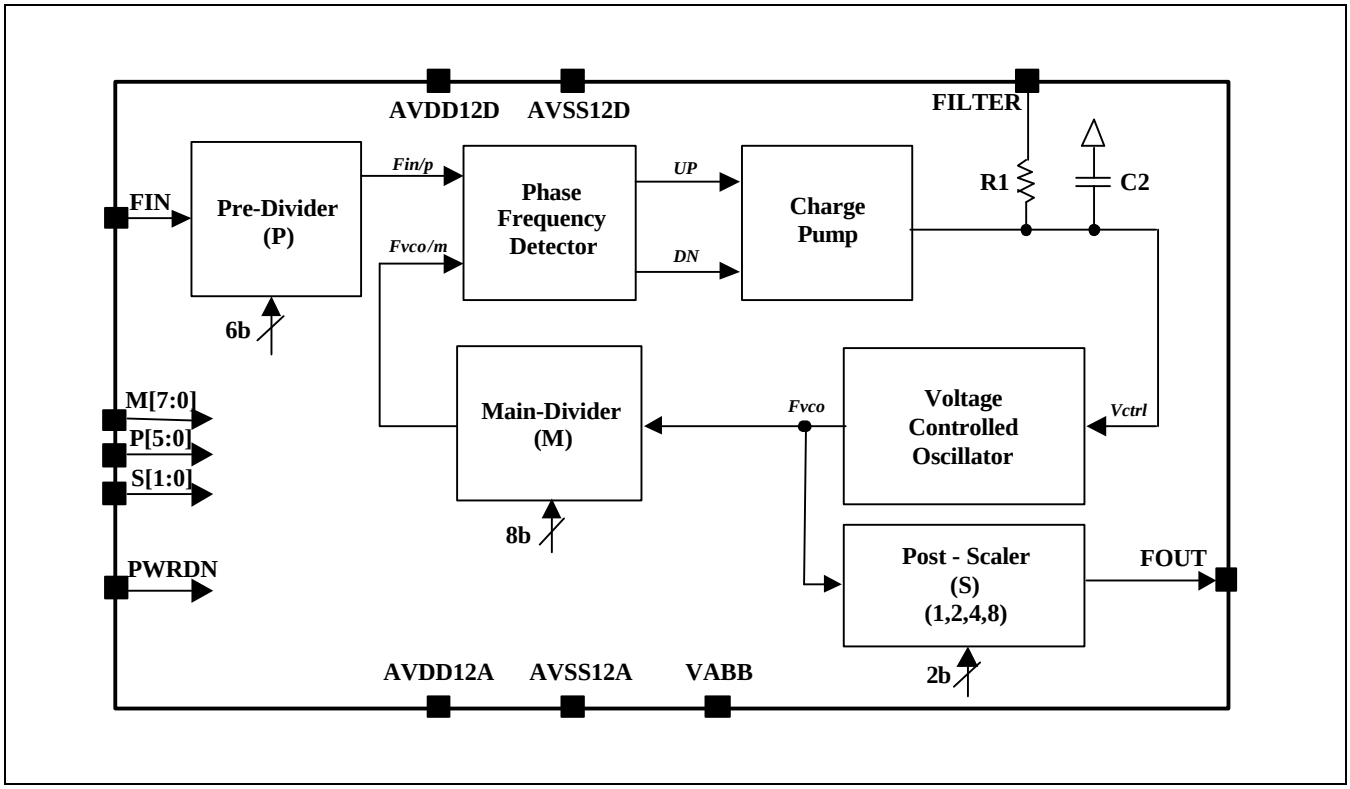


Figure 1. Block Diagram

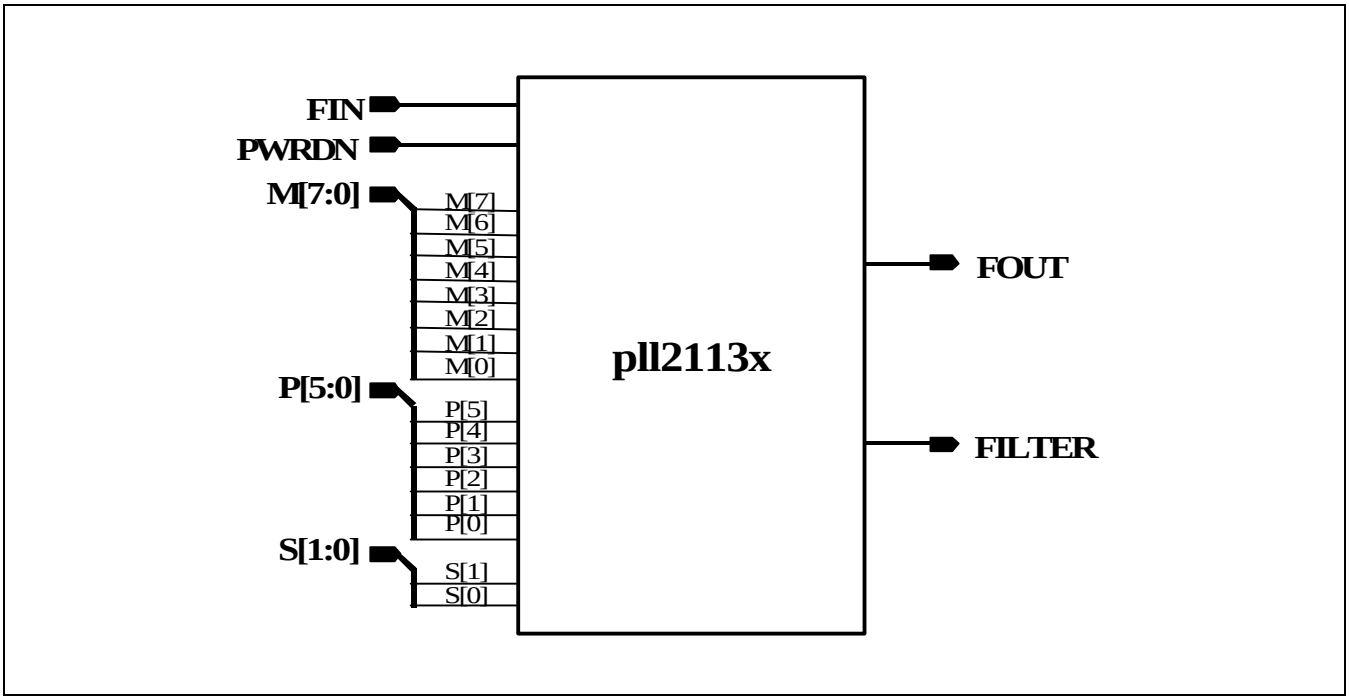
CORE PIN DESCRIPTION

Name	I/O Type	Pin Description
AVDD12D	DP	Digital power supply
AVSS12D	DG	Digital ground
AVDD12A	AP	Analog power supply
AVSS12A	AG	Analog ground
VABB	AB/DB	Analog / Digital bulk bias
FIN	DI	PLL clock input
FOUT	DO	50MHz ~ 300MHz clock output
FILTER	AO	The external loop filter capacitor should be connected between FILTER and analog ground
PWRDN	DI	Power down. - If PWRDN is high, power down mode is enabled.
P[5:0]	DI	6-bit programmable pre-divider.
M[7:0]	DI	8-bit programmable main-divider.
S[1:0]	DI	2-bit programmable post-scaler.

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AP: Analog Power
— AG: Analog Ground
— AB: Analog Sub Bias
— DP: Digital Power
— DG: Digital Ground
— DB: Digital Sub Bias
— BD: Bi-directional Port

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATING

Characteristics	Symbol	Value	Unit	Applicable Pin
Supply voltage	AVDD12D AVDD12A	1.8	V	AVDD12D, AVDD12A
Storage temperature	Tstg	–65 ~ 150	°C	–

NOTES:

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage differential	AVDD12D-AVDD12A	–0.1		+0.1	V	
External loop filter capacitor	LF		2.2		nF	capacitor tolerance (±5%)
Operating temperature	Topr	–40		85	°C	

NOTE: It is strongly recommended that all the supply pins (AVDD12D, AVDD12A) be powered to the same supply voltage to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	AVDD12D/AVDD12A	1.14	1.20	1.26	V
Digital input voltage high	V_{IH}	0.7VDD	–	–	V
Digital input voltage low	V_{IL}	–	–	0.3VDD	V
Dynamic current	I_{DD}	–	3	TBD	mA
Power down current	I_{PD}	–	–	TBD	uA

NOTE: Operating voltage Min/Max are preliminary values and expected to be updated.

AC ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Min	Typ	Max	Unit
Input frequency		Fin	10	–	40	MHz
VCO output frequency		Fvco	100	–	300	MHz
Output frequency		Fout	50	–	300	MHz
Input clock duty ratio		T_{ID}	40	50	60	%
Output clock duty ratio		T_{OD}	40	50	60	%
Locking time		T_{LT}	–	300	–	us
Cycle to cycle jitter	50M ~ 100MHz	T_{JCC}	–	±600	TBD	ps
	100M ~ 200MHz	T_{JCC}	–	±300	TBD	ps
	200M ~ 300MHz	T_{JCC}	–	±150	TBD	ps

FUNCTIONAL DESCRIPTION

PLL is a circuit which synchronizes output signal (generated by an VCO) and reference signal (or input signal) in frequency as well as in phase. The pll2113x can provide frequency multiplication capabilities, but does not support functions such as deskew and phase synchronization between Fin and Fout.

PLL2113X consists of the following basic blocks.

— The phase frequency detector (PFD) detects the phase difference between the reference clock and feedback clock, then generates UP/DOWN error signals. If reference clock leads or lags feedback clock, the charge pump charges or discharges the following loop filter according to UP/DOWN signal.

— The loop filter suppresses high frequency components and allows dc value (Vctrl) to Voltage-Controlled Oscillator (VCO).

— The VCO generates clock signals proportional to the control voltage (Vctrl).
Required frequency is produced by appropriate selection of P, M and S dividers.

Fout = Fin × m/(p × s)

m = M+8 , p = P+2 , s = 1, 2, 4, 8

— Don't set the value P or M to all zero. That is, 000000 (in case of P) or 00000000 (in case of M) are not allowed.

— The range of P and M: $1 \le P \le 62$, $1 \le M \le 248$

— The M and P must be selected considering stability and VCO range.
VCO output frequency range of pll2113x is from 100MHz to 300MHz.

Digital Data Format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTE: M[7] - M[0]: main-divider $1 \le M \le 248$
P[5] - P[0]: pre-divider $1 \le P \le 62$
S[1] - S[0]: post-scaler $0 \le S \le 3$

Important Notice: Please contact SEC application engineer for proper selection of M, P, S values.

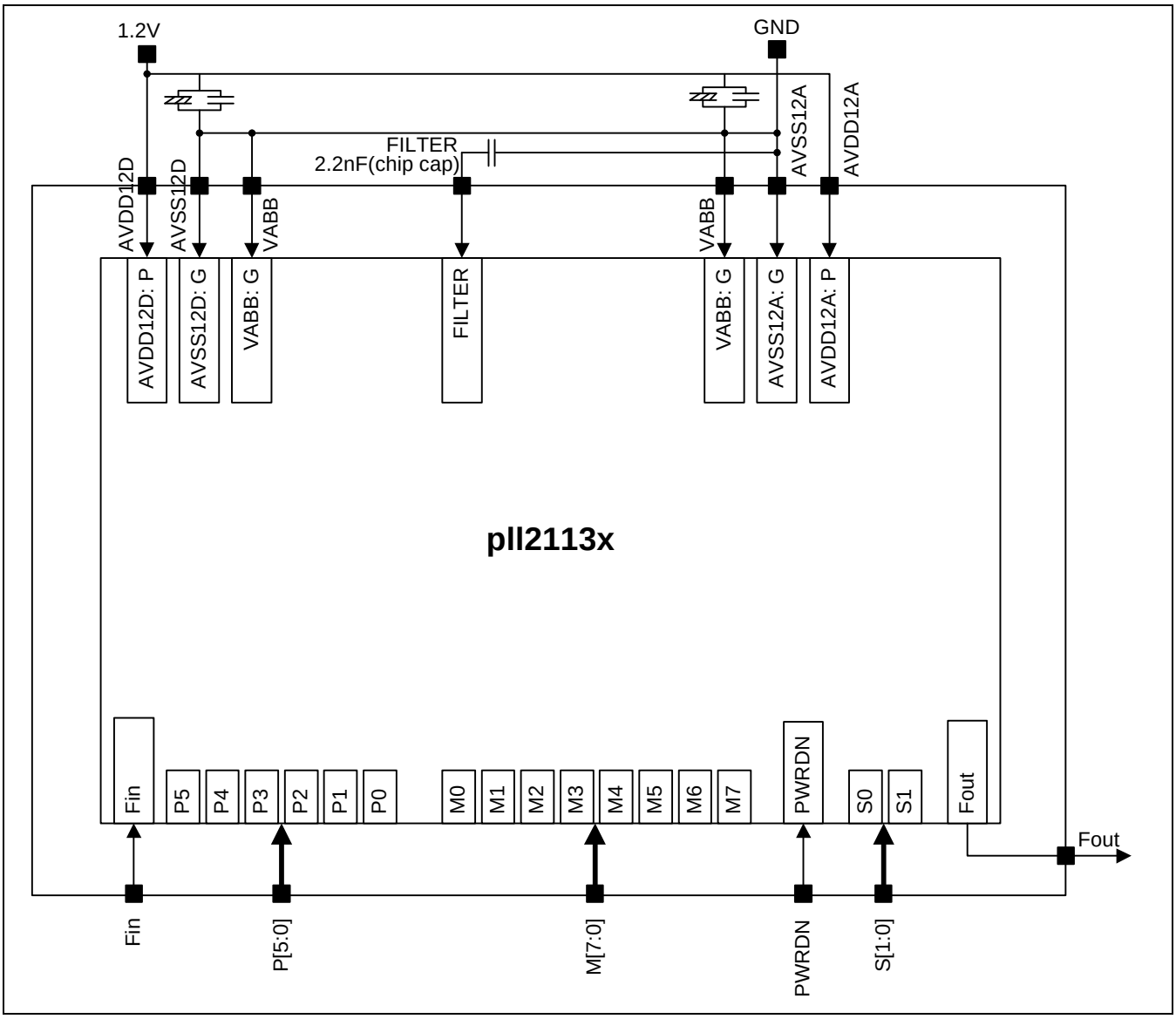
CORE EVALUATION GUIDE

You can generate various output frequencies by changing M/P/S setting. There are two methods of controlling divider values.

— Method 1: 16-bit register can be used for easy control of divider values.

— Method 2: P, M and S pins are bypassed to the external port, and you can control each port directly.

It is undesirable to connect P[5:0], M[7:0] and S[1:0] to the internal power or ground directly because of ESD issue.



NOTE: ZZZ : 10uF electrolytic capacitor
Unless otherwise specified

: 0.1uF ceramic capacitor
Unless otherwise specified

CORE LAYOUT GUIDE

1. The Digital power(AVDD12D, AVSS12D) and the analog power(AVDD12A, AVSS12A) must be dedicated to PLL only and separated. Please consult PLL dedicated I/O assign with SEC application engineer.
2. The FOUT and FILTER pins and routings must be placed far from the internal signals in order to avoid cross-talk.
3. Those blocks consume a large amount of digital switching current must be located away from the PLL core.

LAYOUT DESIGN CONSIDERATIONS

The following design considerations must be applied.

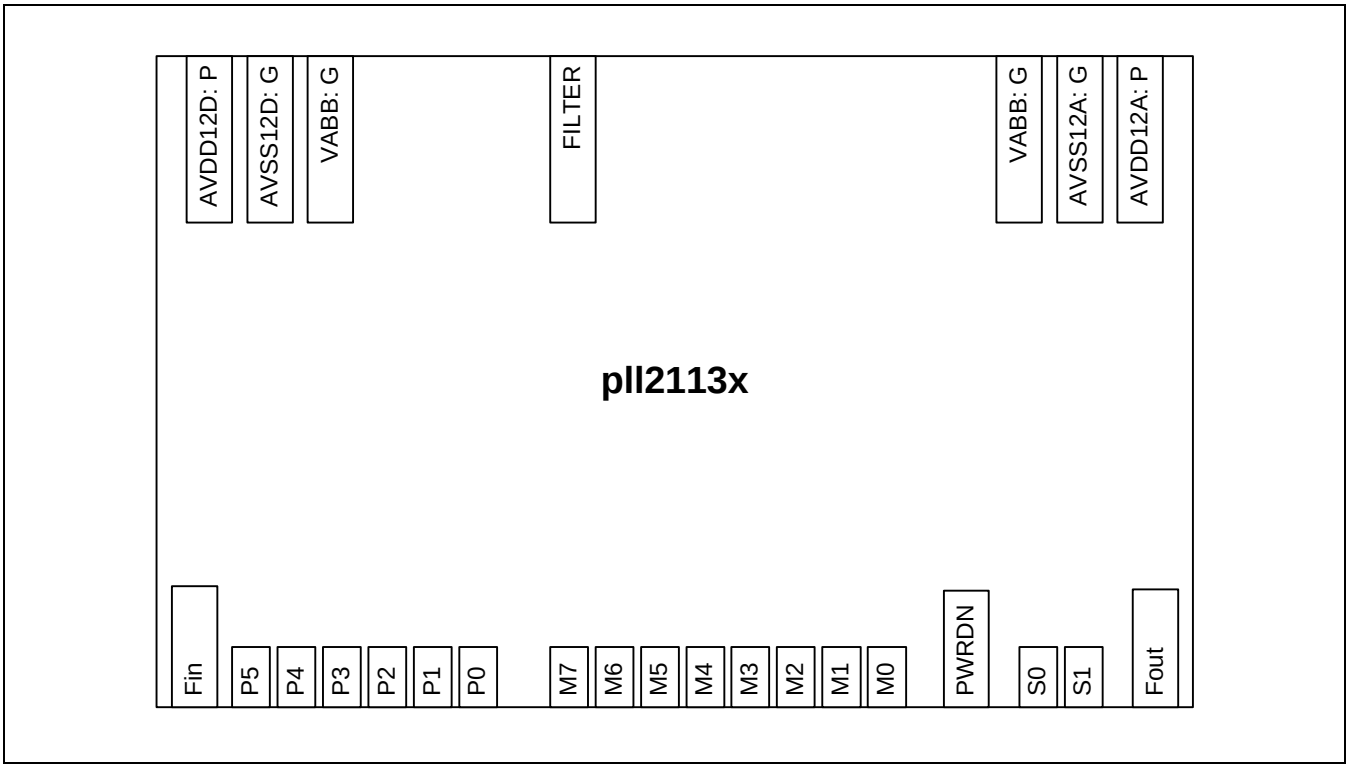
1. Jitter is affected by the power noise, substrate noise, etc. It depends on embedded environment noise level.
2. A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
3. The use of two, or more PLLs requires special layout considerations. Please consult it with SEC application engineer for more information.
4. The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pads & pins.
5. It is not recommended to locate high frequency noise-generating signals and cores near the PLL and its I/O cells. For example, data buses, high frequency outputs and high current consuming cells.

PHANTOM CELL INFORMATION

Pins of the core can be assigned externally(package pins) or internally(internal ports) depending on design methods.

— The term "external" implies that the pins should be assigned externally like power pins.

— The term "internal/external" implies that those pins are user dependent.



PIN LAYOUT GUIDE

Pin Name	Pin Usage	Pin Layout Guide
AVDD12D	External	– Use dedicated power/ground pins for PLL – Power cuts are required to provide on-chip isolation → between dedicated PLL power/ground and all other power/ground – Use good power and ground source on board
AVSS12D	External	
AVDD12A	External	
AVSS12A	External	
VABB	External	
FIN	External	– Do not place noisy, high frequency and high power consuming circuitry pads near the FIN pin. – Use proper low jitter reference clock
FOUT	External/Internal	– Do not place noisy, high frequency and high power consuming circuitry pads near the FOUT pin. – Internal routing path should be as short as possible. This will minimize loading effect. – FOUT signals should not be crossed by any signals and should not run next to digital signals. This will minimize capacitive coupling between the two signals.
FILTER	External	– Do not place the noisy, high frequency and high power consuming circuitry pads near the FILTER. – Ground shielding is needed for internal routing path. – FILTER routing path should not be crossed by any other signals and should not be placed next to digital signals. – External loop filter pin should be placed between analog power and ground to avoid stray coupling outside the chip and magnetic coupling via bond wires. – External loop filter components and internal routing should be as short as possible.
PWRDN	Internal /External	
M[7] ~ M[0]	Internal/External	
P[5] ~ P[0]	Internal/External	
S[1] ~ S[0]	Internal/External	

FEEDBACK REQUEST

Thank you for having an interest in our products. Please fill out this form, especially the items which you want to request.

Parameter		Customer	SEC	Unit
Process			0.13um CMOS	
Supply voltage (VDD)			1.2 ± 0.06	V
Input frequency (FIN)			10 ~ 40	MHz
Output frequency (FOUT)			50 ~ 300	MHz
Cycle to cycle jitter (TJCC)	50M ~ 100M		TBD	psec (pk-pk)
	100M ~ 200M		TBD	
	200M ~ 300M		TBD	
Period jitter (TJP)	50M ~ 100M		TBD	psec (pk-pk)
	100M ~ 200M		TBD	
	200M ~ 300M		TBD	
Output duty ratio (TOD)			40 ~ 60	%
Lock up time (TLT)			TBD	usec
Dynamic current			< 3m	A
Stand by current			TBD	A
Filter capacitor			External	–

— How many PLLs are embedded in your system ?

— Do you need synchronization between input clock and output clock ?

— Do you need another spec of jitter ?

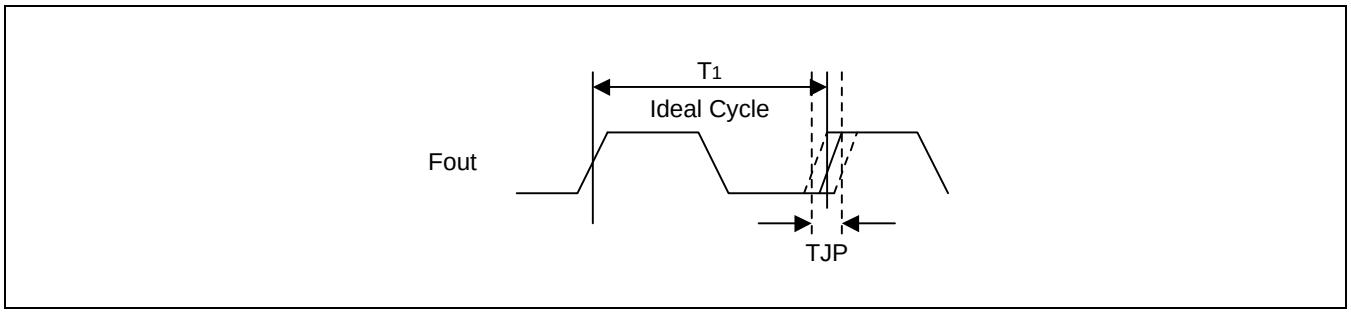
Parameter	Customer	Unit
Long-term jitter (TJLT)		psec (pk-pk)
Tracking Jitter (TJT)		psec (pk-pk)

If you have another special request, please describe below.

JITTER DEFINITION

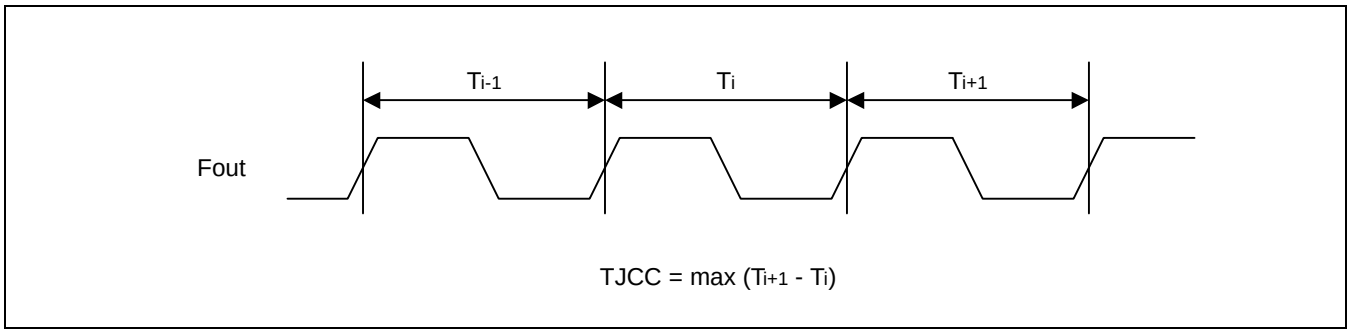
Period Jitter

Period jitter is the maximum deviation of output clock's transition from its ideal position.



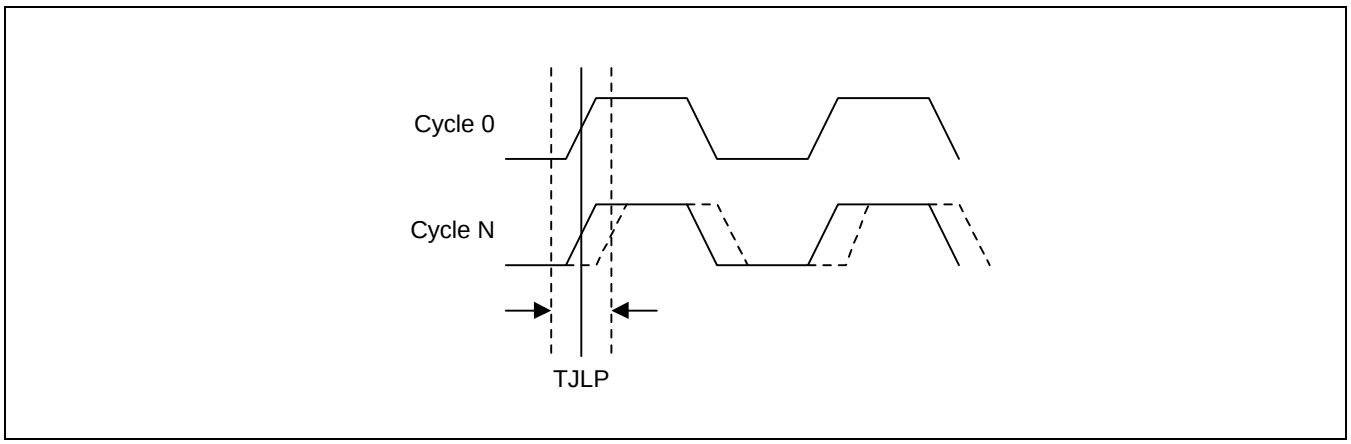
Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the maximum deviation of output clock's transition from its corresponding position of the previous cycle.



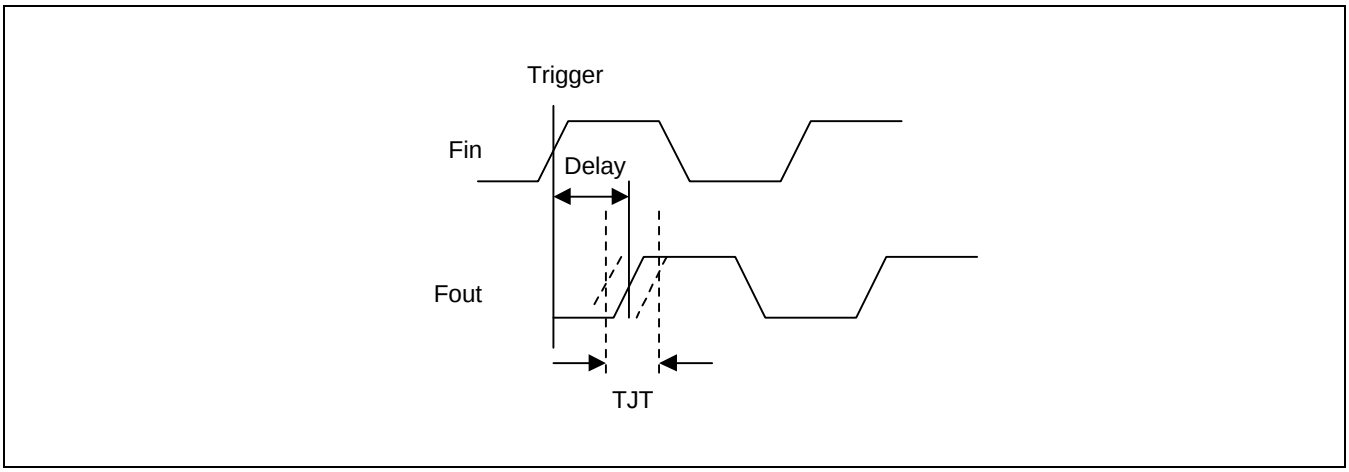
Long-Term Jitter

Long-term jitter is the maximum deviation of output clock' transition from its ideal position, after many cycles. The term "many" depends on the application and the frequency.



Tracking Jitter

Tracking jitter is the maximum deviation of output clock(FOUT)'s transition from input clock (FIN) position.



Appendix A

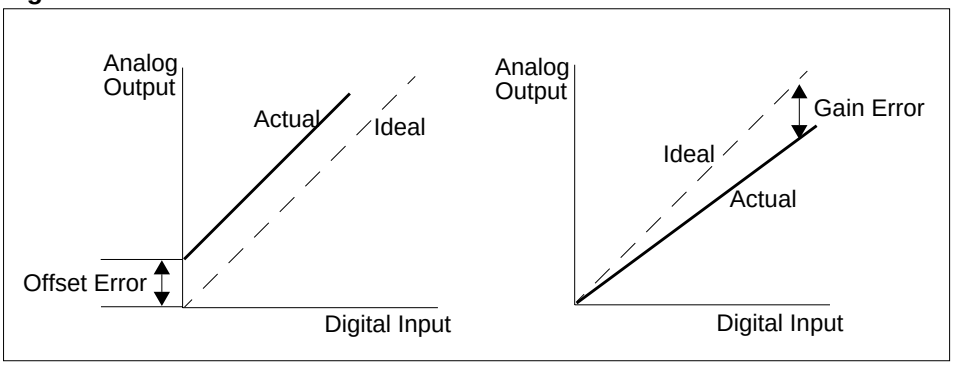
Glossary of Analog Terms

Digital-to-Analog Converter

1. Resolution - An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have resolution of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span.

2. Accuracy - Error of a DAC is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Source of error include gain error, offset error, linearity error and noise. Error is usually commensurate with resolution, less than $2^{-(n+1)}$, or 1/2LSB of full scale.

Figure 1-1. Error of DAC



3. LSB (Least-Significant Bit) - In a system in which a numerical magnitude is represented by a series of binary digits, the LSB is that bit that carries the smallest value or weight. It represents the smallest analog change that can be resolved by an n-bit converter.

$$\text{LSB (Analog Value)} = \text{FSR}/2^n$$

FSR = Full-Scale Range, n = number of bits

4. MSB (Most-Significant Bit) - The binary digit with the largest numerical weighting. Normally, the MSB of a digital word has a weighting of 1/2 the full range.

5. Compliance-Voltage Range - For a current output DAC, the maximum range of(output) terminal voltage for which the device will provide the specified current-output characteristics.

6. Glitch - A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V × ns) or current (mA × ns) and time duration or charge transferred.

7. Harmonic Distortion (and Total Harmonic Distortion) - The DAC is driven by the digitized representation of sine wave. The ratio of the RMS sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second through fifth.

$$\text{THD} = 20\log\frac{(V2^2+V3^2+V4^2+V5^2)^{1/2}}{V1}$$

V1: RMS amplitude of the fundamental

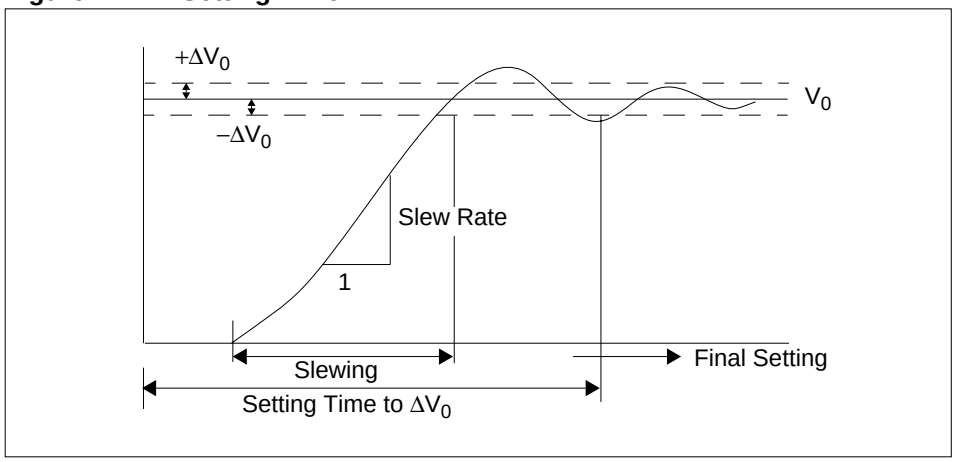
8. Signal-to-Noise Ratio (SNR) - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follows the theoretical formula;

$$S/N_{max} = 6.02N + 1.76dB$$

9. Slew Rate - Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge of capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75V/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output (if one is used).

10. Settling Time - The time required, following a prescribed data change from the 50% point of the login input change, for the output of a DAC to reach and to remain within a given fraction (usually ±1/2LSB) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DAC is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Figure 1-2. Setting Time



11. Power-Supply Sensitivity -The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% DC change in the power supply. Power supply sensitivity may be also expressed in relation to the specified DC shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed 1/2LSBfor 3% change in power supply. Even better specifications are necessary for converters designed for battery operation.

12. INL (Integral Non Linearity) - Linearity error of a converter, expressed in %, ppm of full-scale range or multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviation of the actual transfer characteristics from this straight line; or it can be a straight line passing through the endpoints of the transfer characteristic after they have been calibrated (sometimes referred to as "endpoint" linearity). Endpoint linearity error is similar to relative accuracy error. For multiplying DAC, the analog linearity error,

at a specified digital code, is defined in the same way as for multipliers, by deviation from a "best straight line" through the plot of the analog output-input response.

13. DNL (Differential Non Linearity) - Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2^n of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called differential linearity error expressed in multiplies of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to non-monotonic response in a DAC and missed codes in an ADC.

14. Monotonic - A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a differential nonlinearity specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behaviour.

2. Analog-to-Digital Converter

1. INL (Integral Non Linearity) - Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs for an analog value 1/2LSB before the first code transition. "Full scale" is defined as a level 1/2LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

2. DNL (Differential Non Linearity) - An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes are guaranteed.

3. Offset Error - The first transition should occur at a level "zero". Offset is defined as the deviation of the actual first code transition from that point.

4. Gain Error - The first code transition should occur for an analog value of nominal negative full scale. The last transition should occur for an analog value 1LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

5. Pipeline Delay (Latency) - The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

6. Effective Number of Bits (ENOB) - This is a measure of a device's dynamic performance and may be obtained from the SNDR or from a sine wave curve test fit according to the following expression:

ENOB = SNDR - 1.76/6.02

ENOB = N-log2[RMS error (actual) / RMS error (ideal)]

7. Analog Bandwidth - The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

8. Aperture Delay - The delay between the sampling clock and the instant the analog input signal is sampled.

9. Aperture Jitter - The sample to sample variation in aperture delay.

10. Bit Error Rate (BER) - The number of spurious code errors produced for any given input sine wave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sine wave.

11. Signal to Noise Ratio - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follow the theoretical formula;

$$S/N_{max} = 6.02N + 1.76dB$$

3. Phase Locked Loop

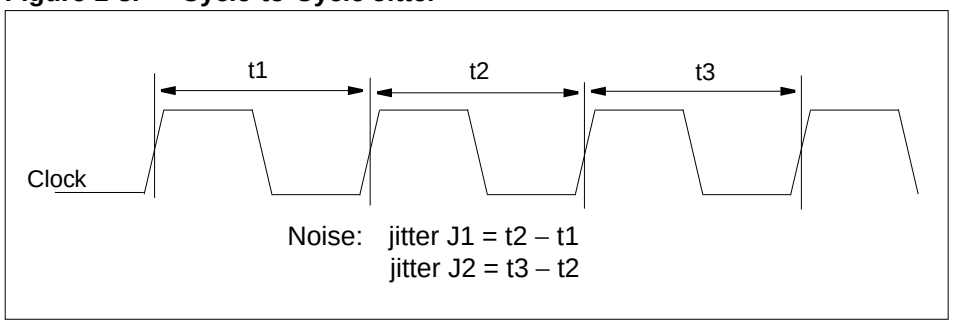
1. Lock Time - The time it takes the PLL to lock onto the system clock. Fast or slow lock time may be controlled by the loop filter characteristics. The loop filter characteristics are controlled by varying the R and C components. (Remember that R and C define the damping-factor as well)

2. Phase Error - The phase difference between the feedback and the system clock signal.

3. Clock Jitter - The deviations in a clock's output transitions from their ideal positions define the clock jitter. Jitter is sometimes specified as an absolute value in nanoseconds. All jitter measurement are made at a specified voltage.

1) Cycle-to-Cycle Jitter: The change in a clock's output transition from its corresponding position in the previous cycle. This kind of jitter is the most difficult to measure and usually requires a time-interval analyzer.

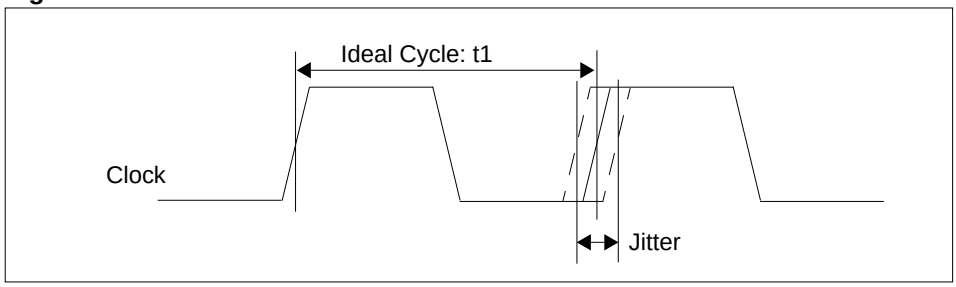
Figure 1-3. Cycle-to-Cycle Jitter



The maximum of such values over multiple cycles (J1, J2...) is the max. cycle-to-cycle jitter.

2) Period Jitter: Period jitter measures the maximum change in a clock's output transition from its ideal position. You can use period jitter measurements to calculate timing margins in systems.

Figure 1-4. Period Jitter



3) Long-Term Jitter: Long-term jitter measures the maximum change in a clock's output transition from its ideal position over many cycles. How many cycles depend on the application and the frequency. A classic example of system affected by long-term jitter is a graphics card driving a CRT.

4) Power Down Mode: PLL state in which the quiescent current is lowered to a very low level to conserve power.

5) Synthesize Clock: A system clock may run at a relatively low rate compared to system components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. Designers can use PLL technology to synthesize a higher frequency on-chip clock using the system clock as a reference.

6) Deskew Clock: Multiple chips on a printed circuit board or cores of different sizes within a single system on a chip experience clock skew. By using PLL or DLL technology to shift the phase of the reference clock within each chip or core, designers can minimize skew tune a system to perform up its potential.

7) Duty Ratio: The percentage of the period that the output is in a high state.

8) Output Frequency Range: The maximum output frequency range minus the minimum output frequency that is produced with an input signal for which the cell specifications still apply.

Appendix B

Timings

Equivalent Standard Loads for 4-layer and 5-layer Metal Interconnect

Gate Count	Fanouts													
	1	2	3	4	5	6	7	8	16	32	64	130	131	132
4LM														
5000	0.569	0.996	1.646	2.364	2.748	3.364	3.766	5.041	7.224	12.585	24.466	27.283	48.047	52.874
10000	0.594	1.443	1.817	2.720	3.079	4.278	4.933	5.957	8.581	14.628	29.120	31.937	54.478	58.819
50000	0.661	1.801	2.528	4.228	5.175	6.356	7.533	7.974	10.281	15.988	31.185	35.624	57.228	60.929
100000	0.982	2.004	3.126	4.518	5.404	6.579	8.691	9.118	11.872	17.179	34.996	43.248	70.549	74.464
150000	3.803	5.152	5.740	7.283	7.874	8.941	9.579	10.276	13.037	19.028	36.644	43.970	77.254	77.852
200000	5.313	6.031	6.783	7.819	8.587	9.561	10.232	10.817	13.707	20.150	38.169	45.913	81.195	81.827
300000	5.846	6.405	7.461	8.705	9.535	10.602	11.331	11.968	15.146	22.238	40.201	47.244	89.551	90.246
400000	6.382	7.348	8.083	9.394	10.313	11.480	12.285	12.951	16.374	23.994	42.291	47.925	96.621	97.354
500000	7.116	8.598	9.081	10.535	11.555	12.852	13.746	14.526	17.427	25.545	45.378	51.010	102.829	103.634
600000	7.620	9.073	9.778	11.327	12.409	13.799	14.750	15.616	17.929	26.283	48.248	52.472	105.777	106.622
800000	8.778	11.100	11.360	13.134	14.374	15.967	17.059	18.106	19.374	28.411	53.894	56.709	114.309	115.246
1000000	9.860	11.602	12.841	14.823	16.205	17.992	19.215	20.435	20.718	30.394	56.413	60.638	122.236	123.260
1500000	12.833	15.508	16.870	19.425	21.213	23.528	25.108	26.785	29.642	36.346	68.258	72.482	146.100	147.376
2000000	15.610	19.274	20.650	23.744	25.902	28.715	30.626	32.736	38.303	41.915	76.518	83.559	168.425	169.933
2500000	18.213	23.191	24.183	27.781	30.293	33.567	35.795	38.305	41.838	47.116	88.273	93.905	189.277	191.004
3000000	20.650	25.447	27.490	31.559	34.394	38.104	40.624	43.514	45.138	51.970	99.332	103.559	208.730	210.659
4000000	23.689	28.614	31.539	36.207	39.457	43.714	46.606	49.919	53.762	59.626	113.175	118.809	239.464	241.681
5000000	26.563	34.346	35.364	40.596	44.246	49.018	52.262	55.974	55.268	66.858	119.138	133.220	268.511	270.996
6000000	29.787	37.789	39.651	45.522	49.614	54.962	58.602	62.766	65.667	74.966	140.927	149.380	301.082	303.868
7000000	32.419	45.929	49.329	54.305	57.604	61.360	65.423	72.876	76.525	93.260	185.830	188.960	374.548	378.017
8000000	36.354	51.498	55.311	60.892	64.590	68.805	73.360	81.716	85.472	104.569	189.592	208.370	419.981	423.867
5LM														
5000	0.518	0.906	1.496	2.150	2.498	3.059	3.423	4.583	6.567	11.441	22.242	24.803	43.679	48.067
10000	0.541	1.311	1.652	2.472	2.799	3.888	4.484	5.415	7.801	13.297	26.472	29.033	49.525	53.472
50000	0.600	1.638	2.297	3.844	4.705	5.778	6.848	7.250	9.346	14.535	28.350	32.386	52.025	55.390
100000	0.894	1.821	2.843	4.106	4.911	5.980	7.902	8.289	10.793	15.618	31.815	39.317	64.136	67.695
150000	3.457	4.683	5.218	6.622	7.157	8.128	8.709	9.341	11.852	17.297	33.313	39.972	70.230	70.775
200000	4.831	5.482	6.167	7.108	7.805	8.691	9.301	9.833	12.461	18.317	34.699	41.740	73.813	74.388
300000	5.315	5.823	6.781	7.913	8.669	9.638	10.301	10.880	13.770	20.216	36.545	42.949	81.409	82.041
400000	5.801	6.681	7.348	8.539	9.376	10.437	11.169	11.774	14.886	21.813	38.447	43.569	87.829	88.504
500000	6.468	7.817	8.256	9.577	10.504	11.683	12.496	13.205	15.842	23.222	41.252	46.372	93.480	94.212
600000	6.927	8.248	8.888	10.297	11.281	12.545	13.409	14.197	16.299	23.894	43.862	47.703	96.161	96.929
800000	7.980	10.091	10.327	11.939	13.067	14.516	15.508	16.461	17.612	25.829	48.994	51.553	103.917	104.769
1000000	8.965	10.547	11.673	13.474	14.732	16.356	17.468	18.577	18.835	27.630	51.285	55.126	111.124	112.055
1500000	11.665	14.098	15.337	17.659	19.283	21.388	22.825	24.350	26.947	33.041	62.053	65.894	132.819	133.978
2000000	14.191	17.522	18.772	21.585	23.547	26.104	27.842	29.760	34.821	38.104	69.561	75.962	153.114	154.484
2500000	16.557	21.083	21.984	25.256	27.539	30.516	32.541	34.823	38.035	42.833	80.248	85.368	172.071	173.639
3000000	18.772	23.134	24.990	28.691	31.268	34.640	36.931	39.557	41.033	47.246	90.303	94.144	189.754	191.507
4000000	21.535	26.014	28.671	32.915	35.870	39.740	42.370	45.382	48.874	54.205	102.886	108.008	217.694	219.710
5000000	24.148	31.224	32.150	36.905	40.224	44.561	47.510	50.886	50.244	60.779	108.307	121.110	244.102	246.360
6000000	27.079	34.354	36.047	41.384	45.104	49.966	53.275	57.059	59.697	68.151	128.116	135.799	273.710	276.244
7000000	29.472	41.754	44.844	49.368	52.368	55.781	59.476	66.250	69.569	84.781	168.937	171.781	340.499	343.651
8000000	33.049	46.817	50.283	55.356	58.718	62.549	66.691	74.287	77.703	95.063	172.356	189.427	381.800	385.334

Equivalent Standard Loads for 6-layer and 7-layer Metal Interconnect

Gate Count	Fanouts													
	1	2	3	4	5	6	7	8	16	32	64	130	131	132
6LM														
5000	0.467	0.815	1.346	1.935	2.248	2.754	3.081	4.124	5.909	10.297	20.018	22.323	39.311	43.260
10000	0.486	1.179	1.486	2.224	2.520	3.498	1.035	4.874	7.022	11.968	23.825	26.130	44.573	48.126
50000	0.541	1.474	2.067	3.461	4.234	5.201	6.163	6.526	8.411	13.083	25.516	29.148	46.823	49.850
100000	0.805	1.638	2.559	3.695	4.419	5.382	7.112	7.461	9.715	14.057	28.634	35.386	57.722	60.925
150000	3.110	4.215	4.697	5.961	6.441	7.821	7.839	8.405	10.667	15.567	29.982	35.974	63.207	63.699
200000	4.348	4.935	5.551	6.398	7.026	7.821	8.372	8.850	11.215	16.484	31.228	37.567	66.431	66.949
300000	4.783	5.240	6.104	7.122	7.803	8.673	9.272	9.791	12.392	18.195	32.892	38.653	73.268	73.836
400000	5.220	6.014	6.614	7.685	8.439	9.394	10.053	10.596	13.398	19.632	34.602	39.213	79.045	79.653
500000	5.821	7.035	7.431	8.618	9.453	10.516	11.246	11.884	14.258	20.900	37.126	41.734	84.132	84.791
600000	6.234	7.423	8.000	9.268	10.154	11.291	12.069	12.778	14.669	21.504	39.476	42.933	86.545	87.236
800000	7.183	9.081	9.293	10.746	11.760	13.065	13.957	14.815	15.850	23.246	44.094	46.398	93.525	94.293
1000000	8.069	9.492	10.506	12.128	13.260	14.720	15.722	16.718	16.951	24.866	46.157	49.614	100.012	100.850
1500000	10.498	12.689	13.803	15.894	17.354	19.248	20.543	21.915	24.252	29.738	55.848	59.305	119.537	120.580
2000000	12.772	15.770	16.894	19.425	21.193	23.494	25.059	26.783	31.339	34.293	62.604	68.366	137.803	139.035
2500000	14.902	18.974	19.785	22.730	24.785	27.465	29.287	31.340	34.232	38.549	72.222	76.831	154.864	156.275
3000000	16.894	20.821	22.492	25.821	28.142	31.175	33.238	35.600	36.929	42.522	81.273	84.730	170.777	172.356
4000000	19.382	23.411	25.805	29.624	32.283	35.766	38.134	40.844	43.986	48.783	92.596	97.206	195.925	197.740
5000000	21.732	28.102	28.935	33.215	36.203	40.104	42.760	45.797	45.220	54.701	97.476	109.000	219.692	221.724
6000000	24.370	30.919	32.443	37.246	40.594	44.970	47.949	51.352	53.726	61.336	115.305	122.218	246.340	248.620
7000000	26.526	37.579	40.360	44.431	47.132	50.203	53.529	59.626	62.612	76.303	152.043	154.602	306.450	309.285
8000000	29.744	42.136	45.256	49.821	52.846	56.293	60.022	66.858	69.933	85.557	155.120	170.484	343.621	346.800
7LM														
5000	0.419	0.734	1.213	1.742	2.024	2.478	2.774	3.7133	5.319	9.268	18.016	20.091	35.380	38.935
10000	0.439	1.061	1.339	2.002	2.268	3.150	3.632	4.386	6.319	10.772	21.443	23.518	40.116	43.313
50000	0.486	1.327	1.860	3.114	3.811	4.679	5.547	5.872	7.571	11.774	22.965	26.232	42.140	44.866
100000	0.724	1.474	2.303	3.327	3.978	4.844	6.400	6.715	8.742	12.652	25.770	31.846	51.951	54.833
150000	2.799	3.793	4.226	5.364	5.797	6.583	7.053	7.565	9.600	14.010	26.984	32.378	56.886	57.329
200000	3.913	4.441	4.996	5.758	6.323	7.039	7.533	7.965	10.092	14.837	28.106	33.809	59.789	60.254
300000	4.305	4.717	5.492	6.409	7.022	7.807	8.344	8.813	11.154	16.376	29.602	34.789	65.941	66.453
400000	4.699	5.411	5.953	6.917	7.594	8.455	9.047	9.537	12.057	17.669	31.142	35.291	71.142	71.689
500000	5.240	6.333	6.687	7.758	8.508	9.463	10.122	10.695	12.833	18.811	33.413	37.561	75.718	76.313
600000	5.610	6.681	7.199	8.341	9.138	10.161	10.862	11.500	13.203	19.354	35.527	38.640	77.892	78.512
800000	6.465	8.173	8.364	9.671	10.585	11.758	12.561	13.333	14.266	20.921	39.685	41.758	84.173	84.864
1000000	7.262	8.543	9.455	10.913	11.933	13.248	14.150	15.047	15.256	22.380	41.541	44.651	90.010	90.764
1500000	9.449	11.419	12.423	14.305	15.620	17.325	18.488	19.724	21.827	26.764	50.264	53.374	107.582	108.521
2000000	11.494	14.193	15.205	17.484	19.073	21.144	22.553	24.106	28.205	30.864	56.344	61.529	124.021	125.132
2500000	13.411	17.077	17.807	20.457	22.307	24.718	26.358	28.207	30.809	34.695	65.000	69.147	139.378	140.647
3000000	15.205	18.738	20.242	23.240	25.327	28.059	29.913	32.041	33.236	38.270	73.146	76.256	153.700	155.122
4000000	17.443	21.071	23.224	26.661	29.055	32.189	34.319	36.760	39.589	43.905	83.336	87.486	176.332	177.966
5000000	19.559	25.291	26.041	29.894	32.583	36.094	38.482	41.218	40.697	49.232	87.728	98.098	197.722	199.551
6000000	21.933	27.827	29.199	33.522	36.535	40.472	43.153	46.218	48.354	55.203	103.773	109.998	221.872	223.827
7000000	23.872	33.821	36.325	39.988	42.417	45.183	48.175	53.663	56.350	68.673	136.838	139.143	275.805	278.358
8000000	26.770	37.921	40.730	44.838	47.561	50.665	54.020	60.173	62.939	77.002	139.608	153.435	309.259	312.121

Appendix C

Maximum Fanouts

Maximum Fanouts of Internal Macrocells

(When input t_R/t_F = 0.073ns, one fanout (SL) = 0.00412pF)

Cell Name	Output Pin	Maximum Fanouts
ad2	Y	110
ad2b	Y	110
ad2bd2	Y	221
ad2bd4	Y	445
ad2bd8	Y	889
ad2d2	Y	221
ad2d4	Y	444
ad2d8	Y	885
ad3	Y	110
ad3d2	Y	222
ad3d4	Y	446
ad4	Y	110
ad4d2	Y	223
ad4d4	Y	447
ad5	Y	54
ad5d2	Y	109
ad5d4	Y	443
ao21	Y	54
ao211	Y	34
ao2111	Y	25
ao2111d2	Y	222
ao211d2	Y	69
ao211d4	Y	445
ao21d2	Y	108
ao21d4	Y	444
ao22	Y	53
ao221	Y	34
ao221d2	Y	221
ao221d4	Y	446
ao222	Y	33
ao2222	Y	23
ao2222d2	Y	222
ao2222d4	Y	447
ao222a	Y	51
ao222d2a	Y	103
ao222d2	Y	221
ao222d4	Y	445
ao22a	Y	53
ao22d2a	Y	106
ao22d2	Y	106
ao22d4	Y	444
ao31	Y	52
ao31d2	Y	106
ao31d4	Y	444
ao311	Y	33
ao311d2	Y	221
ao3111	Y	24
ao3111d2	Y	222
ao31d2	Y	106
ao31d4	Y	444
ao32	Y	52
ao321	Y	33
ao321d2	Y	221
ao322	Y	32
ao32d2	Y	221
ao33	Y	51
ao331	Y	32
ao331d2	Y	222
ao332	Y	32
ao332d2	Y	222
ao33d2	Y	221
busholder	Y	10000
cglp	GCK	110
cglpd2	GCK	221
cglpd4	GCK	445
fa	S	110
	CO	110
fad2	S	222
	CO	222
fad4	S	448
	CO	448
fd1	Q	110
	QN	110
fd1d2	Q	222
	QN	222
fd1d4	Q	443
	QN	443
fd1cs	Q	110
	QN	110
fd1csd2	Q	222
	QN	221
fd1csd4	Q	442
	QN	444
fd1q	Q	110
fd1qd2	Q	221
fd1qd4	Q	443
fd1s	Q	110
	QN	110
fd1sd2	Q	222
	QN	222
fd1sd4	Q	443
	QN	444
fd1sq	Q	110
fd1sqd2	Q	221
fd1sqd4	Q	442
fd2	Q	110
	QN	109
fd2d2	Q	222
	QN	221
fd2d4	Q	444
	QN	443
fd2cs	Q	110
	QN	110
fd2csd2	Q	222
	QN	221
fd2csd4	Q	443
	QN	443
fd2q	Q	110
fd2qd2	Q	222
fd2qd4	Q	443
fd2s	Q	110
	QN	110
fd2sd2	Q	222
	QN	220
fd2sd4	Q	444
	QN	444
fd2sq	Q	110
fd2sqd2	Q	222
fd2sqd4	Q	443
fd3	Q	110
	QN	110
fd3d2	Q	222
	QN	221
fd3cs	Q	110
	QN	110
fd3csd2	Q	221
	QN	222
fd3q	Q	110

Cell Name	Output Pin	Maximum Fanouts
fd3qd2	Q	221
fd3s	Q	110
	QN	110
fd3sd2	Q	222
	QN	222
fd3sq	Q	110
fd3sqd2	Q	221
fd4	Q	110
	QN	110
fd4d2	Q	222
	QN	221
fd4cs	Q	110
	QN	110
fd4csd2	Q	221
	QN	222
fd4q	Q	110
fd4qd2	Q	221
fd4s	Q	110
	QN	110
fd4sd2	Q	222
	QN	221
fd4sq	Q	110
fd4sqd2	Q	221
fd5	Q	110
	QN	110
fd5d2	Q	223
	QN	222
fd5s	Q	110
	QN	110
fd5sd2	Q	223
	QN	222
fd6	Q	110
	QN	110
fd6d2	Q	222
	QN	220
fd6s	Q	111
	QN	110
fd6sd2	Q	222
	QN	220
fd7	Q	111
	QN	110
fd7d2	Q	223
	QN	222
fd7s	Q	111
	QN	110
fd7sd2	Q	223
	QN	222
fd8	Q	111
	QN	110
fd8d2	Q	222
	QN	221
fd8s	Q	111
	QN	110
fd8sd2	Q	222
	QN	221
fds2	Q	110
	QN	110
fds2d2	Q	222
	QN	221
fds2cs	Q	110
	QN	110
fds2csd2	Q	222
	QN	221
fds2s	Q	110
	QN	110

Cell Name	Output Pin	Maximum Fanouts
fds2sd2	Q	222
	QN	222
fds3	Q	110
	QN	110
fds3d2	Q	222
	QN	222
fds3cs	Q	110
	QN	110
fds3csd2	Q	221
	QN	222
fds3s	Q	110
	QN	110
fds3sd2	Q	222
	QN	222
fj2	Q	111
	QN	110
fj2d2	Q	223
	QN	220
fj2s	Q	111
	QN	110
fj2sd2	Q	223
	QN	221
fj4	Q	111
	QN	110
fj4d2	Q	222
	QN	221
fj4s	Q	111
	QN	110
fj4sd2	Q	223
	QN	221
ft2	Q	110
	QN	110
ft2d2	Q	223
	QN	221
ha	S	110
	CO	110
had2	S	222
	CO	221
had4	S	446
	CO	444
iv	Y	111
ivd2	Y	223
ivd3	Y	335
ivd4	Y	447
ivd6	Y	671
ivd8	Y	893
ivd16	Y	1786
ivd24	Y	2665
ivt	Y	104
ivtd2	Y	215
ivtd4	Y	437
ivtd8	Y	880
ivtd16	Y	1778
ld1	Q	110
	QN	110
ld1d2	Q	223
	QN	221
ld1d4	Q	443
	QN	444
ld1q	Q	110
ld1qd2	Q	222
ld1qd4	Q	443
ld2	Q	111
	QN	110

Cell Name	Output Pin	Maximum Fanouts
ld2d2	Q	223
	QN	221
ld2q	Q	110
ld2qd2	Q	223
ld3	Q	110
	QN	110
ld3d2	Q	221
	QN	222
ld4	Q	110
	QN	110
ld4d2	Q	220
	QN	221
ld5	Q	111
	QN	110
ld5d2	Q	223
	QN	221
ld5q	Q	110
ld5qd2	Q	222
ld6	Q	111
	QN	110
ld6d2	Q	223
	QN	221
ld6q	Q	110
ld6qd2	Q	223
mx2	Y	110
mx2d2	Y	222
mx2d4	Y	447
mx2d8	Y	895
mx2i	YN	53
mx2ia	YN	53
mx2id2	YN	107
mx2id2a	YN	106
mx2id4	YN	444
mx2id4a	YN	444
mx4	Y	111
mx4d2	Y	223
mx4d4	Y	448
mx8	Y	111
mx8d2	Y	223
mx8d4	Y	442
nd2	Y	103
nd2b	Y	104
nd2bd2	Y	209
nd2bd4	Y	419
nd2bd8	Y	887
nd2d2	Y	210
nd2d4	Y	420
nd2d8	Y	887
nd3	Y	68
nd3b	Y	68
nd3bd2	Y	137
nd3bd4	Y	442
nd3bd8	Y	888
nd3d2	Y	137
nd3d4	Y	442
nd3d8	Y	888
nd4	Y	51
nd4d2	Y	102
nd4d4	Y	443
nd5	Y	109
nd5d2	Y	220
nd5d4	Y	442
nd6	Y	109
nd6d2	Y	220
nd6d4	Y	443

Cell Name	Output Pin	Maximum Fanouts
nd8	Y	70
nd8d2	Y	221
nd8d4	Y	443
nid	Y	110
nid16	Y	1778
nid2	Y	221
nid3	Y	332
nid4	Y	445
nid6	Y	664
nid8	Y	892
nid24	Y	2659
nit	Y	104
nitd16	Y	1773
nitd2	Y	215
nitd4	Y	438
nitd8	Y	882
nr2	Y	54
nr2a	Y	110
nr2b	Y	54
nr2bd2	Y	109
nr2bd4	Y	218
nr2bd8	Y	889
nr2d2	Y	109
nr2d4	Y	219
nr2d8	Y	888
nr3	Y	35
nr3a	Y	72
nr3d2	Y	72
nr3d4	Y	444
nr4	Y	110
nr4d2	Y	221
nr4d4	Y	444
nr5	Y	110
nr5d2	Y	221
nr5d4	Y	445
nr6	Y	110
nr6d2	Y	221
nr6d4	Y	444
nr8	Y	110
nr8d2	Y	222
nr8d4	Y	447
oa21	Y	54
oa211	Y	53
oa2111	Y	53
oa2111d2	Y	107
oa211d2	Y	107
oa211d4	Y	444
oa21d2	Y	108
oa21d4	Y	444
oa22	Y	52
oa221	Y	51
oa221d2	Y	102
oa221d4	Y	445
oa222	Y	49
oa2222	Y	47
oa2222d2	Y	222
oa2222d4	Y	445
oa222d2	Y	99
oa222d4	Y	446
oa22a	Y	54
oa22d2	Y	104
oa22d2a	Y	108
oa22d4	Y	444
oa22d4a	Y	444
oa31	Y	35

Cell Name	Output Pin	Maximum Fanouts
oa311	Y	34
oa3111	Y	34
oa31d2	Y	70
oa31d4	Y	444
oa32	Y	34
oa32d2	Y	221
oa321	Y	33
oa321d2	Y	221
oa322	Y	32
oa322d2	Y	222
oa33	Y	33
oa33d2	Y	222
or2	Y	109
or2b	Y	109
or2bd2	Y	220
or2bd4	Y	442
or2bd8	Y	889
or2d2	Y	220
or2d4	Y	441
or2d8	Y	888
or3	Y	110
or3d2	Y	221
or3d4	Y	441
or4	Y	103
or4d2	Y	208
or4d4	Y	416
or5	Y	103
or5d2	Y	208
or5d4	Y	416
scg1	Y	68
scg1d2	Y	137
scg2	Y	110
scg2d2	Y	221
scg2d4	Y	446
scg3	Y	68
scg3d2	Y	137
scg3d4	Y	275
scg4	Y	104
scg4d2	Y	209
scg4d4	Y	420
scg5	Y	110
scg5d2	Y	223
scg5d4	Y	447
scg6	Y	110
scg6d2	Y	221
scg6d4	Y	446
scg7	Y	104
scg7d2	Y	209
scg7d4	Y	421
scg8	Y	110
scg8d2	Y	222
scg9	Y	110
scg9d2	Y	221
scg9d4	Y	446
scg10	Y	110
scg10d2	Y	222
scg10d4	Y	446
scg11	Y	35
scg11d2	Y	72
scg12	Y	54
scg12d2	Y	109
scg12d4	Y	218
scg13	Y	104
scg13d2	Y	208
scg13d4	Y	419

Cell Name	Output Pin	Maximum Fanouts
scg14	Y	104
scg14d2	Y	209
scg14d4	Y	420
scg15	Y	68
scg15d2	Y	137
scg15d4	Y	274
scg16	Y	54
scg16d2	Y	108
scg16d4	Y	443
scg17	Y	104
scg17d2	Y	210
scg17d4	Y	420
scg18	Y	68
scg18d2	Y	137
scg18d4	Y	274
scg19	Y	54
scg19d2	Y	108
scg20	Y	54
scg20d2	Y	109
scg20d4	Y	218
scg21	Y	35
scg21d2	Y	72
scg22	Y	54
scg22d2	Y	108
scg22d4	Y	443
xn2	Y	110
xn2d2	Y	222
xn2d4	Y	448
xn2d8	Y	896
xn3	Y	111
xn3d2	Y	224
xn3d4	Y	444
xo2	Y	110
xo2d2	Y	223
xo2d4	Y	448
xo2d8	Y	899
xo3	Y	111
xo3d2	Y	223
xo3d4	Y	446

Maximum Fanouts of I/O Cells

(When input t_R/t_F = 0.073ns, one fanout (SL) = 0.00412pF)

Cell Name	Output Pin	Maximum Fanouts
phic	Y	693
phic_abb	Y	469
phicc_abb	Y	477
phicd	Y	692
phicd_abb	Y	469
phicen_abb	Y	344
phicu	Y	692
phicu_abb	Y	469
phis	Y	693
phis_abb	Y	470
phisd	Y	693
phisd_abb	Y	469
phisu	Y	693
phisu_abb	Y	469
phsckdc2	Y	1452
phsckdc4	Y	2913
phsckdc6	Y	4359
phsckdc8	Y	5807
phsckdcd2	Y	1451
phsckdcd4	Y	2917
phsckdcd6	Y	4354
phsckdcd8	Y	5808
phsckdcu2	Y	1452
phsckdcu4	Y	2916
phsckdcu6	Y	4358
phsckdcu8	Y	5815
phsckds2	Y	1451
phsckds4	Y	2918
phsckds6	Y	4355
phsckds8	Y	5809
phsckdsd2	Y	1452
phsckdsd4	Y	2913
phsckdsd6	Y	4358
phsckdsd8	Y	5807
phsckdsu2	Y	1451
phsckdsu4	Y	2918
phsckdsu6	Y	4355
phsckdsu8	Y	5808
phtic	Y	692
phticd	Y	692
phticu	Y	692
phtis	Y	693
phtisd	Y	693
phtisu	Y	693
phsosck1	YN	362
phsosck17	YN	362
phsoscm1	YN	231
phsoscm16	YN	231
phsoscm2	YN	1103
phsoscm26	YN	1106
phsoscm3	YN	1100
phsoscm36	YN	1104
pmic	Y	692
pmic_abb	Y	386
pmicc_abb	Y	392
pmicd	Y	693
pmicd_abb	Y	386
pmicen_abb	Y	250
pmicu	Y	694
pmicu_abb	Y	386
pmis	Y	693
pmis_abb	Y	386
pmisd	Y	693
pmisd_abb	Y	386
pmisu	Y	693
pmisu_abb	Y	386
pmsckdc2	Y	1450
pmsckdc4	Y	2918
pmsckdc6	Y	4352
pmsckdc8	Y	5810
pmsckdcd2	Y	1453
pmsckdcd4	Y	2914
pmsckdcd6	Y	4354
pmsckdcd8	Y	5807
pmsckdcu2	Y	1451
pmsckdcu4	Y	2916
pmsckdcu6	Y	4358
pmsckdcu8	Y	5815
pmsckds2	Y	1453
pmsckds4	Y	2913
pmsckds6	Y	4359
pmsckds8	Y	5813
pmsckdsd2	Y	1453
pmsckdsd4	Y	2913
pmsckdsd6	Y	4359
pmsckdsd8	Y	5813
pmsckdsu2	Y	1452
pmsckdsu4	Y	2917
pmsckdsu6	Y	4354
pmsckdsu8	Y	5807
pmsosck1	YN	362
pmsoscm1	YN	231
pmsoscm2	YN	1104
pmtic	Y	692
pmticd	Y	693
pmticu	Y	694

Maximum Fanouts for CK and NID Cells

<Condition>

- Library = STDH150
- V_{DD} = 1.2V
- Fanout = 0.00438pF (= input cap for CK pin of FD1)
- Standard Load (SL) = 0.00412pF
- Input slope = 0.073ns
- Maximum output transition time (mott) = 1.1ns
- Maximum frequency ≤ 300MHz
- Net length (μm/fanout): branch net length for each fanout except trunk

Table 1-1. Maximum Fanout for NID Cells

Trunk width (μm)	0.2		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	2000	5000	2000	5000	
nid	8	-	-	-	110
nid2	36	-	3	-	221
nid3	57	-	12	-	332
nid4	73	-	20	-	445
nid6	94	-	38	14	664
nid8	107	-	55	30	892
nid16	130	-	120	88	1778
nid24	139	-	182	138	2659

For high fanout nets including clock net, Samsung strongly recommends using clock tree synthesis.

Appendix D

Package Capabilities

Package

The most current package availability and capability can be obtained from your local Samsung Technology and Design Centers.

■ In-house ❑ Sub-contractor

LQFP												
Package	**Pitch**	**Lead Inductance**	**Lead Count**									
			32	48	64	80	100	128	144	160	176	208	256
0707 mm	0.8		■										
	0.5	< 3nH		■									
1010 mm	0.5	< 5nH			■								
1212 mm	0.5	< 5nH				■							
1420 mm	0.5	< 12nH						■					
1414 mm	0.8	< 6nH			■								
	0.5	< 6nH					■						
	0.4	v						■					
2020 mm	0.4								■				
2024 mm	0.5									■	■		
2828 mm	0.5	< 17nH										■	
	0.4	< 17nH											■
TQFP													
1212 mm	0.5	< 5nH				■							
1414 mm	0.5	< 5nH					■						
1420 mm	0.065	< 10nH					■						

PQFP (PQ2 Thermally Enhanced)									
Package	**Pitch**	**Lead Count**							
		100	120	128	144	160	208	240	304
1420 mm	0.65	❑							
	0.5			❑					
2828 mm	0.8		❑	❑					
	0.65				❑	❑			
	0.5						❑		
3232 mm	0.5							❑	
4040 mm	0.5								❑
QFP (with Heat Spreader)									
1420 mm	0.65	■							
	0.5								
2828 mm	0.8		❑	■					
	0.65				❑	❑			
	0.5						❑		
3232 mm	0.5							❑	
4040 mm	0.5								❑

■ In-house ❑ Sub-contractor

PLCC									
Package	**Pitch**	**Lead Inductance**	**Lead Count**						
			18	28	32	44	52	68	84
7.37 x 12.35 mm	1.27		■						
11.53 x 11.53 mm				■					
11.44 x 13.98 mm					■				
16.61 x 16.61 mm		< 5nH				■			
19.10 x 19.10 mm							■		
24.23 x 24.23 mm								■	
29.31 x 29.31 mm		< 13nH							■

SOP								
Package	**Pitch**	**Lead Count**						
		32	48	64(56)	68	69	100	256
8.34 x 20.30 mm	1.27	■						
TSOP1								
1014 mm	0.4		■					
PLCC								
24.33 x 24.23mm	1.27				■			
QFP								
1420 mm	0.65						■	
FBGA								
0909 mm	0.75			■				
0911 mm	0.8					■		
1717 mm	1.00							■

SBGA									
Package	**Pitch**	**Lead Inductance**		**Lead Count**					
		Lp/g	**Lsig**	256	304	352	540	648	696
2727 mm	1.27	< 3nH	< 7nH	❑					
3131 mm		< 3nH	< 8nH		❑				
3535 mm		< 3nH	< 8nH			❑			
42.5 x 47.5 mm		< 3nH	<9nH				❑		
4545 mm		< 3nH	<9nH					❑	
47.5 x 47.5 mm									❑

Package Parameter Guide for PBGAs and FBGAs

Lead Inductance							
Package Type	**Stack-Up (layer)**	**PCB Size (mm x mm)**	**L_p/g (nH)**	**L_wire (nH)**	**L_total (nH)**	**T (mm)**	**L_sig (nH)**
PBGA	2L	23 x 23	< 3.5	1.5	< 4.5	5	< 7
	2L	27 x 27	< 4	1.5	< 5.5	6	< 7.5
	2L	31 x 31	< 4.1	1.5	< 5.6	7	< 8.5
	2L	35 x 35	< 4.5	1.5	< 6	8	< 10
	4L	23 x 23	< 1.3	1.5	< 2.8	5	< 3.5
	4L	27 x 27	< 1.5	1.5	< 3	6	< 4
	4L	31 x 31	< 1.6	1.5	< 3.1	7	< 4.5
	4L	35 x 35	< 1.7	1.5	< 3.2	8	< 5.5
FBGA	2L	06 x 06	< 2	1.5	< 3.5	2	< 2.5
	2L	08 x 08	< 2	1.5	< 3.5	2	< 3.5
	2L	09 x 09	< 2	1.5	< 3.5	2	< 4.5
	2L	10 x 10	< 2	1.5	< 3.5	2	< 4.5
	2L	12 x 12	< 2	1.5	< 3.5	2	< 5
	2L	13 x 13	< 2	1.5	< 3.5	2	< 6
	2L	14 x 14	< 2	1.5	< 3.5	2	< 6
	2L	16 x 16	< 2	1.5	< 3.5	2	< 7
	2L	17 x 17	< 2	1.5	< 3.5	2	< 8
	2L	18 x 18	< 2	1.5	< 3.5	2	< 8

NOTES: Condition to use above package parameter guide;

1. Above data are estimated calculations with below assumptions.
2. Center balls are all ground balls for PBGA ball map design.
3. For a ball map design, the power/ground ball pair should be arranged next to each other and located on the center closed inside row and column.
4. Distance between power/ground bonding pad and ball must be less than listed above T[mm] column distance.
5. The bonding wire length between power/ground ball and PCB bonding pad should be less than 2mm.
6. L_total = L_p/g + L_wire; L_p/g: Total inductance of power/ground pad L_sig: Signal line inductance.
7. Contact IPT development P/T for ball map design request form in special case, other than above 1) ~ 6) notes. Special guide will be provided.

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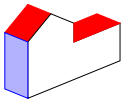

SSI

3655 North First Street San Jose CA, 95134, U.S.A.
TEL (1)-408-544-4740
FAX (1)-408-544-4950

SWDC

3345 Michelson Drive, Suite 250, Irvine, CA 92612, U.S.A.
TEL (1)-408-544-4885
FAX (1)-408-544-4950

CDI

85 West Tasman Road San Jose, CA 95134
TEL (1)-408-544-4553
FAX (1)-408-544-4979

SSEL

Samsung Electronics Europe ASIC Design Center Great West House, Great West Road, Brentford, Middlesex TW8 9DQ
TEL (44)-20-8380-7101
FAX (44)-20-8380-7095

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FAX (65)-6425-2022

CoAsia

Samsung Electronics Taiwan ASIC Center 9F, No. 69, Chou Tze St., Nei hu, Taipei, Taiwan, R.O.C.
TEL (886)-2-2658-2020
FAX (886)-2-8780-0101

Si-Plaza

Unit 2505, 25F, Cosco Tower, 183 Queen's Road Central, HK
TEL (852)-2907-6388
FAX (852)-2907-7188

AlphaChips

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