

MN101D09E

VTR Servo

Type	MN101D09E	
ROM (×8-bit)	80 K	
RAM (×8-bit)	2 K	
Package	QFP100-P-1818B *Lead-free	
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)
	When sub-clock operated	71.5 μs (at 2.7 V to 5.5 V fixed to 14.32 MHz internal frequency division)
		61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
Interrupts	• RESET • Runaway • External 0, 1, 2, 3, 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Capstan FG • Control • HSW • Cylinder FG • Servo VSYNC • Synchronous output • OSD • XDS • Serial 1 • Serial 2 • PWM 4 • OSDVSYNC	
Timer Counter	Timer counter 0: 8-bit × 1 (timer function) Clock source 1/4, 1/16 of system clock frequency Interrupt source overflow of timer counter 0 Timer counter 1: 8-bit × 1 (timer function, linear timer counter function) Clock source 1/4 of system clock frequency; CTL signal Interrupt source overflow of timer counter 1 Timer counter 2: 16-bit × 1 (timer function, input capture (DCTL specified edge), duty judgment of DCTL signal) Clock source 1/4, 1/16, 1/24 of system clock frequency Interrupt source overflow of timer counter 2; input of DCTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register Timer counter 3: 16-bit × 1 (timer function, detection of serial indexing, generation of remote control output carrier frequency) Clock source 1/4, 1/16 of system clock frequency Interrupt source overflow of timer counter 3 Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function) Clock source system clock Watchdog interrupt source .. 1/2¹⁶, 1/2¹⁹ of timer counter 5 frequency Clear by stable oscillation .. after 256 counts by timer counter 5 (2¹⁸ counts of OSC oscillation clock) Timer counter 6: 16-bit × 1 (clock function [max. 2 s]) Clock source 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency Interrupt source 1/2¹³, 1/2¹⁴, 1/2¹⁵ overflow of timer counter 6	
Serial Interface	Serial 1: 8-bit × 1 (synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function) Clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; <u>SBT1</u> pin input Serial 2: 8-bit × 1 (I²C) (master transmission/reception, slave transmission/reception) Clock source 1/144 to 1/252 of system clock; SCK pin input	

OSD		OSD mode:Accommodation with menu or super impose display	
		Applicable broadcasting system : NTSC, PAL, PAL-M, PAL-N	
		Screen configuration : 24 characters × 2n rows (n = 1 to 6)	
		Character type : max. 128 character types (variable)	
		Character size : 12 × 18 dots (Vertical direction: 1 dot for 2H at × 1 setting.)	
		Enlarged characters : each × 2 settings in horizontal and vertical	
		Character interpolation : none	
		Line background color : 8-hue settable (settable in the row unit at menu display)	
		Line background intensity : 8 gradations settable in the row unit	
		Screen background color : 8-hue settable (at output of composite video signal)	
		Character color : white	
		Character intensity : 8 gradations settable in the row unit	
		Frame function : 1-dot frame in 4 directions	
		Frame intensity : 4 gradations settable in the row unit	
		Blinking : none (covered by software)	
		Inverted character : settable in the character unit	
		Halftone : none	
		Common: Input : composite video signal input (output level: 1 V[p-p] / 2 V[p-p])	
		Clamp method : sync chip clamp, clamp level in 4 levels	
		Output : composite video output	
		Measure against image fluctuation : built-in AFC circuit	
		Dot clock : 1/2 of OSC oscillation clock (automatic phase adjustment)	
XDS		Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)	
ROM Correction		Correcting address designation: up to 3 addresses possible	
		Correction method: correction program being saved in internal RAM	
I/O Pins	I/O	56	• Common use: 56 ports 0, 1, 2, 4, 6, 7, B (by bit)
	Input	1	• Common use: 1
A/D Inputs		8-bit × 11-ch. (without S/H)	
PWM		13-bit × 2-ch. (at repetition cycle 572 μs, 14.32 MHz), 10-bit × 2-ch.(at repetition cycle 71.5 μs, 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 35.7 μs, 14.32 MHz)	
ICR		18-bit × 6-ch.	
OCR		16-bit × 7-ch. , 8-bit × 1-ch.	
Special Ports		3-state output (PTO) VLP pin; synchronous output: 7; 3-state synchronous output: 4; CTL amp; built-in FG amp; output of 1/4 OSC oscillation clock (1 V[p-p])	
Notes		VISS/VASS detection function	

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V			20	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

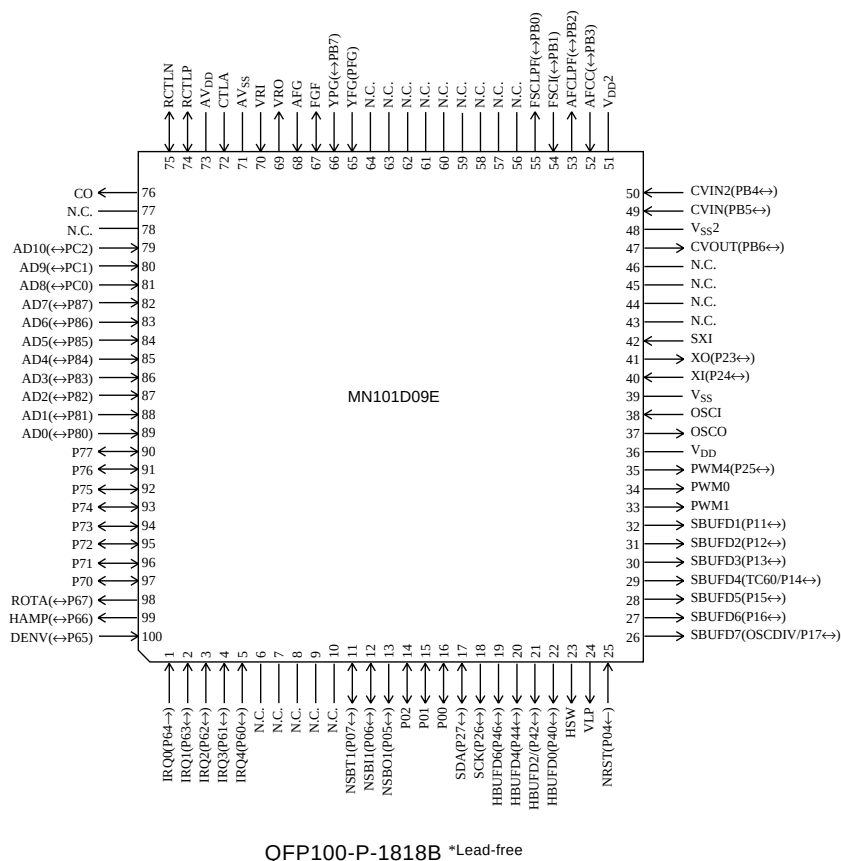
(Ta = 25°C ± 2°C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25°C ± 2°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



Support Tool

In-circuit Emulator

PX-ICE101C / D + PX-PRB101D08-QFP100-P-1818B-M

Flash Memory Built-in Type

Type MN101DF09G [ES (Engineering Sample) available]

ROM (× 8-bit) 128 K

RAM (× 8-bit) 4 K

Minimum instruction execution time 0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)

71.5 μs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division)

Package QFP100-P-1818B *Lead-free

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