

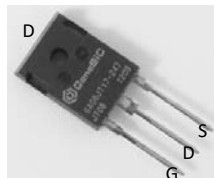
Normally – OFF Silicon Carbide Junction Transistor

| | | |
|-----------------------------------|---|--------|
| V_{DS} | = | 1700 V |
| $R_{DS(ON)}$ | = | 230 mΩ |
| I_D @ $T_C=125^{\circ}\text{C}$ | = | 8 A |
| h_{FE} $T_C=25^{\circ}\text{C}$ | = | 60 |

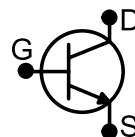
Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package



TO-247AB



Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Value | Unit | Notes |
|-----------------------------------|-----------|--|--|------|---------|
| Drain – Source Voltage | V_{DS} | $V_{GS} = 0\text{ V}$ | 1700 | V | Fig. 6 |
| Continuous Drain Current | I_D | $T_C = 125^{\circ}\text{C}$ | 8 | A | Fig. 19 |
| Continuous Gate Current | I_{GM} | | 1.5 | A | |
| Turn-Off Safe Operating Area | RBSOA | $T_{VJ} = 175^{\circ}\text{C}$, $I_G = 1\text{ A}$, Clamped Inductive Load | $I_{D,max} = 8$ @ $V_{DS} \leq V_{DSmax}$ | A | Fig. 16 |
| Short Circuit Safe Operating Area | SCSOA | $T_{VJ} = 175^{\circ}\text{C}$, $I_G = 1\text{ A}$, $V_{DS} = 1200\text{ V}$, Non Repetitive | 20 | μs | |
| Reverse Gate – Source Voltage | V_{SG} | | 30 | V | |
| Reverse Drain – Source Voltage | V_{SD} | | 50 | V | |
| Power Dissipation | P_{tot} | $T_C = 125^{\circ}\text{C}$ | 48 | W | Fig. 14 |
| Storage Temperature | T_{stg} | | -55 to 175 | °C | |

Electrical Characteristics

| Parameter | Symbol | Conditions | Value | | | Unit | Notes |
|------------------------------|----------------------|---|-------|---------|------|------|--------|
| | | | Min. | Typical | Max. | | |
| On State Characteristics | | | | | | | |
| Drain – Source On Resistance | R _{DS(ON)} | I _D = 8 A, T _J = 25 °C | | 230 | | mΩ | Fig. 5 |
| | | I _D = 8 A, T _J = 125 °C | | 410 | | | |
| | | I _D = 8 A, T _J = 175 °C | | 560 | | | |
| Gate Forward Voltage | V _{GS(FWD)} | I _G = 500 mA, T _J = 25 °C | | 3.0 | | V | Fig. 4 |
| | | I _G = 500 mA, T _J = 175 °C | | 2.8 | | | |
| DC Current Gain | h _{FE} | V _{DS} = 5 V, I _D = 8 A, T _J = 25 °C | | 60 | | – | Fig. 5 |
| | | V _{DS} = 5 V, I _D = 8 A, T _J = 175 °C | | 40 | | | |
| Off State Characteristics | | | | | | | |
| Drain Leakage Current | I _{DSS} | V _R = 1700 V, V _{GS} = 0 V, T _J = 25 °C | | 0.2 | 10 | μA | Fig. 6 |
| | | V _R = 1700 V, V _{GS} = 0 V, T _J = 125 °C | | 0.5 | 50 | | |
| | | V _R = 1700 V, V _{GS} = 0 V, T _J = 175 °C | | 2.0 | 100 | | |
| Gate Leakage Current | I _{SG} | V _{SG} = 20 V, T _J = 25 °C | | 20 | | nA | |

Electrical Characteristics

| Parameter | Symbol | Conditions | Value | | | Unit | Notes |
|--|------------------------------------|--|-------|---------|------|------|-------------|
| | | | Min. | Typical | Max. | | |
| Capacitance Characteristics | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _D = 800 V, f = 1 MHz | | 850 | | pF | Fig. 7 |
| Reverse Transfer/Output Capacitance | C _{rss} /C _{oss} | V _D = 800 V, f = 1 MHz | | 20 | | pF | Fig. 7 |
| Output Capacitance Stored Energy | E _{OSS} | V _{GS} = 0 V, V _D = 1000 V, f = 1 MHz | | 8.6 | | μJ | Fig. 8 |
| Switching Characteristics ¹ | | | | | | | |
| Internal Gate Resistance, Zero Bias | R _{G(INT-ZERO)} | f = 1 MHz, V _{AC} = 25 mV, T _J = 175 °C | | 6.0 | | Ω | |
| Internal Gate Resistance, On | R _{G(INT-ON)} | V _{GS} > 2.5 V | | 0.9 | | Ω | |
| Turn On Delay Time | t _{d(on)} | T _J = 25 °C, V _{DS} = 1100 V, I _D = 8 A, | | 12 | | ns | |
| Fall Time, V _{DS} | t _f | R _{G(EXT)} = 20 Ω, C _G = 9 nF, | | 23 | | ns | Fig. 9, 11 |
| Turn Off Delay Time | t _{d(off)} | V _G = 20/-5 V, Load = 138 Ω | | 20 | | ns | |
| Rise Time, V _{DS} | t _r | Refer to Fig. 20 for I _G Waveform | | 14 | | ns | Fig. 10, 12 |
| Turn On Delay Time | t _{d(on)} | T _J = 175 °C, V _{DS} = 1100 V, I _D = 8 A, | | 12 | | ns | |
| Fall Time, V _{DS} | t _f | R _{G(EXT)} = 20 Ω, C _G = 9 nF, | | 22 | | ns | Fig. 9 |
| Turn Off Delay Time | t _{d(off)} | V _G = 20/-5 V, Load = 138 Ω | | 31 | | ns | |
| Rise Time, V _{DS} | t _r | Refer to Fig. 20 for I _G Waveform | | 11 | | ns | Fig. 10 |
| Turn-On Energy Per Pulse | E _{on} | T _J = 25 °C, V _{DS} = 1100 V, I _D = 8 A, | | 267 | | μJ | Fig. 9, 11 |
| Turn-Off Energy Per Pulse | E _{off} | R _{G(EXT)} = 20 Ω, C _G = 9 nF, | | 23 | | μJ | Fig. 10, 12 |
| Total Switching Energy | E _{tot} | V _G = 20/-5 V, Load = 1.05 mH | | 290 | | μJ | |
| Turn-On Energy Per Pulse | E _{on} | T _J = 175 °C, V _{DS} = 1100 V, I _D = 8 A, | | 253 | | μJ | Fig. 9 |
| Turn-Off Energy Per Pulse | E _{off} | R _{G(EXT)} = 20 Ω, C _G = 9 nF, | | 12 | | μJ | Fig. 10 |
| Total Switching Energy | E _{tot} | V _G = 20/-5 V, Load = 1.05 mH | | 265 | | μJ | |

¹ – All times are relative to the Drain-Source Voltage V_{DS}

Thermal Characteristics

| | | | | |
|-------------------------------------|------------|------|------|---------|
| Thermal resistance, junction - case | R_{thJC} | 1.03 | °C/W | Fig. 17 |
|-------------------------------------|------------|------|------|---------|

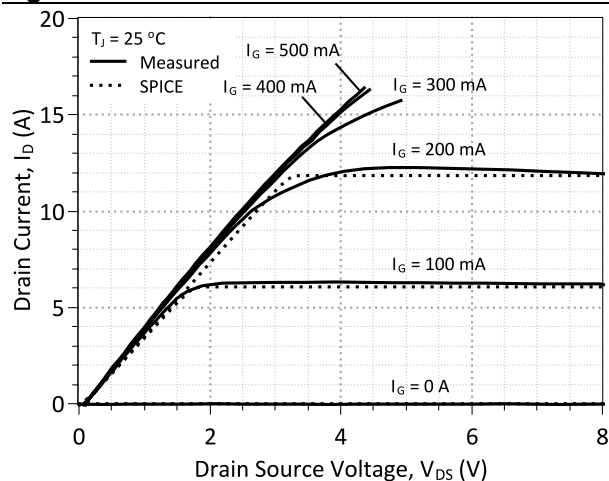
Figures


Figure 1: Typical Output Characteristics at 25 °C

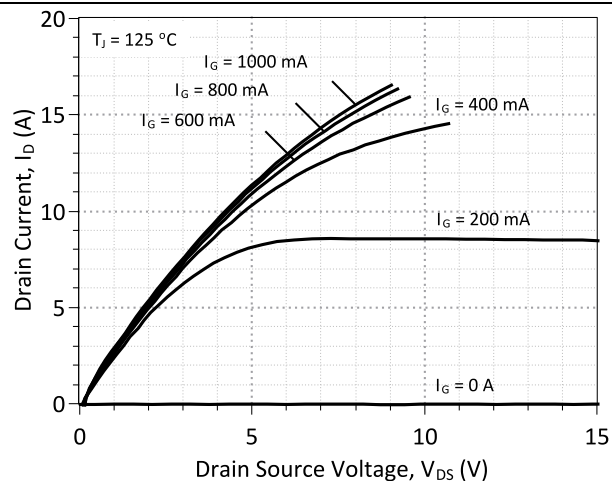


Figure 2: Typical Output Characteristics at 125 °C

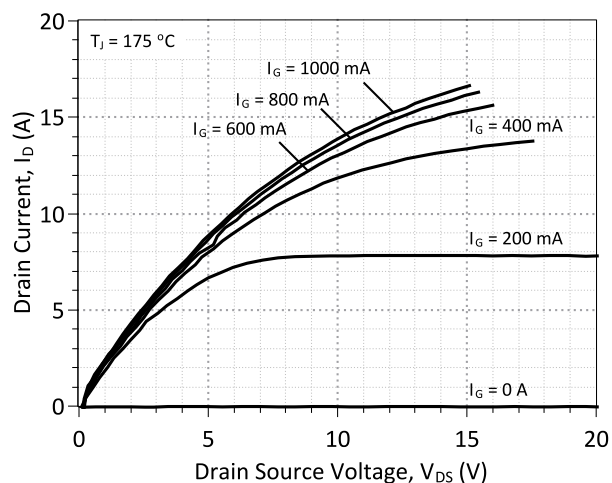


Figure 3: Typical Output Characteristics at 175 °C

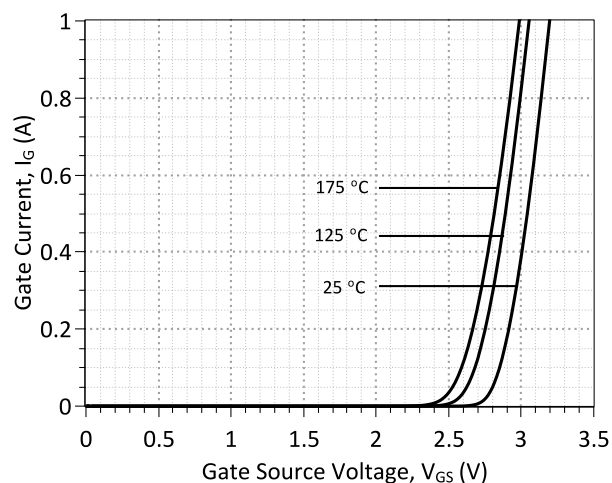


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

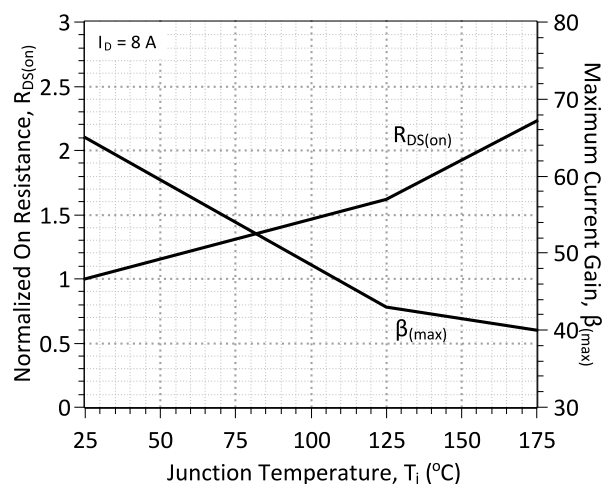


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

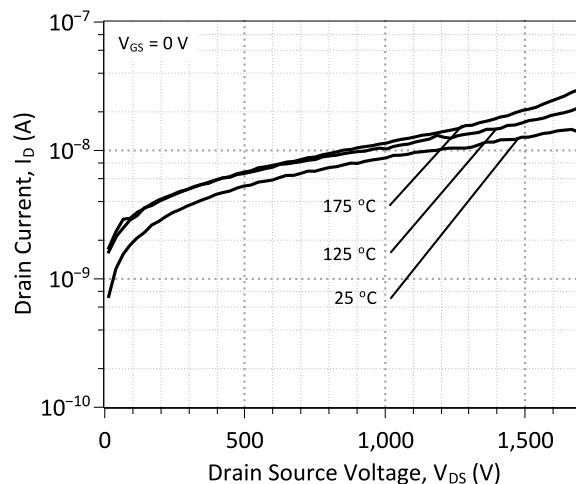


Figure 6: Typical Blocking Characteristics

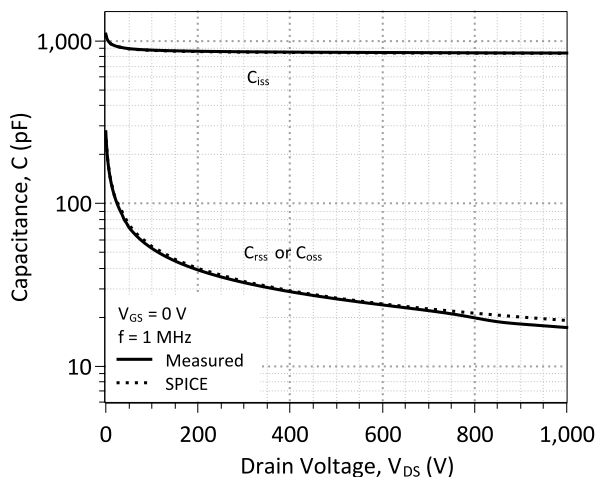


Figure 7: Input, Output, and Reverse Transfer Capacitance

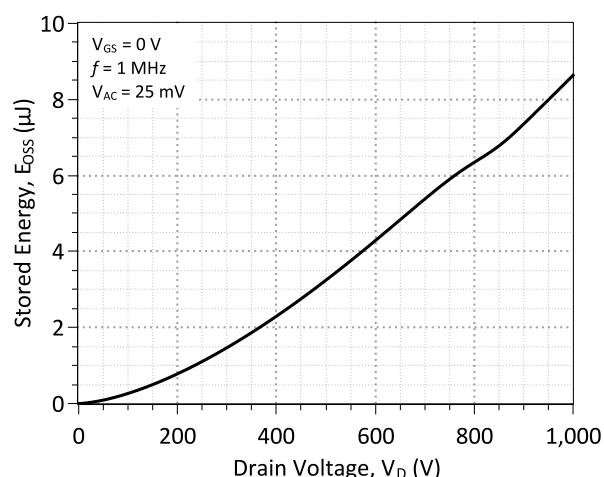


Figure 8: Output Capacitance Stored Energy

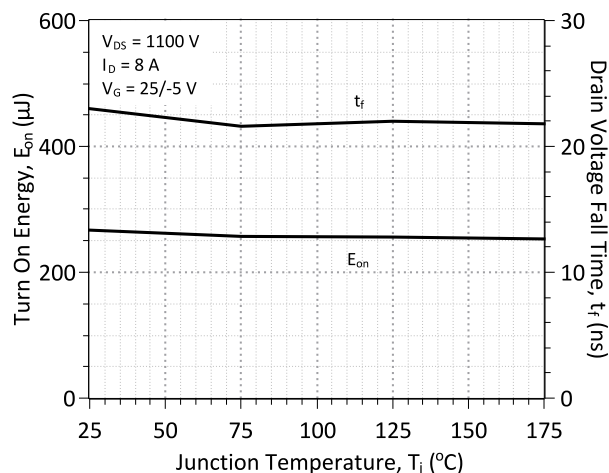


Figure 9: Typical Turn On Energy Losses and Switching Times vs. Temperature

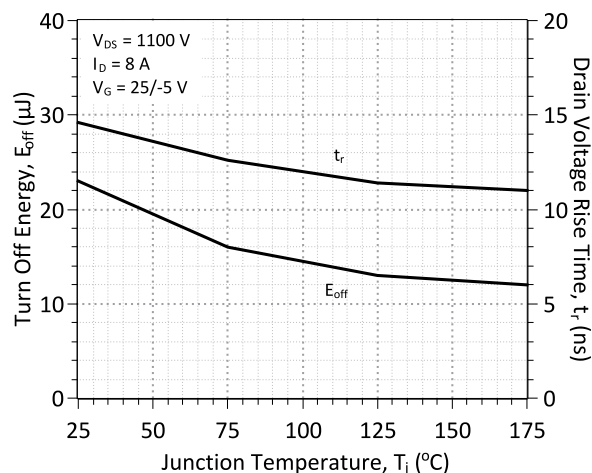


Figure 10: Typical Turn Off Energy Losses and Switching Times vs. Temperature

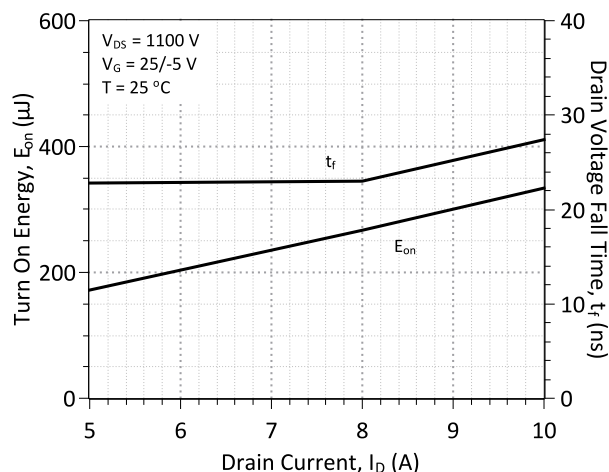


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Drain Current

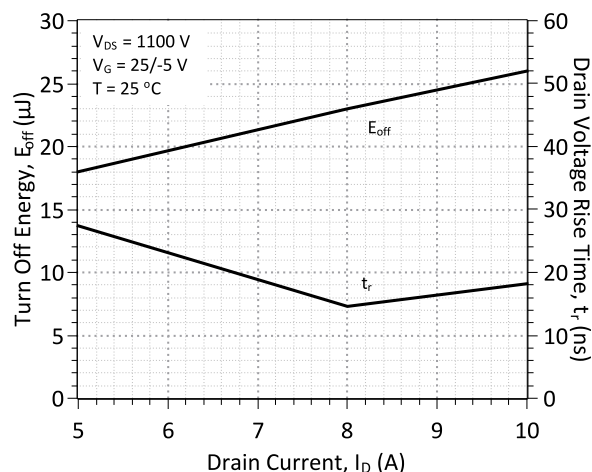


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Drain Current

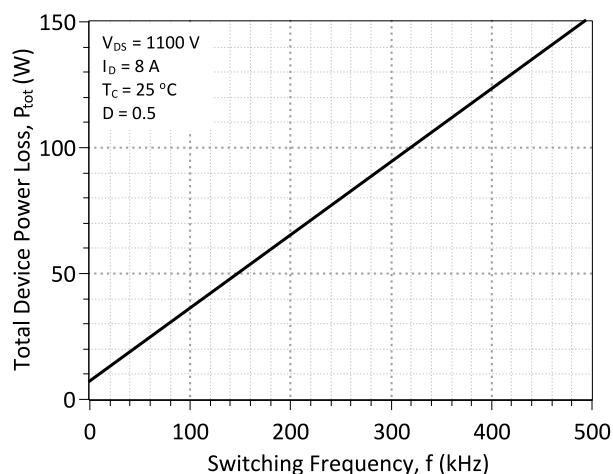


Figure 13: Typical Hard Switched Device Power Loss vs. Switching Frequency²

² – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

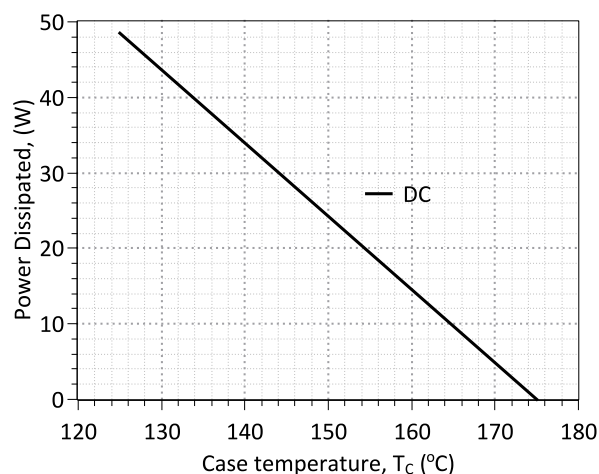


Figure 14: Power Derating Curve

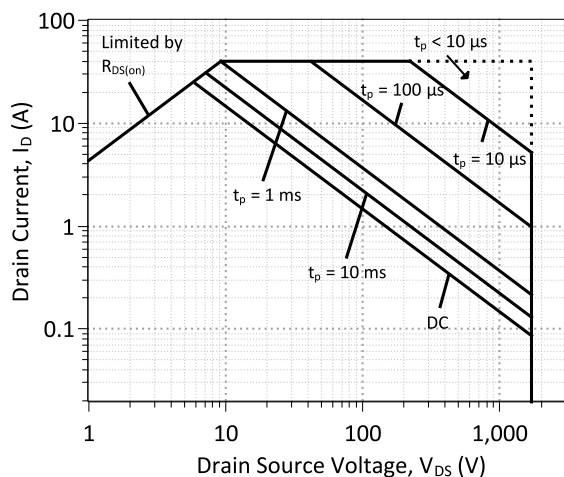


Figure 15: Forward Bias Safe Operating Area at $T_c = 25\text{ }^{\circ}\text{C}$

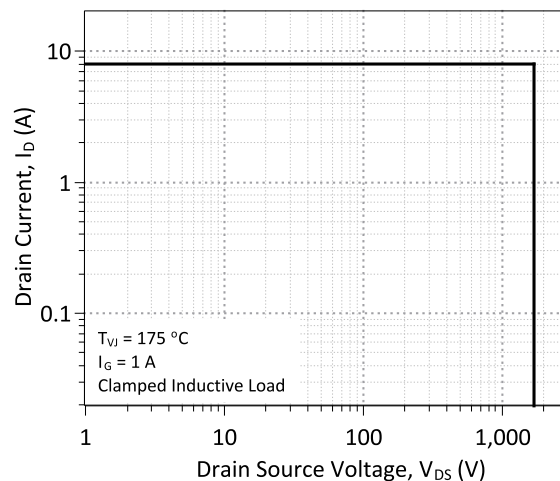


Figure 16: Turn-Off Safe Operating Area

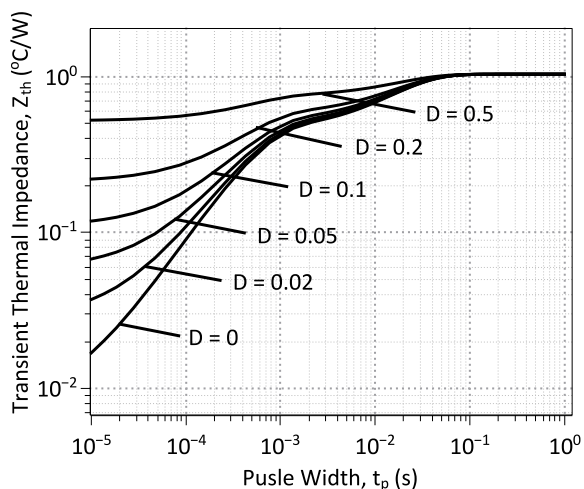


Figure 17: Transient Thermal Impedance

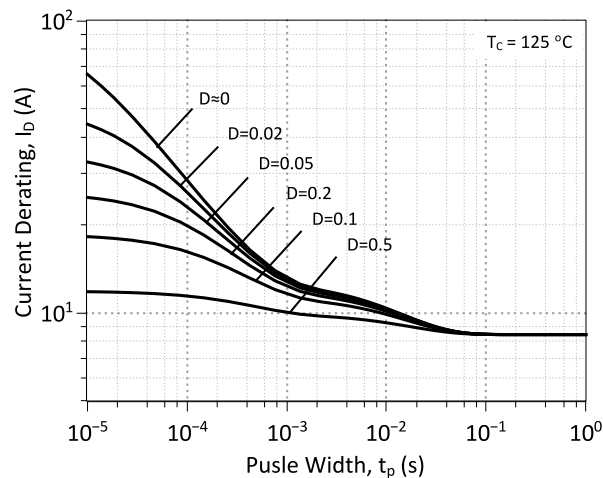


Figure 18: Drain Current Derating vs. Pulse Width

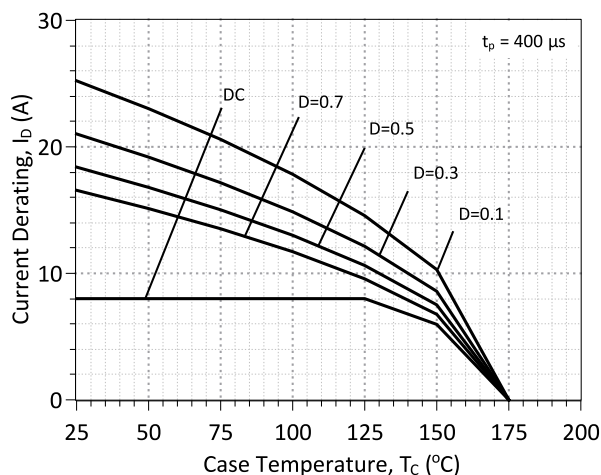


Figure 19: Drain Current Derating vs. Temperature

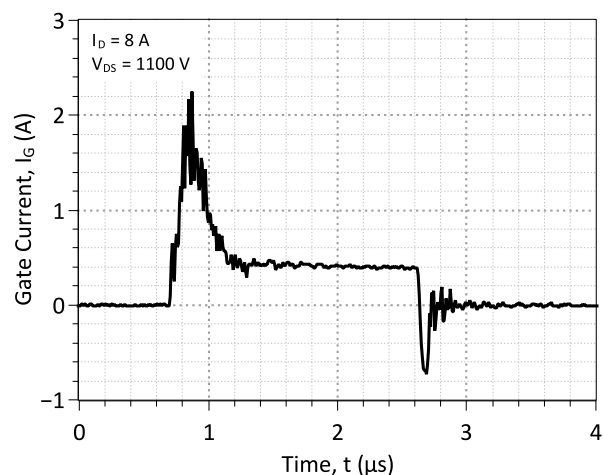


Figure 20: Typical Gate Current Waveform

Driving the GA08JT17-247

A. Gate Drive Theory of Operation

The SJT is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 21.

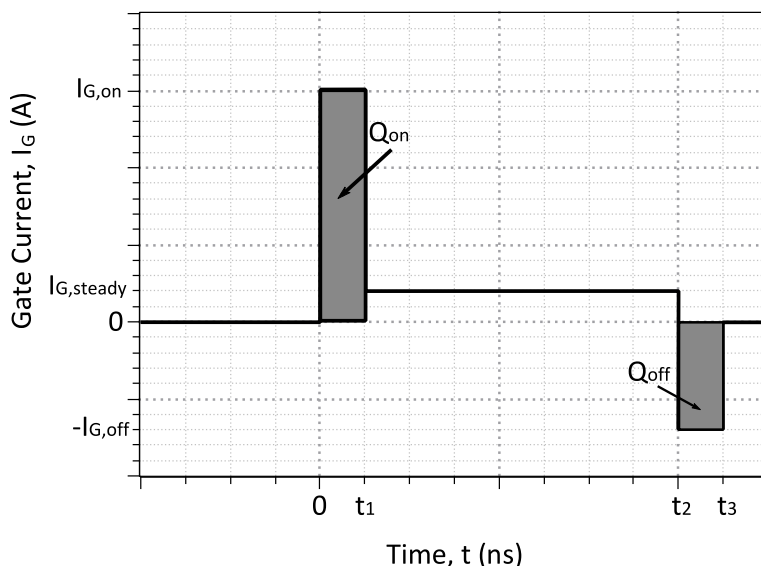


Figure 21: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}/-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G , for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS} , and gate-drain capacitance, C_{GD} , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,on}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the TO-247 package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with $V_{GS} = 0$ V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Steady On-State

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE} , of the device.

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D , DC current gain h_{FE} , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

B. Gate Drive Implementation Examples

Using the IXYS IX2204 Gate Driver

The IXYS IX2204 is a dual output gate drive integrated circuit which can be used to drive an SJT by supplying the required gate drive current I_G in a low-power gate drive solution. This configuration features an external gate capacitor, C_G , which creates the brief current peak $I_{G,on}$ during device turn-on and $I_{G,off}$ during turn-off for fast switching and an external gate resistor $R_{G(EXT)}$ to set the continuous gate current $I_{G,steady}$ required for the device to remain on. This configuration is shown in Figure 22 with further details provided below.

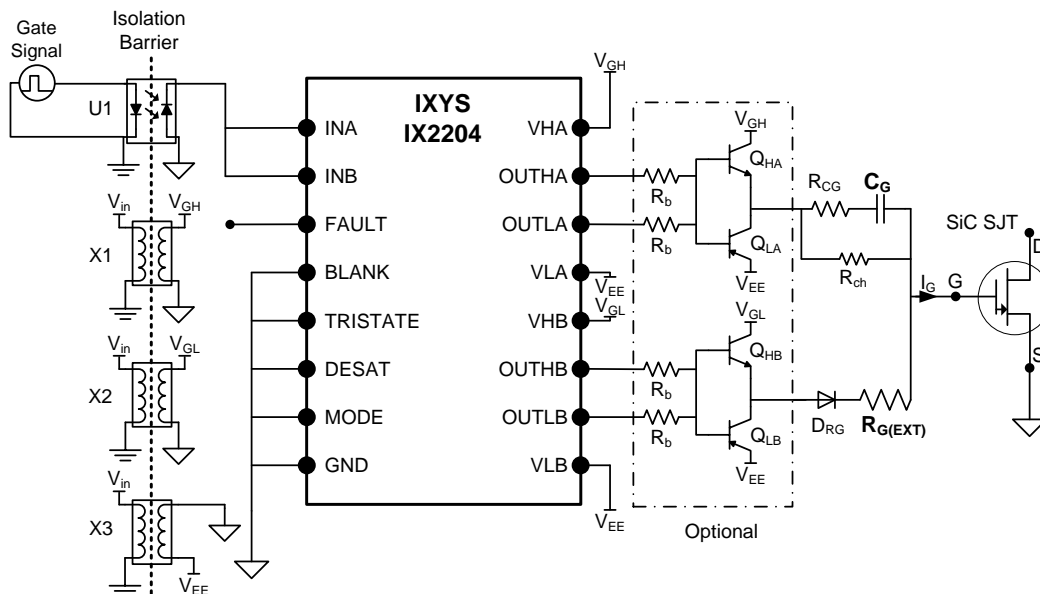


Figure 22: Gate drive configuration using an IXYS IX2204 gate drive IC.

Table 1: Recommended Component List for implementing the IX2204 based Gate Drive for the GA08JT17-247

| Reference | Component | Description | Suggested Part |
|------------------|----------------------------------|--|----------------------|
| $R_{G(EXT)}$ | Gate Resistance, External | 2.0 Ω , 2 W | CRM2512-JW-2R2ELF |
| C_G | Gate Capacitance | 10 nF | C1812C103J1GACTU |
| R_{CG} | Damping Resistor | 1.0 Ω , 0.5 W | ERJ-1TYJ1R0U |
| D_{RG} | Silicon Schottky Diode | 40 V, 2 A | SS24T3G |
| R_b | BJT Base Resistor | 1.0 Ω , 0.5 W | ERJ-1TYJ1R0U |
| Q_{HA}, Q_{HB} | Current Boost NPN | 40 V, 8 A, Silicon NPN BJT | MJD44H11 |
| Q_{LA}, Q_{LB} | Current Boost PNP | 40 V, 8 A, Silicon PNP BJT | MJD45H11 |
| U1 | Signal Isolator | Opto-Isolator –or– Transformer Isolator | ACPL-4800 / ADUM3210 |
| X1 | DC/DC Converter, V_{GH} Supply | $V_{OUT} = +20$ V, $V_{IN} = +12$ V, 2 W, $V_{ISO} = 5.2$ kV | MGJ2D122005SC |
| X2 | DC/DC Converter, V_{GL} Supply | $V_{OUT} = +5$ V, $V_{IN} = +12$ V, 3 W, $V_{ISO} = 3.0$ kV | MEV3S1205SC |
| X3 | DC/DC Converter, V_{EE} Supply | $V_{OUT} = -5$ V, $V_{IN} = +12$ V, 2 W, $V_{ISO} = 5.2$ kV | MGJ2D122005SC |

Voltage Supply Selection

The IX2204 gate drive design requires three supply voltages V_{GH} , V_{GL} , and V_{EE} (listed in Table 2) optionally supplied through DC/DC converters. During device turn-on, V_{GH} charges the external capacitor C_G thereby delivering the narrow width, high current pulse $I_{G,on}$ to the SJT gate and charges the SJT's internal terminal capacitances C_{GD} and C_{GS} . For a given level of parasitic inductance in the gate circuit and SJT package, the rise time of $I_{G,on}$ is controlled by the choice of V_{GH} and C_G . During the steady on-state, V_{GL} in combination with the internal and external gate resistances provides a continuous gate current for the GA08JT17-247 to remain on. The V_{EE} supply sets the gate negative during turn-off and steady off-state for faster switching and to avoid spurious turn-on which may be caused by external circuit noise. The power rating of the voltage supplies should be adequate to meet the gate drive power requirements as determined by

$$P_{min,VGH} = \frac{1}{2} C_G V_{GH}^2 f_{sw}$$

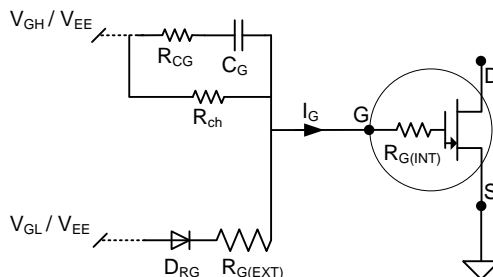
$$P_{min,VEE} = \frac{1}{2} C_G V_{EE}^2 f_{sw}$$

$$P_{min,VGL} = V_{GL} I_{G,steady} D$$

Table 2: IX2204 Gate Drive Example Component List

| Symbol | Parameter | Values | |
|----------|---------------------------------|-----------|---------|
| | | Range | Typical |
| V_{GH} | Supply Voltage, Driver Output A | 15 – 20 | + 20.0 |
| V_{GL} | Supply Voltage, Driver Output B | 5.0 – 7.0 | + 5.0 |
| V_{EE} | Negative Supply Voltage | -10 – GND | - 5.0 |

Gate Capacitor C_G Selection


Figure 23: Primary gate drive circuit passive components with series gate resistance Schottky rectifier.

An external gate capacitor C_G connected directly to the device gate pin delivers the positive current peak $I_{G,on}$ during device turn-on and the negative current peak $I_{G,off}$ during turn-off. A low value resistor R_{CG} is connected in series with C_G to damp potential high-frequency oscillation. A high value resistor R_{ch} in parallel with C_G sets the SJT gate to a defined potential ($-V_{EE}$) during steady off-state.

At device turn-on, C_G is pulled to V_{GH} which produces a transient peak of gate voltage and current. This current peak rapidly charges the internal SJT C_{GS} and C_{GD} capacitances. A Schottky diode, D_{RG} , in series with $R_{G(EXT)}$ blocks any C_G induced current from draining out through $R_{G(EXT)}$ and ensures that all of the charge within C_G flows only into the device gate, allowing for an ultra-fast device turn-on. During steady on-state, a potential of $V_{GH} - V_{GS} = V_{GH} - 3\text{ V}$ is across C_G . When the device is turned off, C_G is pulled to negative V_{EE} and V_{GS} is pulled to a transient peak of $V_{GS,turn-off} = V_{EE} - (V_{GH} - 3\text{ V})$, this induces the negative current peak $I_{G,off}$ out of the gate which discharges the SJT internal capacitances.

External Gate Resistor $R_{G(EXT)}$ Selection

An external gate resistor $R_{G(EXT)}$ connected directly to the SJT gate pin acts to deliver a continuous current $I_{G,steady}$ during steady on-state. The gate current is determined by:

$$I_{G,steady} = \frac{V_{GL} - V_{GS(FWD)} - V_{Sch}}{R_{G(EXT)} + R_{G(INT-ON)}}$$

The on-state gate-source voltage $V_{GS(FWD)}$ can be approximated to 3 V and the Schottky on-state voltage V_{Sch} can be approximated to 0.3 V which simplifies the equation to:

$$I_{G,steady} = \frac{V_{GL} - 3.3V}{R_{G(EXT)} + R_{G(INT-ON)}}$$

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D , DC current gain β , and a 50 % safety margin to avoid operating the device in saturation. $I_{G,steady}$ may also be approximated from the temperature dependent on-state curves of the device in Figures **Error! Reference source not found.** – **Error! Reference source not found.**, provided that a 50 % increase is given.

Table 3: Passive Output Component List

| Symbol | Parameter | Values | | Units |
|-----------------|-------------------------------------|-----------|---------|----------|
| | | Range | Typical | |
| C_G | Gate Capacitor, External | 5 – 20 | 10 | nF |
| R_{CG} | Damping Resistor of Gate Capacitor | 0.5 – 2.0 | 1.0 | Ω |
| R_{ch} | Charging Resistor | 500 – 10k | 1k | Ω |
| $R_{G(EXT)}$ | Gate Resistor, External | 0.4 – 5 | 2 | Ω |
| $R_{G(INT-ON)}$ | Gate Resistance, Internal, On-State | 0.5 – 1.5 | 0.9 | Ω |
| D_{RG} | Schottky Diode of Gate Resistor | -- | -- | |

Optional Gate Current Boost Network

An optional output totem-pole network may be attached to the IX2204 output pins as shown in Figure 22 using either silicon BJTs (shown) or MOSFETs. This configuration allows the IX2204 to directly drive the BJT bases or MOSFET gates and not supply the full peak and steady state gate current entering the SJT gate. The primary gate current delivery device is transferred to the discrete components which have higher power dissipation ratings than the IX2204.

Voltage Supply Isolation

The DC/DC supply voltage converters are suggested to provide isolation at a minimum of twice the working V_{DS} on the SJT transistor during off-state to provide adequate protection to circuitry external to the gate drive circuit. Suggested DC/DC converters have an isolation of 3.0 kV or greater. Alternatively, DC/DC converter galvanic isolation may be bypassed and direct connection of variable voltage supplies may be done, this may be convenient during testing and prototyping but carries risk and is not suggested for extended usage.

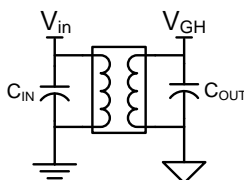


Figure 24: Typical DC/DC converter configuration

Signal Isolation

The gate supply signal is suggested to be isolated to twice the working V_{DS} on the SJT during off-state to provide adequate protection to circuitry external to the gate drive circuit. This may be done using opto or galvanic isolation techniques.

Additional Features

The IX2204 has additional functionality available which is unused in the given configuration. Desaturation detection and fault status monitoring may be implemented by un-grounding the DESAT, BLANK, and TRISTATE pins and configuring them as recommended in the IX2204 datasheet, available from IXYS. Active miller clamping is also available on other gate drive ICs which may also be desired in some SJT switching applications but is not required, refer to specific gate drive IC datasheets for more information.

C. Alternative Gate Drive ICs

dividual product manufacturers.

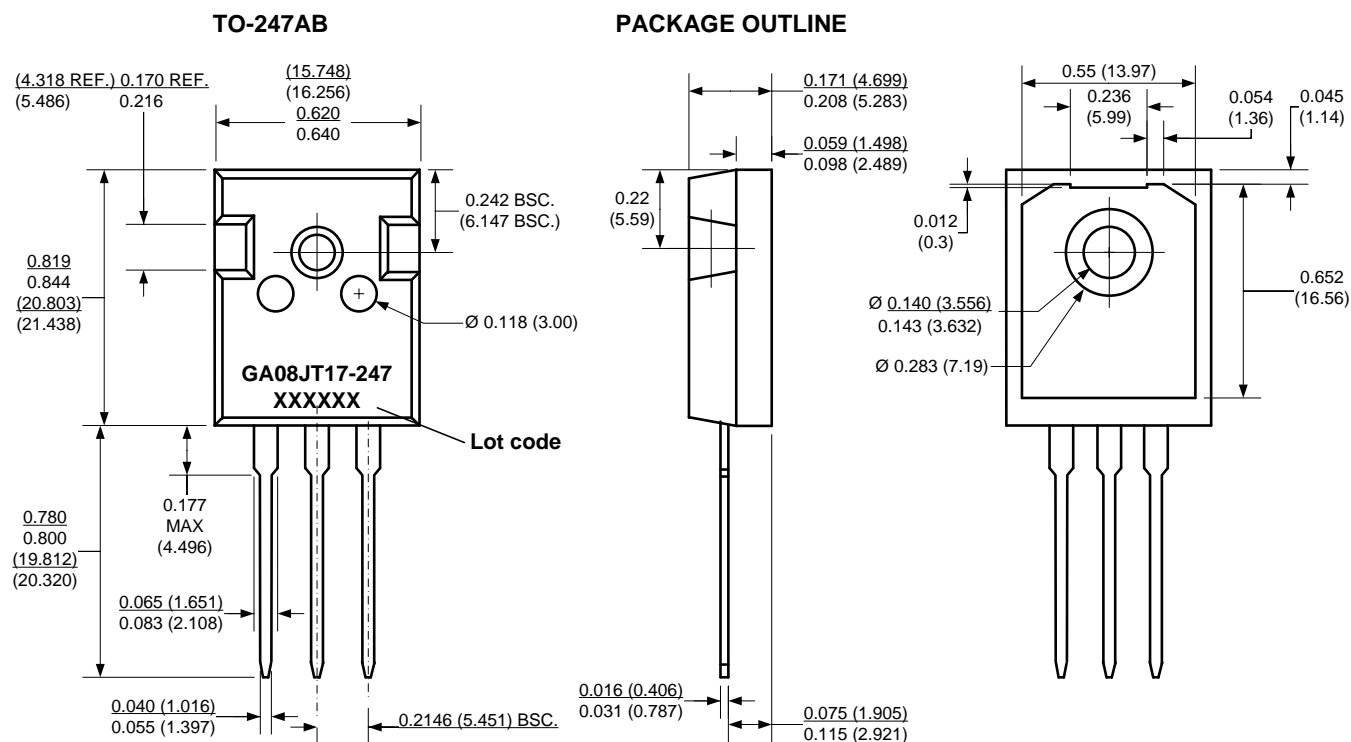
Table 4 features a partial list of alternative gate drive ICs which may be used for driving the GA08JT17-247; specific product information should be obtained from the individual product manufacturers.

Table 4: Additional Commercial Gate Drivers Compatible with GA08JT17-247

| Manufacturer | Part Number | Features | | | | |
|-------------------|-------------|--------------------------|------------------------|--|----------------------|-------------------|
| | | Optical Signal Isolation | Desaturation Detection | Active Miller Gate Clamping ³ | High Side Capability | Number of Outputs |
| Avago Tech. | HCPL-316J | ✓ | ✓ | – | ✓ | 1 |
| Avago Tech. | HCPL-322J | ✓ | ✓ | ✓ | ✓ | 1 |
| IXYS | IXD_604 | – | – | – | ✓ | 2 |
| IXYS | IXD_614 | – | – | – | ✓ | 1 |
| Micrel | MIC4452YN | – | – | – | ✓ | 1 |
| Microsemi | LX4510 | – | – | – | ✓ | 1 |
| Texas Instruments | UCC27322 | – | – | – | ✓ | 1 |

³ – Active Miller Gate Clamping recommended for $V_{EE} = \text{GND}$ switching applications as SJT and/or output BJT secondary gate discharge path.

Package Dimensions:



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

| Revision History | | | |
|------------------|----------|------------------------------------|------------|
| Date | Revision | Comments | Supersedes |
| 2014/08/26 | 8 | Updated Electrical Characteristics | |
| 2014/06/23 | 7 | Updated Electrical Characteristics | |
| 2014/02/06 | 6 | Updated Electrical Characteristics | |
| 2013/12/18 | 5 | Updated Gate Drive Section | |

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SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/sit/GA08JT17-247_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA08JT17-247.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.3                $
*      $Date:      26-AUG-2014        $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA08JT17 NPN
+ IS      3.73E-47
+ ISE     5.50E-27
+ EG      3.2
+ BF      63
+ BR      0.55
+ IKF     200
+ NF      1
+ NE      2.021
+ RB      6.0
+ RBM     0.9
+ IRB     1e-4
+ RE      0.103394007
+ RC      0.151605993
+ CJC     2.77E-10
+ VJC     3.023103628
+ MJC     0.460762158
+ CJE     8.23E-10
+ VJE     2.945448229
+ MJE     0.498044294
+ XTI     3
+ XTB     -0.7
+ TRC1    7.50E-3
+ VCEO    1700
+ ICRATING 8
+ MFG      GeneSiC_Semiconductor
*End of GA08JT17 SPICE Model
```