

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VCX16821FT

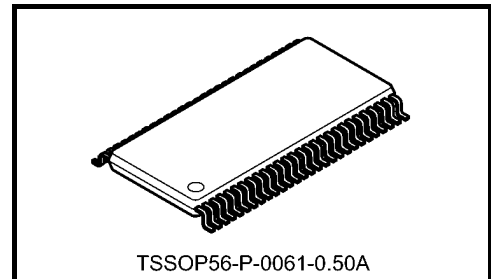
## Low-Voltage 20-Bit D-Type Flip-Flop with 3.6-V Tolerant Inputs and Outputs

The TC74VCX16821FT is a high-performance CMOS 20-bit D-type flip-flop. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CK) transition. When the  $\overline{OE}$  input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.

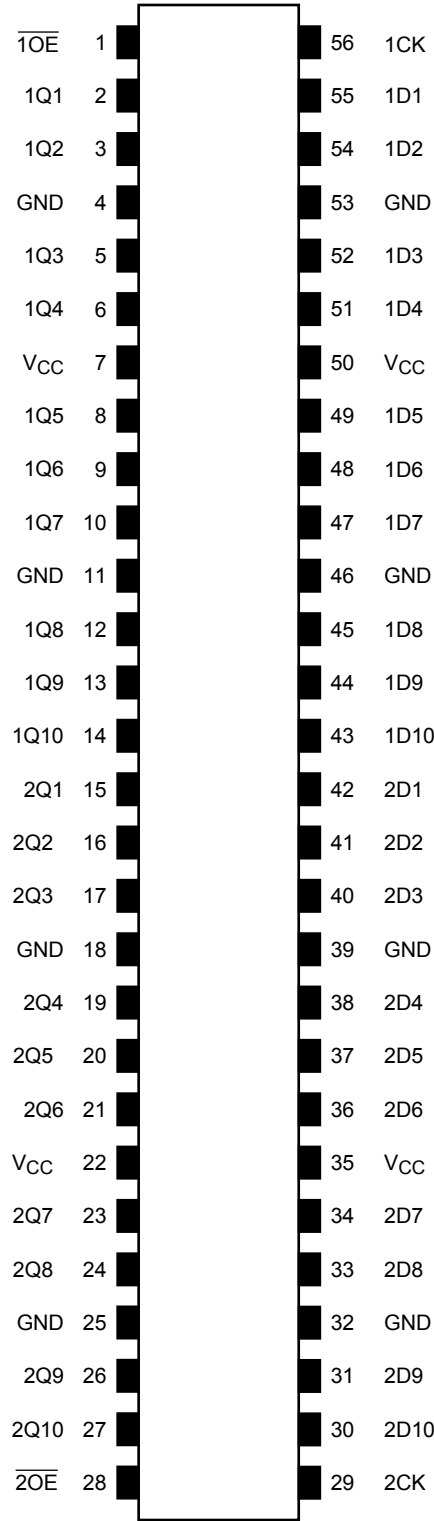


Weight: 0.25 g (typ.)

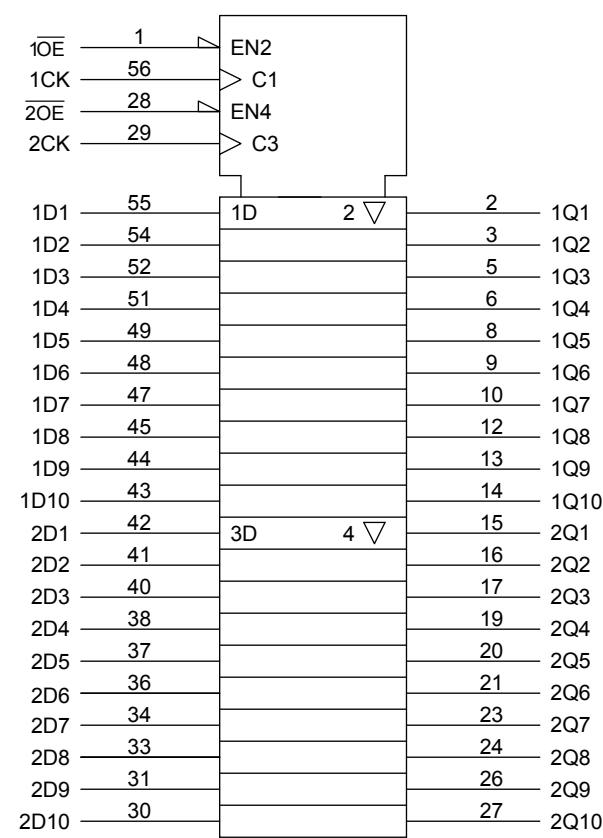
### Features

- Low-voltage operation:  $V_{CC} = 1.8$  to  $3.6$  V
- High-speed operation :  $t_{pd} = 3.5$  ns (max) ( $V_{CC} = 3.0$  to  $3.6$  V)  
:  $t_{pd} = 4.4$  ns (max) ( $V_{CC} = 2.3$  to  $2.7$  V)  
:  $t_{pd} = 8.8$  ns (max) ( $V_{CC} = 1.8$  V)
- Output current:  $I_{OH}/I_{OL} = \pm 24$  mA (min) ( $V_{CC} = 3.0$  V)  
:  $I_{OH}/I_{OL} = \pm 18$  mA (min) ( $V_{CC} = 2.3$  V)  
:  $I_{OH}/I_{OL} = \pm 6$  mA (min) ( $V_{CC} = 1.8$  V)
- Latch-up performance:  $-300$  mA
- ESD performance: Machine model  $\geq \pm 200$  V  
Human body model  $\geq \pm 2000$  V
- Package: TSSOP
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs




Pin Assignment (top view)






IEC Logic Symbol



## Truth Table

Inputs			Outputs
$\overline{1OE}$	1CK	1D1-1D10	1Q1-1Q10
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

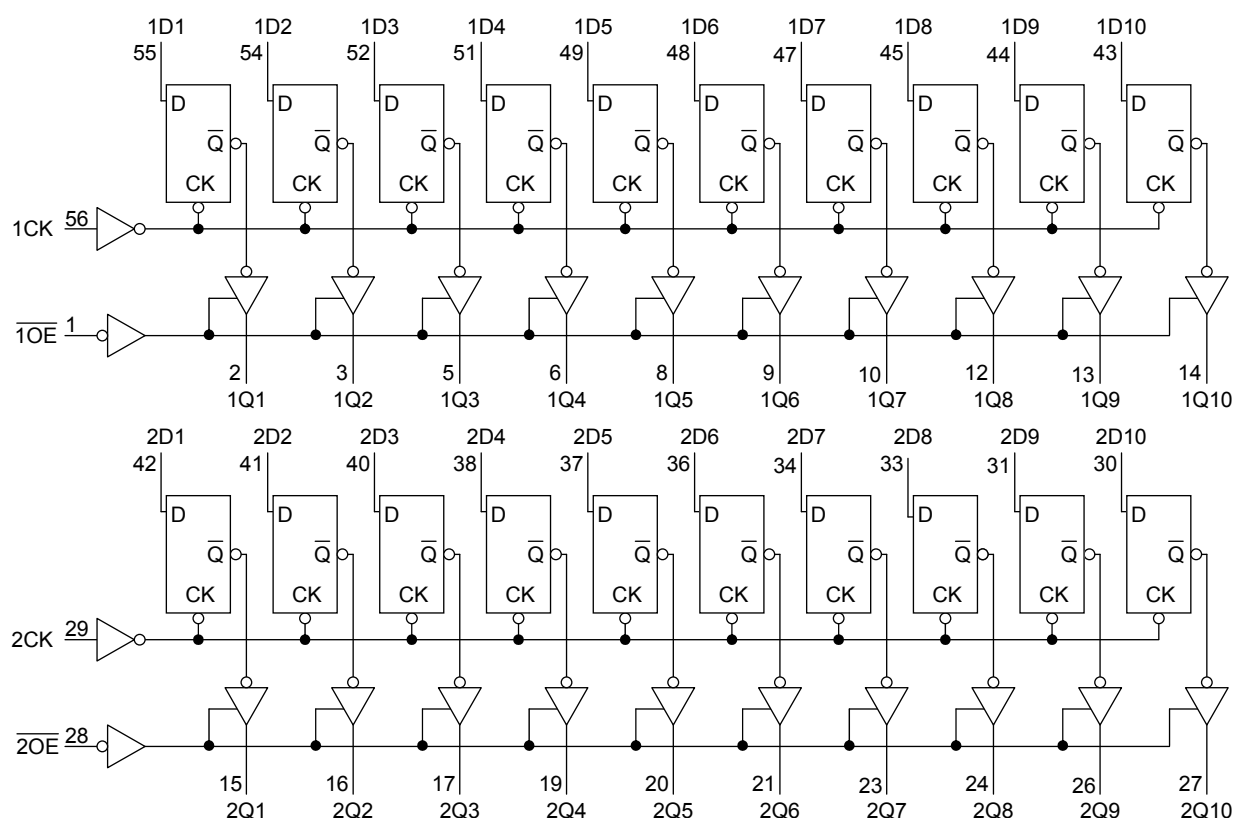
Inputs			Outputs
$\overline{2OE}$	2CK	2D1-2D10	2Q1-2Q10
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

X: Don't care

Z: High impedance

Qn: No change

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 4.6	V
DC input voltage	$V_{IN}$	-0.5 to 4.6	V
DC output voltage	$V_{OUT}$	-0.5 to 4.6 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 4)	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	400	mW
DC $V_{CC}$ /ground current per supply pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	1.8 to 3.6	V
		1.2 to 3.6 (Note 2)	
Input voltage	$V_{IN}$	-0.3 to 3.6	V
Output voltage	$V_{OUT}$	0 to 3.6 (Note 3)	V
		0 to $V_{CC}$ (Note 4)	
Output current	$I_{OH}/I_{OL}$	$\pm 24$ (Note 5)	mA
		$\pm 18$ (Note 6)	
		$\pm 6$ (Note 7)	
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dv$	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5:  $V_{CC} = 3.0$  to 3.6 V

Note 6:  $V_{CC} = 2.3$  to 2.7 V

Note 7:  $V_{CC} = 1.8$  V

Note 8:  $V_{IN} = 0.8$  to 2.0 V,  $V_{CC} = 3.0$  V

## Electrical Characteristics

DC Characteristics ( $T_a = -40$  to  $85^\circ\text{C}$ ,  $2.7\text{ V} < V_{CC} \leq 3.6\text{ V}$ )

Characteristics		Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.7 to 3.6	2.0	—	V
	L-level	V <sub>IL</sub>	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12 mA	2.7	2.2	—	
				I <sub>OH</sub> = -18 mA	3.0	2.4	—	
				I <sub>OH</sub> = -24 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7 to 3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 18 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V	2.7 to 3.6	—	±5.0	μA	
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V	2.7 to 3.6	—	±10.0	μA	
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V	0	—	10.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.7 to 3.6	—	20.0	μA	
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V	2.7 to 3.6	—	±20.0		
Increase in I <sub>CC</sub> per input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V	2.7 to 3.6	—	750		

DC Characteristics ( $T_a = -40$  to  $85^\circ\text{C}$ ,  $2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$ )

Characteristics		Symbol	Test Condition			Min	Max	Unit
					V <sub>CC</sub> (V)			
Input voltage	H-level	V <sub>IH</sub>	—		2.3 to 2.7	1.6	—	V
	L-level	V <sub>IL</sub>	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.3 to 2.7	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -6 mA	2.3	2.0	—	
				I <sub>OH</sub> = -12 mA	2.3	1.8	—	
				I <sub>OH</sub> = -18 mA	2.3	1.7	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.3 to 2.7	—	0.2	
				I <sub>OL</sub> = 12 mA	2.3	—	0.4	
				I <sub>OL</sub> = 18 mA	2.3	—	0.6	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.3 to 2.7	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics ( $T_a = -40$  to  $85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{CC} < 2.3\text{ V}$ )

Characteristics		Symbol	Test Condition			Min	Max	Unit
					V <sub>CC</sub> (V)			
Input voltage	H-level	V <sub>IH</sub>	—		1.8 to 2.3	0.7 × V <sub>CC</sub>	—	V
	L-level	V <sub>IL</sub>	—		1.8 to 2.3	—	0.2 × V <sub>CC</sub>	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −100 μA	1.8	V <sub>CC</sub> − 0.2	—	V
				I <sub>OH</sub> = −6 mA	1.8	1.4	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.8	—	0.2	
				I <sub>OL</sub> = 6 mA	1.8	—	0.3	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		1.8	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V		1.8	—	±20.0	

**AC Characteristics** ( $T_a = -40$  to  $85^\circ\text{C}$ , input:  $t_r = t_f = 2.0$  ns,  $C_L = 30$  pF,  $R_L = 500$   $\Omega$ ) (Note 1)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Maximum clock frequency	$f_{\max}$	Figure 1, Figure 2	1.8	100	—	MHz
			$2.5 \pm 0.2$	200	—	
			$3.3 \pm 0.3$	250	—	
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	Figure 1, Figure 2	1.8	1.5	8.8	ns
			$2.5 \pm 0.2$	1.0	4.4	
			$3.3 \pm 0.3$	0.8	3.5	
3-state output enable time	$t_{pZL}$ $t_{pZH}$	Figure 1, Figure 3	1.8	1.5	9.8	ns
			$2.5 \pm 0.2$	1.0	4.7	
			$3.3 \pm 0.3$	0.8	3.7	
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$	Figure 1, Figure 3	1.8	1.5	7.6	ns
			$2.5 \pm 0.2$	1.0	4.2	
			$3.3 \pm 0.3$	0.8	3.7	
Minimum pulse width (CK)	$t_W$ (H) $t_W$ (L)	Figure 1, Figure 2	1.8	4.0	—	ns
			$2.5 \pm 0.2$	1.5	—	
			$3.3 \pm 0.3$	1.5	—	
Minimum setup time	$t_s$	Figure 1, Figure 2	1.8	2.5	—	ns
			$2.5 \pm 0.2$	1.5	—	
			$3.3 \pm 0.3$	1.5	—	
Minimum hold time	$t_h$	Figure 1, Figure 2	1.8	1.0	—	ns
			$2.5 \pm 0.2$	1.0	—	
			$3.3 \pm 0.3$	1.0	—	
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note 2)	1.8	—	0.5	ns
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: For  $C_L = 50$  pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.

( $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$ )

**Dynamic Switching Characteristics**
**(Ta = 25°C, input:  $t_r = t_f = 2.0$  ns,  $C_L = 30$  pF,  $R_L = 500$   $\Omega$ )**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 1.8 V, V <sub>IL</sub> = 0 V (Note)	1.8	0.25	V
		V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V (Note)	2.5	0.6	
		V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V (Note)	3.3	0.8	
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 1.8 V, V <sub>IL</sub> = 0 V (Note)	1.8	-0.25	V
		V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V (Note)	2.5	-0.6	
		V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V (Note)	3.3	-0.8	
Quiet output minimum dynamic V <sub>OH</sub>	V <sub>OHV</sub>	V <sub>IH</sub> = 1.8 V, V <sub>IL</sub> = 0 V (Note)	1.8	1.5	V
		V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V (Note)	2.5	1.9	
		V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V (Note)	3.3	2.20	

Note: Parameter guaranteed by design.

**Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Input capacitance	C <sub>IN</sub>	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C <sub>O</sub>	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

 Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/20 \text{ (per bit)}$$



AC Test Circuit

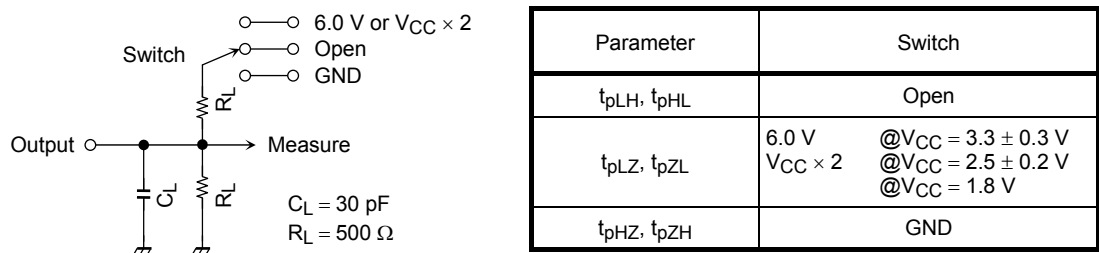


Figure 1

AC Waveform

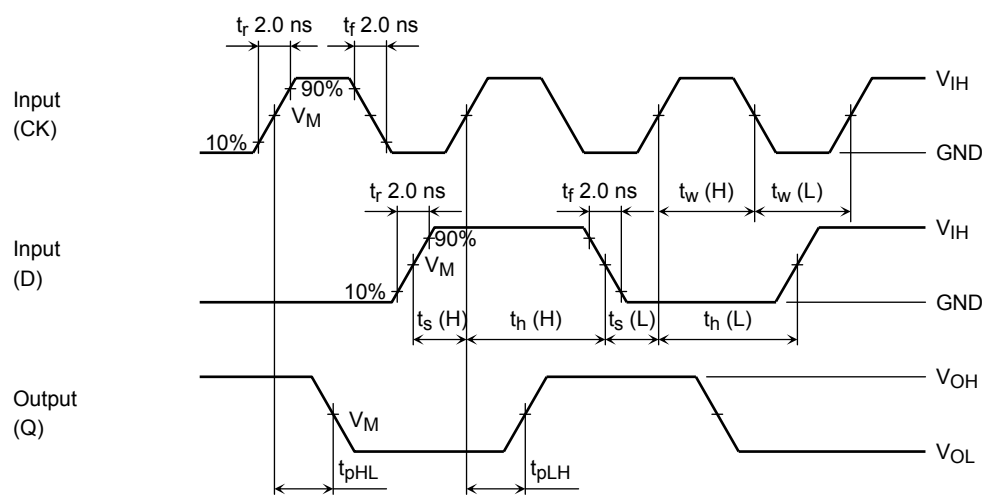
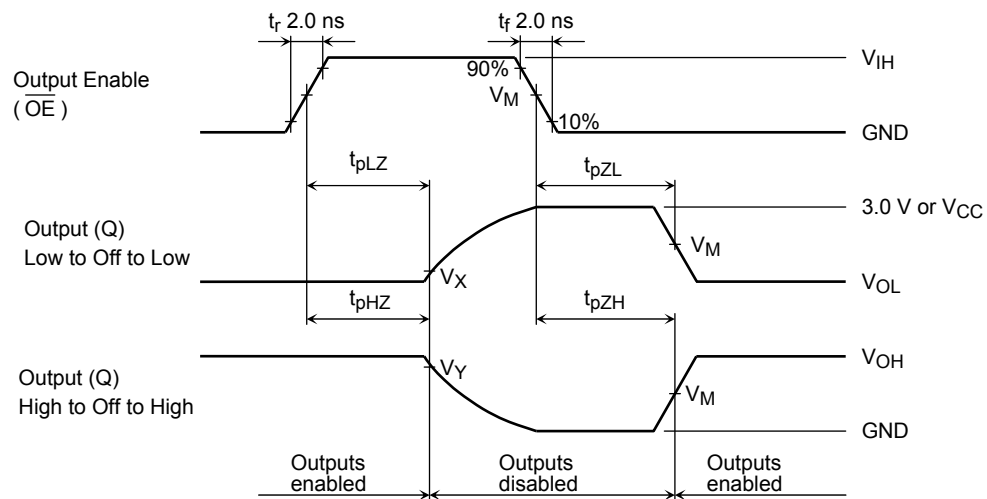


Figure 2  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$

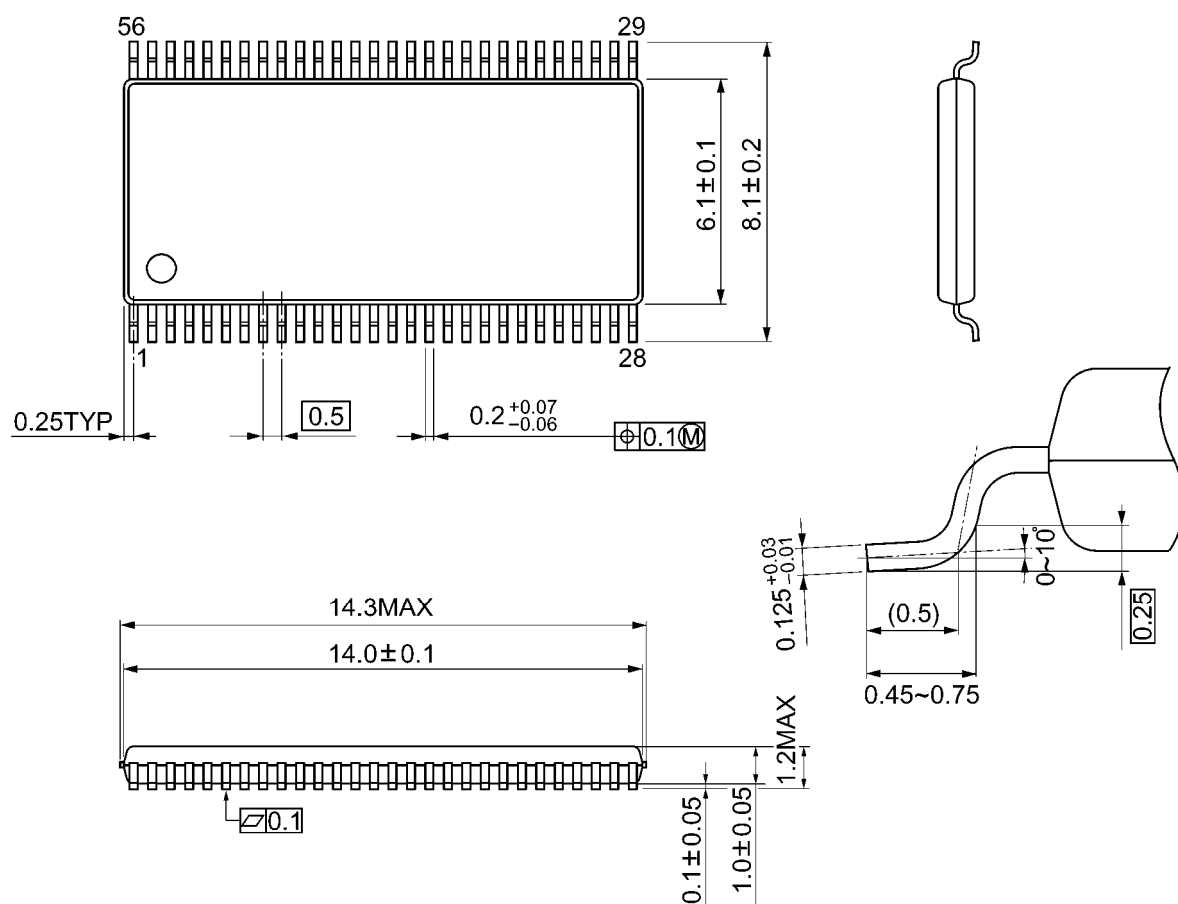

**Figure 3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$** 

Symbol	$V_{CC}$		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
$V_{IH}$	2.7 V	$V_{CC}$	$V_{CC}$
$V_M$	1.5 V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
$V_Y$	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

## Package Dimensions

TSSOP56-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

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