

1 Megabit Static RAM 256K x 4-Bit Revolutionary Pinout

Features

- ☐ High speed access times
Com'l: 10, 12, 15, 17 and 20 ns
Ind'l: 12, 15, 17 and 20 ns
- ☐ Low power operation (typical)
 - PDM41038SA
Active: 400 mW
Standby: 150 mW
 - PDM41038LA
Active: 350 mW
Standby: 100 mW
- ☐ Single +5V ($\pm 10\%$) power supply
- ☐ TTL-compatible inputs and outputs
- ☐ Packages
 - Plastic SOJ (300 mil) - SO 3
 - Plastic SOJ (400 mil) - SO4
 - Plastic TSOP - T

Description

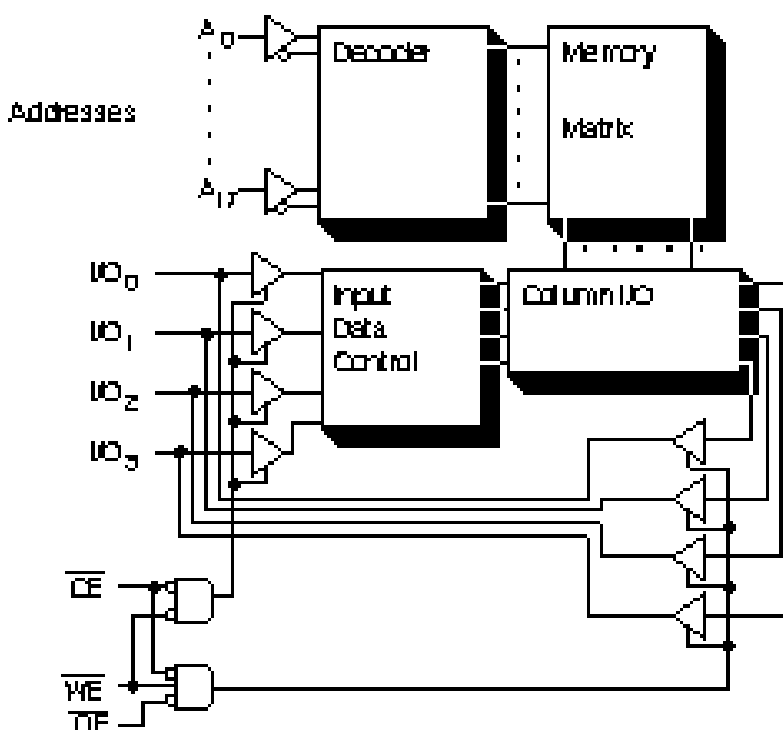
The PDM41038 is a high-performance CMOS static RAM organized as 262,144 x 4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM41038 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41038 comes in two versions, the standard power version PDM41038SA and a low power version the PDM41038LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41038 is available in a 32-pin 300-mil SOJ, 32-pin TSOP, and a 32-pin 400-mil SOJ for surface mount applications in revolutionary pinout.

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Functional Block Diagram



Pin Configuration

TSOP

NC	1	32	A17
A0	2	31	A16
A1	3	30	A15
A2	4	29	A14
A3	5	28	A13
OE	6	27	OE
I/O0	7	26	IO3
V _{CC}	8	25	V _{SS}
V _{SS}	9	24	V _{CC}
I/O1	10	23	IO2
WE	11	22	A12
A4	12	21	A11
A5	13	20	A10
A6	14	19	A9
A7	15	18	A8
NC	16	17	NC

SOJ

NC	1	32	A17
A0	2	31	A16
A1	3	30	A15
A2	4	29	A14
A3	5	28	A13
OE	6	27	OE
IO0	7	26	IO3
V _{CC}	8	25	V _{SS}
V _{SS}	9	24	V _{CC}
IO1	10	23	IO2
WE	11	22	A12
A4	12	21	A11
A5	13	20	A10
A6	14	19	A9
A7	15	18	A8
NC	16	17	NC

Pin Description

Name	Description
A17-A0	Address Inputs
I/O3-I/O0	Data Inputs/Outputs
OE	Output Enable Input
WE	Write Enable Input
CE	Chip Enable Input
NC	No Connect
V _{CC}	Power (+5V)
V _{SS}	Ground

Truth Table⁽¹⁾

OE	WE	CE	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D _{OUT}	Read
X	L	L	D _{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to V _{SS}	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions		PDM41038SA		PDM41038LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	$V_{CC} = \text{MAX.}, V_{IN} = V_{SS} \text{ to } V_{CC}$	Com'l/ Ind.	-5	5	-5	5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{MAX.}, \overline{CE} = V_{IH}, V_{OUT} = V_{SS} \text{ to } V_{CC}$	Com'l/ Ind.	-5	5	-5	5	μA
V_{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = 10 \text{ mA}, V_{CC} = \text{Min.}$		—	0.4 0.5	—	0.4 0.5	V V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$		2.4	—	2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0V$ for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	Power	-10	-12		-15		-17		-20		Unit
			Com'l.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	
I _{CC}	Operating Current CE = V _{IL}	SA	250	230	240	185	195	165	175	155	165	mA
	f = f _{MAX} = 1/t _{RC} V _{CC} = Max. I _{OUT} = 0 mA	LA	230	210	220	165	175	155	165	140	150	mA
I _{SB}	Standby Current CE = V _{IH}	SA	80	70	70	55	55	50	50	45	45	mA
	f = f _{MAX} = 1/t _{RC} V _{CC} = Max.	LA	75	65	65	50	50	45	45	40	40	mA
I _{SB1}	Full Standby Current CE ≥ V _{HC}	SA	20	20	25	10	15	10	15	10	15	mA
	f = 0 V _{CC} = Max., V _{IN} ≥ V _{CC} – 0.2V or ≤ 0.2V	LA	10	10	10	5	10	5	10	5	10	mA

NOTES: All values are maximum guaranteed values.

$V_{LC} \leq 0.2V, V_{HC} \geq V_{CC} - 0.2V$

Capacitance⁽¹⁾ ($T_A = +25^\circ C, f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

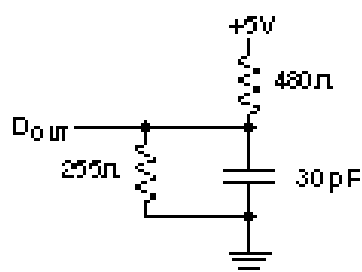


Figure 1. Output Load Equivalent

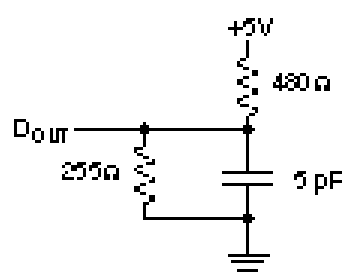


Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE} , t_{LZOE} , t_{HZOE})

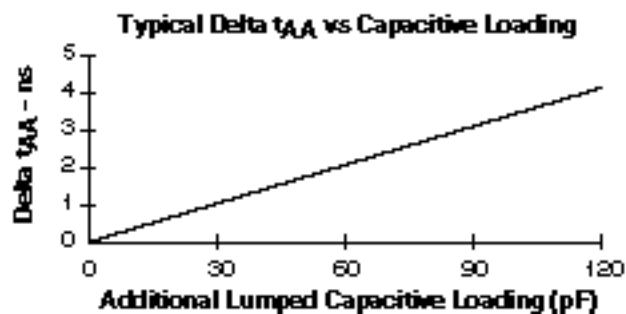
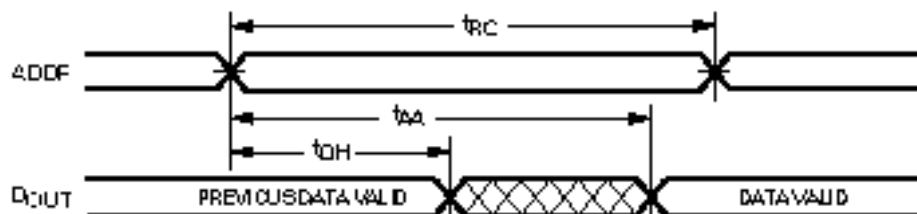
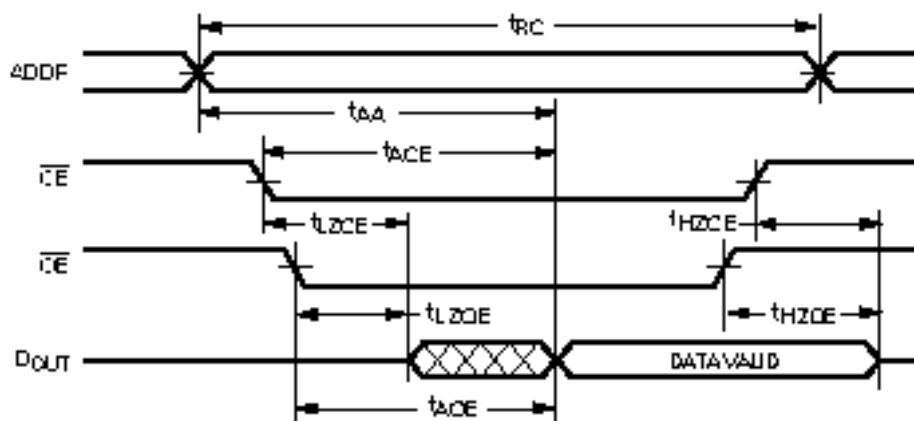


Figure 4.

Read Cycle No. 1(4, 5)



Read Cycle No. 2(2, 4, 6)



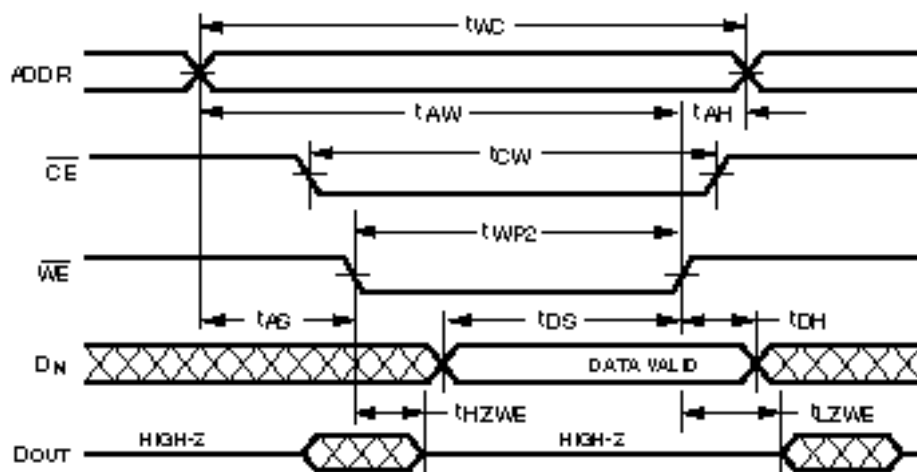
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AC Electrical Characteristics

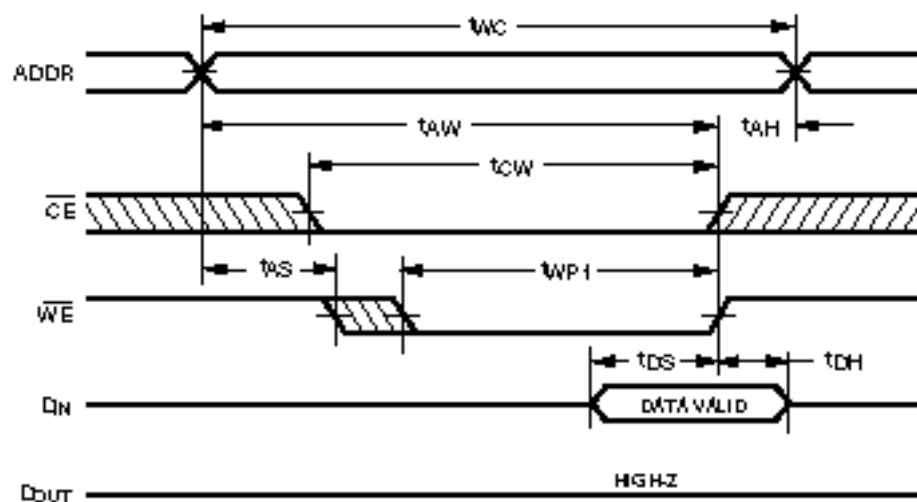
Description		-10 ⁽⁷⁾		-12 ⁽⁷⁾		-15		-17		-20		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t _{RC}	10		12		15		17		20		ns
Address access time	t _{AA}		10		12		15		17		20	ns
Chip enable access time	t _{ACE}		10		12		15		17		20	ns
Output hold from address change	t _{OH}	3		3		3		3		3		ns
Chip enable to output in low Z ^(1,3)	t _{LZCE}	5		5		5		5		5		ns
Chip disable to output in high Z ^(1,2,3)	t _{HZCE}		6		6		7		7		8	ns
Chip enable to power up time ⁽³⁾	t _{PU}	0		0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t _{PD}		10		12		15		17		20	ns
Output enable access time	t _{AOE}		6		6		6		6		6	ns
Output enable to output in low Z ^(1,3)	t _{LZOE}	0		0		0		0		0		ns
Output disable to output in high Z ^(1,3)	t _{HZOE}		6		6		6		6		6	ns

Notes referenced are after Data Retention Table.

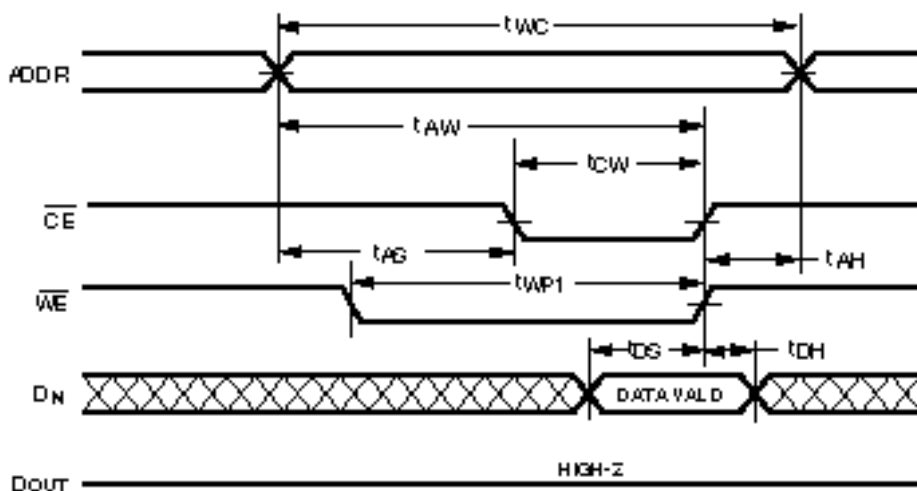
Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Write Enable Controlled)



Write Cycle No. 3 (Chip Enable Controlled)

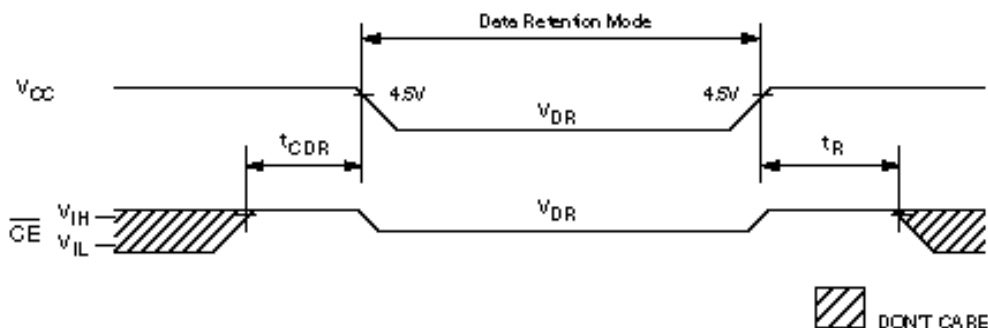


NOTE: Output Enable ($\overline{OE}$) is inactive (high)

AC Electrical Characteristics

Description		-10 ⁽⁷⁾		-12 ⁽⁷⁾		-15		-17		-20		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE cycle time	t _{WC}	10		12		15		17		20		ns
Chip enable active time	t _{CW}	10		10		11		12		13		ns
Address valid to end of write	t _{AW}	10		10		11		12		13		ns
Address setup time	t _{AS}	0		0		0		0		0		ns
Address hold from end of write	t _{AH}	0		0		0		0		0		ns
Write pulse width	t _{WP1}	9		10		11		12		13		ns
Write pulse width	t _{WP2}	10		11		12		13		14		ns
Data setup time	t _{DS}	7		7		7		8		8		ns
Data hold time	t _{DH}	0		0		0		0		0		ns
Write disable to output in low Z ^(1, 3)	t _{LZWE}	0		0		0		0		0		ns
Write enable to output in high ^(1, 3)	t _{HZWE}		7		7		7		8		8	ns

Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{DR}	VCC for Retention Data			2	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	V _{CC} = 2V	—	—	500	μA
			V _{CC} = 3V	—	—	750	μA
t _{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time			t _{RC}	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
3. This parameter is sampled.
4. $\overline{WE}$ is high for a READ cycle.
5. The device is continuously selected. Chip Enable is held in its active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.
7. V_{CC} = 5V ± 5%.

Ordering Information

PDM	xxxxx Device Type	x Power	xx Speed	x Package Type	x Process Temp. Range	
						Blank Commercial (0° to +70°C)
						I Industrial (−40°C to +85°C)
						TSO 32-pin 300-mil Plastic SOJ
						SO 32-pin 400-mil Plastic SOJ
						T 32-pin Plastic TSOP
						10 Commercial Only
						12
						15
						17
						20
						SA Standard Power
						LA Low Power
						41038 256K x 4 Static RAM