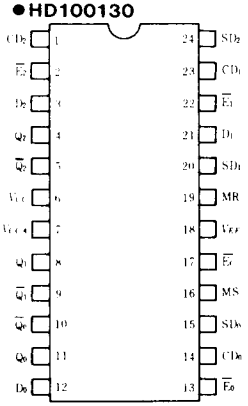
Triple D-type Latches

The HD100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{Ec}$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{En}$), Direct Set (SDn) and Direct Clear (CDn) inputs.
The Q output follows its Data (D) input when both $\overline{En}$ and $\overline{Ec}$ are low. When either $\overline{En}$ or $\overline{Ec}$ or both are high, a latch stores the last valid data present on its Dn input before $\overline{En}$ or $\overline{Ec}$ when high. Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs.
The individual CDn and SDn also override the Enable inputs.

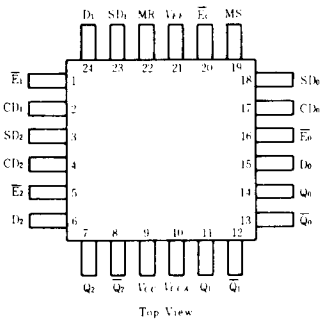
■PIN ARRANGEMENT

●HD100130



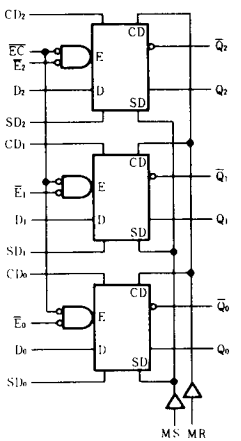
(Top View)

●HD100130F



Top View

■LOGIC DIAGRAM



■TRUTH TABLE

D_n	$\overline{E_n}$	$\overline{Ec}$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
×	H	×	L	L	*
×	×	H	L	L	*
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
* = Ratains data present before $\overline{E}$ positive transition
U = Undefined

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, $V_{CC} = V_{CCA}$ = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		61	88	128	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	D_n input	—	—	350	μA
			CD_n, SD_n input	—	—	530	
			$\overline{E_n}$ input	—	—	240	
			$\overline{Ec}$, MR, MS input	—	—	450	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS ($V_{EE} = -2.2$ to -2.8V, $V_{CC} = V_{CCA} = 2.0$V)

● HD100130

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	D_n input	0.45	1.20	0.50	0.85	1.20	0.50	1.35	ns
			CD_n, SD_n, E_n input	0.65	1.40	0.65	1.10	1.40	0.65	1.45	
			$\overline{E_C}$ input	0.75	1.15	0.75	1.15	1.45	0.75	1.50	
			MS, MR input	1.05	2.20	1.10	1.40	2.20	1.10	2.20	
Transition Time	t_{TLH}, t_{THL}			0.30	1.50	0.30	0.70	1.50	0.30	1.50	ns
Setup Time	t_{SU}		D_n	0.70	—	0.70	—	—	0.80	—	ns
			CD_n, SD_n (Release Time)	1.10	—	1.10	—	—	1.10	—	
			MR, MS (Release Time)	1.90	—	1.90	—	—	1.90	—	
Hold Time	t_h		D_n	0.20	—	0.20	—	—	0.20	—	ns
Pulse Width	$t_{W(L)}$		$\overline{E_n}$, $\overline{E_C}$	1.20	—	1.20	—	—	1.20	—	ns
	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.35	—	1.35	—	—	1.35	—	

● HD100130F

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	D_n input	0.50	1.15	0.50	0.95	1.15	0.50	1.25	ns
			CD_n, SD_n, E_n input	0.60	1.45	0.60	1.10	1.45	0.60	1.55	
			$\overline{E_C}$ input	0.75	1.55	0.75	1.20	1.55	0.75	1.55	
			MS, MR input	1.10	2.20	1.10	1.40	2.20	1.10	2.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.30	0.40	0.60	1.30	0.40	1.30	ns
Setup Time	t_{SU}		D_n	0.65	—	0.60	—	—	0.60	—	ns
			CD_n, SD_n (Release Time)	1.00		1.00	—	—	1.00	—	
			MR, MS (Release Time)	1.80	—	1.80	—	—	1.80	—	
Hold Time	t_h		D_n	0.20	—	0.20	—	—	0.20	—	ns
Pulse Width	$t_{W(L)}$		$\overline{E_n}$, $\overline{E_C}$	1.00	—	1.00	—	—	1.00	—	ns
	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.15	—	1.15	—	—	1.15	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

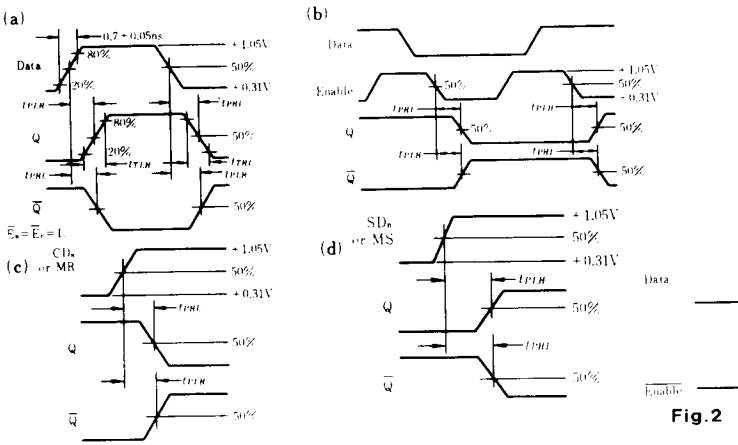


Fig.1 Propagation Delay Time

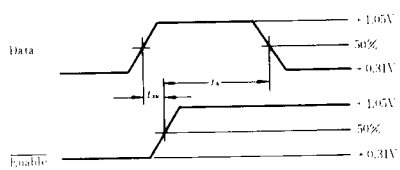


Fig.2 Set-up, and Hold Time