International
IOR Rectifier

# IR213(6,62,63,65,66,67,68)(J&S) & PbF

**Data Sheet No. PD60166 revU**

## IR2136/IR21362/IR21363/IR21365/ IR21366/IR21367/IR21368 (J&S) & (PbF)

## 3-PHASE BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V (IR2136/ IR21368), 11.5 V to 20 V (IR21362D), or 12 V to 20 V (IR21363/IR21365/IR21366/IR21367)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Low side output out of phase with inputs. High side outputs out of phase (IR213(6,63, 65, 66, 67, 68)), or in phase (IR21362) with inputs
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

### Packages

**28-Lead SOIC**

**28-Lead PDIP**

**44-Lead PLCC w/o 12 Leads**

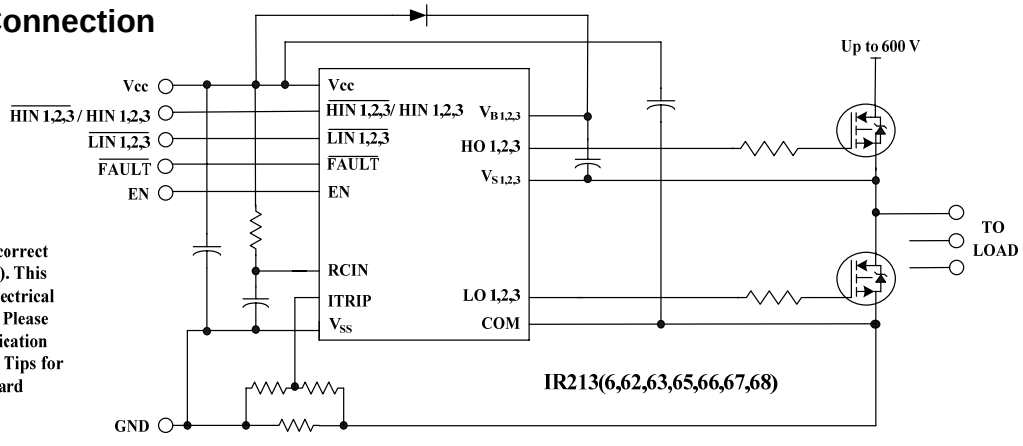
### Description

The IR2136x (J&S) are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

**Feature Comparison: IR213(6,62,63,65,66,67,68)**

| Part | IR2136 | IR21362 | IR21363 | IR21365 | IR21366 | IR21367 | IR21368 |
|---|---|---|---|---|---|---|---|
| Input Logic | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ | HIN, $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$, $\overline{\text{LIN}}$ |
| Ton (typ.) | 400 ns | 400 ns | 400 ns | 400 ns | 250 ns | 250 ns | 400 ns |
| Toff (typ.) | 380ns | 380 ns | 380 ns | 380 ns | 180 ns | 180 ns | 380 ns |
| $V_{IH}$ (typ.) | 2.7 V | 2.7 V | 2.7 V | 2.7 V | 2.0 V | 2.0 V | 2.0 V |
| $V_{IL}$ (typ.) | 1.7 V | 1.7 V | 1.7 V | 1.7 V | 1.3 V | 1.3 V | 1.3 V |
| Vitrip+ | 0.46 V | 0.46 V | 0.46 V | 4.3 V | 0.46 V | 4.3 V | 4.3 V |
| UVCC/BS+ | 8.9 V | 10.4 V | 11.2 V | 11.2 V | 11.2 V | 11.2 V | 8.9 V |
| UVCC/BS- | 8.2 V | 9.4 V | 11.0 V | 11.0 V | 11.0 V | 11.0 V | 8.2 V |

### Typical Connection




(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_S$ | High side offset voltage | | $V_{B\,1,2,3}$ - 25 | $V_{B\,1,2,3}$ + 0.3 | V |
| $V_B$ | High side floating supply voltage | | -0.3 | 625 | |
| $V_{HO}$ | High side floating output voltage | | $V_{S1,2,3}$ - 0.3 | $V_{B\,1,2,3}$ + 0.3 | |
| $V_{CC}$ | Low side and logic fixed supply voltage | | -0.3 | 25 | |
| $V_{SS}$ | Logic ground | | $V_{CC}$ - 25 | $V_{CC}$ + 0.3 | |
| $V_{LO1,2,3}$ | Low side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Input voltage LIN, HIN, ITRIP, EN | | $V_{SS}$ -0.3 | Lower of ($V_{SS}$ + 15) or $V_{CC}$ + 0.3) | |
| $V_{RCIN}$ | RCIN input voltage | | $V_{SS}$ -0.3 | $V_{CC}$ + 0.3 | |
| $V_{FLT}$ | $\overline{\text{FAULT}}$ output voltage | | $V_{SS}$ -0.3 | $V_{CC}$ + 0.3 | |
| dV/dt | Allowable offset voltage slew rate | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25$ °C | (28 lead PDIP) | — | 1.5 | W |
| | | (28 lead SOIC) | — | 1.6 | |
| | | (44 lead PLCC) | — | 2.0 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (28 lead PDIP) | — | 83 | °C/W |
| | | (28 lead SOIC) | — | 78 | |
| | | (44 lead PLCC) | — | 63 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

## Recommended Operating Conditions

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The $V_S$ offset ratings are tested with all supplies biased at a 15 V differential.

| Symbol | Definition | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{B1,2,3}$ | High side floating supply voltage | IR213(6,68) | $V_{S1,2,3}$ +10 | $V_{S1,2,3}$ + 20 | V |
| | | IR21362 | $V_{S1,2,3}$ +11.5 | $V_{S1,2,3}$ + 20 | |
| | | IR213(6,63,65,66,67) | $V_{S1,2,3}$ +12 | $V_{S1,2,3}$ + 20 | |
| $V_{S\,1,2,3}$ | High side floating supply offset voltage | | Note 1 | 600 | |
| $V_{HO\,1,2,3}$ | High side output voltage | | $V_{S1,2,3}$ | $V_{B1,2,3}$ | |
| $V_{LO1,2,3}$ | Low side output voltage | | 0 | $V_{CC}$ | |
| $V_{CC}$ | Low side and logic fixed supply voltage | IR213(6,68) | 10 | 20 | |
| | | IR21362 | 11.5 | 20 | |
| | | IR213(6,63,65,66,67) | 12 | 20 | |
| $V_{SS}$ | Logic ground | | -5 | 5 | |
| $V_{FLT}$ | $\overline{\text{FAULT}}$ output voltage | | $V_{SS}$ | $V_{CC}$ | |
| $V_{RCIN}$ | RCIN input voltage | | $V_{SS}$ | $V_{CC}$ | |

**Note 1:** Logic operational for $V_S$ of (COM - 5 V) to (COM + 600 V). Logic state held for $V_S$ of (COM - 5 V) to (COM – $V_{BS}$). (Please refer to the Design Tip DT97-3 for more details).

**Note 2:** All input pins and the ITRIP and EN pins are internally clamped with a 5.2 V zener diode.

## Recommended Operating Conditions - (Continued)

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The $V_S$ offset ratings are tested with all supplies biased at a 15 V differential.

| Symbol | Definition | Min | Max | Units |
|---|---|---|---|---|
| $V_{ITRIP}$ | ITRIP input voltage | $V_{SS}$ | $V_{SS}$ + 5 | V |
| $V_{IN}$ | Logic input voltage $\overline{LIN}$, $\overline{HIN}$ (IR213(6,63,65,66,67,68)), HIN (IR21362), EN | $V_{SS}$ | $V_{SS}$ + 5 | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

**Note 2:** All input pins and the ITRIP and EN pins are internally clamped with a 5.2 V zener diode.

## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$,$V_{BS1,2,3}$) = 15 V unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to $V_{SS}$ and are applicable to all six channels ($\overline{HIN1,2,3}$ and $\overline{LIN1,2,3}$). The $V_O$ and $I_O$ parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

| Symbol | Definition | | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR213(6,63,65) Logic "1" input voltage HIN1,2,3 IR21362 | | 3.0 | — | — | V | |
| | Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR213(66,67,68) | | 2.5 | — | — | | |
| $V_{IL}$ | Logic "1" input Voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR213(6,63,65) Logic "0" input voltage HIN1,2,3 IR21362 | | — | — | 0.8 | | |
| | Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ IR213(66,67,68) | | | | | | |
| $V_{EN,TH+}$ | Enable positive going threshold | | — | — | 3 | | |
| $V_{EN,TH-}$ | Enable negative going threshold | | 0.8 | — | — | | |
| $V_{IT,TH+}$ | ITRIP positive going threshold | IR2136(2)(3)(6) | 0.37 | 0.46 | 0.55 | | |
| | | IR21365(7)(8) | 3.85 | 4.30 | 4.75 | | |
| $V_{IT,HYS}$ | ITRIP input hysteresis | IR2136(2)(3)(6) | — | 0.07 | — | | |
| | | IR21365(7)(8) | — | .15 | — | | |
| $V_{RCIN, TH+}$ | RCIN positive going threshold | | — | 8 | — | | |
| $V_{RCIN, HYS}$ | RCIN input hysteresis | | — | 3 | — | | |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | | — | 0.9 | 1.4 | | Io = 20 mA |
| $V_{OL}$ | Low level output voltage, $V_O$ | | — | 0.4 | 0.6 | | |
| $V_{CCUV+}$ $V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | IR2136(8) | 8.0 | 8.9 | 9.8 | | |
| | | IR21362 | 9.6 | 10.4 | 11.2 | | |
| | | IR21363(5)(6)(7) | 10.6 | 11.1 | 11.6 | | |

## Static Electrical Characteristics - (Continued)

$V_{BIAS}$ ($V_{CC}$,$V_{BS1,2,3}$) = 15 V unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to $V_{SS}$ and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The $V_O$ and $I_O$ parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

| Symbol | Definition | | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{CCUV-}$ $V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | IR2136(8) | 7.4 | 8.2 | 9.0 | V | |
| | | IR21362 | 8.6 | 9.4 | 10.2 | | |
| | | IR2136(3,5,6,7) | 10.4 | 10.9 | 11.4 | | |
| $V_{CCUVH}$ $V_{BSUVH}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage lockout hysteresis | IR2136 | 0.3 | 0.7 | — | | |
| | | IR21362 | 0.5 | 1.0 | — | | |
| | | IR2136(3,5) | — | 0.2 | — | | |
| $I_{LK}$ | Offset supply leakage current | | — | — | 50 | µA | $V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | | — | 70 | 120 | | $V_{IN}$ = 0 V or 5 V |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | | — | 1.6 | 2.3 | mA | |
| $V_{IN,CLAMP}$ | Input clamp voltage (HIN, LIN, ITRIP and EN) | | 4.9 | 5.2 | 5.5 | V | $I_{IN}$ =100 µA |
| $I_{LIN+}$ | Input bias current (LOUT = HI) | IR2136(2,3,5) | — | 200 | 300 | µA | $V_{LIN}$ = 5 V |
| | | IR2136(6,7,8) | — | 30 | 100 | | |
| $I_{LIN-}$ | Input bias current (LOUT = LO) | IR2136(2,3,5) | — | 100 | 220 | | $V_{LIN}$ = 0 V |
| | | IR2136(6,7,8) | — | 0 | 1 | | |
| $I_{HIN+}$ | Input bias current (HOUT = HI) | IR2136(3,5) | — | 200 | 300 | | $V_{HIN}$ = 5 V |
| | | IR21362 | — | 30 | 100 | | |
| | | IR2136(6,7,8) | — | 30 | 100 | | |
| $I_{HIN-}$ | Input bias current (HOUT = LO) | IR2136(3,5) | — | 100 | 220 | | $V_{HIN}$ = 0 V |
| | | IR2136(2,6,7,8) | — | 0 | 1 | | |
| $I_{ITRIP+}$ | “High” ITRIP input bias current | | — | 30 | 100 | | $V_{ITRIP}$ = 5 V |
| $I_{ITRIP-}$ | “Low” ITRIP input bias current | | — | 0 | 1 | | $V_{ITRIP}$ = 0 V |
| $I_{EN+}$ | “High” ENABLE input bias current | | — | 30 | 100 | | $V_{ENABLE}$ = 5 V |
| $I_{EN-}$ | “Low” ENABLE input bias current | | — | 0 | 1 | | $V_{ENABLE}$ =0 V |
| $I_{RCIN}$ | RCIN input bias current | | — | 0 | 1 | | Vrcin= 0 V or 15 V |
| $I_{O+}$ | Output high short circuit pulsed current | | 120 | 200 | — | mA | Vo =0 V, PW ≤10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | | 250 | 350 | — | | Vo =15 V, PW ≤10 µs |
| $R_{on\_RCIN}$ | RCIN low on resistance | | — | 50 | 100 | Ω | |
| $R_{on\_FAULT}$ | $\overline{FAULT}$ low on resistance | | — | 50 | 100 | | |

## Dynamic Electrical Characteristics

$V_{CC}$ = $V_{BS}$ = $V_{BIAS}$ = 15 V, $V_{S1,2,3}$ = $V_{SS}$ = COM, $T_A$ = 25 °C and CL = 1000 pF unless otherwise specified.

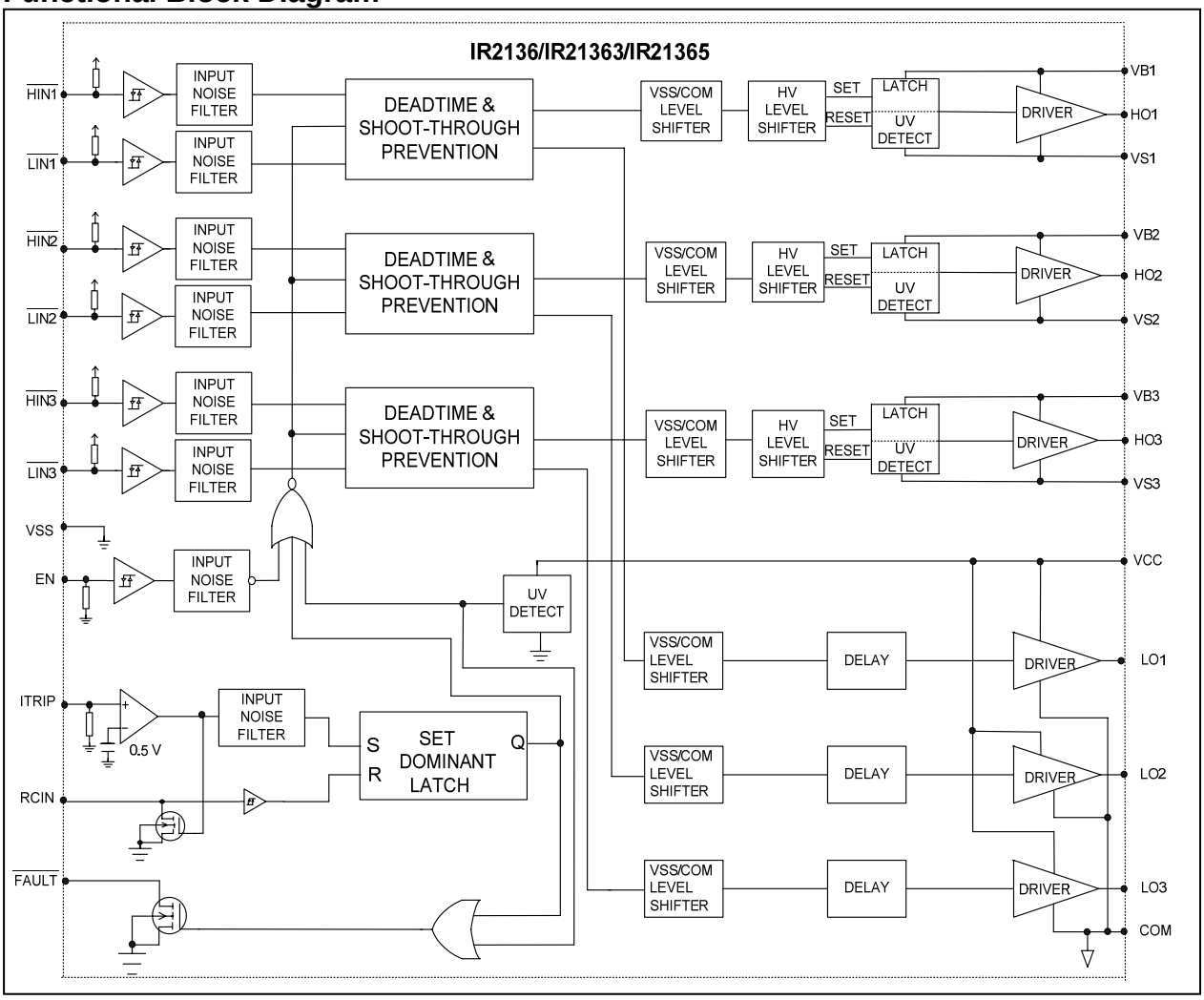
| Symbol | Definition | | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | IR2136(2,3,5,8) | 300 | 425 | 550 | ns | $V_{IN}$ = 0 V & 5 V |
| | | IR2136(6,7) | — | 250 | — | | |
| $t_{off}$ | Turn-off propagation delay | IR2136(2,3,5,8) | 250 | 400 | 550 | | |
| | | IR2136(6,7) | — | 180 | — | | |
| $t_r$ | Turn-on rise time | | — | 125 | 190 | | |
| $t_f$ | Turn-off fall time | | — | 50 | 75 | | |
| $t_{EN}$ | ENABLE low to output shutdown propagation delay | IR2136(2,3,5,8) | 300 | 450 | 600 | | $V_{IN}$, $V_{EN}$ = 0 V or 5 V |
| | | IR2136(6,7) | 100 | 250 | 400 | | |
| $t_{ITRIP}$ | ITRIP to output shutdown propagation delay | | 500 | 750 | 1000 | | $V_{ITRIP}$ = 5 V |
| $t_{bl}$ | ITRIP blanking time | | 100 | 150 | — | | $V_{IN}$ = 0 V or 5 V $V_{ITRIP}$ = 5 V |
| $t_{FLT}$ | ITRIP to $\overline{FAULT}$ propagation delay | | 400 | 600 | 800 | | |
| $t_{FILIN}$ | Input filter time (HIN, LIN) (IR213(6,62,63,65,68) only) | | 100 | 200 | — | | $V_{IN}$ = 0 V & 5 V |
| $t_{FLTCLR}$ | FAULT clear time RCIN: R = 2 MΩ, C = 1 nF | | 1.3 | 1.65 | 2 | ms | $V_{IN}$ = 0 V or 5 V $V_{ITRIP}$ = 0 V |
| DT | Deadtime | | 220 | 290 | 360 | ns | $V_{IN}$ = 0 V & 5 V |
| MT | Matching delay ON and OFF | | — | 40 | 75 | | External dead time >400 ns |
| MDT | Matching delay, max ($t_{on}$, $t_{off}$) – min ($t_{on}$, $t_{off}$), ($t_{on}$, $t_{off}$ are applicable to all 3 channels) | | — | 25 | 70 | | |
| PM | Output pulse width matching (pwin-pwout) (Fig.2) | | — | 40 | 75 | | |

**Note:** For high side PWM, HIN pulse width must be ≥ 1 µs.

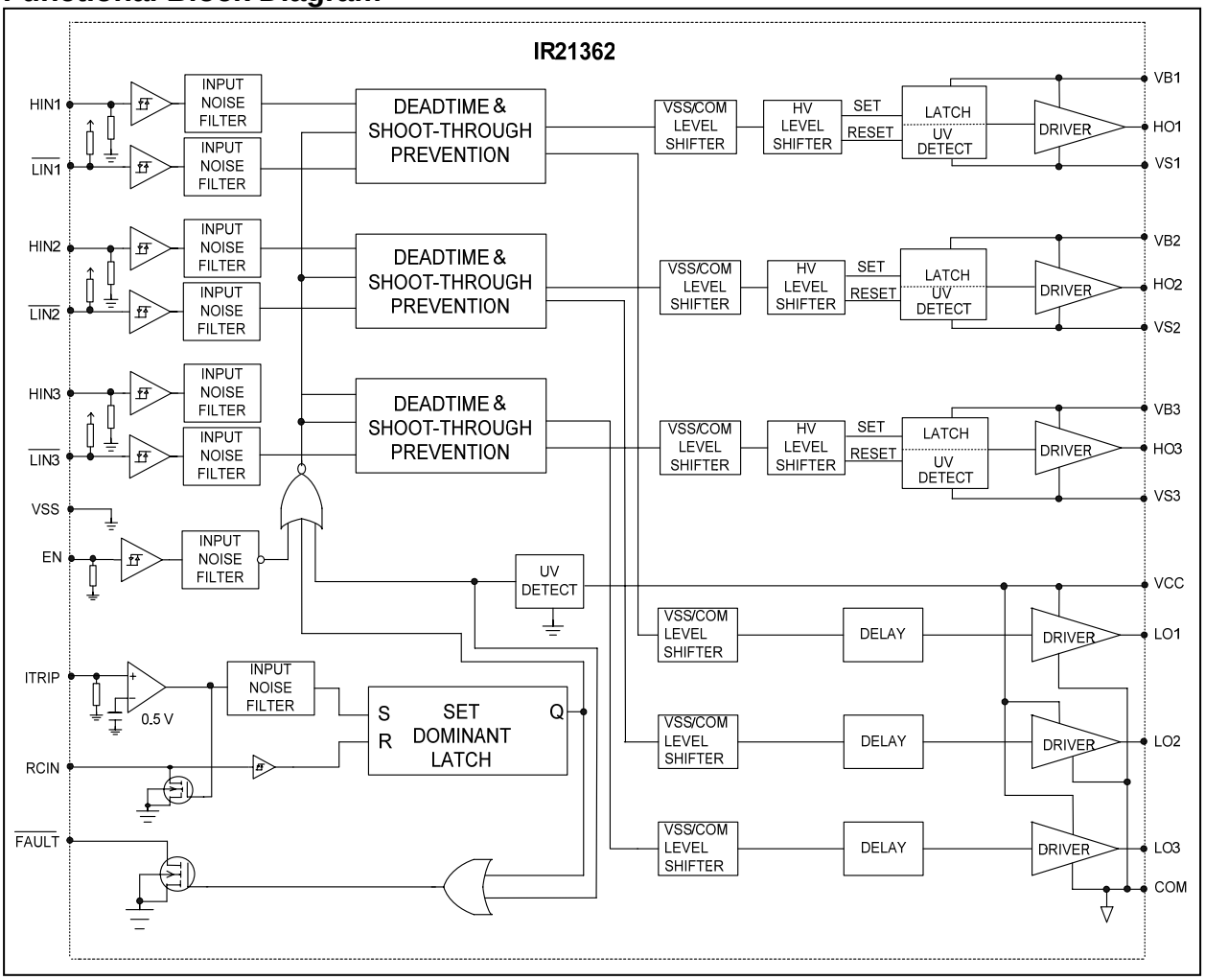
| VCC | VBS | ITRIP | ENABLE | FAULT | LO1,2,3 | HO1,2,3 |
|---|---|---|---|---|---|---|
| <UVCC | X | X | X | 0 (note 1) | 0 | 0 |
| 15 V | <UVBS | 0 V | 5 V | high imp | LIN1,2,3 | 0 |
| 15 V | 15 V | 0 V | 5 V | high imp | LIN1,2,3 | HIN1,2,3 |
| 15 V | 15 V | >$V_{ITRIP}$ | 5 V | 0 (note 2) | 0 | 0 |
| 15 V | 15 V | 0 V | 0 V | high imp | 0 | 0 |

**Note 1:** A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
**Note 2:** UVCC is not latched, when $V_{CC}$ > $UV_{CC}$, FAULT returns to high impedance.
**Note 3**: When ITRIP < $V_{ITRIP}$, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ $V_{CC}$ = 15 V).

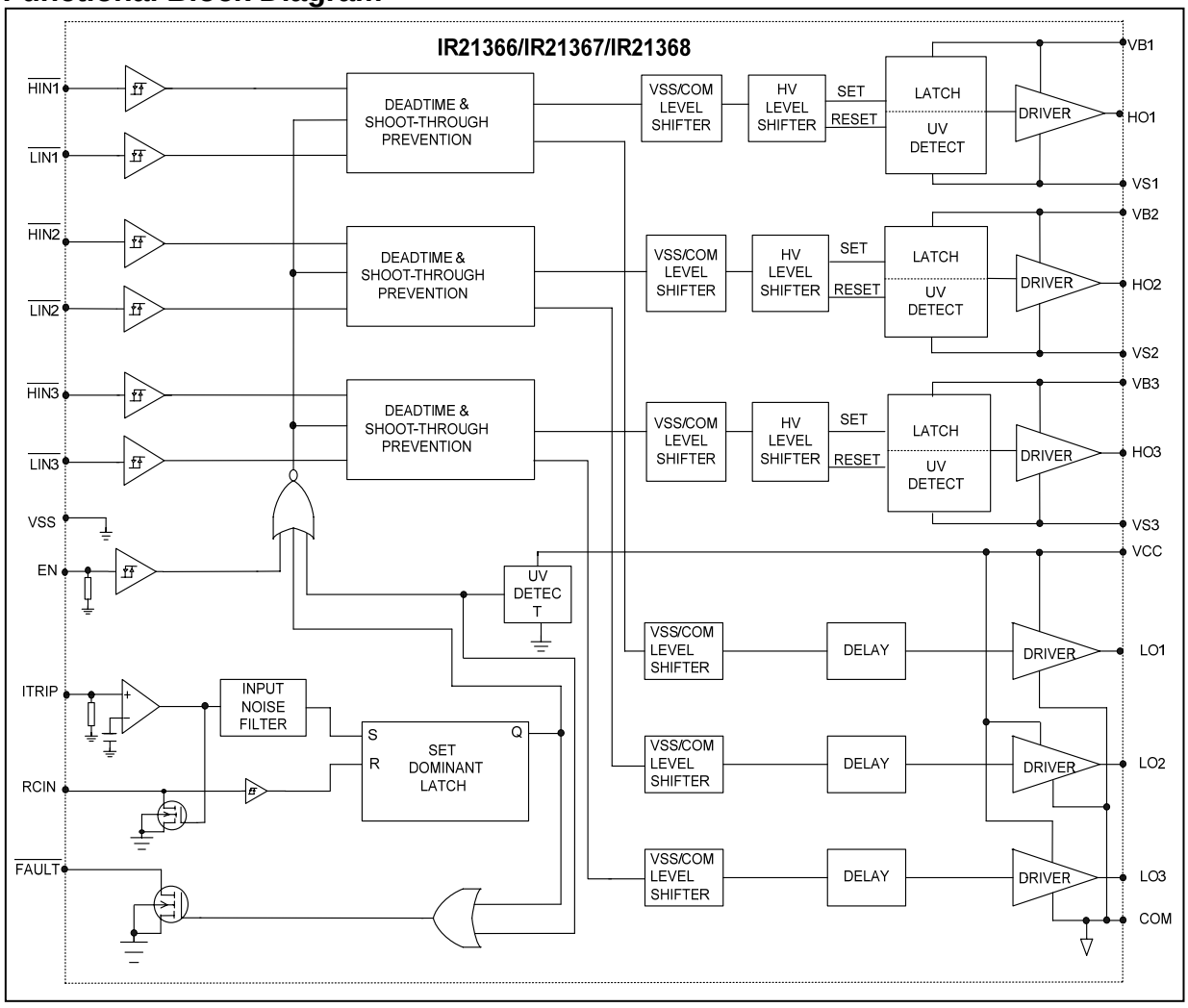
## Functional Block Diagram



## Functional Block Diagram



## Functional Block Diagram

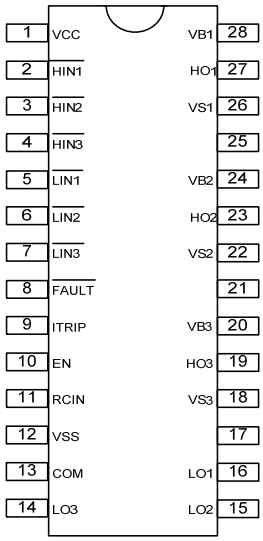


## Lead Definitions

| Symbol | Description |
|---|---|
| $V_{CC}$ | Low side and logic fixed supply |
| $V_{SS}$ | Logic ground |
| $\overline{HIN1,2,3}$<br>HIN1,2,3 | Logic inputs for high side gate driver outputs (HO1,2,3), out of phase [IR213(6,63,65,66,67,68)]<br>Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362) |
| $\overline{LIN1,2,3}$ | Logic input for low side gate driver outputs (LO1,2,3), out of phase |
| FAULT | Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output |
| EN | Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on FAULT and not latched |
| ITRIP | Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time $T_{FLTCLR}$, then automatically becomes inactive (open-drain high impedance). |
| RCIN | External RC network input used to define FAULT CLEAR delay, $T_{FLTCLR,}$ approximately equal to R*C. When RCIN>8 V, the FAULT pin goes back into open-drain high-impedance |
| COM | Low side gate drivers return |
| $V_{B1,2,3}$ | High side floating supply |
| HO1,2,3 | High side gate driver outputs |
| $V_{S1,2,3}$ | High voltage floating supply return |
| LO1,2,3 | Low side gate driver outputs |

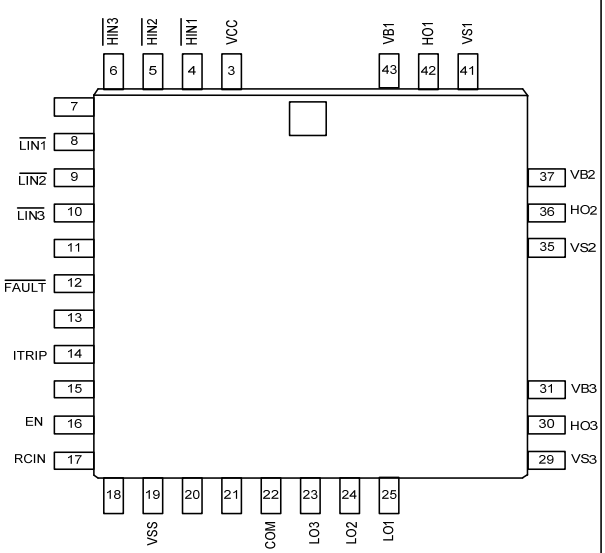
**Note**: All input pins and the ITRIP pin are internally clamped with a 5.2 V zener diode.

## Lead Assignments



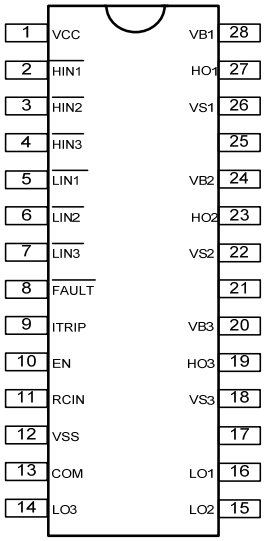

28 Lead PDIP

IR213(6, 63, 65, 66, 67,68)



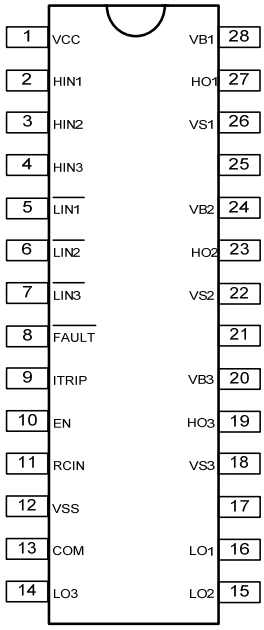

44 Lead PLCC w/o 12 leads

IR213(6, 63, 65, 66, 67,68)J



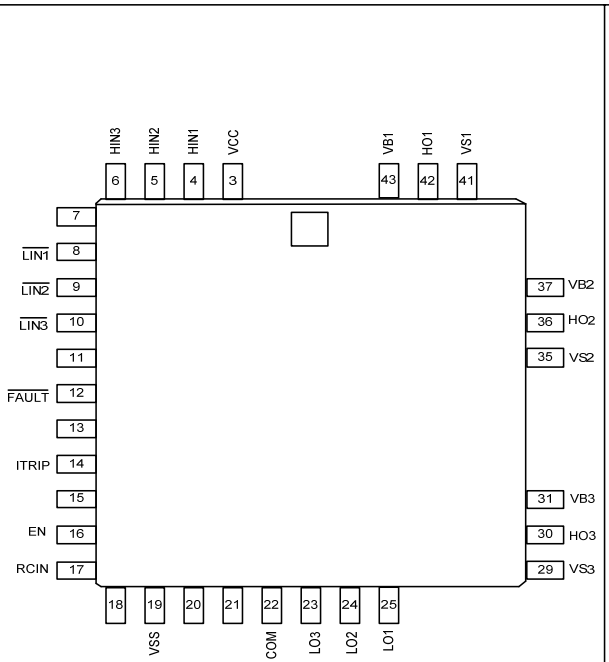

28 Lead SOIC (wide body)

IR213(6, 63, 65, 66, 67,68)S



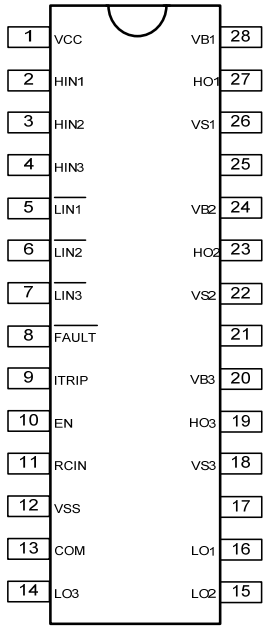

28 Lead PDIP

IR21362




44 Lead PLCC w/o 12 leads

IR21362J




28 Lead SOIC (wide body)

IR21362S

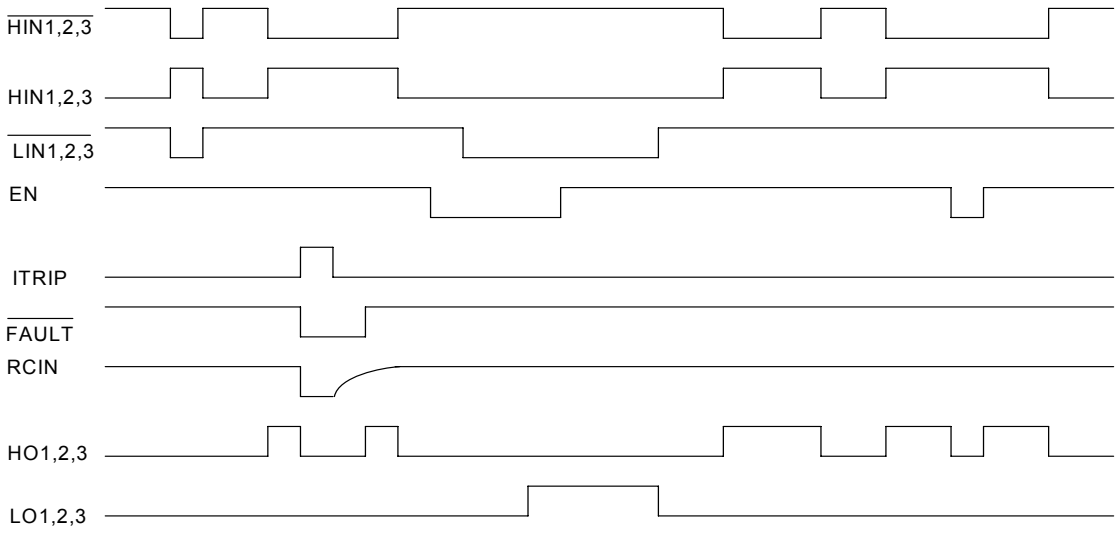



**Fig. 1. Input/Output Timing Diagram**

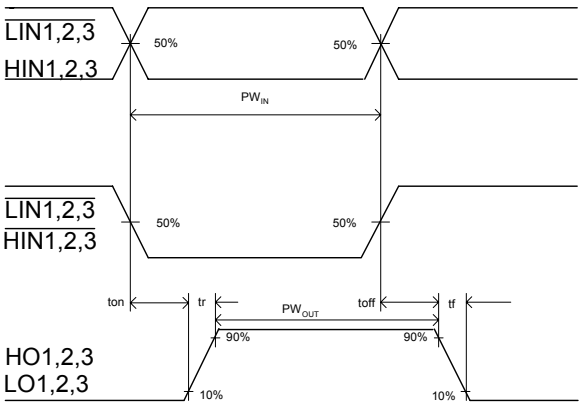



**Fig. 2. Switching Time Waveforms**

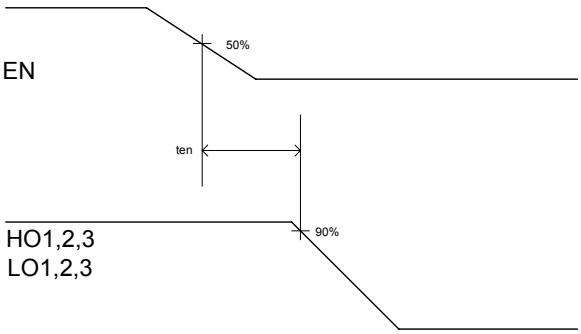



**Fig. 3. Output Enable Timing Waveform**

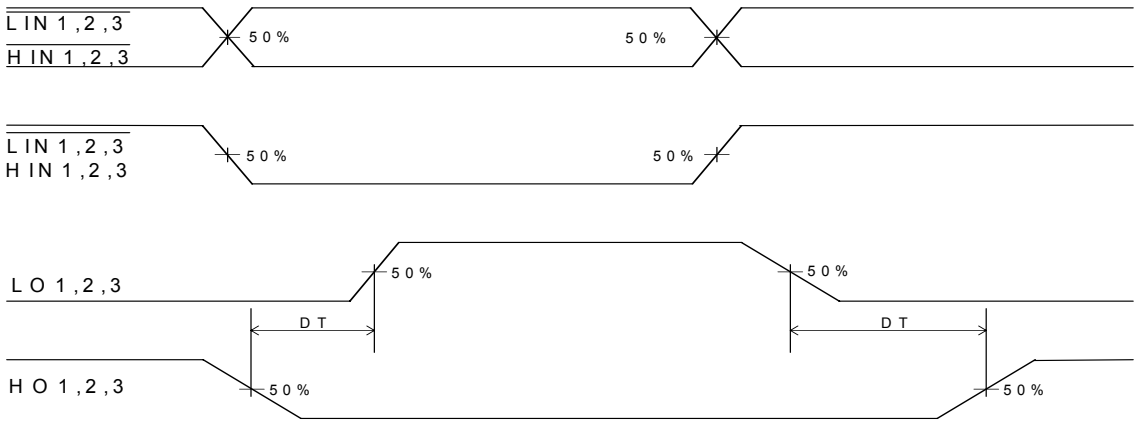



**Fig. 4. Internal Deadtime Timing Waveforms**

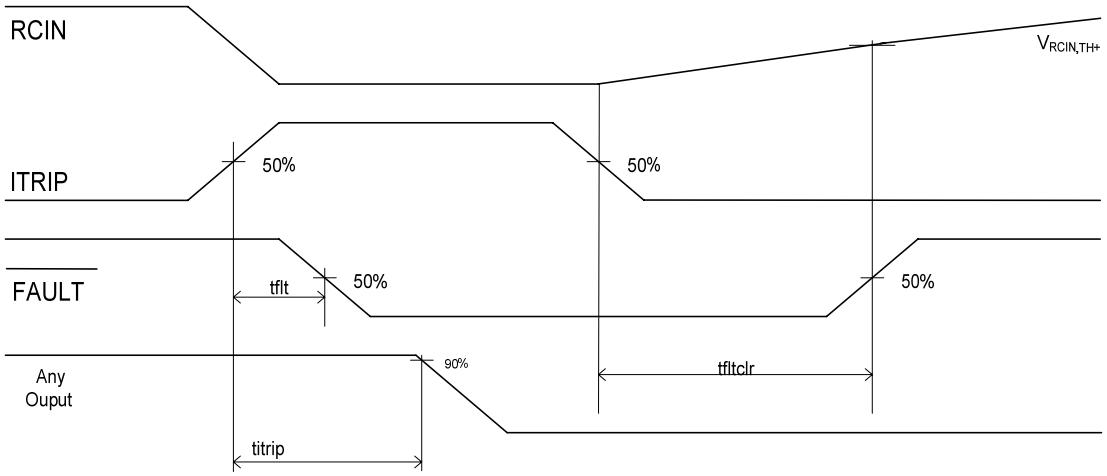



**Fig. 5. ITRIP/RCIN Timing Waveforms**

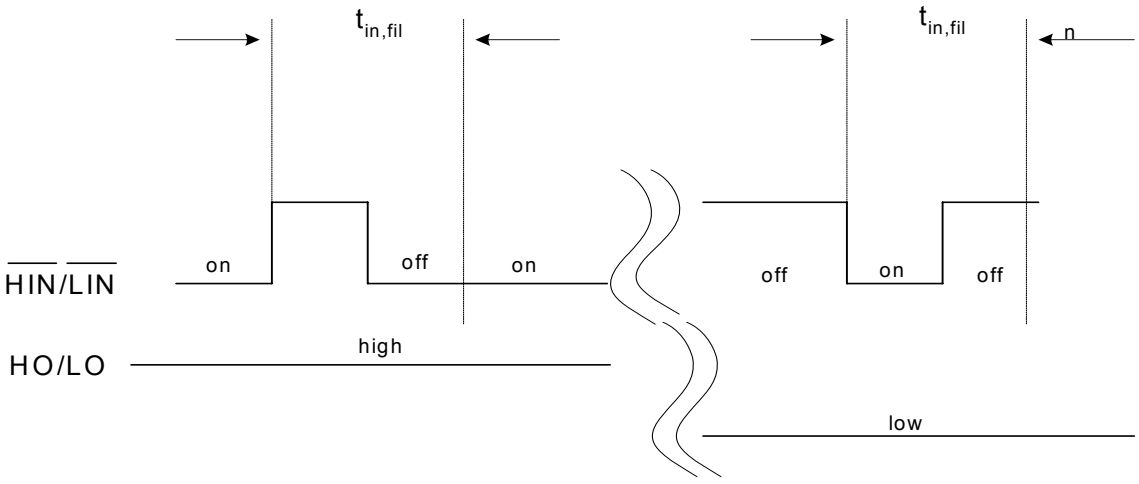



**Fig. 6. Input Filter Function**

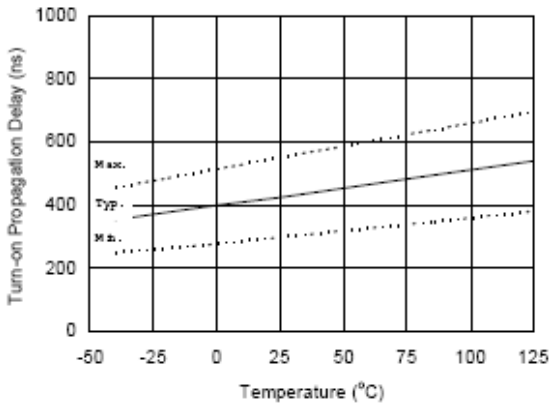



Figure 6A. Turn-on Propagation Delay vs. Temperature

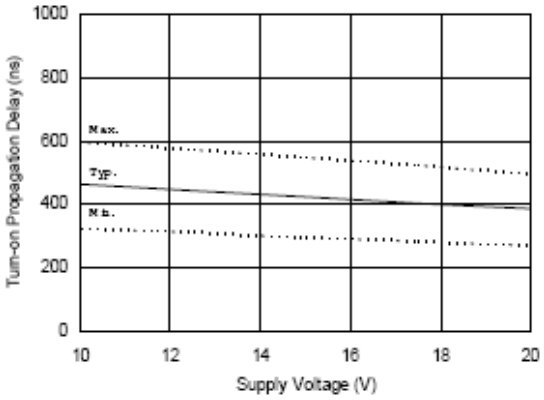



Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

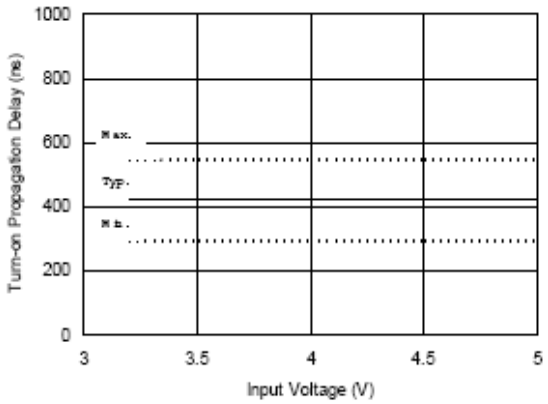



Figure 6C. Turn-on Propagation Delay vs. Input Voltage

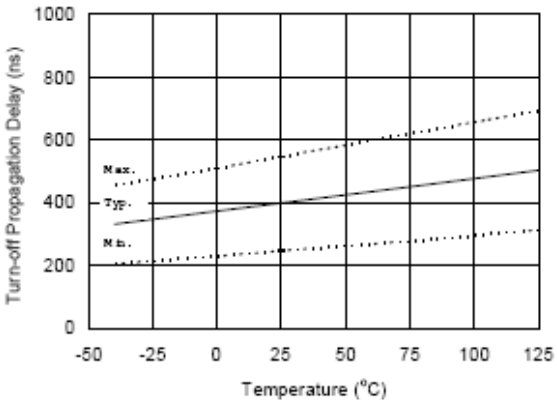



Figure 7A. Turn-off Propagation Delay vs. Temperature

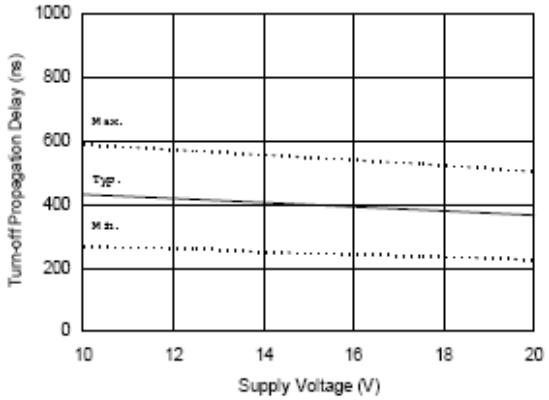



Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

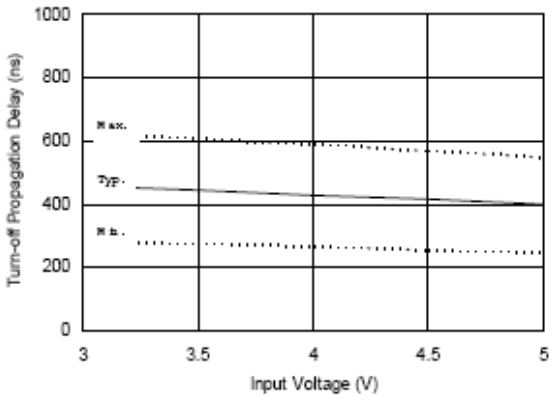



Figure 7C. Turn-off Propagation Delay vs. Input Voltage

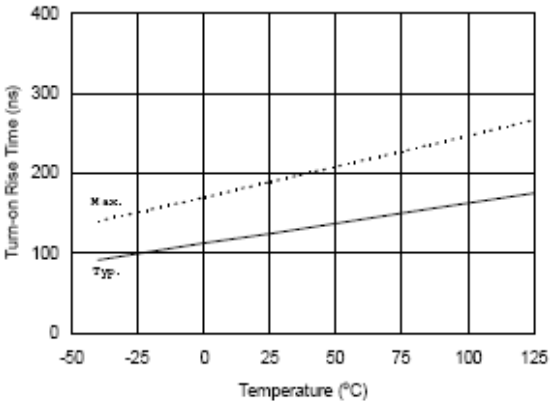



Figure 8A. Turn-on Rise Time vs. Temperature

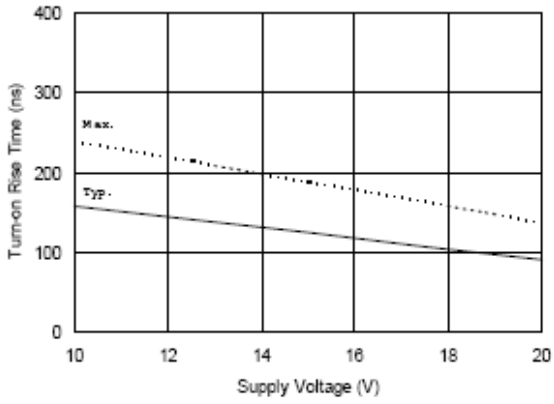



Figure 8B. Turn-on Rise Time vs. Supply Voltage

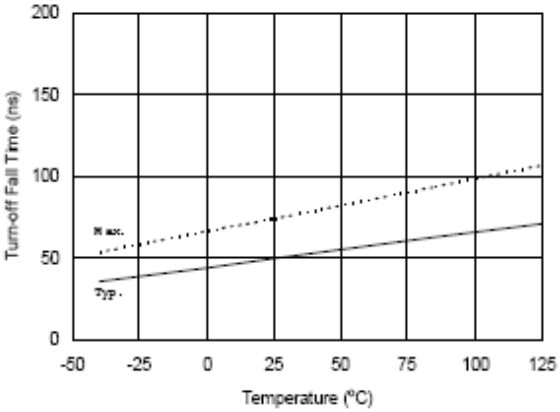



Figure 9A. Turn-off Fall Time vs. Temperature

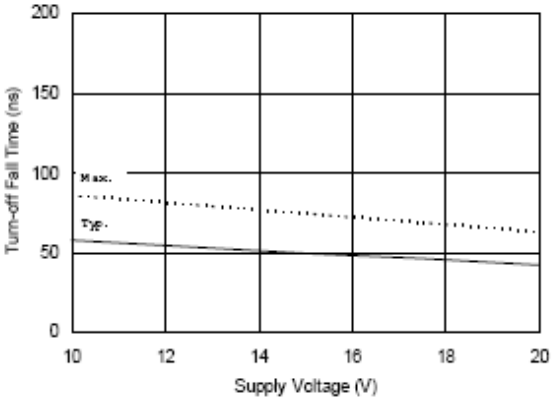



Figure 9B. Turn-off Fall Time vs. Supply Voltage

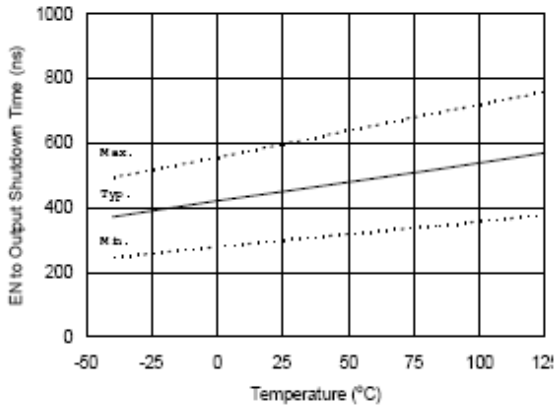



Figure 10A. EN to Output Shutdown Time vs. Temperature

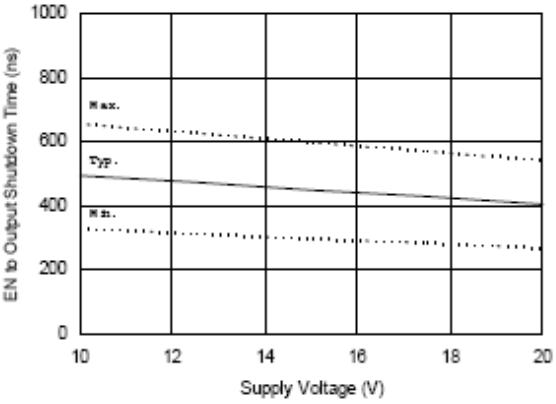



Figure 10B. EN to Output Shutdown Time vs. Supply Voltage

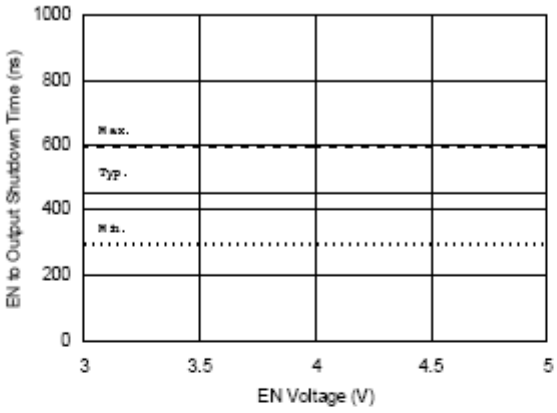



Figure 10C. EN to Output Shutdown Time vs. EN Voltage

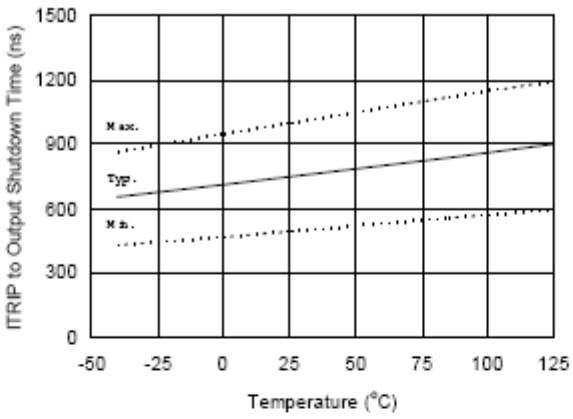



Figure 11A. ITRIP to Output Shutdown Time vs. Temperature

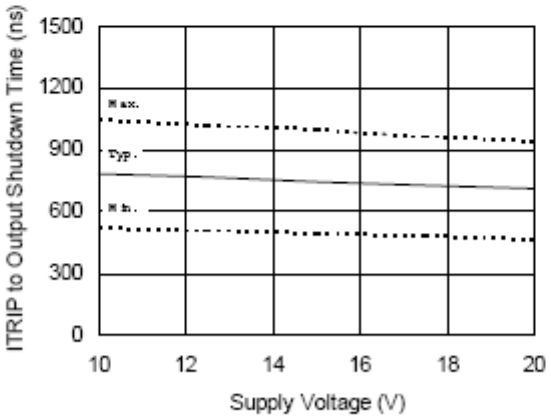



Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage

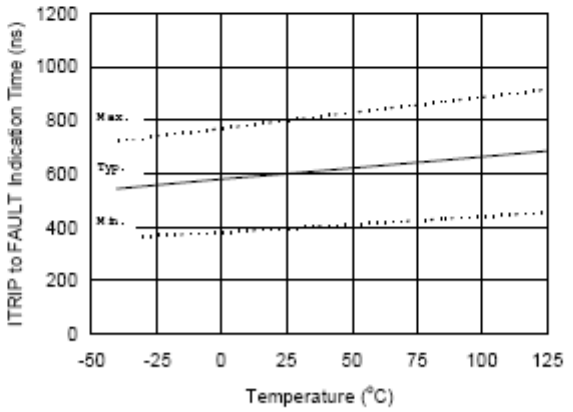



Figure 12A. ITRIP to FAULT Indication Time vs. Temperature

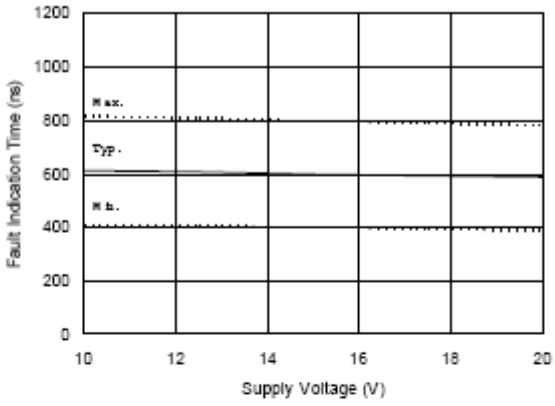



Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage

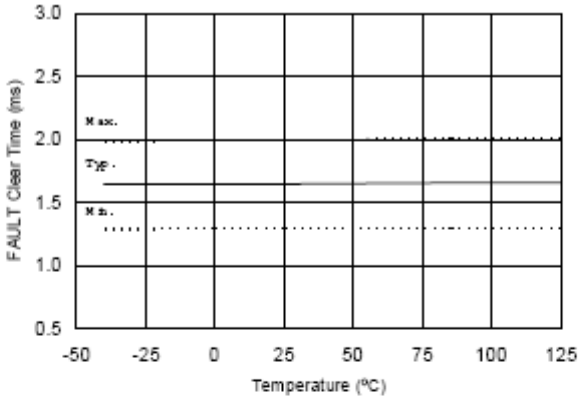



Fig13A. FAULT Clear Time vs. Temperature

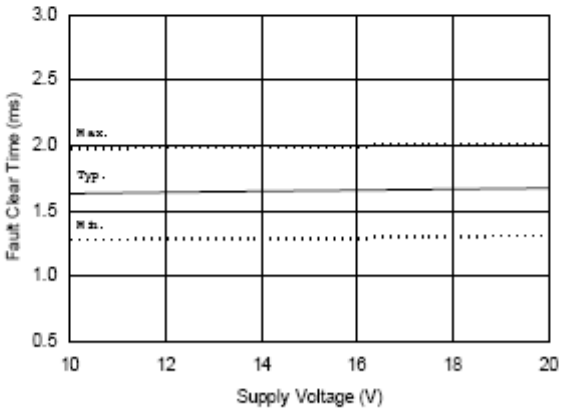



Figure 13B. FAULT Clear Time vs. Supply Voltage

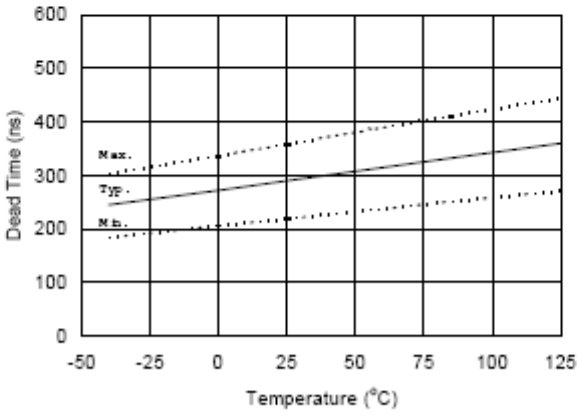



Figure 14A. Dead Time vs. Temperature

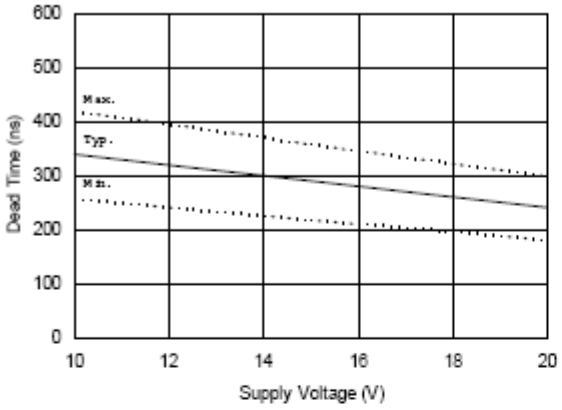



Figure 14B. Dead Time Time vs. Supply Voltage

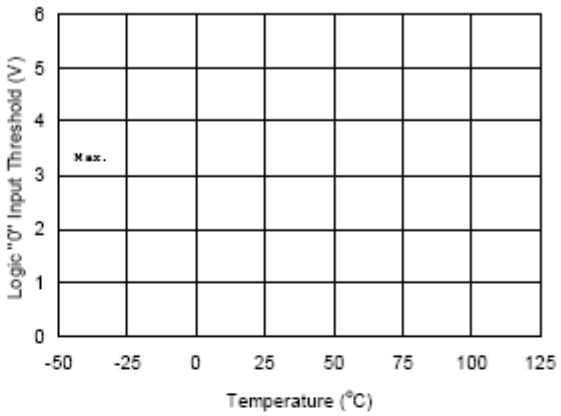



Figure 15A. Logic "0" Input Threshold vs. Temperature

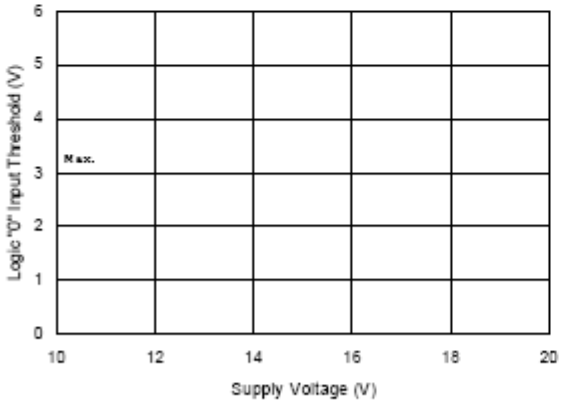



Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

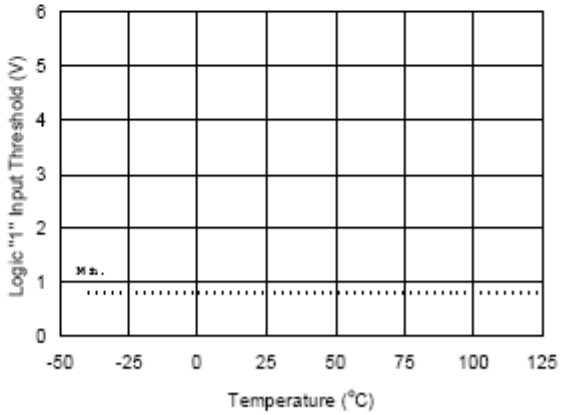



Figure 16A. Logic "1" Input Threshold vs. Temperature

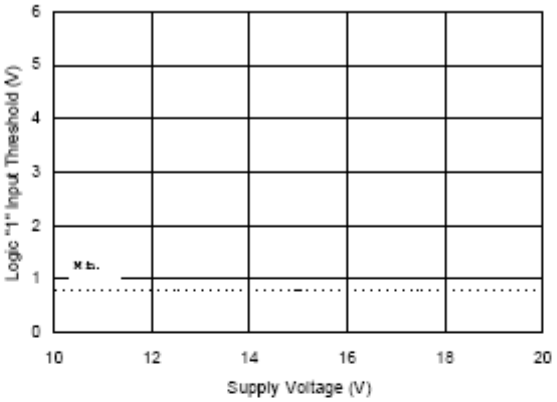



Figure 16B. Logic "1" Input Threshold vs. Supply Voltage

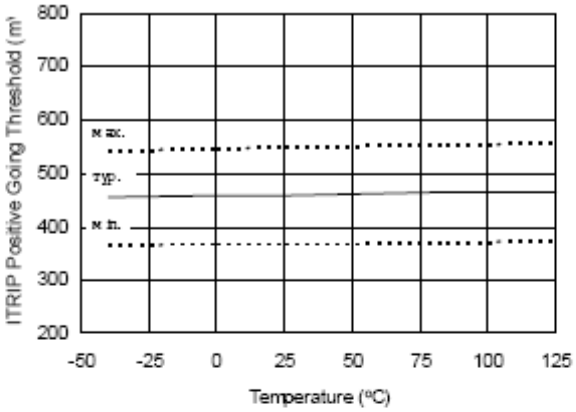



Figure 17A. ITRIP Positive Going Threshold vs. Temperature (IR2136/21362/21363/IR21366 Only)

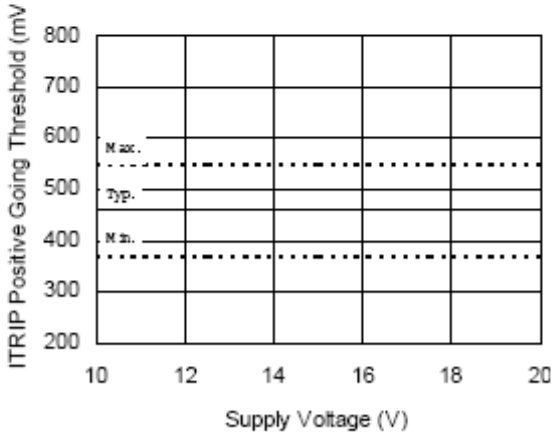



Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage (IR2136/21362/21363/IR21366 Only)

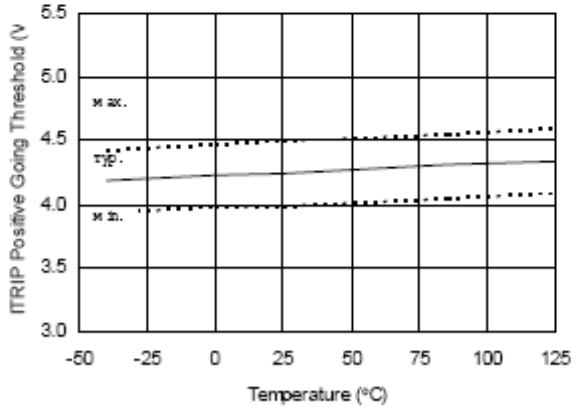



Figure 17C. ITRIP Positive Going Threshold vs. Temperature (IR21365/IR21367/IR21368 Only)

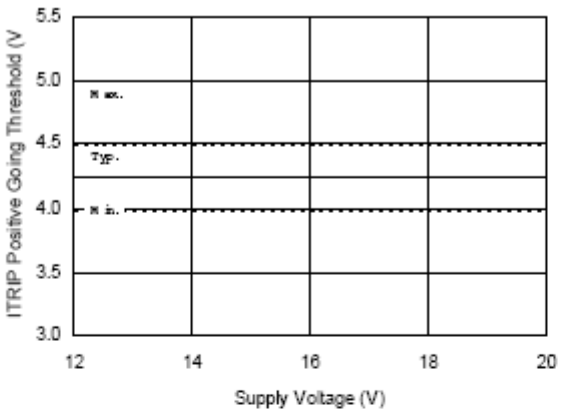



Figure 17D. ITRIP Positive Going Threshold vs. Supply Voltage (IR21365/IR21367/IR21368 Only)

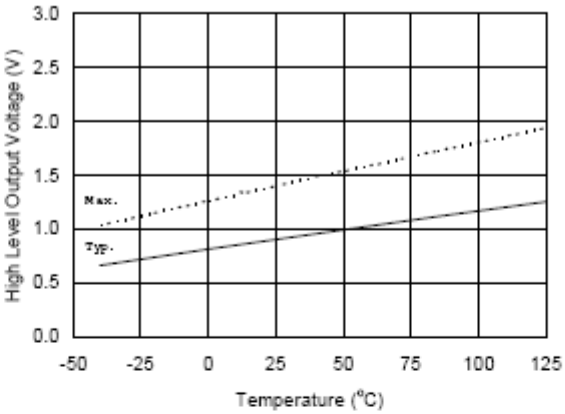



Figure 18A. High Level Output vs. Temperature

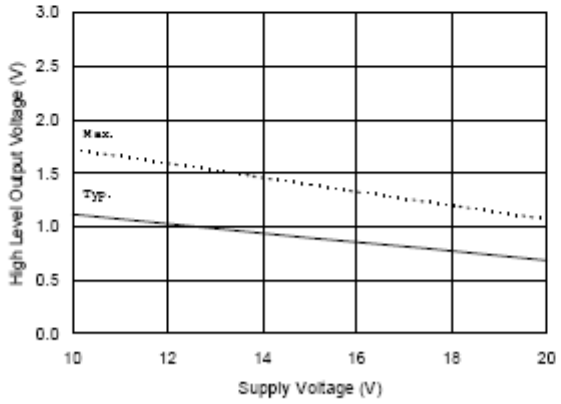



Figure 18B. High Level Output vs. Supply Voltage

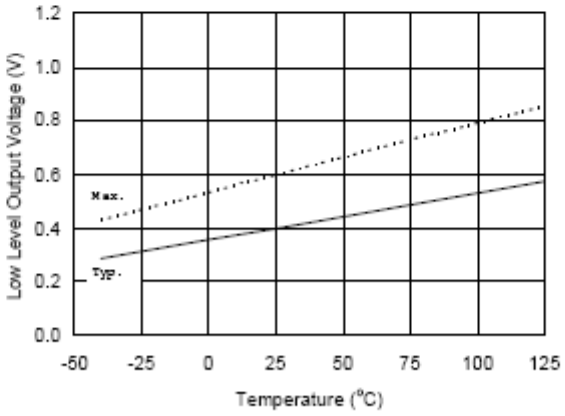



Figure 19A. Low Level Output vs. Temperature

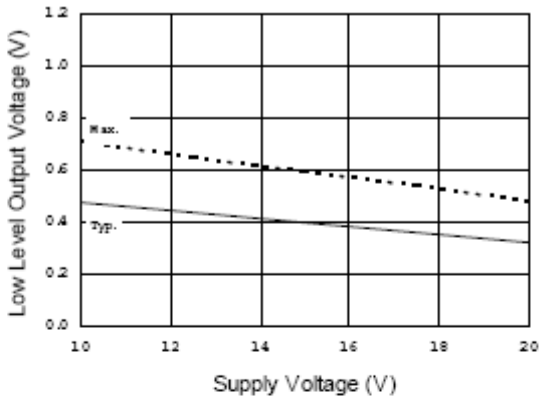



Figure 19B. Low Level Output vs. Supply Voltage

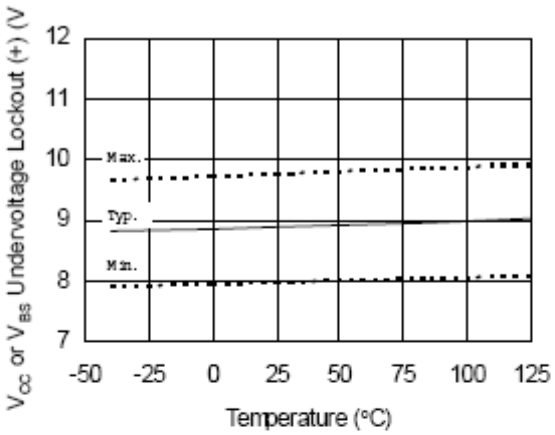



Figure 20. $V_{CC}$ or $V_{BS}$ Undervoltage (+) vs. Temperature (IR2136/IR21368 Only)

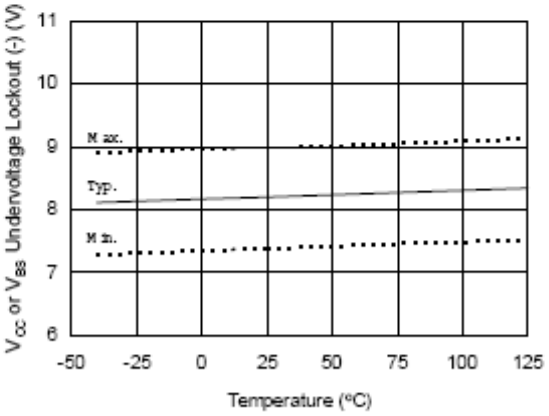



Figure 21. $V_{CC}$ or $V_{BS}$ Undervoltage (-) vs. Temperature (IR2136/IR21368 Only)

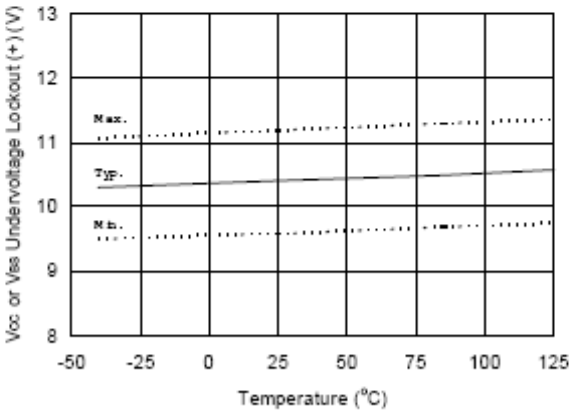



Figure 22. $V_{CC}$ or $V_{BS}$ Undervoltage (+) vs. Temperature (IR21362 Only)

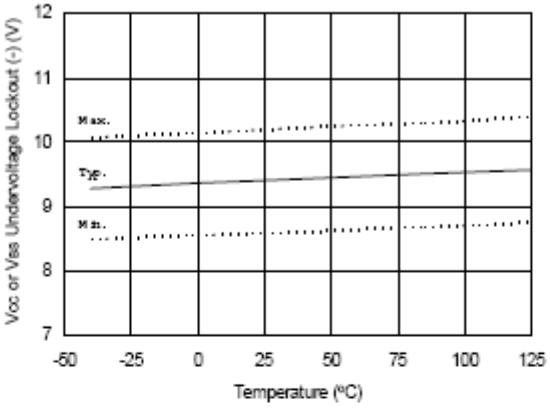



Figure 23. $V_{CC}$ or $V_{BS}$ Undervoltage (-) vs. Temperature (IR21362 Only)

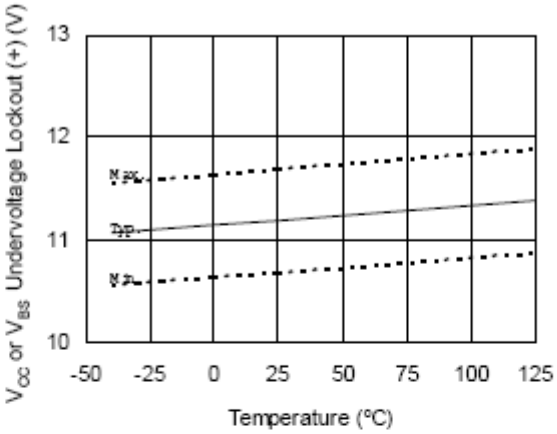



Figure 24. $V_{CC}$ or $V_{BS}$ Undervoltage (+) vs. Temperature (IR21363/21365/IR21366/IR21367 Only)

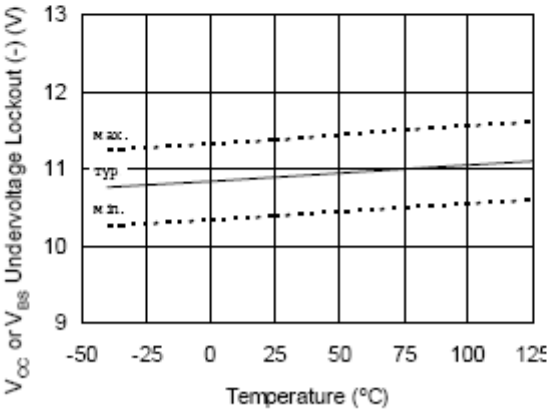



Figure 25. $V_{CC}$ or $V_{BS}$ Undervoltage (-) vs. Temperature (IR21363/21365/IR21366/IR21367 Only)

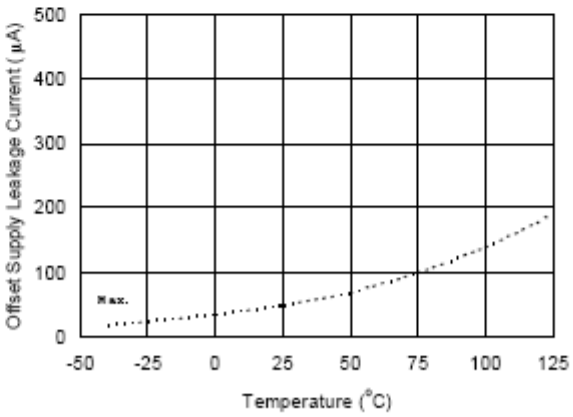



Figure 26A. Offset Supply Leakage Current vs. Temperature

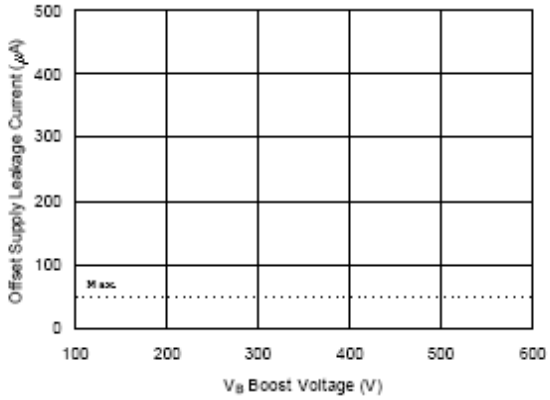



Figure 26B. Offset Supply Leakage Current vs. $V_B$ Boost Voltage

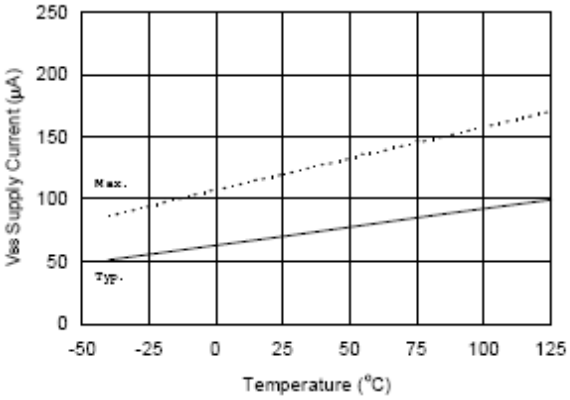



Figure 27A. $V_{BS}$ Supply Current vs. Temperature

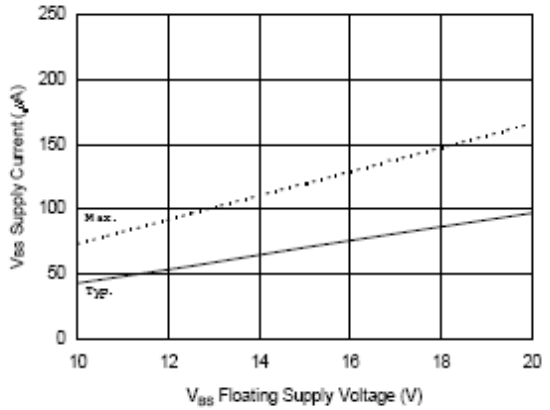



Figure 27B. $V_{BS}$ Supply Current vs. $V_{BS}$ Floating Supply Voltage

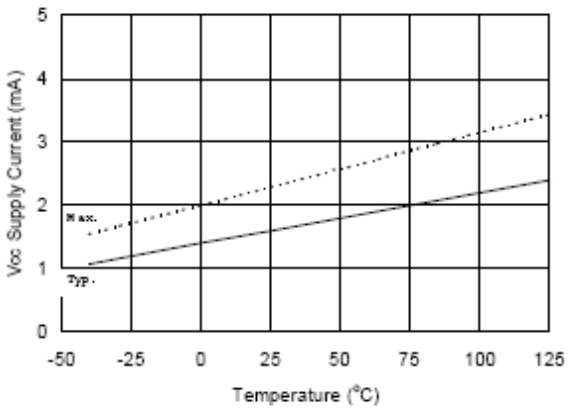



Figure 28A. $V_{CC}$ Supply Current vs. Temperature

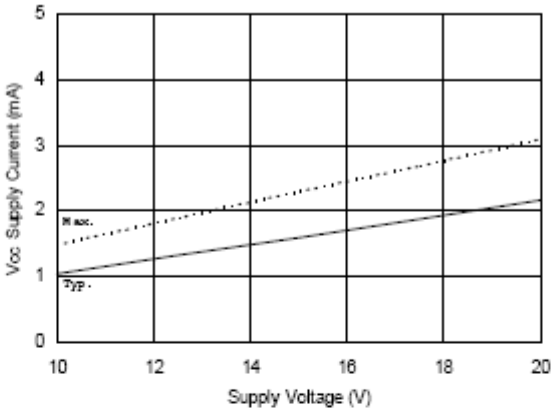



Figure 28B. $V_{CC}$ Supply Current vs. $V_{CC}$ Supply Voltage

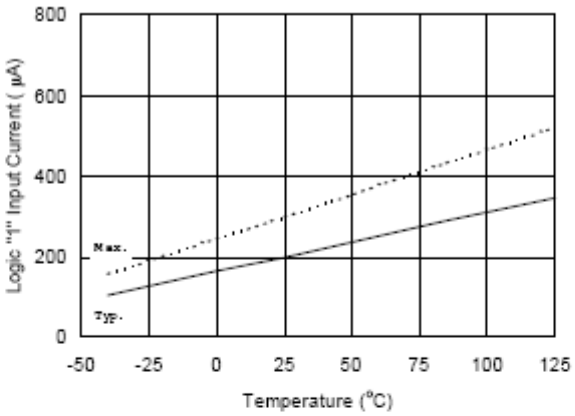



Figure 29A. Logic "1" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

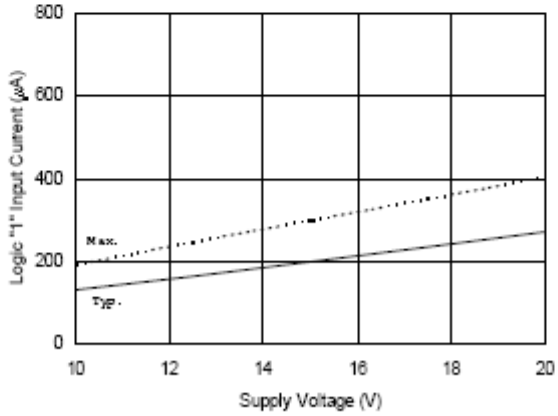



Figure 29B. Logic "1" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

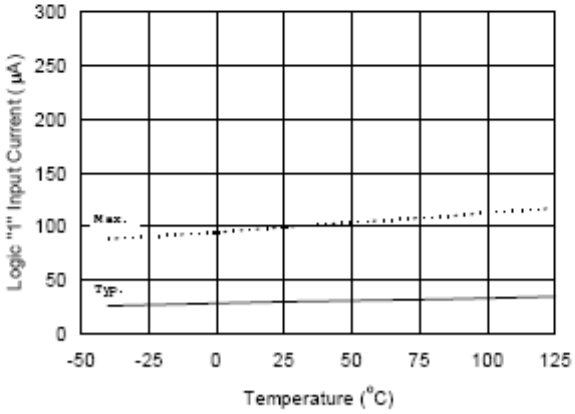



Figure 29C. Logic "1" Input Current vs. Temperature (IR21362 High Side Only)

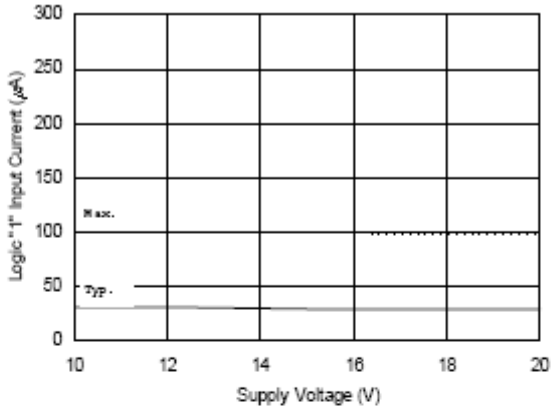



Figure 29D. Logic "1" Input Current vs. Supply Voltage (IR21362 High Side Only)

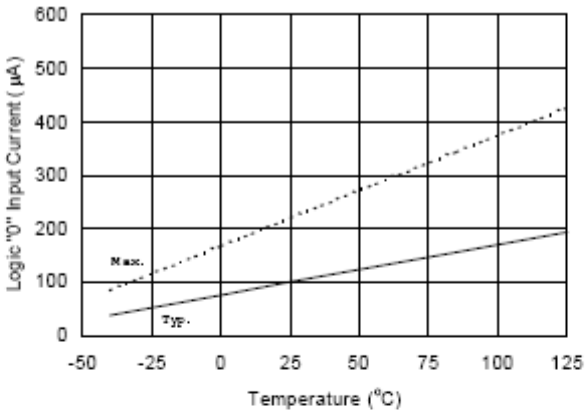



Figure 30A. Logic "0" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)

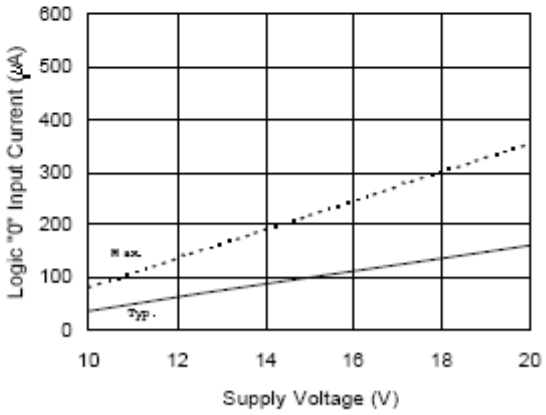



Figure 30B. Logic "0" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)

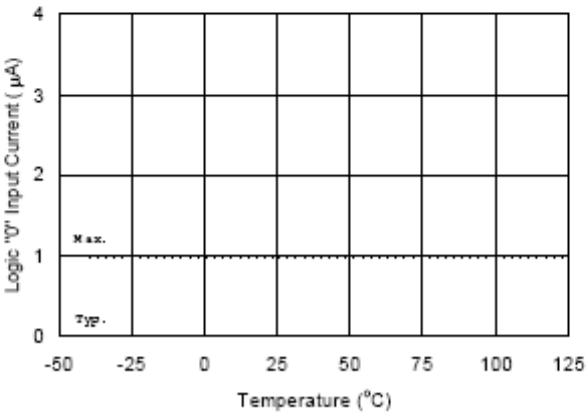



Figure 30C. Logic "0" Input Current vs. Temperature (IR21362 High Side Only)

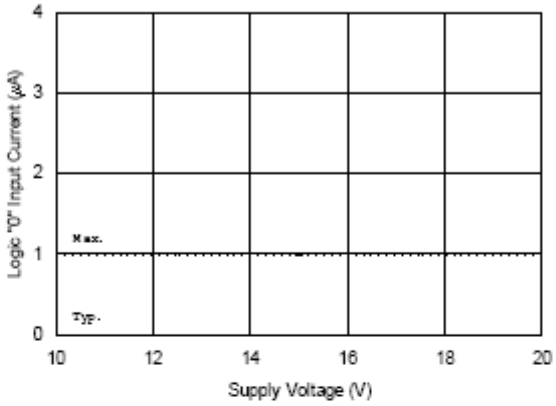



Figure 30D. Logic "0" Input Current vs. Supply Voltage (IR21362 High Side Only)

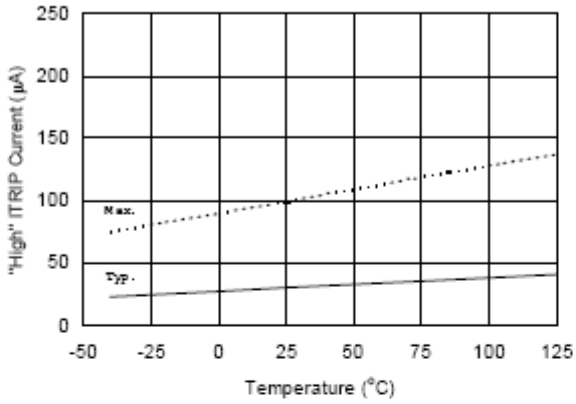



Figure 31A. "High" ITRIP Current vs. Temperature

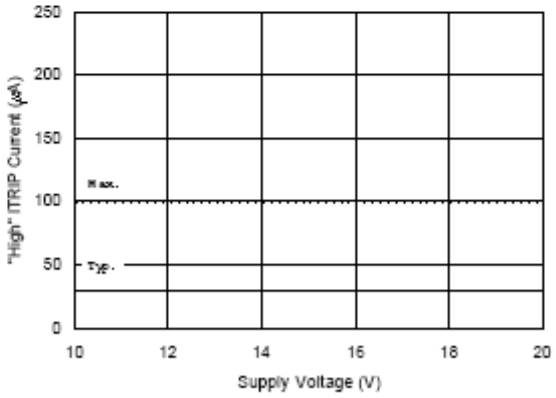



Figure 31B. "High" ITRIP Current vs. Supply Voltage

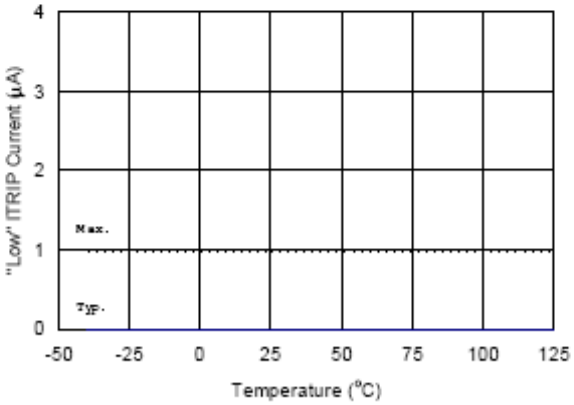



Figure 32A. "Low" ITRIP Current vs. Temperature

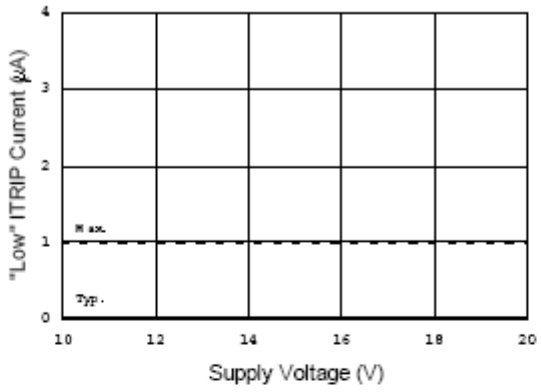



Figure 32B. "Low" ITRIP Current vs. Supply Voltage

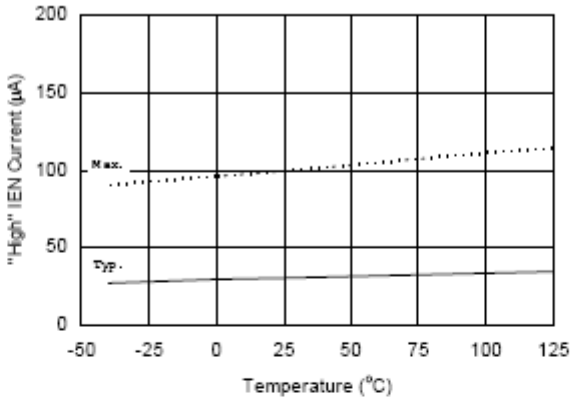



Figure 33A. "High" IEN Current vs. Temperature

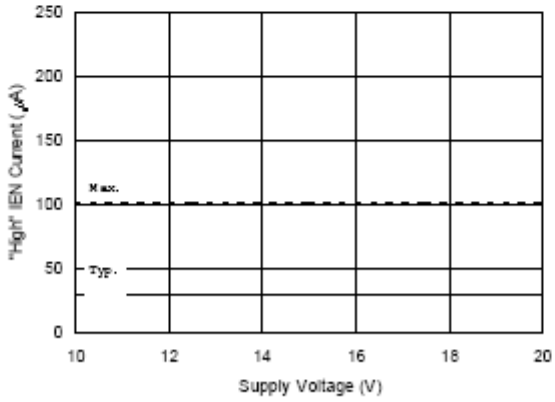



Figure 33B. "High" IEN Current vs. Supply Voltage

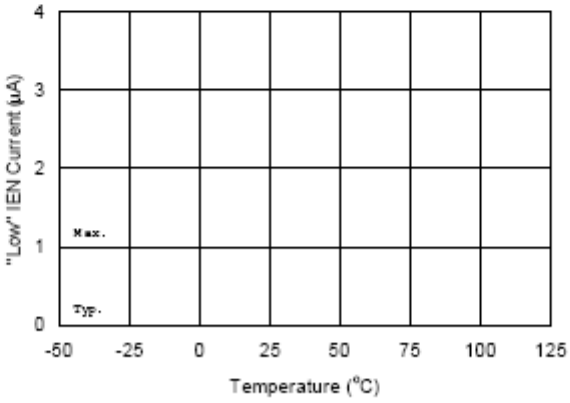



Figure 34A. "Low" IEN Current vs. Temperature

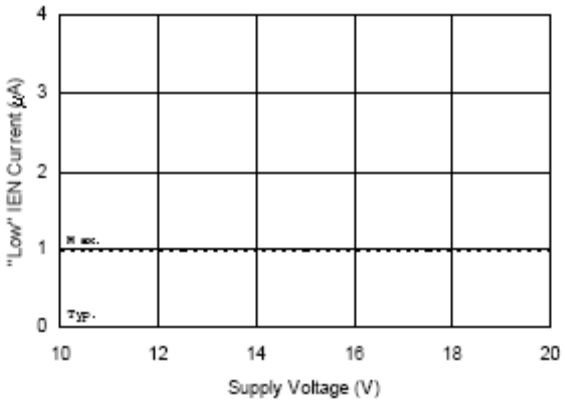



Figure 34B. "Low" IEN Current vs. Supply Voltage

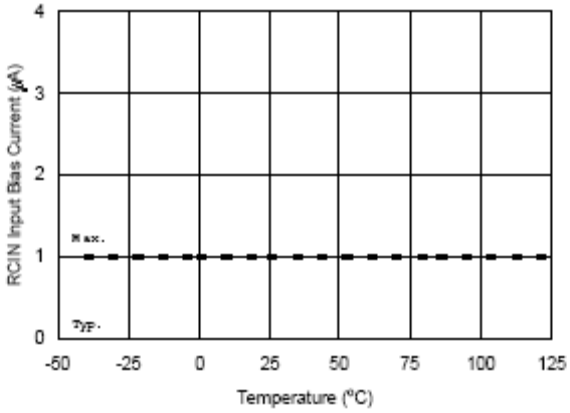



Figure 35A. RCIN Input Bias Current vs. Temperature

Figure 34B. "Low" IEN Current vs. Supply Voltage

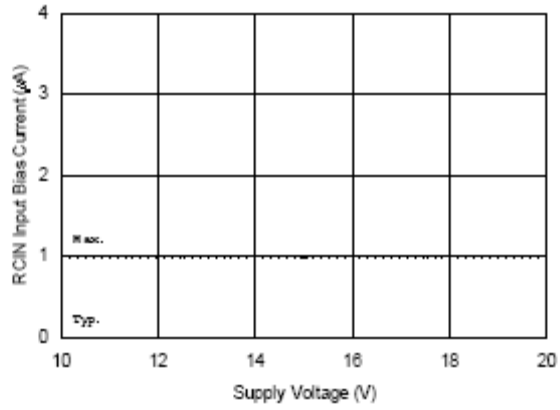



Figure 35B. RCIN Input Bias Current vs. Supply Voltage

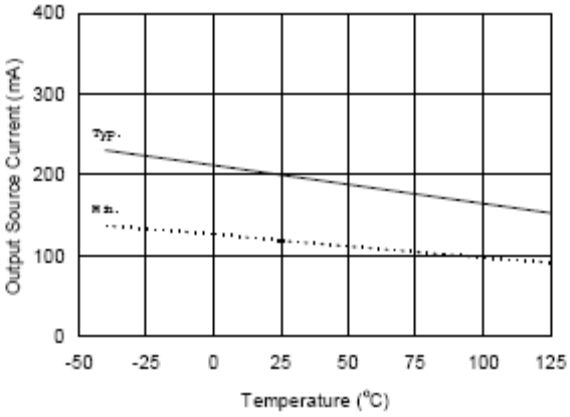



Figure 36A. Output Source Current vs. Temperature

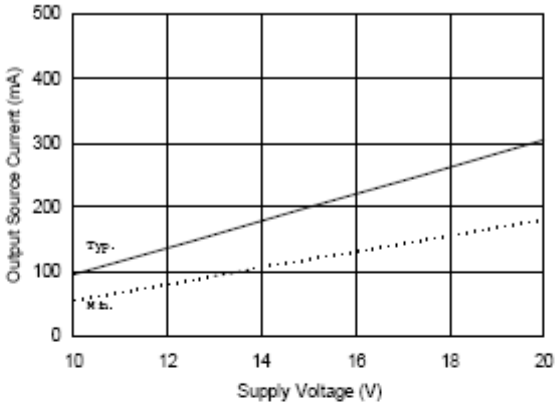



Figure 36B. Output Source Current vs. Supply Voltage

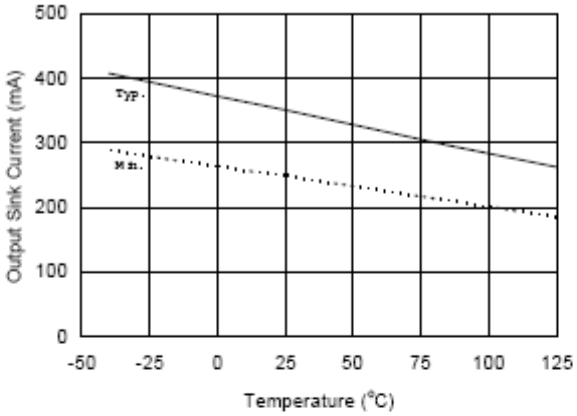



Figure 37A. Output Sink Current vs. Temperature

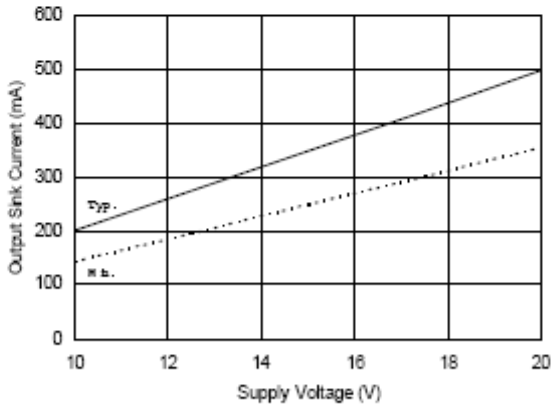



Figure 37B. Output Sink Current vs. Supply Voltage

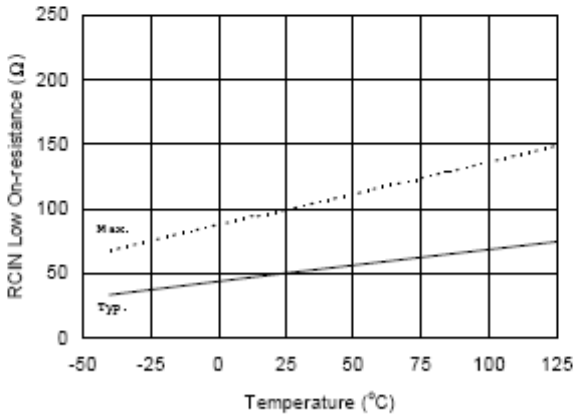



Figure 38A. RCIN Low On-resistance vs. Temperature

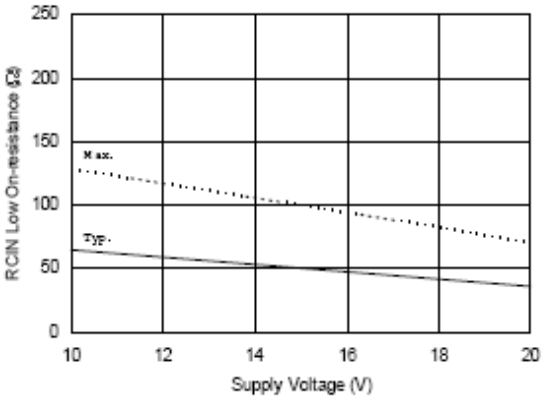



Figure 38B. RCIN Low On-resistance vs. Supply Voltage

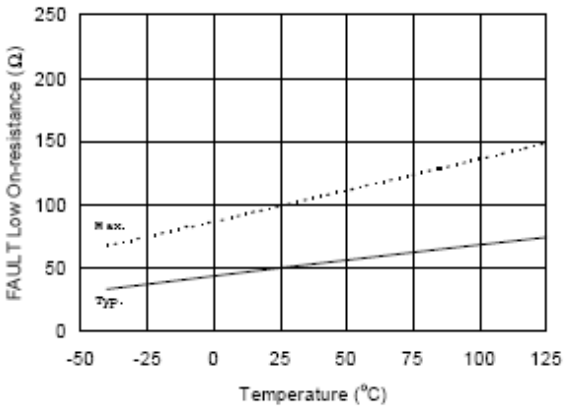



Figure 39A. FAULT Low On-resistance vs. Temperature

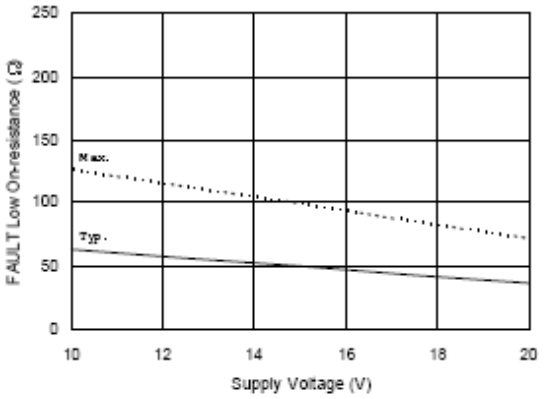



Figure 39B. FAULT Low On-resistance vs. Supply Voltage

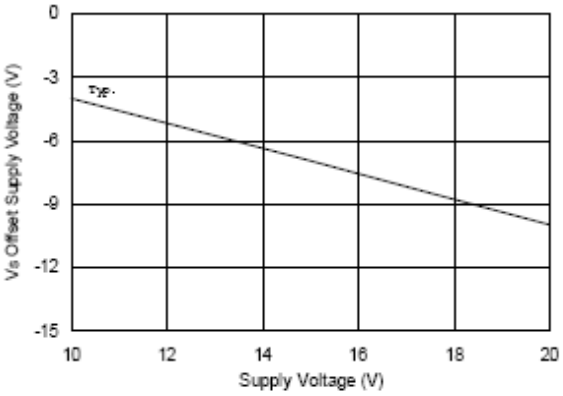



Figure 40. Maximum $V_S$ Negative Offset vs. $V_{BS}$ Supply Voltage

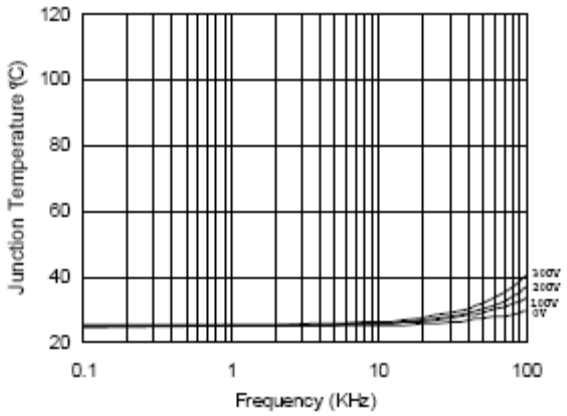



Figure 41. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC20W), Rgate=33Ω, Vcc=15V

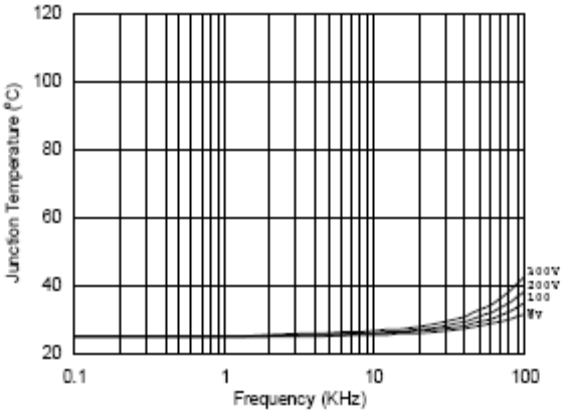



Figure 42. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC30W), Rgate=15Ω, Vcc=15V

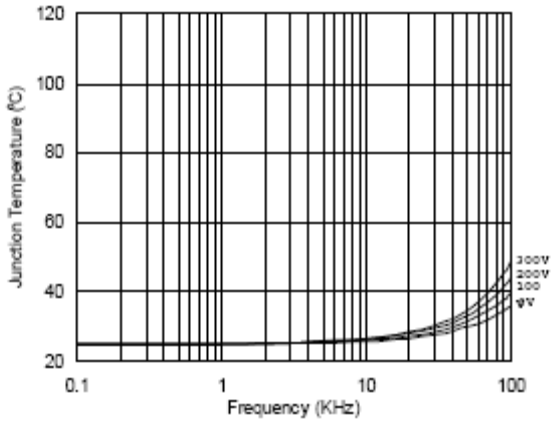



Figure 43. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4BC40W), Rgate=10Ω, Vcc=15V

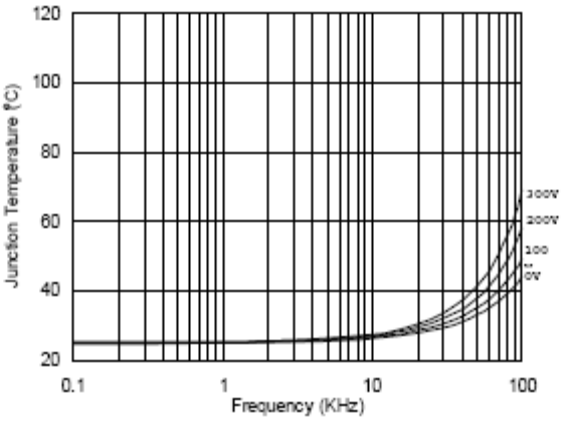



Figure 44. IR2136/IR21362(3)(5)(6)(7)(8)
vs. Frequency (IRG4PC50W), Rgate=5Ω, Vcc=15V

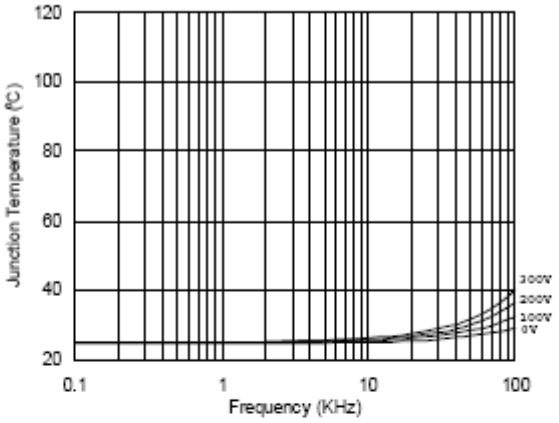



Figure 45. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC20W), Rgate=33Ω, Vcc=15V

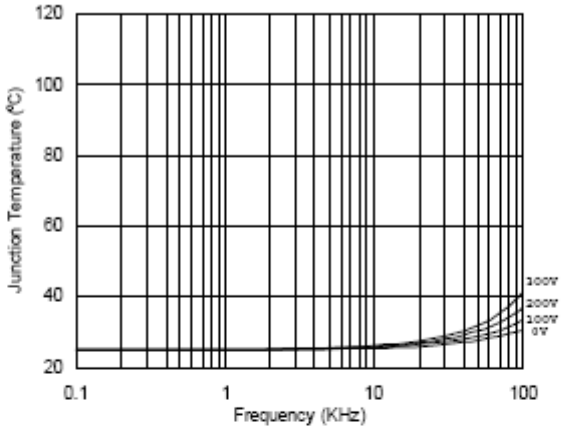



Figure 46. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC30W), Rgate=15Ω, Vcc=15V

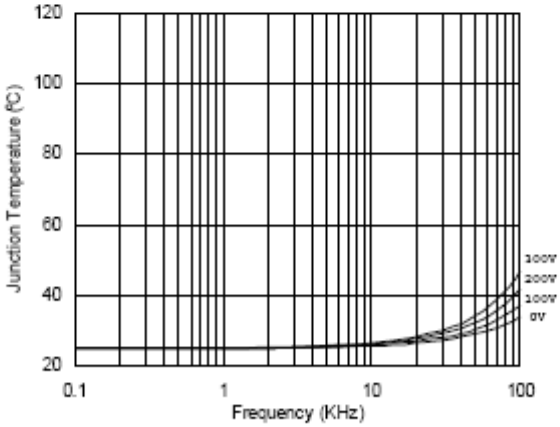



Figure 47. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4BC40W), Rgate=10Ω, Vcc=15V

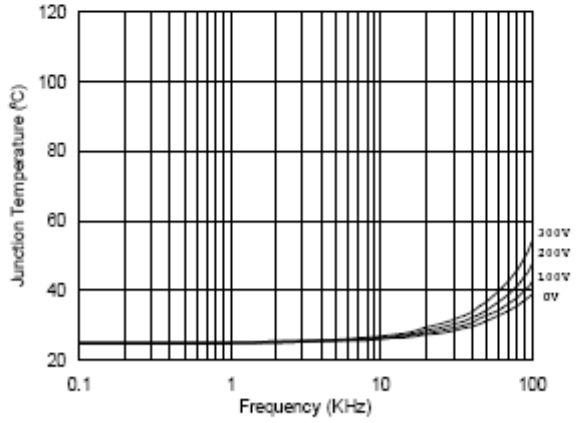



Figure 48. IR2136/IR21362(3)(5)(6)(7)(8) (J) vs. Frequency (IRG4PC50W), Rgate=5Ω, Vcc=15V

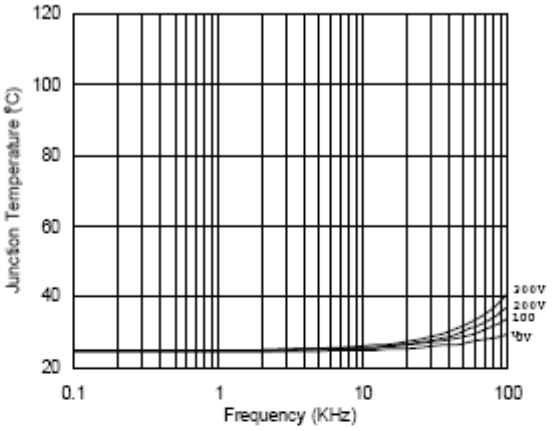



Figure 49. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC20W), Rgate=33Ω, Vcc=15V

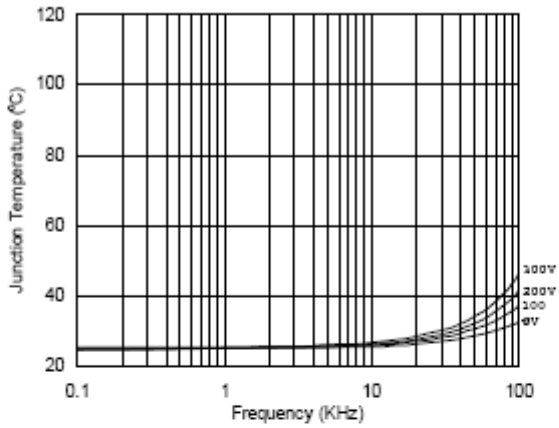



Figure 50. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC30W), Rgate=15Ω, Vcc=15V

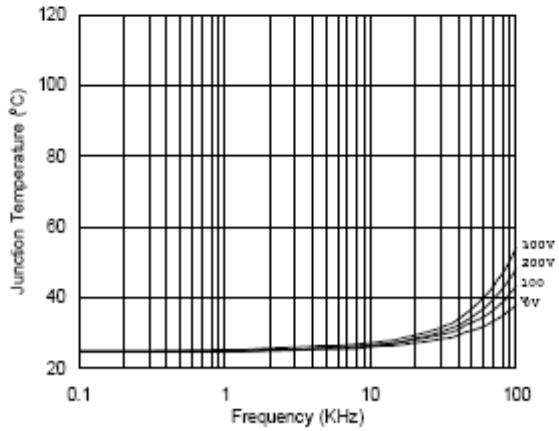



Figure 51. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4BC40W), Rgate=10Ω, Vcc=15V

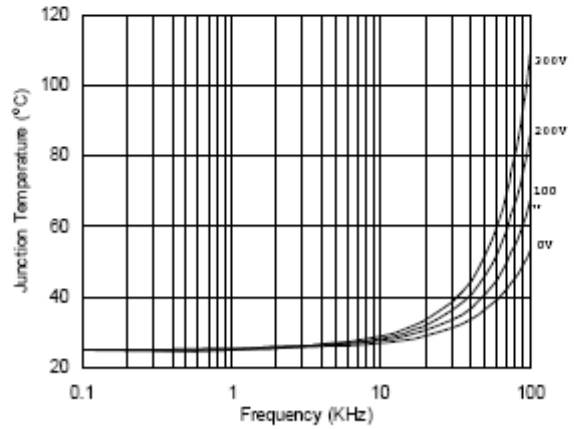
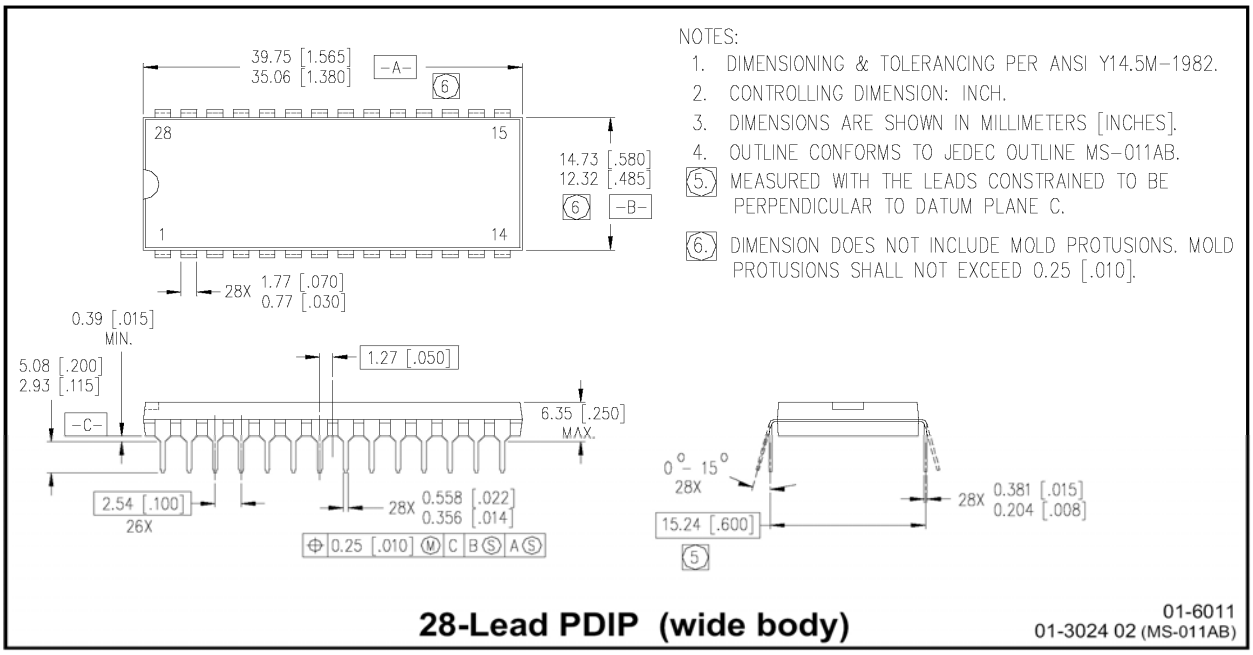
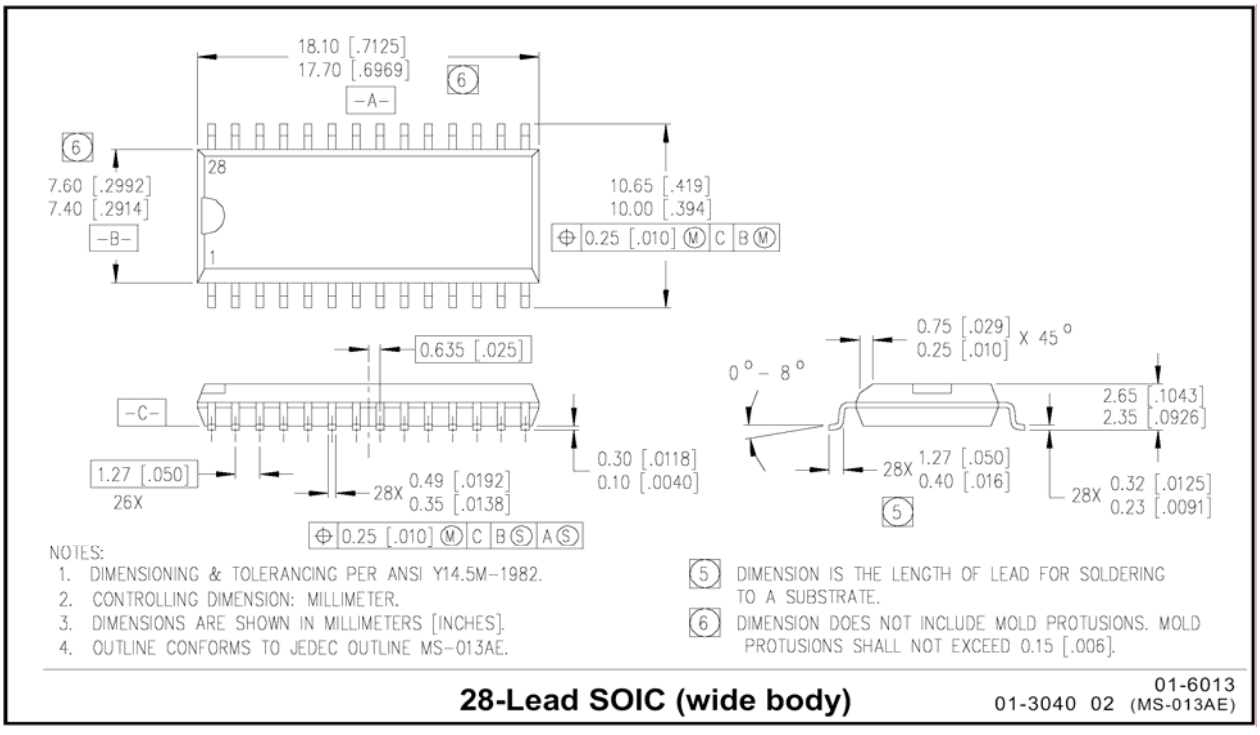


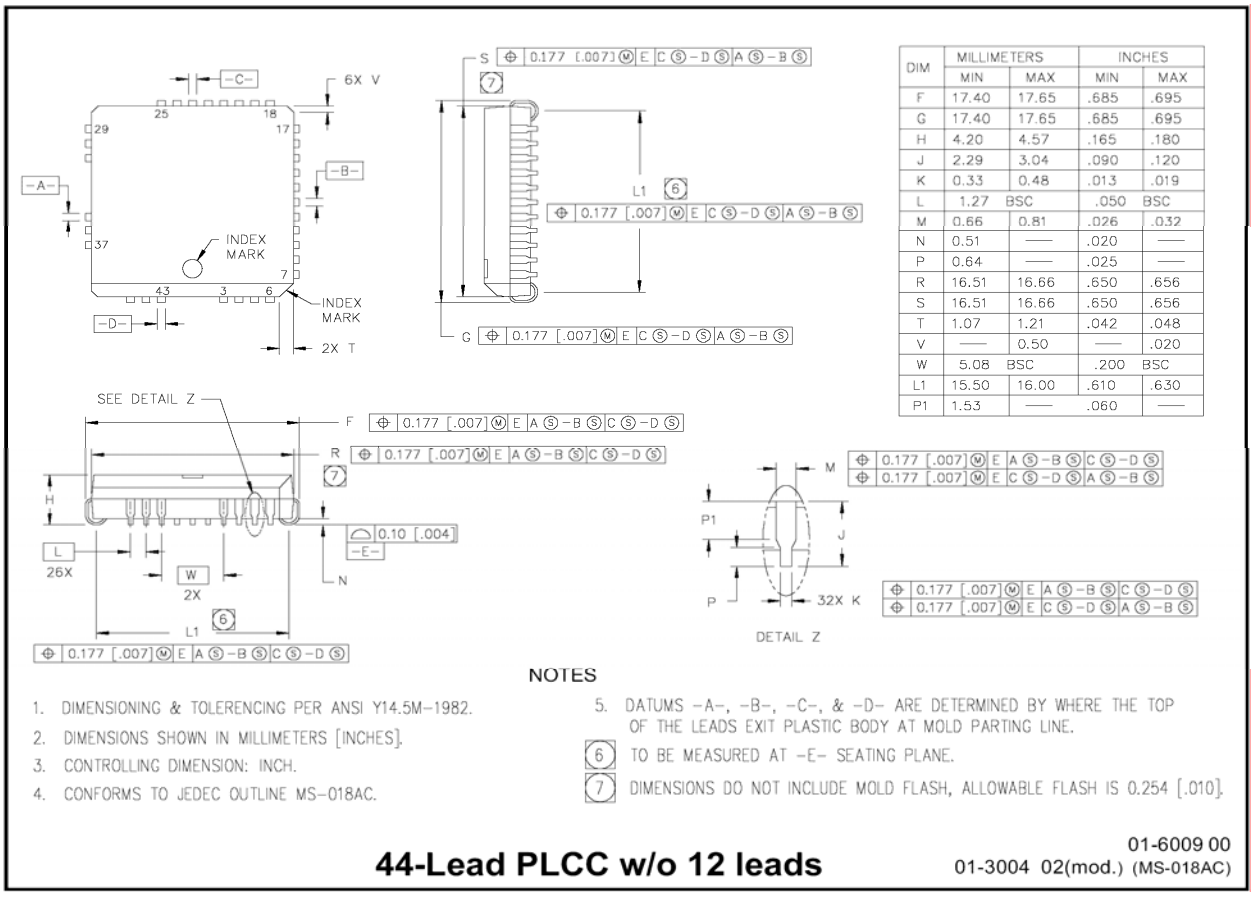

Figure 52. IR2136/IR21362(3)(5)(6)(7)(8) (S) vs. Frequency (IRG4PC50W), Rgate=5Ω, Vcc=15V

## Case Outlines



## Case Outlines




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| F | 17.40 | 17.65 | .685 | .695 |
| G | 17.40 | 17.65 | .685 | .695 |
| H | 4.20 | 4.57 | .165 | .180 |
| J | 2.29 | 3.04 | .090 | .120 |
| K | 0.33 | 0.48 | .013 | .019 |
| L | 1.27 BSC | | .050 BSC | |
| M | 0.66 | 0.81 | .026 | .032 |
| N | 0.51 | — | .020 | — |
| P | 0.64 | — | .025 | — |
| R | 16.51 | 16.66 | .650 | .656 |
| S | 16.51 | 16.66 | .650 | .656 |
| T | 1.07 | 1.21 | .042 | .048 |
| V | — | 0.50 | — | .020 |
| W | 5.08 BSC | | .200 BSC | |
| L1 | 15.50 | 16.00 | .610 | .630 |
| P1 | 1.53 | — | .060 | — |

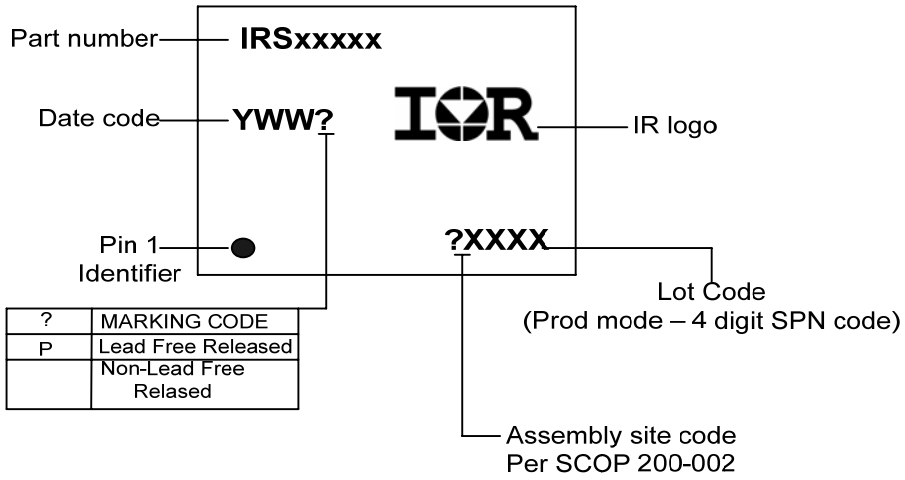
NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018AC.
5. DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT –E– SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

**44-Lead PLCC w/o 12 leads**

01-6009 00
01-3004 02(mod.) (MS-018AC)

## LEAD-FREE PART MARKING INFORMATION




| ? | MARKING CODE |
|---|---|
| P | Lead Free Released |
| | Non-Lead Free Relased |

## ORDER INFORMATION

| | |
|---|---|
| **Basic Part** | |
| 28-Lead PDIP IR2136(3,5,6,7,8) | Order IR2136(3,5,6,7,8) |
| 28-Lead SOIC IR2136(3,5,6,7,8)S | Order IR2136(3,5,6,7,8)S |
| 44-Lead PLCC IR2136(3,5,6,7,8)J | Order IR2136(3,5,6,7,8)J |
| 28-Lead PDIP IR21362 | Order IR21362 |
| 28-Lead SOIC IR21362S | Order IR21362S |
| 44-Lead PLCC IR21362J | Order IR21362J |
| **Lead-Free Part** | |
| 28-Lead PDIP IR2136(3,5,6,7,8) | Order IR2136(3,5,6,7,8)PbF |
| 28-Lead SOIC IR2136(3,5,6,7,8)S | Order IR2136(3,5,6,7,8)(S)PbF |
| 44-Lead PLCC IR2136(3,5,6,7,8)J | Order IR2136(3,5,6,7,8)(J)PbF |
| 28-Lead PDIP IR21362 | Order IR21362PbF |
| 28-Lead SOIC IR21362S | Order IR21362SPbF |
| 44-Lead PLCC IR21362J | Order IR21362JPbF |

International
IOR Rectifier

**WORLDWIDE HEADQUARTERS:** 233 Kansas Street, El Segundo, CA 90245 Tel: (310) 252-7105

**This part has been qualified per industrial level**

http://www.irf.com Data and specifications subject to change without notice. 7/08/2008