SEMICONDUCTOR
THE EMBEDDED CHIPSET COMPANY

Application Note:

Interfacing the PowerPC™ 603/603e/ 604/604e CPUs to the PCI Bus

1. Objective

This application note describes how to interface 64-bit synchronous PowerPC™ 60x microprocessors with the V292PBC (PBC) PCI bridge and V292BMC (BMC) DRAM controller. Target applications include PCI based adapter cards and PowerPC™ 60x based embedded systems.

Throughout this document, references will be made to the operation of the V292PBC and V292BMC components. Basic familiarity with these devices is assumed. If you don't have the relevant data sheets and user manuals for them then please contact V3. You can also download them from the V3 Semiconductor web site. Contact information (including the location of the V3 web site) is located on the back of this document.

2. Overview

Although the V292PBC is designed to interface gluelessly to the AMD Am29030/40™ processors, it can also be adapted for the PowerPC™ 60x processors. Both the Am29030/ 40 and PowerPC™ 60x processors are synchronous processors capable of bursting 32-bit data up to 40MHz (160MB/sec). Adapting the V292PBC as a PowerPC™ 60x processors interface involves conversion of the Am29K™ protocol of the V292PBC to the PowerPC™ 60x style bus access interface.

There are two possible interface methods:

- Adapt the PowerPC™ 60x to the V292PBC/V292BMC bus: In this scenario, the Am29K protocol of the V292PBC/V292BMC will be used as the internal local bus protocol. This is accomplished by converting the PowerPC™ 60x signals into Am29K equivalents. Since the Am29K protocol, as implemented by the V292PBC/ V292BMC, provides a long bust capability, this arrangement facilitates high speed movement of data directly to/from local memory and the PCI bus.

- Adapt the V292PBC to the PowerPC™ 60x bus: In this scenario, the common local bus will be PowerPC™ 60x based and the Am29K protocol of the V292PBC will be converted to PowerPC™ 60x protocol. This method is desirable when the local bus peripherals are designed specifically for the PowerPC™ 60x bus. There are several important performance drawbacks to this method that should be considered. First, the PowerPC™ 60x bus is not capable of performing long bursts which is essential for high throughput PCI designs. The second problem is that the burst protocol of the PowerPC™ 60x bus is not compatible with the PCI protocol. The PCI bus indicates burst length only at the end of the burst as opposed to the PowerPC™ 60x protocol which demands that transfer size be asserted at the beginning of the access. This

poses no problem when converting the PowerPC™ 60x as a master into signals for the V292PBC as a slave. However, optimal conversion in the other direction is not possible and performance must be sacrificed.

2.1 POWERPC™ 60X/AM29K PROTOCOL COMPARISON

This section will describe the main protocol differences and similarities between the PowerPC™ 60x bus and Am29K bus as implemented in the PBC/BMC.

Main Protocol Similarities

- Synchronous buses that generate and sample all signals on the rising edge of the clock.
- $\overline{\text{DBB}}$ (PowerPC™ 60x) acts like a $\overline{\text{REQ}}$ (PBC/BMC) to indicate a cycle is in progress.
- $\overline{\text{TA}}$ (PowerPC™ 60x) acts like a $\overline{\text{RDY}}$ (PBC/BMC) to indicate that data is ready on that clock.
- TT[1] (PowerPC™ 60x) acts like a R/$\overline{\text{W}}$ (PBC/BMC) Read/Write indication.
- The functional operation of the address bus is the same.

Main Protocol Differences

- PowerPC™ 60x uses 64-bit data bus while PBC/BMC uses 32-bit data bus.
- PowerPC™ 60x uses A2:0 and SIZ2:0 instead of the byte enables used by the PBC/BMC.
- PowerPC™ 60x uses $\overline{\text{TSBT}}$ to indicate burst access with a fixed burst length of 32-bytes at the beginning of a cycle. PBC/BMC determine burst size with the $\overline{\text{BURST}}$ signal.
- Bursts in the PowerPC™ 60x protocol are modulo 4 words while both Am29K and PCI bursts are sequential.
- Bus arbitration on the PowerPC™ 60x uses 5 signals ($\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{ABB}}$, $\overline{\text{DBG}}$ and $\overline{\text{DBB}}$) and not the 2 signals used by the Am29K. The PowerPC™ 60x protocol provides independent arbitration for address and data bus to support pipelined and split-bus transaction as oppose to a single address and data bus arbitration supported by the PBC/BMC.

Conversion between protocols requires a relatively small and inexpensive programmable logic device plus data buffers to facilitate multiplexing between the upper/lower 32-bit word on to the PBC/BMC data path. However, the approach chosen can drastically affect the overall performance of the system. The main factor affecting performance is the burst length. This alone will make the Am29K based local bus approach the best choice although both approaches will be detailed in the next sections.

3. AM29K Protocol Based Design

In this section, interfacing of the PowerPC™ 60x processor (as a local bus master) to the V292PBC/V292BMC will be discussed. This assumes that all peripherals in the system will be operating as Am29K style master/slaves and the protocol of the PowerPC™ 60x will be converted when it is the bus master.

3.1 BURST GENERATION

In comparing the burst protocols of the PowerPC™ 60x and Am29K, it was noted that the PowerPC™ 60x asserts TSBT at the beginning of an access to indicate burst transfer with a fixed burst length of 32-bytes. For a given cycle, if TSBT indicates that a burst is necessary then BURST is asserted with TS. A 3-bit counter is loaded also at TS and decremented on every TA. When the count is about to expire, BURST is de-asserted.

Another burst related issue to be aware of is the fact that the PowerPC™ 60x will wrap a burst **read** on a 8-word modulo boundary (Burst write transfers are always performed zero double word first). That is, if a burst of 4 double word begins on an address in which bits A4:3 are non-zero, the burst address will go from 0xnnnnnnXC back to 0xnnnnnnX0 where nnnnnnX are the upper 27 bits of the address.

- An approach that can be used with the V292PBC is to break any burst that could wrap a modulo boundary by de-asserting BURST when A4:2 is “111”.

3.2 BYTE ENABLE GENERATION

Byte enable outputs are derived using combinational logic from A2:0 and SIZ2:0. An 8-bit access results in only a single byte enable being asserted. Two are asserted for an aligned 16-bit access and all 4 when an aligned 32-bit or cache line burst is initiated. Although the Am29K protocol uses byte enables for write only, they can also be driven for reads when used by the V292PBC and V292BMC. The V292BMC will ignore the state of the byte enables during reads and always return all 32 bits of data.

3.3 BUS ARBITRATION

Although it is possible for both the V292PBC and PowerPC™ 60x to support preemption, for the purposes of clarity this feature will not be provided in this application note. The arbiter will drive either BG together with DBG back to the PowerPC™ 60x or LBGNT back to the V292PBC. The priority favors the PowerPC™ 60x. LBGNT is returned only when the

PowerPC™ 60x negates its $\overline{BR}$. Once the V292PBC takes control, it will retain mastership until de-asserting its bus request. In this scheme, $\overline{ABB}$ is not generated back to the CPU since $\overline{BG}$ is never returned until after the V292PBC is safely off the bus.

3.4 INTERCONNECTION

The interface between the PowerPC™ 60x, V292PBC and V292BMC is shown in Figure 1. It consists of a small PLD to generate the $\overline{BURST}$, $\overline{RDY}$, byte enable and buffer control signals. Most of the interface involves direct connection of PowerPC™ 60x, V292PBC and V292BMC signals. The reset and clock signals for the PowerPC™ 60x processor, PLD, PBC and BMC are also tied directly together. The 64-bit data path is multiplexed through four 74FCT16543 style buffers into a 32-bit data path with buffer control signals from the PLD as shown in Figure 2.

Figure 1: Conversion of PowerPC™ 60x Signals into Am29K Protocol

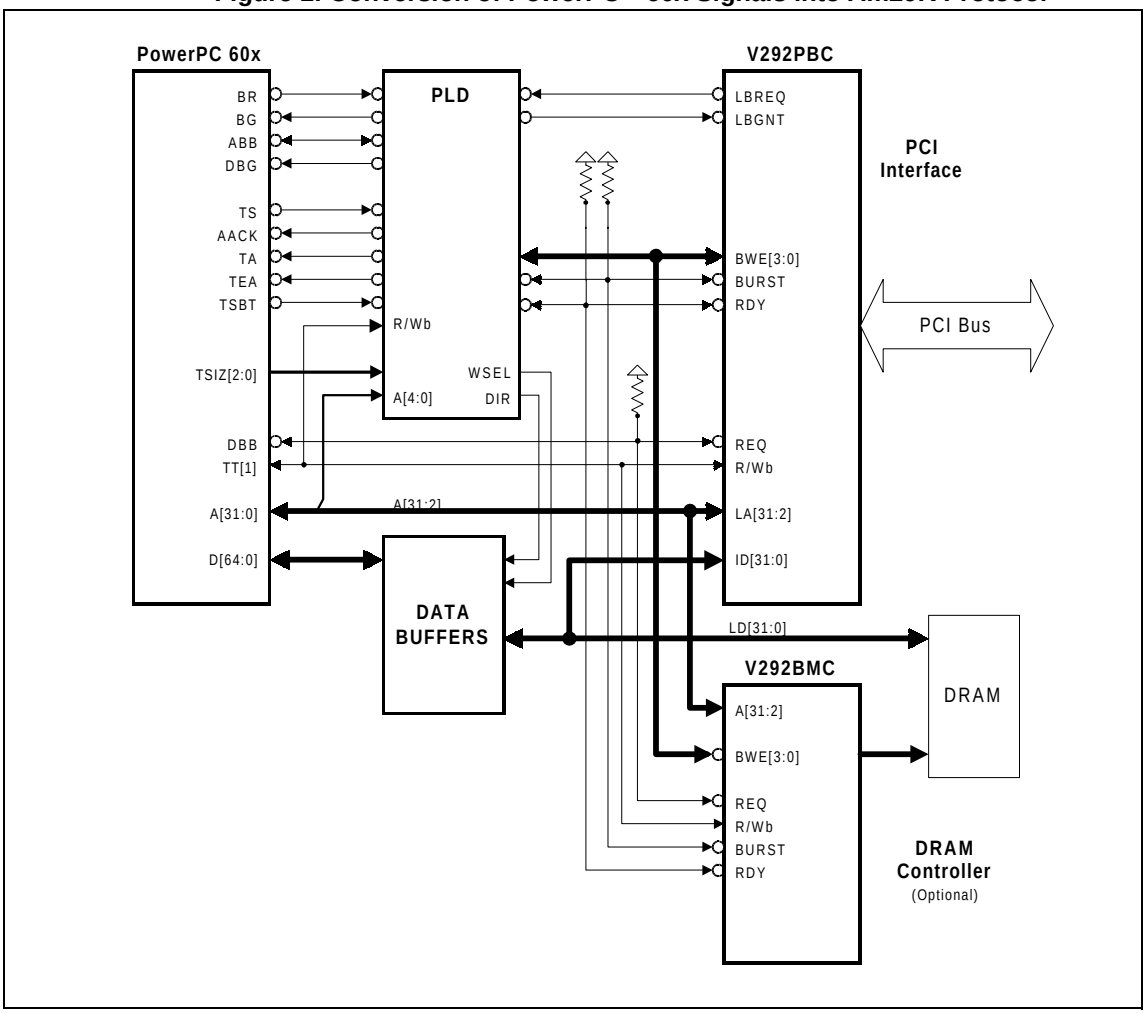


Figure 2: Data Path Buffers

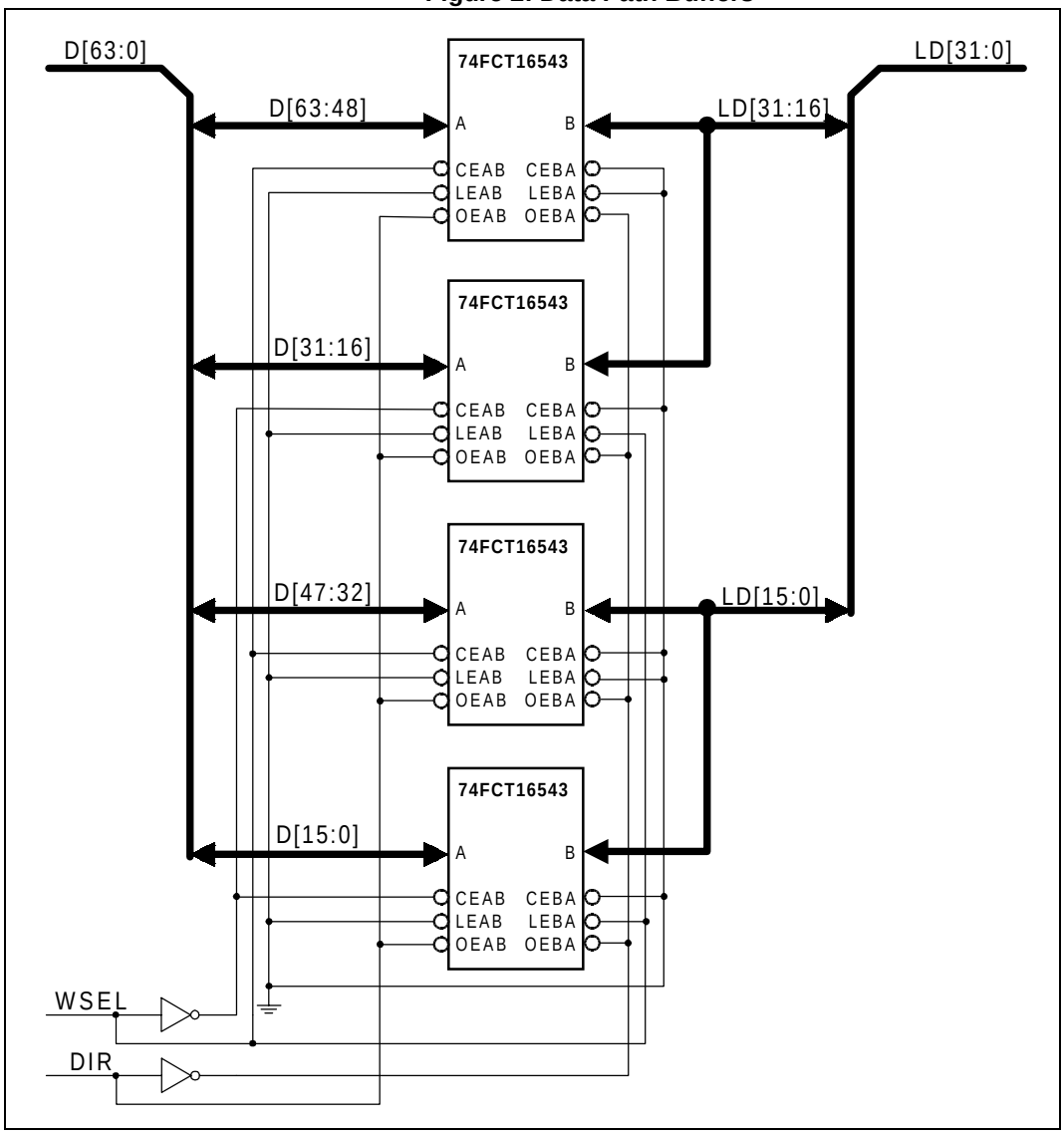
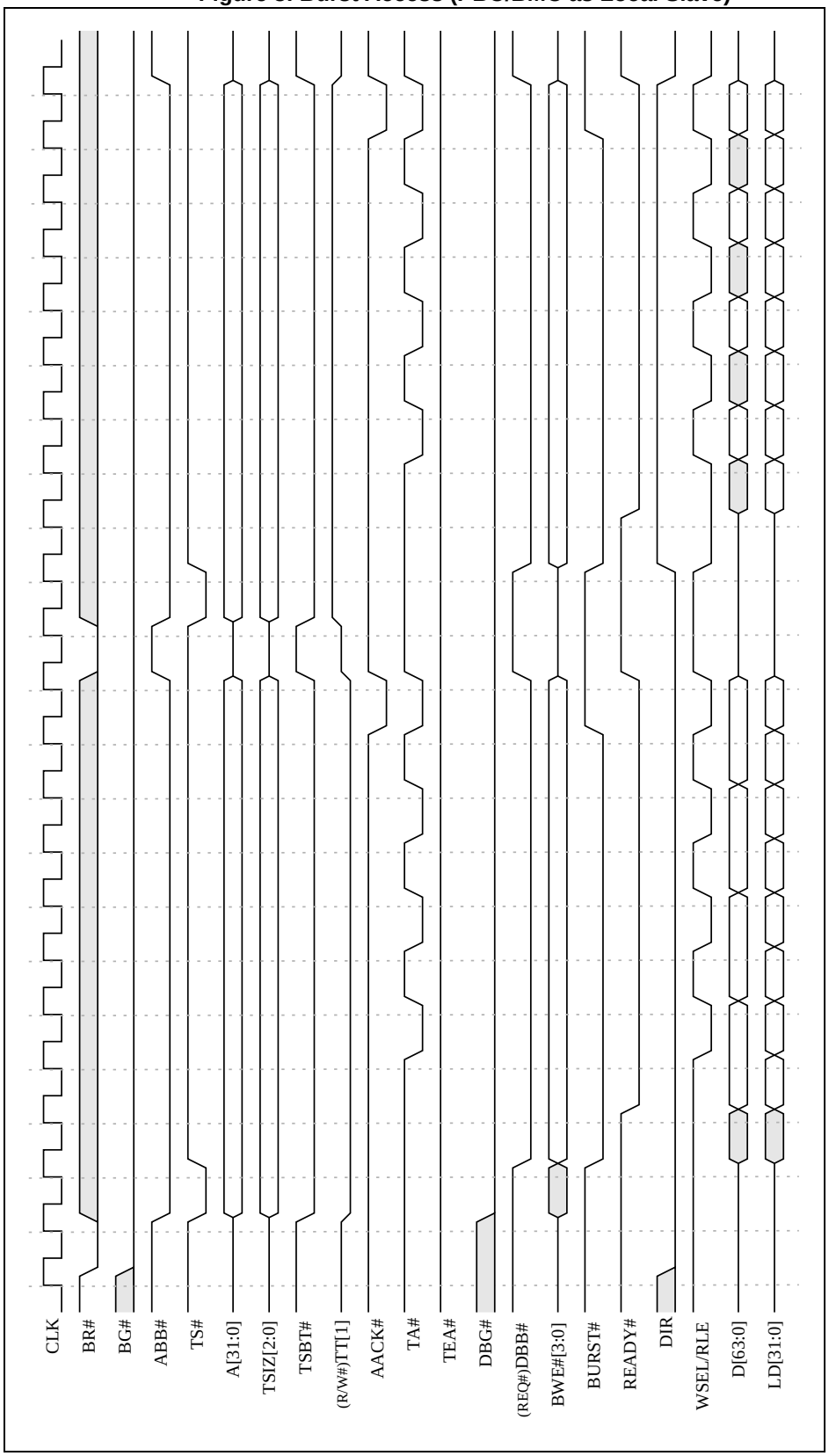


Figure 3: Burst Access (PBC/BMC as Local Slave)



4. Performance

The performance of the various alternatives have been calculated in the following tables. "Real world" performance will depend on a number of factors:

Bursting: The best performance will depend on the ability to burst long data transfers with no wait states. Since the PowerPC™ 60x processors are limited to 32 byte bursts, it is better to use the DMA controller on the V292PBC to transfer large volumes of data. It is capable of sustaining up to 1KB bursts. For this reason, a controller such as the V292BMC is highly recommended since it supports long zero-wait bursting.

Data Flow: It is better to “push” (write) data rather than “pulling” (reading). Pushing takes advantage of the large 256 byte write FIFOs on the V292PBC. Writes can also be posted so that the final target device doesn’t have to respond in order for the originating master to start data transfer. Reading non-consecutive locations will require a new address to be transferred to the target before any progress can be made with data movement.

Sequential Reads: If a pushing data flow cannot be accommodated then reading should be done as sequential bursts. This will take advantage of the read prefetching buffers. When possible use the dual apertures to the best advantage since they each have their own prefetch buffers.

System Bottlenecks: If non-bursting or slow target devices are used then obviously performance is affected. Also, other traffic on the PCI or local bus will allow less time for V292PBC transfers. PCI system main memory can also be a bottleneck since the V292PBC must compete with the host CPU to get access to this shared resource. Host CPU intensive applications that are cache bound will allow improved PCI data movement since the CPU doesn’t need access to main memory very often.

Table 1: Performance as a PCI Master

Transaction Type	Number of PCLKs	PCLK=33MHz Rate (MB/s)
Single Posted Writes	3	44.0
Burst Write of 4 words	6	88.0
Burst Write of 8 words	10	105.6
Burst Write of 16 words	18	117.3
Burst Write of 256 words	258	131.0

Table 2: Performance as a PCI Target

Transaction Type	Number of PCLKs	PCLK=33MHz Rate (MB/s)
Single Posted Writes	3	44.0
Burst Write of 4 words	5	105.6
Burst Write of 8 words	9	117.3
Burst Write of 16 words	17	124.2
Burst Write of 256 words	257	131.5

Table 3: Performance with V292PBC as Master, V292BMC as Target

	Using V292PBC Bus Mode		
Transaction Type	Number of LCLKs	LCLK=33MHz Rate (MB/s)	LCLK=40MHz Rate (MB/s)
Single Posted Writes	2	66.0	80.0
Burst Write of 4 words	5	105.6	128.0
Burst Write of 8 words	9	117.3	142.2
Burst Write of 16 words	17	124.2	150.6
Burst Write of 256 words	257	131.5	159.4

Table 4: Performance with PowerPC™ 60x as Master, V292PBC as Target Cycles

	Using V292PBC Bus Mode		
Transaction Type	Number of LCLKs	LCLK=33MHz Rate (MB/s)	LCLK=40MHz Rate (MB/s)
Single Writes (64-bit)	4	66.0	80.0
Burst Write of 4 Double words	10	105.6	128.0

5. Conclusion

The V292PBC from V3 provides a high performance PCI solution for various members of the PowerPC™ 60x family. When used together with the V292BMC burst DRAM controller, the limited burst capabilities of the PowerPC™ 60x are easily overcome. Only a small (44 pin) low cost PLD and four 74FCT16543 style buffers are required in addition to the highly integrated V292PBC and optional V292BMC.

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